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Wireless
Semiconductor Solutions
Device Data - Vol. I

"Creating the World of Tomorrow with Technology Today."

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Wireless Semiconductor Solutions
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FOREWORD

This publication includes technical information for the several product families that comprise the Motorola portfolio of Wireless Semiconductor RF and RF/IF Products. The product families include bipolar, LDMOS, MOSFET RF Power, and gallium arsenide chip technologies in a variety of ceramic and plastic surface mount packages. Discrete components, hybrid modules, and integrated circuits provide different levels of complexity in an effort to provide solutions for our customers' needs.

All devices are in alphanumeric order in the *Device Index* of this book. Just turn to the appropriate page for technical details of the known device. Complete device specifications are provided in the form of *Data Sheets* which are categorized by product type into five chapters for easy reference. *Selector Guides* by product family are provided at the beginning of the book as well as in the beginning of each chapter to enable quick comparisons of performance characteristics and to aid you in identifying devices that meet your functional performance requirements of frequency, output power, gain, or other parameters.

Chapters on Tape and Reel Options, Packaging Information, Applications and Product Literature include additional information to aid you in the design process.

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274. Please refer to our section on *On–line Access to Wireless Semiconductor Data* so that you will always have easy access to the most current information available on Motorola's Wireless Semiconductor product portfolio.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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ABOUT THIS REVISION

The Wireless Semiconductor Solutions Device Data Book is contained in two volumes. This edition encompasses a considerable number of changes that have occurred since our last printing. Some devices have been removed from this book due to package changes or new technology replacements and many new devices have been added.

Application Notes, Engineering Bulletins and Article Reprints of special interest to designers of RF and RF/IF equipment are available on the Motorola Semiconductor Product Sector Web site or are available through the Motorola Literature Distribution Center. Phone and fax numbers for ordering literature are listed on the back cover of this book and in our Accessing Data On–line section. The majority of the documents are available in one book, titled *RF Applications Report* (order by HB215/D). See Section Ten for a complete listing of Application Literature.

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Chapter One

Wireless Semiconductor Solutions Selector Guide

While Motorola is a worldwide leader in semiconductor products, there is not a category in which the selection is more diverse, or more complete, than in products designed for RF system applications. From MOS, bipolar power and signal transistors to integrated circuits, Motorola's RF components cover the entire spectrum from HF to microwave to personal communications. Yet, product expansion continues — not only to keep pace with the progressive needs of the industry, but to better serve the needs of designers for a reliable and comprehensive source of supply.

How to Use This Selector Guide

The products in this guide are separated FIRST into major categories by power level (RF Monolithic Integrated Circuits, RF/IF Integrated Circuits, Small Signal, Medium Power Transistors, Power FETs, Power Bipolar, Power Amplifier Modules and CATV Distribution Amplifiers). SECOND, within each category parts are listed by frequency band, except for medium power transistors, small signal transistors and monolithic integrated circuits, which are divided by application. Small signal transistor applications are low noise, linear amplifiers, switches, and oscillators. Monolithic integrated circuit application groupings are switching, receiver functions and transmitter functions. THIRD, within a frequency band, transistors are further grouped by operating voltage and, finally, output power.

To Replace Devices in an Existing Design

Call your local Motorola Sales Office or Distributor to determine Motorola's closest replacement device.

Applications Assistance

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

Access Data On–Line!

Use the Motorola SPS World Marketing Internet Server to access Motorola Semiconductor Product data at http://motorola.com/sps/ or http://motorola.com/sps/rf/. The SPS World Marketing Server provides you with instant access to data sheets, selector guide information, package outlines, on–line technical support and much more.

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Wireless Semiconductor Solutions Selector Guide

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Motorola RF Monolithic Integrated Circuits

Motorola's RF monolithic integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SOIC–8, SOIC–16, SOT–143, TSSOP–16, Micro–8, TSSOP–20, TSSOP–20HS, TQFP–48 or PFP–16 packages.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

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Motorola RF Monolithic Integrated Circuits

Switching

Antenna Switches/Local Oscillator Switches

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current μA (Typ)	P_{in}, 1 dB Compression dBm (Typ)	TX Insertion Loss dB (Typ)	Isolation dB (Typ)	Package	System Applicability
MRFIC1801[18b]	1500–2500	2.7–5.5	300	29	0.6	20	SO–8	DECT, PHS, PCS, ISM
MRFIC0903[18b]	100–2000	2.7–5.0	60	35.5	0.65	21	SO–8	AMPS, Class 4 & 5 GSM, DCS1800, PHS, PCS

Receiver Functions

General Purpose Integrated Circuits

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915[18c,46a]	100–2000	2.7–5.0	2.2	16.5	1.9	38	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS
MRFIC0916[18c]	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	Input Third Order Intercept	Package	System Applicability
MRF9820T1[18c]★	100–1500	2–5	1.0	16	–3	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS

900 MHz Front End

LNA + Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2001[18b]	500–1000	0–250	2.7–5.0	4.7	23	–10	SO–8	CT2, ISM

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

★New Product

Receiver Functions (continued)

1.5 – 2.2 GHz Front End

Integrated LNA

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC1501[18b] ★	1000–2000	3–5	5.7	18	1.1	26	SO–8	GPS
MRFIC1808[18b] ★	1700–2100	2.7–4.5	5.0	17	1.6	37	SO–8	DECT, PHS, PCS
MRFIC1808DM[18g,46a]	1700–2100	2.7–4.5	5.0	17	1.6	32	Micro–8	DECT, PHS, PCS

GPS Receiver

MRFIC1502★	1570–1580	4.5–5.5	50	65	9.5	—	TQFP–48	GPS

Integrated LNA/Downconverter

Device	RF Freq. Range GHz	IF Freq. Range GHz	Supply Volt. Range Vdc	Supply Current RX Mode mA (Typ)	Mixer Conv. Gain dB (Typ)	LNA Gain dB (Typ)	LNA Noise Figure dB (Typ)	Package	System Applicability
MRFIC1804[18b]	1.8–2.0	70–325	2.7–3.3	10	4	14	2.3	SO–16	DECT,PHS,PCS
MRFIC1814[18b] ★	1.8–2.0	70–325	2.7–4.5	13	8	17	2.5	TSSOP–16	DECT,PHS,PCS

2.4 GHz Front End

Integrated LNA/Downconverter

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	LNA Noise Figure dB (Typ)	Isolation Lo to RF, Lo to IF dB (Typ)	Package	System Applicability
MRFIC2401[18b]	2400–2500	100–350	4.75–5.25	9.5	21	1.9	20	SO–16	WLAN, MMDS, ISM

Transmitter Functions

General Purpose Integrated Circuits

Quadrature Modulator

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Gain Control dB (Typ)	Lo Leakage dBm (Typ)	SSB P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC0001[18b]	50–260	2.7–5.5	10	30	–55	–10	TSSOP–20	DCS1800, GSM, NADC PDC, PHS, PCS1900

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915[18c,46a]	100–2000	2.7–5.0	2.2	16.5	1.9	38	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS
MRFIC0916[18c]	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

★New Product

Transmitter Functions (continued)

900 MHz Transmit Chain

Transmit Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2002[18b]	500–1000	0–250	2.7–5.0	5.5	0.1	10	–18	SO–8	AMPS,CT1,CT2, GSM, IS–54, ISM
MRFIC2101[18b]	800–1000	0–250	3–4.75	45	2	26.5	4.5	SO–16	AMPS,CT1,CT2, GSM, IS–54, ISM, USPCS, CDMA
MRFIC0931[18b]★	500–2000	0–250	2.7–4.8	38	—	25	1.0	SO–8	AMPS,CT1,CT2, GSM, IS–54, ISM, USPCS, CDMA

Driver Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Gain Control dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2004[18b]	800–1000	2.7–4.0	11	0.7	21.5	34	–1	SO–16	AMPS,CT1,CT2, GSM,ISM
MRFIC2006[18b]	500–1000	1.8–4.0	46	—	23	—	15.5	SO–8	AMPS,CT1,CT2, GSM,ISM
MRFIC0904[18b]	800–1000	2.7–5.0[47]	280	0.05	27	24.5	25.5	SO–16	AMPS,GSM,ISM

Integrated Power Amplifiers

Low Power 900 MHz Power Amplifiers

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Return Loss Input/Output dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2006[18b]	500–1000	1.8–4.0	46	23	15	15.5	SO–8	Silicon

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2101[18b]	800–1000	3 – 4.75	38	2	16	18	SO–16	Silicon

Analog Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0910[18e,46a]	824–905	4.8	50	17.8	–40	30.8/13	PFP–16	LDMOS
MRFIC0912[18e]★	824–905	4.6[47]	55	23.8	–25	30.8/7	PFP–16	GaAs

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

[47] Negative supply required

★New Product

Transmitter Functions: 900 MHz Transmit Chain: Integrated Power Amplifiers (continued)

GSM Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0913[18e]★	880–915	4.8[47]	48	24.5	–30	34.5/10	PFP–16	GaAs
MRFIC0917[18e]★	880–915	3.6[47]	43	22	–30	34/12	PFP–16	GaAs

DCS1800, PCS1900

Device	Freq. Range GHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC1818[18e]★	1.7–1.9	4.8[47]	35	30	–30	33/3	PFP–16	GaAs
MRFIC1817[18e]★	1.7–1.9	3.6[47]	35	27	–30	32/5	PFP–16	GaAs

Two–way Paging, ISM

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Typ)	Package	Semiconductor Technology
MRFIC0920[18b,46b]	890–950	3.4	35	28	–45	30.5/2.5	TSSOP–20HS	LDMOS

1.5 – 2.2 GHz Transmit Chain

Upconverter

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803[18b]	1.7–2.5	2.7–5.0	28	100	10	70–350	–2	SO–16	DECT,PHS, PCS
MRFIC1813[18b]★	1.7–2.5	2.7–4.5	25	100	15	70–350	3	TSSOP–16	CDMA,PCS
MRFIC0931[18b]★	0.5–2.0	2.7–4.8	38	—	20	0–250	–2	SO–8	CDMA,PCS

Power Amplifier

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc[47]	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}/P_{in} dBm (Typ)	1 dB Comp. dBm (Typ)	Pkg	System Applicability
MRFIC1805[18b]★	1.7–2.5	2.7–5.0	170	—	21	21.5/2	24	TSSOP–16	DECT,PHS, PCS
MRFIC1806[18b]	1.5–2.5	3.0–5.0	115	0.25	23	19.5/–3	21	SO–16	DECT,PHS, PCS
MRFIC1807[18b]	1.5–2.2	3.0–5.0	325	0.06	8	26.8/20	25	SO–16	DECT,PHS, PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

[47] Negative supply required

★New Product

Transmitter Functions: 1.5 – 2.2 GHz Transmit Chain (continued)

Power Amplifier

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	PA Supply Current TX Mode mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Insertion Loss RX Mode dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC1807[18b] (Including TX/RX Switch)	1.5–2.2	3.0–5.0	325	0.06	8	1	25	SO–16	DECT, PHS, PCS

2.4 GHz Transmit Chain

Exciter Amplifier

Device	Freq. Range GHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2404[18b]	2.0–3.0	4.75–5.25	9	17	4.3	5	SO–8	WLAN, MMDS, ISM

Power Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Power Control Range dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2403[18b]	2200–2700	4.75–5.25	95	23	20	19	SO–16	WLAN, MMDS, ISM

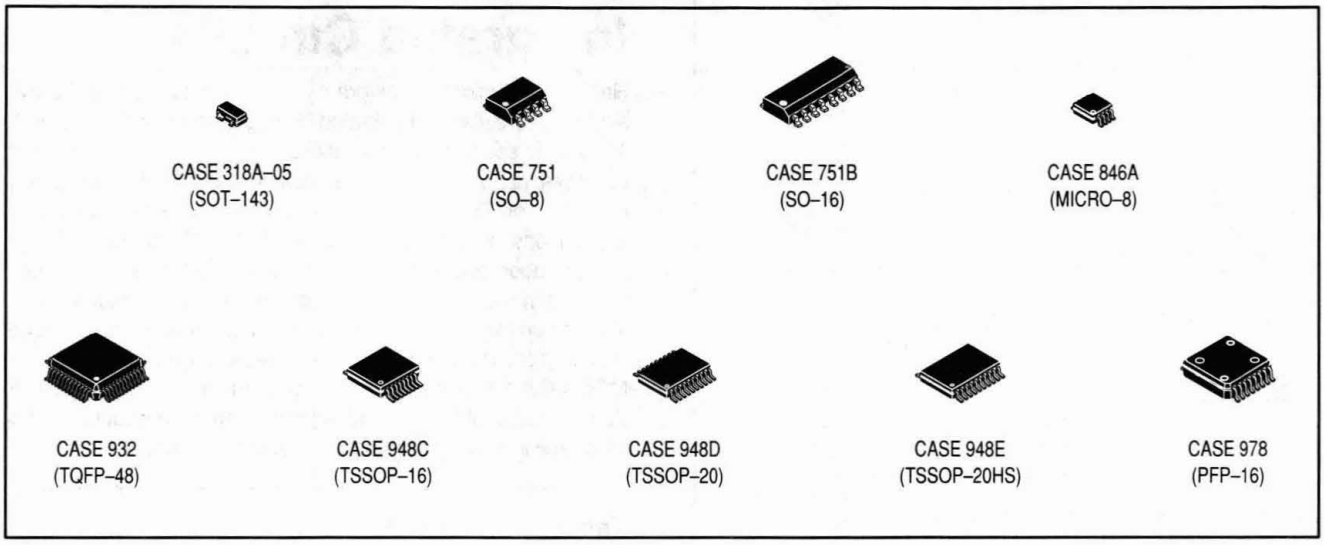
Upconverter

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803[18b]	1.7–2.5	2.7–5.0	28	100	10	70–350	–2	SO–16	WLAN, ISM
MRFIC1813[18b]★	1.7–2.5	2.7–4.5	25	100	15	70–350	3	TSSOP–16	WLAN, ISM
MRFIC2406[18b]	2.4 – 2.5	3.0–5.0	15	0.6	6	100–370	–10	SO–16	WLAN, MMDS,ISM

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

★New Product

RF Monolithic Integrated Circuit Packages



Motorola RF/IF Integrated Circuits

Radio communication has greatly expanded its scope in the past several years. Once dominated by public safety radio, the 30 to 1000 MHz spectrum is now packed with personal and low cost business radio systems. The vast majority of this equipment uses FM or FSK modulation and is targeted at short range applications. From mobile phones and VHF marine radios to garage door openers and radio controlled toys, these new systems have become a part of our lifestyle. Motorola has focused on this technology, adding a wide array of new products including complete receivers processed in our exclusive 3.0 GHz MOSAIC® 1.5 process. New surface mount packages for high density assembly are available for all of these products, as well as a growing family of supporting application notes.

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Motorola RF/IF Monolithic Integrated Circuits

Table 1. RF Front End ICs

Receiver												
Low Noise Amplifier					Mixer				Voltage Cont Osc	V_{CC} (V)	I_{CC} (mA)	Suffix/ Package
Device	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	Input P1dB (dBm)	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	P1dB (dBm)				
MC13142	17	1.8	–5.0	–15	±3.0	12	–3 to +21	3.0	Yes	2.7 to 6.5	13	D/751B
MC13143	–	–	–	–	±3.0	12	–3 to +21	3.0	–	1.8 to 6.5	1.0	D/751
MC13144	13 to 19	1.4	–1.0	–7.0	–	–	–	–	–	1.8 to 6.5	2 to 9	D/751
MC13145	14	1.8	–5.0	–8.0	0	13	9.0	–1.0	Yes	2.7 to 6.5	30	FTA/932
Transmitter												
Low Power Amplifier					Mixer				Voltage Cont Osc	V_{CC} (V)	I_{CC} (mA)	Suffix/ Package
Device	PA Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	Output P1dB (dBm)	P_{IFOut} (dB)	Noise Figure (dB)	IIP3 (dBm)	P1dB (dBm)				
MC13146	15	–	–	8.0	15	–	10	–	Yes	2.7 to 6.5	25	FTA/977

NOTES: All devices operate over a wide range of RF input and IF frequencies, from dc to 2.0 GHz.
Typical performance shown at 900 MHz.

Table 2. Wideband (FM/FSK) IFs

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC13055	3–12 V	25 mA	20 µV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF, includes data shaper	P/648, D/751B
MC13155	3–6 V	7.0 mA	100 µV	250 MHz	–		10 Mb	Video Speed FM IF	D/751B

Table 3. Wideband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3356	3–9 V	25 mA	30 µV	200 MHz	10.7 MHz	✓	✓	500 kb	Includes front end mixer/L.O.	P/738, DW/751D
MC13156	2–6 V	5.0 mA	2.0 µV	500 MHz	21.4 MHz	–			CT–2 FM/Demodulator	DW/751E, FB/873
MC13158	2–6 V	6.0 mA						>1.2 Mb	FM IF/Demodulator with split IF for DECT	FTB/873
MC13159	2.7–5 V	5.5 mA		600 MHz				500 kb	FM IF for PHS	DTB/948F

Table 4. Narrowband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3357	4–8 V	5.0 mA	5.0 μV	45 MHz	455 kHz	✓	–	>4.8 kb	Ceramic Quad Detector/Resonator	P/648, D/751B
MC3359	4–9 V	7.0 mA	2.0 μV						Scan output option	P/707, DW/751D
MC3371	2–8 V	6.0 mA		60 MHz			✓	>4.8 kb	RSSI	P/648, D/751B, DTB/948F
MC3372									RSSI, Ceramic Quad Detector/Resonator	
MC13150	3–6 V	1.8 mA	1.0 μV	500 MHz			✓ 110 dB	>9.6 kb	Coilless Detector with Adjustable Bandwidth	FTB/873, FTA/977

Table 5. Narrowband Dual Conversion Receivers – FM/FSK – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF1	IF2 (Limiter In)	Mute	RSSI	Data Rate	Notes	Suffix/ Package
MC3362	2–7 V	3.0 mA	0.7 μV	180 MHz	10.7 MHz	455 kHz	–	✓	> 4.8 kb	Includes buffered VCO output	P/724, DW/751E
MC3363		4.0 mA	0.4 μV				✓			Includes RF amp/mute	DW/751F
MC13135			1.0 μV				–			Voltage buffered RSSI, LC Quad Detector	DW/751E, P/724
MC13136										Voltage Buffered RSSI, Ceramic Quad Detector	DW/751E

Table 6. Universal Cordless Phone Subsystem ICs

Device	V_{CC}	I_{CC}	Dual Conversion Receiver	Universal Dual PLL	Compander and Audio Interface	Voice Scrambler	Low Battery Detect	Programmable R_X, T_X Trim Gain and LBD Voltage Reference	Suffix/ Package
MC13109	2.0–5.5 V	Active Mode 6.7 mA Inactive Mode 40 μA	✓	✓	✓	–	1	–	FB/848B, FTA/932
MC13110	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 μA	✓	✓	✓	✓	2	✓	FB/848B
MC13111	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 μA	✓	✓	✓	–	2	✓	FB/848B

Table 7. Transmitters – AM/FM/FSK

Device	V_{CC}	I_{CC}	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Package
MC2833	3–8 V	10 mA	–30 dBm to +10 dBm	150 MHz	50 kHz	FM transmitter. Includes two frequency multiplier/amplifier transistors	P/648, D/751B
MC13175	2–5 V	40 mA	8.0 dBm	500 MHz	5.0 MHz	AM/FM transmitter. Single frequency PLL $f_{out} = 8 \times f_{ref}$, includes power down function	D/751B
MC13176				1.0 GHz		$f_{out} = 32 \times f_{ref}$, includes power down function	

Table 8. Balanced Modulator/Demodulator

Device	V_{CC}	I_{CC}	Function	Suffix/ Package
MC1496	3–5 V	10 mA	General purpose balanced modulator/demodulator for AM, SSB, FM detection with Carrier Balance >50 dB	P/646, D/751A

Table 9. Infrared Transceiver

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Max IF Freq	Carr Det	RSSI	Data Rate	Notes	Suffix/ Package
MC13173	3–5 V	6.5 mA	5.0 μV	10.7 MHz	✓	✓	200 kb	Includes Single Frequency PLL for T_x Carrier and R_x L_O	FTB/873

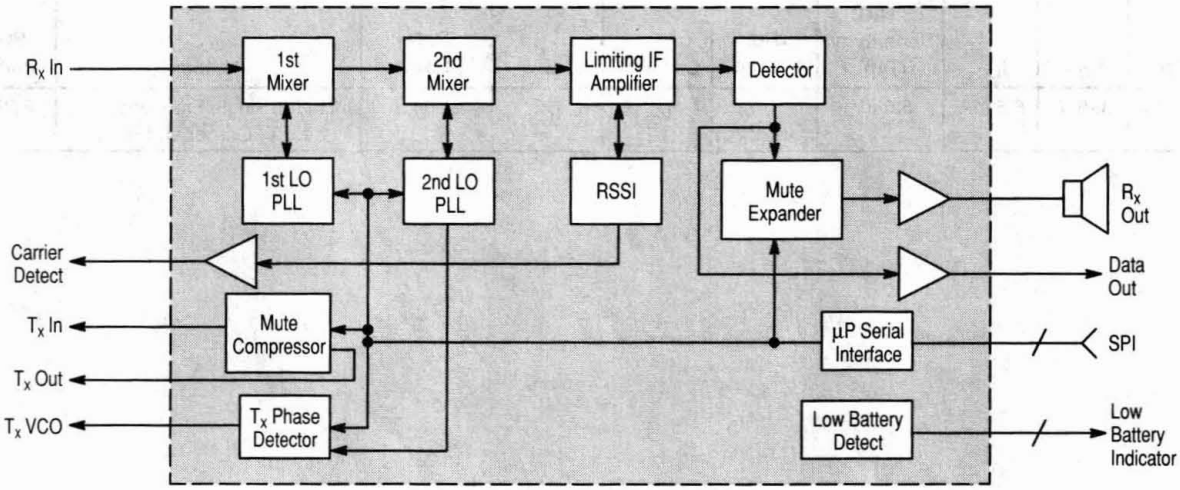
Universal Cordless Telephone Subsystem IC

MC13109FB, FTA

T_A = −20° to +85°C, Case 848B, 932

The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



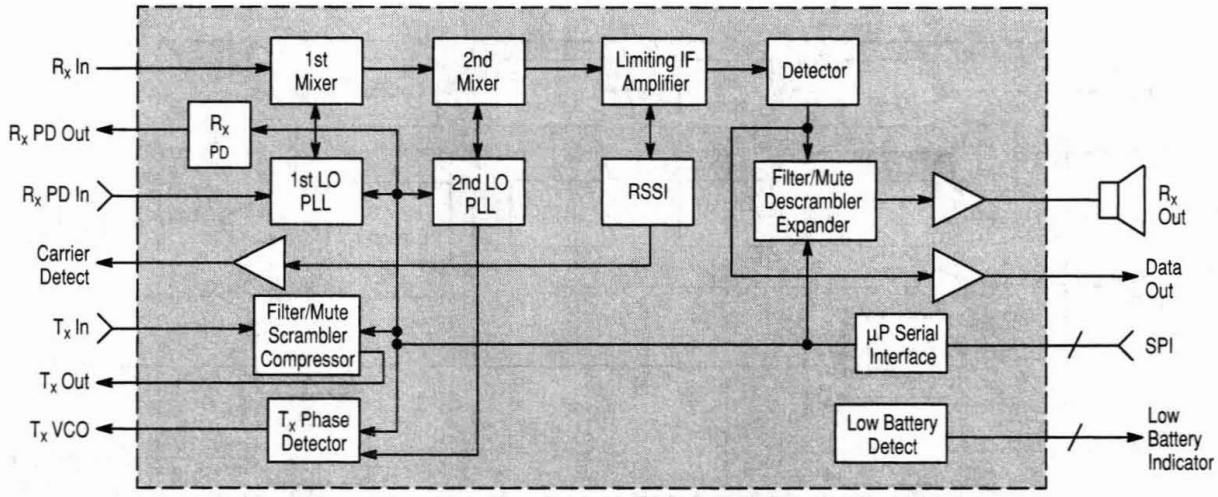
Universal Cordless Telephone Subsystem IC with Scrambler

MC13110FB

T_A = –40° to +85°C, Case 848B

The MC13110 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with New External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Frequency Inversion Scrambler/Descrambler
  - Can Be Enabled/Disabled Via MPU Interface
  - Programmable Carrier Modulation Frequency
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



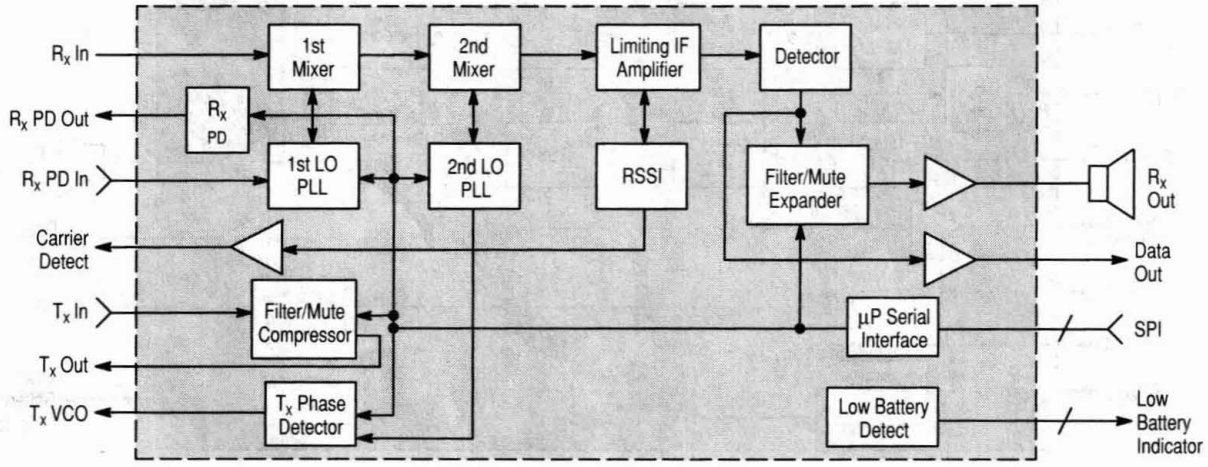
Universal Cordless Telephone Subsystem IC with Scrambler (continued)

MC13111FB

T_A = –40° to +85°C, Case 848B, 932

The MC13111 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, external adjustments, and lowers overall costs. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Programmable Corner Frequency Selection
- MC13111 is Pin–for–Pin Compatible with MC13110
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices
- AN1575: Refer to this Application Note for a List of the "Worldwide Cordless Telephone Frequencies" (List can also be found in Chapter 8 Addendum of DL128 Data Book)



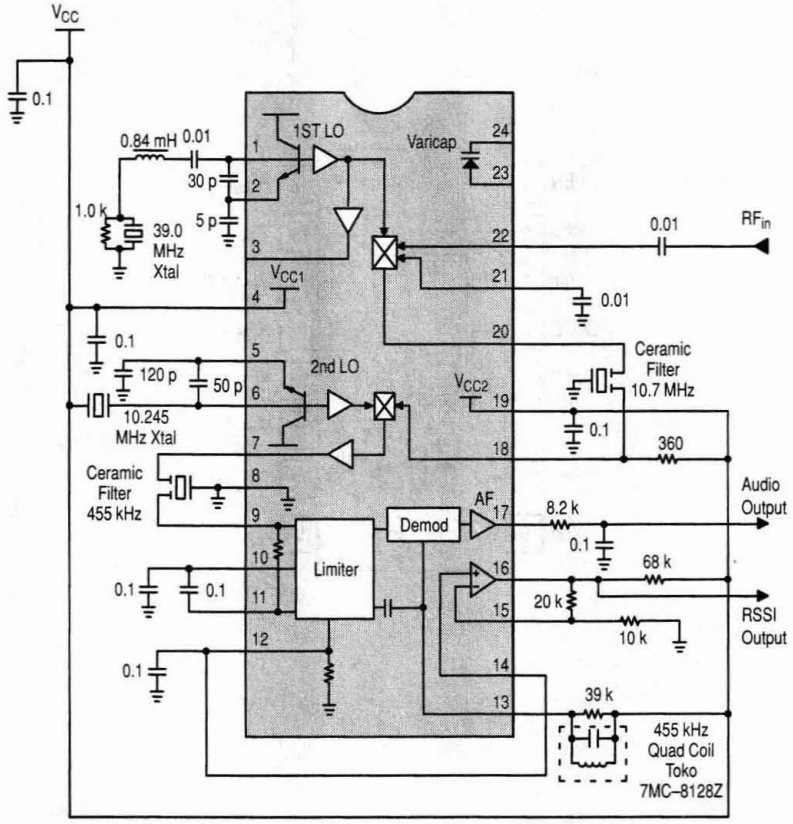
Narrowband FM Receiver

MC13135P,DW, MC13136DW

T_A = –40° to +85°C, Case 724, 751E

The MC13135 is a full dual conversion receiver with oscillators, mixers, Limiting IF Amplifier, Quadrature Discriminator, and RSSI circuitry. It is designed for use in security systems, cordless phones, and VHF mobile and portable radios. Its wide operating supply voltage range and low current make it ideal for battery applications. The Received Signal Strength Indicator (RSSI) has 65 dB of dynamic range with a voltage output, and an operational amplifier is included for a dc buffered output. Also, an improved mixer third order intercept enables the MC13135 to accommodate larger input signal levels.

- Complete Dual Conversion Circuitry
- Low Voltage: 2.0 to 6.0 Vdc
- RSSI with Op Amp: 65 dB Range
- Low Drain Current: 3.5 mA Typical
- Improved First and Second Mixer 3rd Order Intercept
- Detector Output Impedance: 25 Ω Typically



Low Power DC – 1.8 GHz LNA, Mixer and VCO

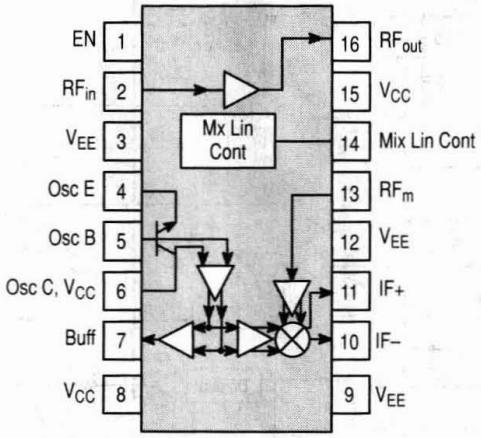
MC13142D

T_A = –40° to +85°C, Case 751B

The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7 – 6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm
- Linearity Adjustment Increases IP_{3in} Up to 20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output

SO–16



Ultra Low Power DC – 2.4 GHz Linear Mixer

MC13143,D

T_A = –40° to +85°C, Case 751

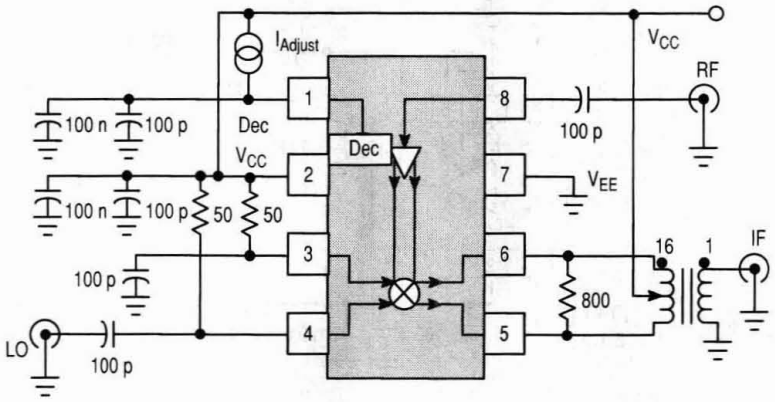
The MC13143 is a high compression linear mixer with single–ended RF input, differential IF output and differential LO inputs which consumes as little as 1.8 mW. A new circuit topology is used to achieve a high third order intermodulation intercept point, high linearity and high 1.0 dB output compression point while maintaining a linear 50 Ω input impedance. It is designed for Up or Down conversion anywhere from dc to 2.4 GHz.

Ultra Low Power: 1.0 mA @ V_{CC} = 1.8 – 6.5 V

- Wide Input Bandwidth: DC–2.4 GHz
- Wide Output Bandwidth: DC–2.4 GHz
- Wide LO Bandwidth: DC–2.4 GHz
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm

Linearity Adjustment of up to IP_{3in} = 20 dBm

- 50 Ω Mixer Input
- Single–Ended Mixer Input
- Double Balanced Mixer Operation
- Differential Open Collector Mixer Output



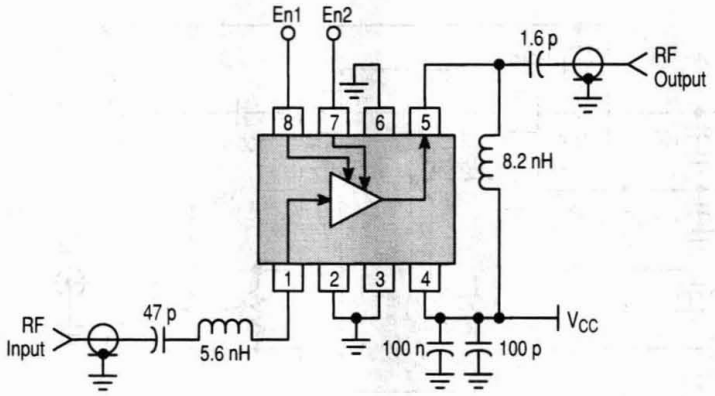
VHF – 2.0 GHz Low Noise Amplifier with Programmable Bias

MC13144,D

T_A = –40° to +85°C, Case 751

The MC13144 is designed in the Motorola High Frequency Bipolar MOSIAC V™ wafer process to provide excellent performance in analog and digital communication systems. It includes a cascoded LNA usable up to 2.0 GHz and at 1.8 Vdc, with 2 bit digital programming of the LNA bias. Targeted applications are in the UHF Family Radio Services, UHF and 800 MHz Special Mobile Radio, 800 MHz Cellular and GSM, PCS, DECT and PHS at 1.8 to 2.0 GHz and Cordless Telephones in the 902 to 928 MHz band covered by FCC Title 47; Part 15. The MC13144 offers the following features:

- 17 dB Gain at 900 MHz
- 1.4 dB Noise Figure at 900 MHz
- 1.0 dB Compression Point of –7.0 dBm; Input Third Order Intercept Point of –5.0 dBm
- Low Operating Supply Voltage (1.8 to 6.0 Vdc)
- Programmable Bias with Enable 1 and Enable 2
- Enable 1 and Enable 2 Programmed High for Optimal Noise Figure and Gain Associated with NF
- Can Override Enable and Externally Program In Up to 15 mA



Narrowband FM Coilless Detector IF Subsystem

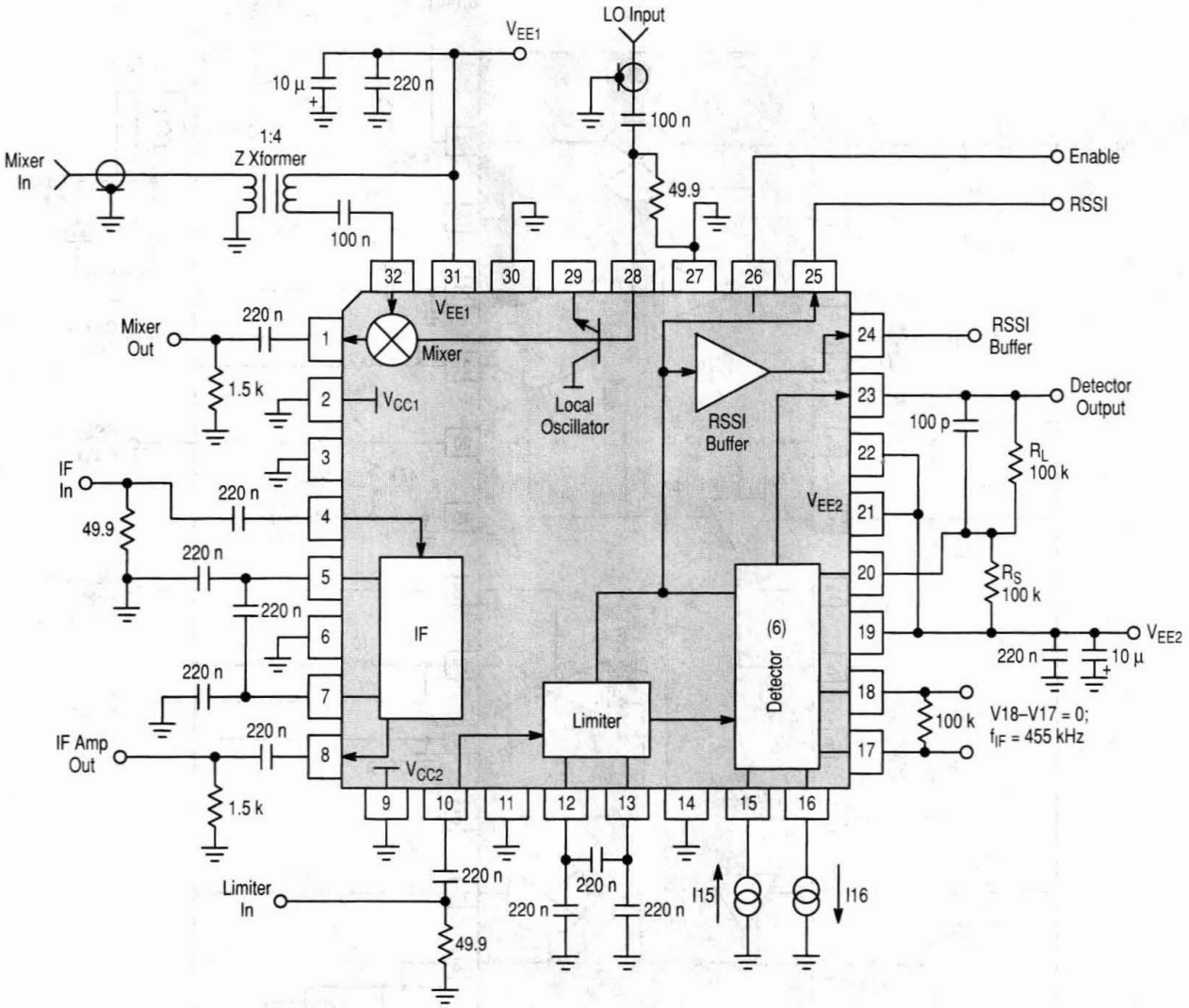
MC13150FTA, FTB

T_A = –40° to +85°C, Case 977, 873

The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 μV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF System

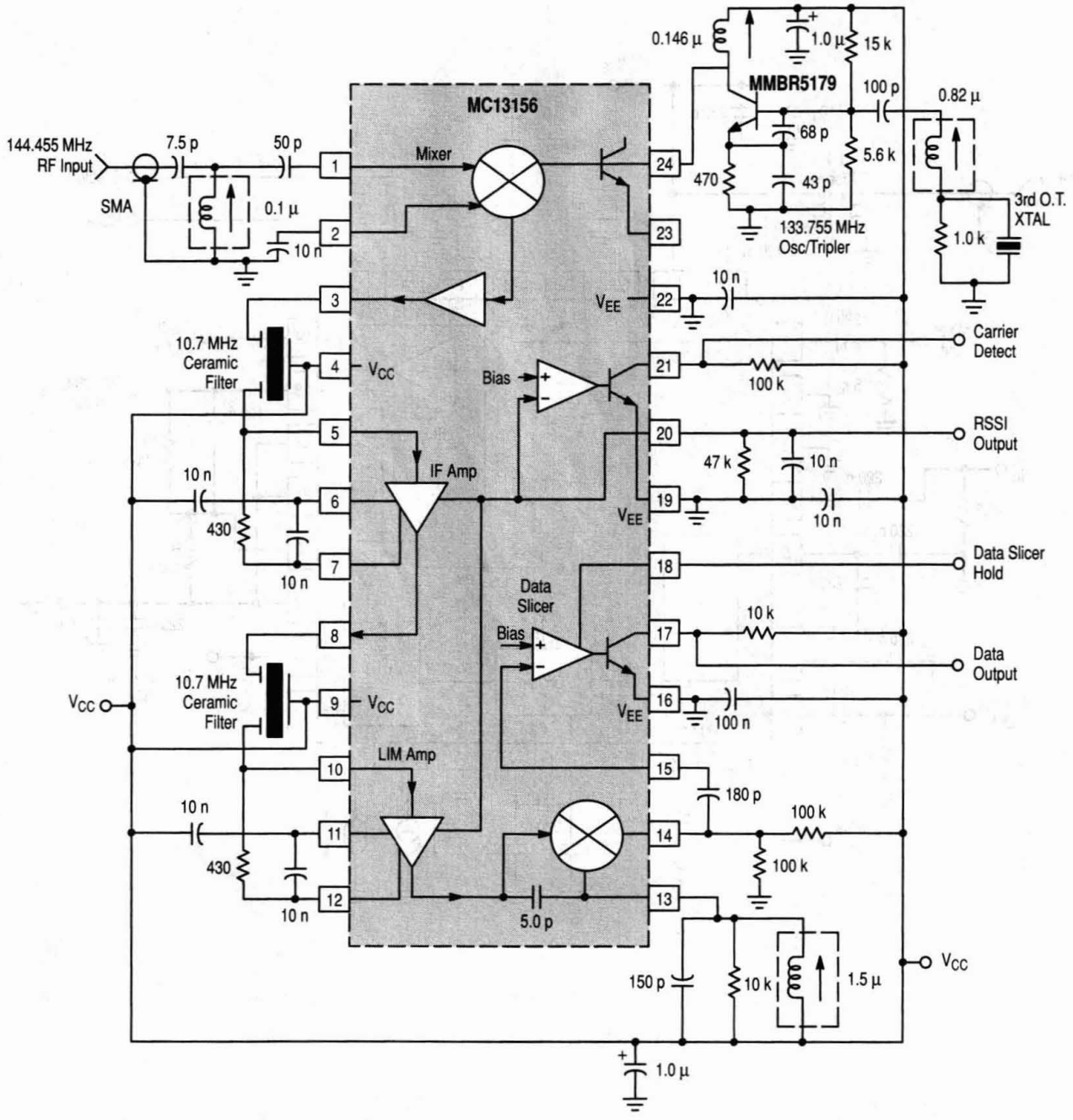
MC13156DW, FB

T_A = –40° to +85°C, Case 751E, 873

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13156 has an onboard Colpitts VCO for PLL controlled multichannel operation. The mixer is useful to beyond 200 MHz and may be used in a differential, balanced, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity of 6.0 μV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 300 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF Subsystem

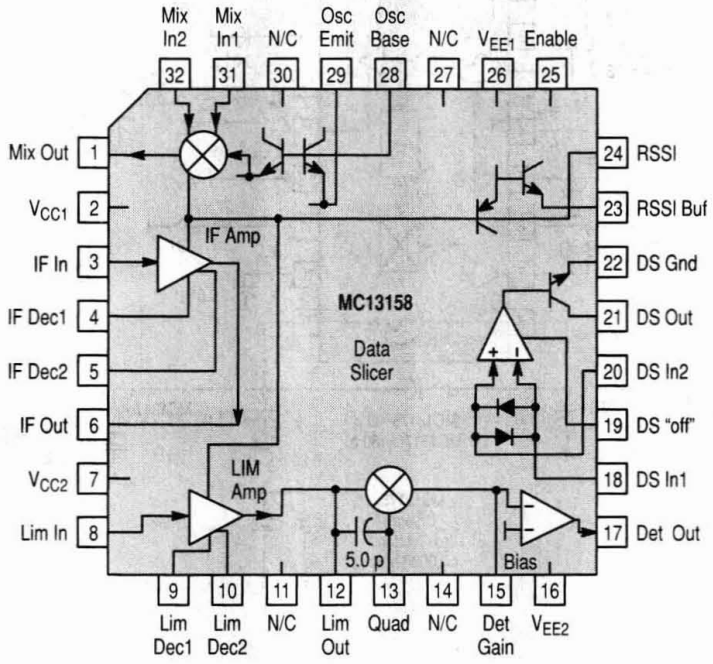
MC13158FTB

T_A = –40° to +85°C, Case 873

The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output "off" to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count



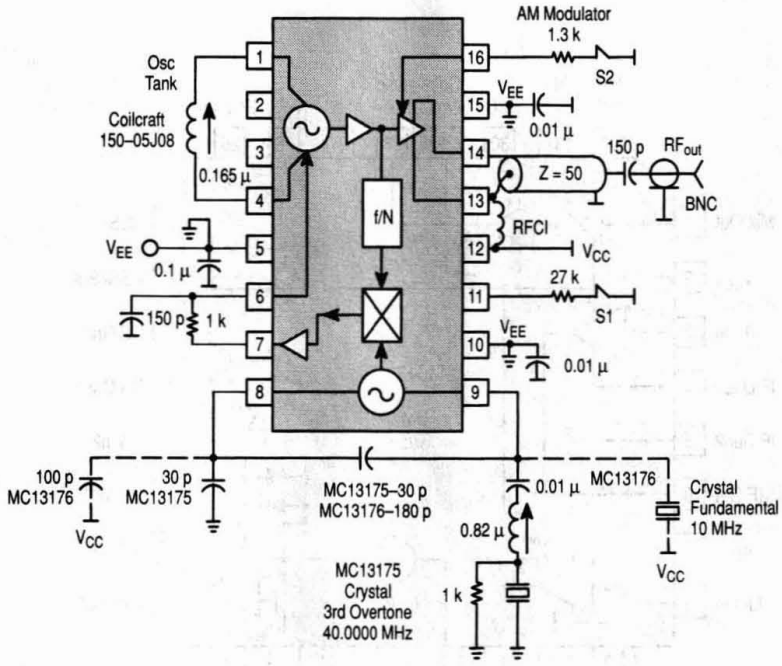
UHF, FM/AM Transmitter

MC13175/176D

T_A = 0° to +70°C, Case 751B

The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems operating in the 260 to 470 MHz band covered by FCC Title 47; Part 15. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷8 (MC13175) or ÷32 (MC13176) prescaler, and phase detector forming a versatile PLL system. Another application is as a local oscillator in a UHF or 900 MHz receiver. MC13175/176 offer the following features:

- UHF Current Controlled Oscillator
- Use Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Low Number of External Parts Required
- Low Operating Supply Voltage (1.8–5 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output "On"/"Off"
- MC13175 – $f_o = 8 \times f_{ref}$
- MC13176 – $f_o = 32 \times f_{ref}$



Phase–Locked Loop Components

Motorola offers a choice of phase–locked loop components ranging from complete functional frequency synthesizers for dedicated applications to a wide selection of general purpose PLL circuit elements. Technologies include CMOS for lowest power consumption and bipolar for high speed operation. Typical applications include TV, CATV, radios, scanners, WLANs, cordless telephones plus home and personal computers.

Table 1. PLL Frequency Synthesizers

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
4 @ 5 V	4.5 to 12	6 @ 5 V	Single–ended 3–state	No	Parallel	MC145106	P/707, DW/751D
15 @ 5 V	3 to 9	–	Two single–ended 3–state		Serial	MC145149*	P/738, DW/751D
		7.5 @ 5 V	Analog			MC145159–1	P/738, DW/751D
20 @ 5 V	3 to 9	7.5 @ 5 V	Single–ended 3–state, double–ended		4–Bit	MC145145–2	P/707, DW/751D
						MC145146–2	P/738, DW/751D
					Parallel	MC145151–2	P/710, DW/751F
			Double–ended			MC145152–2	P/710, DW/751F
			Single–ended 3–state, double–ended		Serial	MC145155–2	P/707, DW/751D
						MC145156–2	P/707, DW/751D
						MC145157–2	P/648, DW/751G
						MC145158–2	P/648, DW/751G
60 @ 3 V	2.5 to 5.5	3 @ 3 V	Two single–ended 3–state	Yes		MC145162*	P/648, D/751B
60 @ 2 V	1.8 to 3.6	1.5 @ 1.8 V				MC145165*	P/648, D/751B
60 @ 3 V	2.5 to 5.5	3 @ 3 V			Parallel	MC145166*	P/648, DW/751G
					Serial	MC145167*	P/648, DW/751G
					Parallel	MC145168*	
					Serial	MC145169*	
85 @ 3 V	2.5 to 5.5	3 @ 3 V				MC145162–1*	P/648, D/751B
40/130 @ 5 V	4.5 to 5.5	9 @ 5 V	Single–ended 3–state, Current source/sink			MC145173	DW/751E
100 @ 3 V 185 @ 5 V	2.5 to 5.5	2 @ 3 V 6 @ 5 V		No		MC145170–1	P/648, D/751B, DT/948C

* Dual PLL

PLL Frequency Synthesizers (continued)

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
1100	4.5 to 5.5	7 @ 5 V	Current source/sink, double–ended	Yes	Serial	MC145190	F/751J, DT/948D
						MC145191	F/751J, DT/948D
1100	2.7 to 5	6 @ 2.7 V				MC145192	F/751J, DT/948D
1100	2.7 to 5.5	12	Two current source/sink, double–ended			MC145220*	F/803C, DT/948D
1200, 400	1.8 to 3.6	5	Loop 1 = Current source/sink Loop 2 = Three–state			MC145225*	FTA/873C
2000	4.5 to 5.5	12 @ 5 V	Current source/sink, double–ended			MC145200	F/751J, DT/948D
2000	4.5 to 5.5	12 @ 5 V				MC145201	F/751J, DT/948D
2000	2.7 to 5.5	4 @ 3 V				MC145202	F/751J, DT/948D
2600, 400	1.8 to 3.6	7	Loop 1 = Current source/sink Loop 2 = Three–state			MC145230*	FTA/873C

* Dual PLL

NOTE: Evaluation kits available for the MC145190, MC145191, MC145192, MC145200, MC145201, MC145202, and MC145220. Order part number MC145_ _ _EVK.

Table 2. Phase–Locked Loop Functions

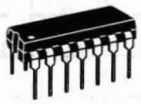
Device	Function	Pins	DIP	SM
MC12002	Analog Mixer	14	P	–
MC12009	480 MHz ÷5/6 Dual Modulus Prescaler	16	P	–
MC12011	550 MHz ÷8/9 Dual Modulus Prescaler	16	P	–
MC12013	550 MHz ÷10/11 Dual Modulus Prescaler	16	P	–
MC12015	225 MHz ÷32/33 Dual Modulus Prescaler	8	P	D
MC12016	225 MHz ÷40/41 Dual Modulus Prescaler	8	P	D
MC12017	225 MHz ÷64/65 Dual Modulus Prescaler	8	P	D
MC12018	520 MHz ÷128/129 Dual Modulus Prescaler	8	P	D
MC12019	225 MHz ÷20/21 Dual Modulus Prescaler	8	P	D
MC12022LVA	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022LVB	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12023	225 MHz ÷64 Prescaler	8	P	D
MC12026A	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12026B	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12028A	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12028B	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12033A	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D
MC12033B	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D

Phase–Locked Loop Components (continued)

Phase–Locked Loop Functions (continued)

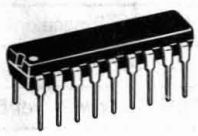
Device	Function	Pins	DIP	SM
MC12034A	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12034B	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12038A	1.1 GHz ÷64/65, ÷127/128, ÷255/256 Low Power Dual Modulus Prescaler	8	P	D
MC12040	Phase-Frequency Detector	14,20	P	–
MC12052A	1.1 GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	8	–	D, SD
MC12053A	1.1 GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler With Stand-By Mode	8	–	D, SD
MC12054A	2.0 GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	8	–	D, SD
MC12058	1.1 GHz ÷126/128. ÷254/256 Low Power Dual Modulus Prescaler	8	–	D, SD
MC12061	Crystal Oscillator	16	P	–
MC12066	1.3 GHz ÷64/256 Prescaler	8	–	D
MC12079	2.8 GHz ÷64/128/256 Prescaler	8	P	D
MC12080	1.1 GHz ÷10/20/40/80 Prescaler	8	P	D
MC12089	2.8 GHz ÷64/128 Prescaler	8	P	D
MC12093	1.1 GHz ÷2/4/8 Low Power Prescaler With Stand-By Mode	8	–	D, SD
MC12095	2.5 GHz ÷2/4 Low Power Prescaler With Stand-By Mode	8	–	D, SD
MC12098	2.5 GHz ÷8192 Prescaler	8	–	D, SD
MCH/K12140	Phase-Frequency Detector	8	–	D
MC12147	Low Power Voltage Controlled Oscillator Buffer	8	–	D, SD
MC12148	Low Power Voltage Controlled Oscillator	8	–	D, SD, P
MC12149	Ultra Low Power Voltage Controlled Oscillator	8	–	D, SD
MC12179	500–2800 MHz Single Channel Frequency Synthesizer	8	–	D
MC12181	125–1000 MHz Frequency Synthesizer	16	–	D

RF/IF Integrated Circuits Packages

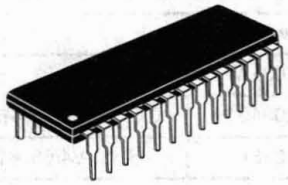


CASE 646
P SUFFIX

CASE 648
P SUFFIX

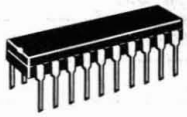


CASE 707
P SUFFIX



CASE 710
P SUFFIX

CASE 724
P SUFFIX



CASE 738
P SUFFIX

CASE 751
D SUFFIX

CASE 751A
D SUFFIX

CASE 751B
D SUFFIX

CASE 751D
DW, FP SUFFIX

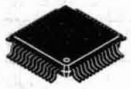
CASE 751E
DW SUFFIX

CASE 751F
DW SUFFIX

CASE 751G
DW SUFFIX

CASE 751J
F SUFFIX

CASE 803C
F SUFFIX



CASE 848B
FB SUFFIX

CASE 873
FB, FTB SUFFIX

CASE 873C
FTA SUFFIX

CASE 932
FTA SUFFIX

CASE 948C
DT SUFFIX

CASE 948D
DT SUFFIX

CASE 948F
DTB SUFFIX

CASE 976
FTB SUFFIX

CASE 977
FTA SUFFIX

Motorola RF Discrete Transistors

Motorola offers the most extensive group of RF Discrete Transistors offered by any semiconductor manufacturer anywhere in the world today.

From Bipolar to FET, from Low Power to High Power, the user can choose from a variety of packages. They include plastic, metal can and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

Major sub–headings are Small Signal, Medium Power, Power MOSFETs and Bipolar Transistors.

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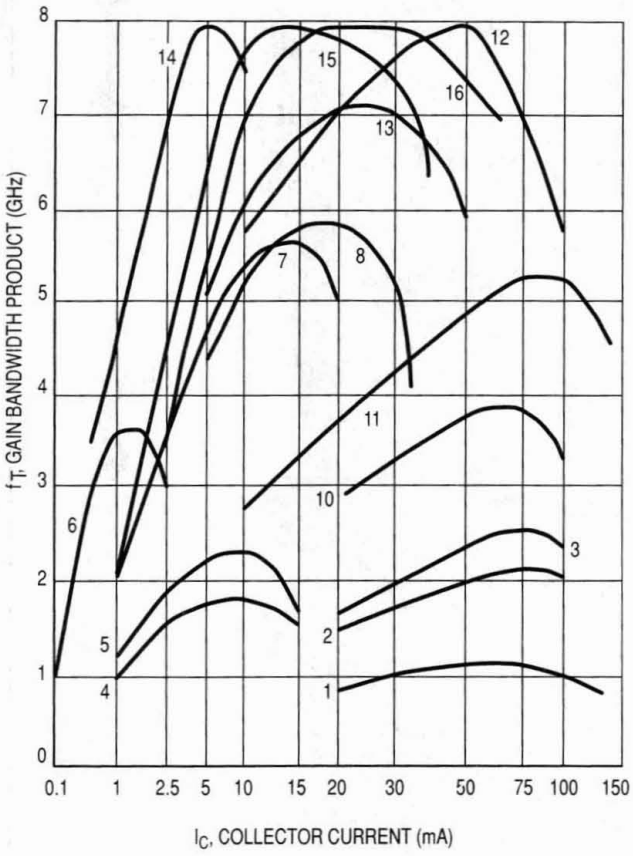
Motorola RF Small Signal Transistors

Motorola's broad line of RF Small Signal Transistors includes NPN and PNP Silicon Bipolar Transistors characterized for low noise amplifiers, mixers, oscillators, multipliers, non–saturated switches and low–power drivers.

These devices are available in a wide variety of package types: plastic Macro–X, ceramic and surface mounted. Most of these transistors are fully characterized with s–parameters.

RF Small Signal Transistor Gain Characteristics



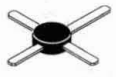
Curve numbers apply to transistors listed in the subsequent tables.

Selection by Package

In small–signal RF applications, the package style is often determined by the end application or circuit construction technique. To aid the circuit designer in device selection, the Motorola broad range of RF small–signal amplifier transistors is organized by package. Devices for other applications such as oscillators or switches are shown in the appropriate preceding tables. **These devices are NPN polarity unless otherwise designated.**

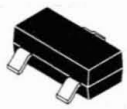
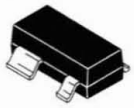
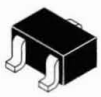
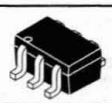
Plastic Packages

Table 1. Plastic

Device	Gain–Bandwidth @ f_T Typ GHz	@ I_C mA	Curve No. Page 1.1–30	NF_{min} @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 317/2 — MACRO–X										
MRF571	8	50	12	1.5	1000	12	1000	10	70	
MRF559	3	100	10	—	—	13	512	18	150	
MRF581	5	75	11	2	500	15.5	500	18	200	
Case 317D/2										
MRF553	—	—	—	—	—	13	175	16	500	
MRF555	—	—	—	—	—	12.5	470	16	400	
MRF557	—	—	—	—	—	9	870	16	400	

Selection by Package (continued)

Table 1. Plastic (continued)

Device	Gain–Bandwidth @ f_T Typ GHz	@ I_C mA	Curve No. Page 1.1–30	NF_{min} @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 318–08/6 — SOT–23										
MMBR521LT1(17,18c)	3.4	–35	—	1.5	500	15	500	–10	–70	
MMBR5031LT1(18c)	1	5	—	2.5	450	17	450	10	20	
BFS17LT1(18c)	1.3	25	—	—	—	—	—	15	—	
BFR92ALT1(18c)	4.5	14	—	—	—	15	—	15	25	
MMBR901LT1(18c)	4	15	7	1.9	1000	12	1000	15	30	
MMBR901LT3(18d)	4	15	7	1.9	1000	12	1000	15	30	
BFR93ALT1(18c)	3.4	30	—	2.5	30	—	—	12	35	
MMBR5179LT1(18c)	1.4	5	4	—	—	15	200	12	50	
MMBR941LT1(18c)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR941LT3(18d)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR941BLT1(18c)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR911LT1(18c)	6	30	8	2	500	17	500	12	60	
MMBR571LT1(18c)	8	50	12	2	500	16.5	500	10	80	
MMBR951LT1(18c)	8	30	16	2.1	2000	7.5	2000	10	100	
MMBR951ALT1(18c)	8	30	16	2.1	2000	7.5	2000	10	100	
Case 318A/1 — SOT–143										
MRF5711LT1(18c)	8	50	12	1.6	1000	13.5	1000	10	70	
MRF5211LT1(17,18c)	4.2	–50	—	2.8	1000	11	1000	–10	–70	
MRF9411LT1(18c)	8	15	15	2.1	2000	9.5	2000	10	50	
MRF5811LT1(18c)	5	75	11	2.0	500	18.4	500	18	200	
MRF9511LT1(18c)	8	30	16	2.1	2000	9	2000	10	100	
Case 419/3 — SC–70/SOT–323										
MRF917T1(18c) ★	6	20	8	2.3	1000	10	1000	12	60	
MRF577T1(18c) ★	7	40	12	1.5	1000	10	1000	10	80	
MRF927T1(18c)	8	5	14	1.7	1000	9.8	1000	10	10	
MRF927T3(18d)	8	5	14	1.7	1000	9.8	1000	10	10	
MRF947T1(18c,d)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF947T3(18d)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF947AT1(18c)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF947BT1(18c,d)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF957T1(18c)	9	30	16	2.0	2000	9	1500	10	100	
Case 419B/16, 17 — SC–70ML/SOT–363										
MRF2947AT1(10,18c)★	9	15	15	1.5	1000	14	1000	10	50	
MRF2947RAT1(10,18c)★	9	15	15	1.5	1000	14	1000	10	50	
Case 463/1 — SC–90/SC–75										
MRF579T1(18c)★	8	40	12	1.5	1000	12	1000	—	80	
MRF949T1(18c)★	9	15	15	1.5	1000	14	1000	—	50	
MRF959T1(18c)★	9	30	15	1.6	1000	8	1000	—	100	

(10)Package contains two transistors.

(17)PNP

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

★New Product

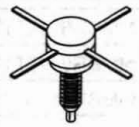
Selection by Package (continued)

Table 1. Plastic (continued)

Device	Gain–Bandwidth @ f_T Typ GHz	Gain–Bandwidth @ I_C mA	Curve No. Page 1.1–30	NF_{min} @ f Typ dB	NF_{min} @ f MHz	Gain @ f Typ dB	Gain @ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	Maximum Ratings I_C mA	Package
Case 751/1 — SO–8										
MRF3866R2[18b]	0.8	50	1	—	—	10.5	400	30	400	
MRF5812R1,R2[18a,b]	5.5	75	11	2	500	15.5	500	15	200	
MRF8372R1,R2[18a,b]	5	75	11	—	—	10	870	16	200	

Ceramic SOE Case

Table 2. Ceramic SOE Case

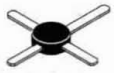
Device	Gain–Bandwidth @ f_T Typ GHz	Gain–Bandwidth @ I_C mA	Curve No. Page 1.1–30	NF @ f Typ dB	NF @ f MHz	Gain @ f Typ dB	Gain @ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	Maximum Ratings I_C mA	Package
Case 244A/1										
MRF587	5.5	90	11	3	500	13	500	15	200	

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

Selection by Application

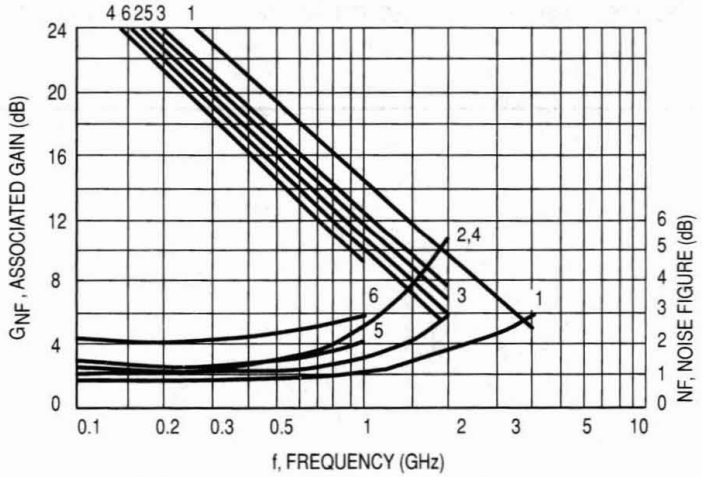
Table 3. Low Noise

The Small–Signal devices listed are designed for low noise and high gain amplifier mixer, and multiplier applications. Each transistor type is available in various packages. **Polarity is NPN unless otherwise noted.**

Package	Name	Case Number	Curve Number (See figure below)					
			1	2[17]	3	4	5	6
	MACRO–X	317/2	—	—	MRF571	MRF581	—	—
	SOT–23	318–08/6	MMBR941LT1 MMBR941LT3 MMBR941BLT1 MMBR951LT1[20]	MMBR521LT1	MMBR571LT1	—	MMBR901LT1 MMBR901LT3	MMBR911LT1
	SC–70/ SOT–323	419/3	MRF917T1 MRF577T1 MRF927T1 MRF927T3 MRF947AT1 MRF947T1 MRF947T3 MRF947BT1 MRF957T1[20]	—	—	—	—	—
	SC–70ML/ SOT–363	419B/ 16, 17	MRF2947AT1 MRF2947RAT1	—	—	—	—	—
	SC–90/ SC–75	463/1	MRF579T1 MRF949T1 MRF959T1	—	—	—	—	—
	SOT–143	318A/1	MRF9411LT1 MRF9511LT1[20]	MRF5211LT1	MRF5711LT1	MRF5811LT1	—	—
	SO–8	751/1	—	—	—	MRF5812R1,R2	—	—

[17]PNP

[20]Higher Current Version



Gain and Noise Figure versus Frequency

Selection by Application (continued)

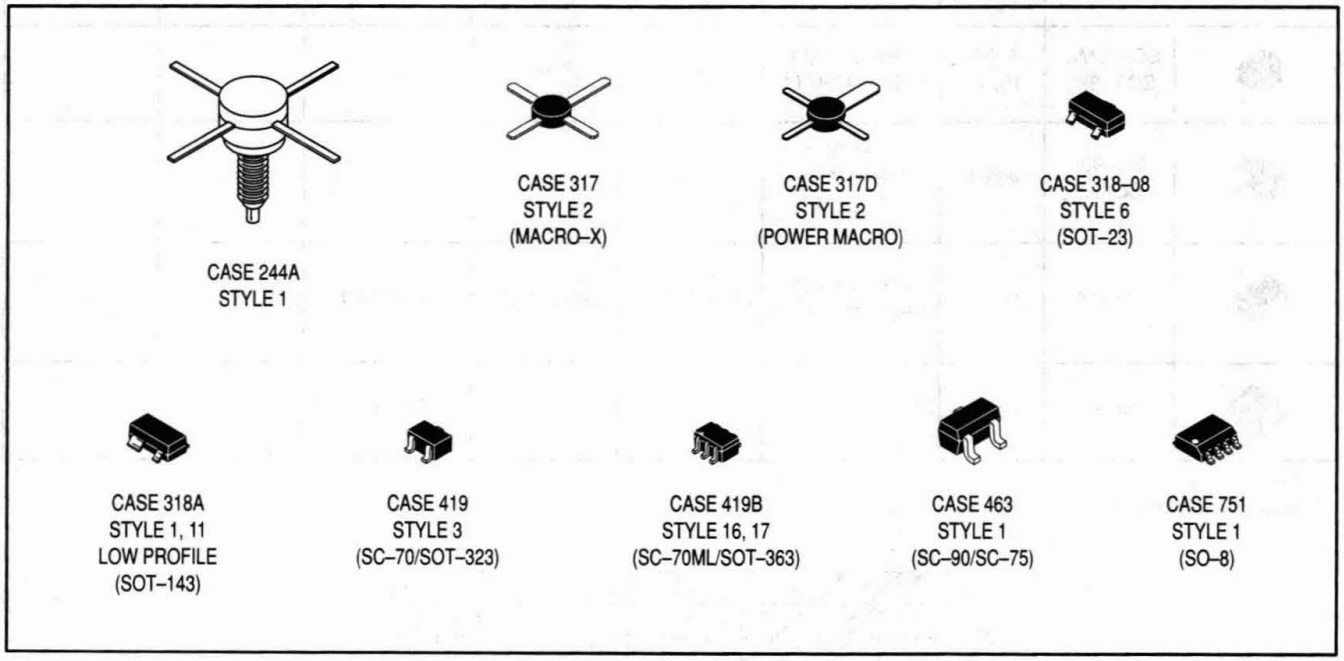
Table 4. CATV, MATV and Class A Linear

For Class A linear CATV/MATV applications. Listed according to increasing gain bandwidth (f_T).

Device	Nominal Test Conditions V_{CE}/I_C Volts/mA	f_T Typ MHz	Noise Figure	Distortion Specifications		$V_{(BR)CEO}$ V	Package/ Style
			Typ/Freq. dB/MHz	3rd Order IMD dBc	Output Level dBmV		
MMBR5179LT1[18c]	6/5	1500	4/450			12	318–08/6
MMBR5031LT1[18c,d]	6/5	2000	1.9/450			10	318–08/6
MRF5812R1,R2[18a,b]	10/75	5000	1.8/500	–65	+50	15	751/1
MRF581	10/75	5000	2.7/300	–65	+50	18	317/2
MRF587	15/90	5500	3/500	–72	+50	17	244A/1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

RF Small Signal Transistors Packages



Motorola RF Medium Power Transistors

RF Medium Power Transistors are used in portable transmitter applications and low voltage drivers for higher power devices. They can be used for analog cellular, GSM and the newer digital handheld cellular phones. GaAs, LDMOS and Bipolar devices are available. RF Medium Power Transistors are supplied in industry standard SOT packages as well as Motorola's high performance PLD line of surface mount power RF packages. Other applications include talkback pagers, wireless modems and LANs, cable modems, highspeed drivers and instrumentation.

Discrete Wireless Transmitter Devices

Device	Freq. MHz	V_{DD} V	Typical Output Power dBm	Typical Drain Eff. %	Typical Gain dB	Semiconductor Technology	Package
3.5 V Applications							
MRF9822T1[18f]★	850	3.5	31.0	70	11	GaAs PHEMT	PLD–1
4.8 V Applications							
MRF9242T1[18f,46a]	900	4.8	31.5	65	9.5	LDMOS	PLD–1
MRF9282T1[18f,46a]	900	4.8	34.0	60	8	LDMOS	PLD–1
5.8 V Applications							
MXR9745T1[18f]★	850	5.8	31.5	60	8.5	LDMOS	SOT–89
MXR9745RT1[18f]★	850	5.8	31.5	60	8.5	LDMOS	SOT–89
MRF9251T1[18c,46a]	900	5.8	23.5	60	10.5	LDMOS	SOT–143
MRF9811T1[18c]★	900	5.8	22	60	15	GaAs MESFET	SOT–143
MRF9745T1[18f]★	900	5.8	30	55	10	LDMOS	PLD–1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

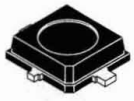
[46]To be introduced: a) 1Q98; b) 2Q98

★New Product

RF Medium Power Transistors Packages

CASE 318A
STYLE 7, 8
(SOT–143)

CASE 345–03
STYLE 8, 9
(SOT–89)



CASE 449
(PLD–1)

Motorola RF High Power Transistors

RF Power MOSFETs

Motorola RF Power MOSFETs are constructed using a planar process to enhance manufacturing repeatability. Th
N–channel field effect transistors with an oxide insulated gate which controls vertical current flow.

Compared with bipolar transistors, RF Power FETs exhibit higher gain, higher input impedance, enhanced thermal stability ar
lower noise. The FETs listed in this section are specified for operation in RF Power Amplifiers and are grouped by frequency range of operation and type of application. Arrangement within each group is first by order of voltage then by increasing output power.

Table 1. To 54 MHz – Vertical MOSFETs

Designed for broadband HF/SSB commercial and industrial applications. The high gain, broadband performance and linear characterization of this device makes it ideal for large–signal, common–source amplifier applications in 12.5 volt mobile and amateur radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	Typical IMD d_3 dB	Typical IMD d_5 dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class AB								
MRF255	55	0.8	16/54	45	–30	–30	1.0	211–11/2

Table 2. To 150 MHz HF/SSB – Vertical MOSFETs

For military and commercial HF/SSB fixed, mobile and marine transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} Typical Gain dB @ 30 MHz	Typical IMD d_3 dB	Typical IMD d_{11} dB	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB							
MRF140	150	4.7	15	–30	–60	0.6	211–11/2
MRF171A[46a]	30	0.45	19	–32	—	1.52	211–07/2
V_{DD} = 50 Volts, Class AB							
MRF148	30	0.5	18	–35	–60	1.5	211–07/2
MRF150	150	3	17	–32	–60	0.6	211–11/2
MRF154	600	12	17	–25	—	0.13	368/2
MRF157	600	6	20	–25	—	0.13	368/2

[46]To be introduced: a) 1Q98; b) 2Q98

Table 3. To 225 MHz VHF AM/FM – Vertical MOSFETs

For VHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Efficiency Typical %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF134	5	0.2	14/150	55	10	211–07/2
MRF136	15	0.38	16/150	60	3.2	211–07/2
MRF136Y	30	1.2	14/150	54	1.8	319B/1
MRF137	30	0.75	16/150	60	1.8	211–07/2
MRF171A(46a)	45	0.56	19/150	65	1.52	211–07/2
MRF173	80	4	13/150	65	0.8	211–11/2
MRF175LV	100	4	14/225	65	0.65	333/1
MRF174	125	8.3	11.8/150	60	0.65	211–11/2
MRF141	150	15	10/175	55	0.6	211–11/2
MRF175GV	200	8	14/225	65	0.44	375/2
MRF141G	300	30	10/175	55	0.35	375/2
V_{DD} = 50 Volts, Class AB						
MRF151	150	7.5	13/175	45	0.6	211–11/2
MRF176GV	200	4	17/225	55	0.44	375/2
MRF151G	300	7.5	16/175	55	0.35	375/2

Table 4. To 500 MHz VHF/UHF AM/FM

For VHF/UHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB – Vertical MOSFETs						
MRF158	2	0.035	17.5/500	52	13.2	305A/2
MRF160	4	0.08	17/500	55	7.2	249/3
MRF166C	20	0.62	15/500	54	2.5	319/3
MRF166W	40	1	13/500	50	1.0	412/1
MRF175LU	100	10	10/400	55	0.65	333/1
MRF177	100	6.4	12/400	60	0.65	744A/2
MRF175GU	150	9.5	12/400	55	0.44	375/2
MRF275L(46a)	100	12.5	9/500	55	0.65	333/2
MRF275G★	150	13.5	10.5/400	55	0.44	375/2
V_{DD} = 50 Volts, Class AB						
MRF176GU	150	6	14/400	50	0.44	375/2

(46)To be introduced: a) 1Q98; b) 2Q98

★New Product

Table 5. To 520 MHz

Designed for broadband VHF & UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{DD} = 7.5 Volts, Class AB – Lateral MOSFET						
MRF1507(18f)★	8	0.6	11/520	65	2.0	466/1
V_{DD} = 12.5 Volts, Class AB – Lateral MOSFET						
MRF1508(18f,46a)	8	0.3	15/520	65	2.0	466/1
V_{DD} = 12.5 Volts, Class AB – Vertical MOSFETs						
MRF5015	15	1.1	11.5/512	55	3.5	319/3
MRF5035	35	6.3	7.5/512	55	1.8	316–01/3

Table 6. To 1.0 GHz – Lateral MOSFETs

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
1.0 GHz, V_{DD} = 26 Volts, Class AB – LDMOS Die						
MRF6522–5(18a,46a)	5	0.06	19/960	55	15	458A/1
MRF6522–10(18a,46a)	10	0.16	18/960	55	6.0	458A/1
800 – 1.0 GHz, V_{DD} = 28 Volts, Class AB – LDMOS Die						
MRF181S(46a)	4	0.16	14/1000	40	3.6	458/1
MRF181Z(46a)	4	0.16	14/1000	40	3.6	458A/1
MRF182	30	1.2	14/1000	60	1.75	360B/1
MRF182S	30	1.2	14/1000	60	1.75	360C/1
MRF183(25)	45	2.3	13/945	36	1.5	360B/1
MRF183S(25)	45	2.3	13/945	36	1.5	360C/1
MRF184	60	1.9	15/1000	60	1.1	360B/1
MRF184S	60	1.9	15/1000	60	1.1	360C/1
MRF185 (3)	85	3.4	14/1000	55	0.7	375B/2
MRF186(3,46a)	120	7.6	12/1000	55	0.6	375B/2

(3)Internal Impedance Matched Push-Pull Transistors

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

(25)Two–tone Performance, Power is PEP

(46)To be introduced: a) 1Q98; b) 2Q98

★New Product

RF Power Bipolar Transistors

Motorola's broad line of bipolar RF power transistors are characterized for operation in RF power amplifiers. Typical applications are in base stations, military and commercial landmobile, avionics and marine radio transmitters. Groupings are by frequency band and type of application. Within each group, the arrangement of devices is by major supply voltage rating, then in the order of increasing output power. All devices are NPN polarity except where otherwise noted.

HF Transistors

Table 1. 1.5 – 30 MHz, HF/SSB

Designed for broadband operation, these devices feature specified Intermodulation Distortion at rated power output. Applications include mobile, marine, fixed station, and amateur HF/SSB equipment, operating from 12.5, 13.6, 28, or 50 volt supplies.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 30 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 or 13.6 Volts, Class AB					
MRF421	100 PEP/CW	10	10	0.6	211–11/1
V_{CC} = 28 Volts, Class AB					
MRF426	25 PEP/CW	0.16	22	2.5	211–07/1
MRF422	150 PEP/CW	15	10	0.6	211–11/1
V_{CC} = 50 Volts, Class AB					
MRF429	150 PEP/CW	7.5	13	0.8	211–11/1
MRF448	250 PEP/CW	15.7	12	0.6	211–11/1

Table 2. 14 – 30 MHz, CB/Amateur Band

These HF transistors are designed for economical, high–volume use in CW, AM and SSB applications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 50 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 or 13.6 Volts, Class AB					
MRF455	60	3	13	1	211–07/1
MRF454	80	5	12	0.7	211–11/1

Table 3. 27 – 50 MHz, Low–Band FM Band

For use in the FM "Low–Band," for Mobile communications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 50 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 or 13.6 Volts, Class AB					
MRF492	70	5.6	11	0.7	211–11/1

VHF Transistors

Table 4. 30 – 200 MHz Band

Designed for Military Radio and Commercial Aircraft VHF bands, these 28–volt devices include the all–gold metallized MRF314/16/17 high–reliability series.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class AB					
MRF314	30	3	10/150	2.2	211–07/1
MRF316[2]	80	8	10/150	0.8	316–01/1
MRF317[2]	100	12.5	9/150	0.65	316–01/1

[2]Internal Impedance Matched

VHF Transistors (continued)

Table 5. 136 – 174 MHz High Band

The "workhorse" VHF FM High–Band is served by Motorola with the broadest range of devices and package combinations in the industry.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 175 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class C					
MRF4427R2[18b]	1	0.016	18[19]	125[1]	751/1
MRF553	1.5	0.11	11.5	25	317D/2
MRF2628	15	0.95	12	4	244/1
MRF1946	30	3	10	1.6	211–07/1
MRF1946A	30	3	10	1.8	145A–09/1
MRF240	40	5	9	2.2	145A–09/1
MRF247[2]	75	15	7	0.7	316–01/1

UHF Transistors

Table 6. 100 – 400 MHz Band

Stringent requirements of the UHF Military band are met by MRF325, 326, 327, 329 and 2N6439 types, with all–gold metal systems, specified ruggedness and programmed wirebond construction, to assure consistent input impedances for internally matched parts.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 400 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C					
MRF325[2]	30	4.3	8.5	2.2	316–01/1
MRF326[2]	40	5	9	1.6	316–01/1
2N6439[2]	60	10	7.8	1.2	316–01/1
MRF327[2]	80	14.9	7.3	0.7	316–01/1
MRF329[2]	100	20	7	0.7	333/1
MRF392[3]	125	19.8	8	0.7	744A/1

Table 7. 400 – 500 MHz Band

Similar to the 100–400 MHz transistors, these devices have bandwidth capabilities operating up to 500 MHz. All have nitride passivated die, gold metal systems, specified ruggedness and controlled wirebond construction to meet the stringent requirements of military space applications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C					
MRF313	1	0.03	15/400	28.5	305A/1
MRF321	10	0.62	12/400	6.4	244/1
MRF323	20	2	10/400	3.2	244/1
MRF338[2]	80	15	7.3/470	0.7	333/1
MRF393[3]	100	18	7.5/500	0.7	744A/1

[1] $R_{\theta JA}$, Thermal Resistance Junction to Ambient.

[2] Internal Impedance Matched

[3] Internal Impedance Matched Push-Pull Transistors

[18] Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[19] Typical

UHF Transistors (continued)

Table 8. 470 – 512 MHz Band

Higher power output devices in this UHF power transistor series feature internally input–matched construction, are designed for broadband operation, and have guaranteed ruggedness under output mismatch and RF overdrive conditions. Devices are specified for handheld, mobile and base station operation.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class C					
MRF581[4]	0.6	0.03	13/500	40	317/2
MRF555	1.5	0.15	10/470	25	317D/2
MRF652	5	0.5	10/512	7	244/1
MRF652S	5	0.5	10/512	7	249/1
MRF653	10	2	7/512	4	244/1
MRF641[2]	15	2.5	7.8/470	4	316–01/1
MRF654[2]	15	2.5	7.8/512	4	244/1
MRF644[2]	25	5.9	6.2/470	1.7	316–01/1
MRF650[2]	50	15.8	5.0/512	1.3	316–01/1
MRF658[2]	65	25	4.15/512	1	316–01/1

900 MHz Transistors

Table 9. 870 – 960 MHz Band

Designed specifically for the 900 MHz mobile radio band, these devices offer superior gain, ruggedness, stability and broadband operation. Devices are for mobile and base station applications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts — Class C — Si Bipolar					
MRF559[5]	0.5	0.08	8/870	50	317/2
MRF581[5]	0.6	0.06	10[19]/870	40	317/2
MRF8372R1,R2[5,18a,b]	0.75	0.11	8/870	45	751/1
MRF557[5]	1.5	0.23	8/870	25	317D/2
MRF842[2,6]	20	5	6/870	1.5	319/1
MRF847[2,6]	45	16	4.5/870	1	319/1

[2]Internal Impedance Matched

[4]Small signal gain. P_o is Typ.

[5]Common Emitter Configuration

[6]Common Base Configuration

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[19]Typical

900 MHz Transistors (continued)

Table 9. 870 – 960 MHz Band (continued)

Device	P_{out} Output Power Watts	Class	P_{in}(Max) Input Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 24 Volts — Si Bipolar						
MRF857S	2.1 (CW)	A	0.4	12.5/900	8.4	305D/1
MRF858	3.6 (CW)	A	0.29	11/900	6.9	319/2
MRF858S	3.6 (CW)	A	0.29	11/900	6.9	319A/2
MRF891	5	AB	0.63	9/900	7	319/2
MRF891S	5	AB	0.63	9/900	7	319A/2
MRF859S	6.5 W (CW)	A	0.46	11.5/900	3.9	319A/2
MRF894(2)	30	C	6	7/900	1.5	319/1
MRF897(3)	30	AB	3	10/900	1.7	395B/1
MRF897R(3)	30	AB	3	10.5/900	1.7	395B/1
MRF898(2)	60	C	12	7/900	1	333A/1
V_{CC} = 26 Volts — Si Bipolar						
MRF6409	20	AB	26/50	10/960	3.8	319/2
MRF6414	50	AB	26/200	8.5/960	1.3	333A/2
MRF899(3)	150	AB	24	8/900	0.8	375A/1

1.5 GHz Transistors

Table 10. 1600 – 1640 MHz Band

Device	P_{out} Output Power Watts	Class	η Eff. (Min) %	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
MRA1600–2	2	C	40	8.4/1600	15	394/1
MRF16006	6	C	40	7.4/1600	6.8	395C/2
MRF3010★	10	AB	45	9.5/1600	3.6	360B/1 (LDMOS)
MRF16030	30	C	40	7.5/1600	1.7	395C/2

Microwave Transistors

Table 11. L–Band Pulse Power

These products are designed to operate in short pulse width, 10 μs, low duty cycle, 1%, power amplifiers operating in the 960–1215 MHz band. All devices have internal impedance matching. The prime application is avionics equipment for distance measuring (DME), area navigation (TACAN) and interrogation (IFF).

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_P (Min) Gain @ 1090 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 18 Volts — Class A & AB Common Emitter					
MRF1000MB	0.2	0.02	10	25	332A/2
V_{CC} = 35 Volts — Class B & C Common Base					
MRF1004MB	4	0.4	10	25	332A/1

(2)Internal Impedance Matched

(3)Internal Impedance Matched Push-Pull Transistors

★New Product

Table 11. L–Band Pulse Power (continued)

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_P (Min) Gain @ 1090 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 50 Volts — Class C Common Base					
MRF1015MB	15	1.5	10	10	332A/1
MRF1035MB	35	3.5	10	5	332A/1
MRF1090MA	90	9	10	0.6	332–04/1
MRF1090MB	90	9	10	0.6	332A/1
MRF1150MA	150	25	7.8	0.3	332–04/1
MRF1150MB	150	25	7.8	0.3	332A/1

Table 12. L–Band Long Pulse Power

These products are designed for pulse power amplifier applications in the 960–1215 MHz frequency range. They are capable of handling up to 10 μs pulses in long pulse trains resulting in up to a 50% duty cycle over a 3.5 millisecond interval. Overall duty cycle is limited to 25% maximum. The primary applications for devices of this type are military systems, specifically JTIDS and commercial systems, specifically Mode S. Package types are hermetic.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 1215 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class C Common Base					
MRF10005	5	0.71	8.5	8	336E/1
V_{CC} = 36 Volts — Class C Common Base					
MRF10031	30	3	10	3	376B/1
MRF10120	120	19	8	0.6	355C/1
V_{CC} = 50 Volts					
MRF10150	150	15	10[7]	0.25	376B/1
MRF10350	350	44	9[7]	0.11	355E/1
MRF10500	500	63	9[7]	0.12	355D/1
MRF10501	500	63	9[7]	0.12	355H/1

Linear Transistors

The following sections describe a wide variety of devices specifically characterized for linear amplification. Included are medium power and high power parts covering frequencies from 100 MHz–4 GHz.

Table 13. To 1 GHz, Class A

These devices offer a selection of performance and price for linear amplification to 1 GHz. The "MRA" prefix parts are input matched and feature high overdrive and extreme ruggedness capability.

Device	P_o @ 1 dB Comp. Point Watts	G_{SS} (Min)/Freq. Small Signal Gain dB/MHz	Bias Point (Vdc/A)	θ_{JC} °C/W	Package/Style
V_{CC} = 19 Volts					
MRA1000–7L	7	9/1000	19/1.2	4	145D–02/1
MRA1000–14L	14	8/1000	19/2.4	2.1	145D–02/1

Device	P_{out} Output Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	Bias Point Per Side (Vdc/MA)	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts					
MRA0510–50H	50	7/1000	28/120	1.4	391–01/1

[7]Typical @ 1090 MHz

Table 14. To 2 GHz, Class A

These parts offer low cost alternatives to matched devices used primarily as pre–drivers to 2 GHz.

Device	P_o @ 1 dB Comp. Point Watts	G_{SS} (Min)/Freq. Small Signal Gain dB/MHz	Bias Point (Vdc/A)	θ_{JC} °C/W	Package/Style
V_{CC} = 20 Volts					
MRF3095[9]	0.8	9/2000	20/0.12	35	328A/2

Table 15. UHF Ultra Linear For TV Applications

The following device has been characterized for ultra–linear applications such as low–power TV transmitters in Band IV and Band V and features diffused ballast resistors and an all–gold metal system to provide enhanced reliability and ruggedness.

Device	P_{ref} (Min) Watts	Gp (Min)/Freq. Small Signal Gain dB/MHz	3 Tone IMD[8] dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class AB					
TPV8100B	100[11]	8.5/860	—	0.7	398/1

[8]Vision Carrier: – 8 dB; Sound Carrier: – 7 dB; Sideband Carrier: – 16 dB

[9]Former Prefix was "RF"

[11]Output power at 1 dB compression in Class AB

Table 16. Microwave Linear for PCN Applications

The following devices have been developed for linear amplifiers in the 1.5–2 GHz region and have characteristics particularly suitable for PDC, PCS or DCS1800 base station applications.

Device	P_{out} Watts	Class	Bias Point Vdc/mA	Gain (Typ)/Freq dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 20 Volts–Bipolar Die						
MRF6401[12]	0.5	A	20/80	10/1880	30	305C/1
V_{CC} = 26 Volts–Bipolar Die						
MRF6402[13]	4.5	AB	26/40	10/1880	5	319/2
MRF6404[16]	30	AB	26/150	8.5/1880	1.4	395C/1
MRF6404K	30	AB	26/150	8.5/1880	1.4	395C/1
MRF6408	12	AB	26/100	8.8/1880	2.8	395C/1
MRF15030	30	A, AB	26/125	9/1490	1.4	395C/1
MRF15060	60	A, AB	26/200	10/1490	0.7	451/1
MRF15060S	60	A, AB	26/200	10/1490	0.7	451A/1
MRF15090	90	A, AB	26/250	7.5/1490	0.7	375A/1
MRF20030★	30	A, AB	26/120	10.5/2000	1.4	395D/1
MRF20060★	60	A, AB	26/200	9.4/2000	0.7	451/1
MRF20060S★	60	A, AB	26/200	9.4/2000	0.7	451A/1
V_{DD} = 26 Volts–LDMOS Die – Lateral MOSFETs						
MRF281S[46a]	4	A, AB	26/25	13.6/2000	8.75	458/1
MRF281Z[46a]	4	A, AB	26/25	13.6/2000	8.75	458A/1
MRF6525–5[18a,46a]	5	AB	26/70	11.5/2000	15	458A/1
MRF6525–10[18a,46a]	10	AB	26/130	10/2000	6.0	458A/1
MRF282S★	10	A, AB	26/75	13/2000	2.9	458/1
MRF282Z★	10	A, AB	26/75	13/2000	2.9	458A/1
MRF284 ★	30	A, AB	26/200	10.5/2000	2.0	360B/1
MRF284S★	30	A, AB	26/200	10.5/2000	2.0	360C/1
MRF286[46b]	60	A, AB	26/500	11/2000	.73	465/1
MRF286S[46b]	60	A, AB	26/500	11/2000	.73	465A/1

[12]Formerly known as "TP4001S"

[13]Formerly known as "TP4004"

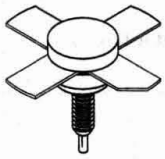
[16]Formerly known as "TP4035"

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

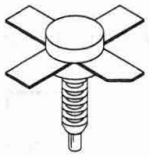
[46]To be introduced: a) 1Q98; b) 2Q98

★New Product

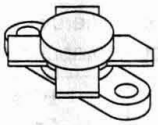
RF Power MOSFETs and Bipolar Transistors Packages



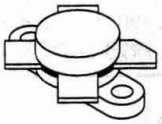
CASE 145A–09
STYLE 1
(.380″ STUD)



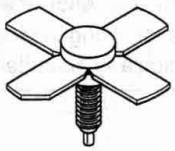
CASE 145D–02
STYLE 1
(.380″ SOE)



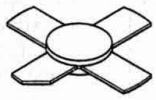
CASE 211–07
STYLE 1, 2
(.380″ FLANGE)



CASE 211–11
STYLE 1, 2
(.500″ FLANGE)

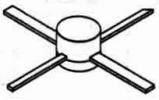


CASE 244
STYLE 1
(.280″ STUD)

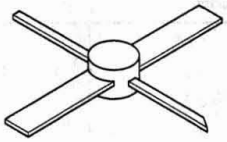


CASE 249
STYLE 1, 3
(.280″ PILL)

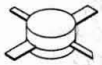
CASE 305
STYLE 1
(.204″ STUD)



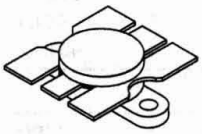
CASE 305A
STYLE 1, 2
(.204″ PILL)



CASE 305C
STYLE 1

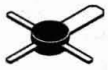


CASE 305D
STYLE 1

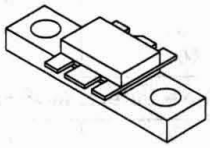


CASE 316–01
STYLE 1, 3
(.500″ CQ)

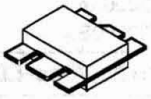
CASE 317
STYLE 1, 2
(MACRO–X)



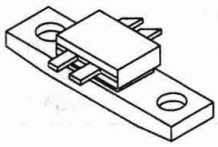
CASE 317D
STYLE 2



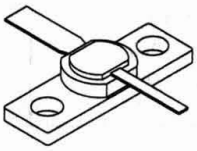
CASE 319
STYLE 1, 2, 3
(CS–12)



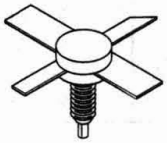
CASE 319A
STYLE 2



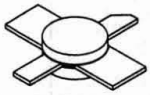
CASE 319B
STYLE 1



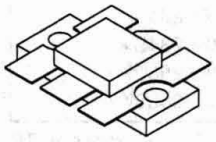
CASE 328A–03
STYLE 1, 2



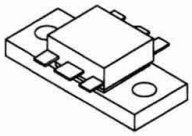
CASE 332–04
STYLE 1, 2
(.280″ STUD)



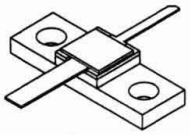
CASE 332A
STYLE 1, 2
(.280″ PILL)



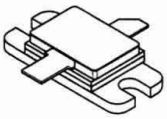
CASE 333
STYLE 1, 2



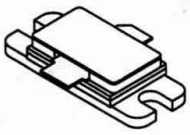
CASE 333A
STYLE 1, 2
(MAAC PAC)



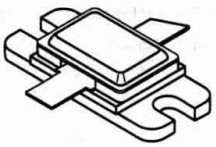
CASE 336E
STYLE 1



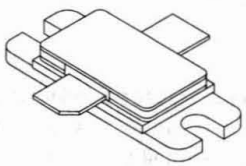
CASE 355C
STYLE 1



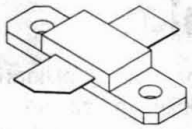
CASE 355D
STYLE 1



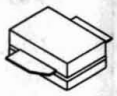
CASE 355E
STYLE 1



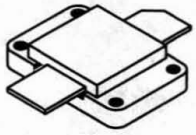
CASE 355H–01
STYLE 1



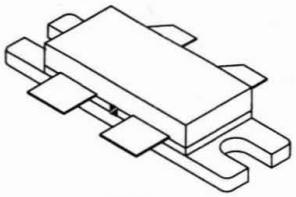
CASE 360B
STYLE 1
(Micro 250)



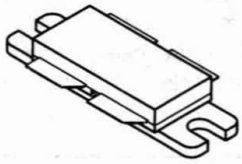
CASE 360C
STYLE 1



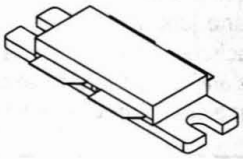
CASE 368
STYLE 2
(HOG PAC)



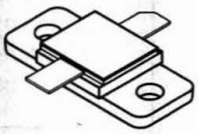
CASE 375
STYLE 2



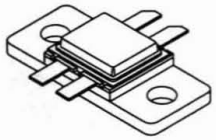
CASE 375A
STYLE 1



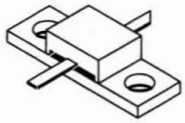
CASE 375B
STYLE 2
(Micro 860)



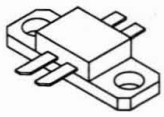
CASE 376B
STYLE 1



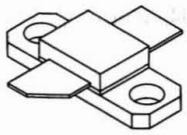
CASE 391
STYLE 1



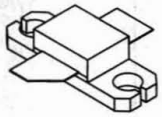
CASE 394
STYLE 1



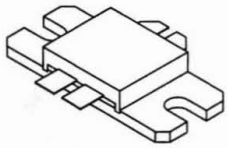
CASE 395B
STYLE 1



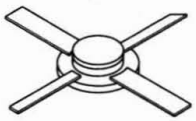
CASE 395C
STYLE 1, 2



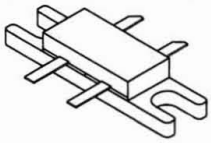
CASE 395D
STYLE 1



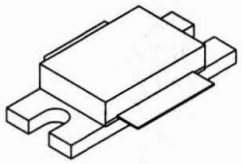
CASE 398
STYLE 1



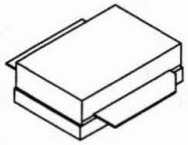
CASE 400
STYLE 1



CASE 412
STYLE 1



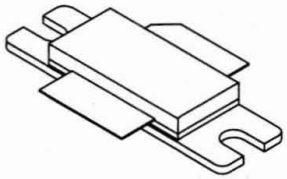
CASE 451
STYLE 1



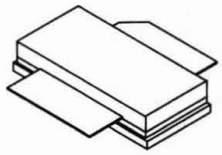
CASE 451A
STYLE 1

CASE 458
STYLE 1

CASE 458A
STYLE 1

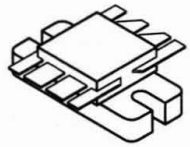


CASE 465
STYLE 1



CASE 465A
STYLE 1

CASE 466
STYLE 1



CASE 744A
STYLE 1, 2

CASE 751
STYLE 1
(SO–8)

Motorola RF Amplifier Modules

Motorola's line of RF amplifiers designed and specified for use in land mobile radios and general purpose wideband amplification applications. They feature small size, matched inputs and outputs, high stability and guaranteed performance specifications. For the user, they offer the benefits of smaller and less complex system designs in less time and at lower overall cost.

Each amplifier uses modern transistor chips which are gold metallized and have silicon nitride passivation for increased reliability and long life. Chip and wire construction features MOS capacitors and laser trimmed nichrome resistors. Circuit substrates and metallization have been selected for optimum performance cost and reliablity.

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Motorola RF Amplifier Modules

Complete amplifiers with 50 ohm in/out impedances are available for a variety of applications including land mobile radios, base stations, and other uses requiring large–signal amplification, both linear and Class C. Frequencies covered range from 68–1990 MHz with power levels extending to 180 watts.

Land Mobile/Portable

The advantages of small size, reproducibility and overall lower cost become more pronounced with increasing frequency of operation. These amplifiers offer a wide range in power levels and gain, with guaranteed performance specifications for bandwidth, stability and ruggedness.

Table 1. VHF/UHF, Class C

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
136–174 MHz, VHF Band — (LDMOS Die) – Lateral MOSFETs						
MHW2627–1[46b]	7	0.02	136–174	25.5	7.5	420AC/1

Device	P_{sat} Watts	ACP (P_{out} = 1.6 W @ f_o ±25 kHz, 18 kHz BW) (dBc)	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
380–470 MHz, Land Mobile Linear (for TransEuropean Trunked Radio – TETRA) — Class AB — (LDMOS Die) – Lateral MOSFETs						
MHW2701–1[46b]	4.5	–30	380–430	28	7	420Z/1
MHW2701–2[46b]	4.5	–30	420–470	28	7	420Z/1

Device	P_{sat} Watts	ACP (P_{out} = 5 W @ f_o ±25 kHz, 18 kHz BW) (dBc)	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
380–470 MHz, Land Mobile Linear (for TransEuropean Trunked Radio – TETRA) — Class AB — (LDMOS Die) – Lateral MOSFETs						
MHW2703–1[46b]	10	–30	380–400	28	7	420Z/1
MHW2723[46b]	12	–30	380–470	30	12.5	420Z/1

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
400–520 MHz, UHF Band — Class D – A (Dynamic Bias via Gate Control) — (LDMOS Die) – Lateral MOSFETs						
MHW2727–1[46b]	7	0.02	400–470	25.5	7.5	420AC/1
MHW2727–2[46b]	7	0.02	450–520	25.5	7.5	420AC/1
806–821 MHz, UHF Band (for Integrated Digital Enhanced Network – iDEN™)— Class AB — (LDMOS Die) – Lateral MOSFETs						
MHW2801 [46a]	0.8	0.00025	806–821	35	6	420L/1

[46]To be introduced: a) 1Q98; b) 2Q98

Land Mobile/Portable (continued)

Table 1. VHF/UHF, Class C (continued)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
806 – 960 MHz, UHF Band — Class AB (LDMOS Die) – Lateral MOSFETs						
MHW2803[46a]	3.5	0.001	806–824	35.5	6	420L/1
MHW2805–1[46a]	5	0.004	806–870	31	7.5	420AB/1
MHW2805–2[46a]	5	0.004	890–950	31	7.5	420AB/1
MHW2820–1[46b]	20	<0.250	806–870	19	12.5	301G/1[42]
MHW2820–2[46b]	18	<0.300	890–950	17.9	12.5	301G/1[42]
MHW2821–1	20	<0.250	806–870	19	12.5	301AB/1
MHW2821–2	18	<0.300	890–950	17.9	12.5	301AB/1

Table 2. UHF, Linear – Lateral MOSFETs

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
824–849 MHz (for Amps) — Class AB (LDMOS Die)						
MIM2901[46a]	1.41	0.004	824–849	25.5	3.6	TBD
880–915 MHz (for GSM) — Class AB (LDMOS Die)						
MIM2906[46a]	3.5	0.316	890–915	30.5	6	467A/1

Base Stations

Designed for applications such as a driver for a macro cell site or the final output in micro cell site, these class AB amplifiers are ideal for GSM based systems at 900 MHz and 2 GHz. These 50 ohm blocks provide 10 to 30 watt outputs with gains up to 30 dB in a compact hybrid module package.

Table 1. Base Stations

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
925–960 MHz (for GSM) — Class AB (LDMOS Die) – Lateral MOSFETs						
MHW910[46a]	10	0.050	925–960	23	24	301AB/1
MHW913	14	0.1	880–915	21.5	12.5	301AB/1
MHW916	16	0.036	925–960	26.5	26	301AB/1
MHW930★	30	0.060	925–960	27	26	301AB/1

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
1805–1880 MHz (for DCS1800) — Class AB (Silicon Bipolar Die)						
MHW1815★	15.0	0.015	1805–1880	30	26	301AK/1
1930–1990 MHz (for PCS1900) — Class AB (Silicon Bipolar Die)						
MHW1915★	15.0	0.019	1930–1990	29	26	301AK/1
MHW1916★	15.0	0.013	1930–1990	31	26	301AK/1

[42]Drop–in for bipolar MHW820

[46]To be introduced: a) 1Q98; b) 2Q98

★New Product

Table 2. Cellular Base Station Pre–Drivers

These 50 ohm amplifiers are recommended for modern, multi–tone, CDMA and/or TDMA base–station pre–driver applications. Their high third–order intercept, tight phase control and excellent group delay characteristics make these amplifiers ideal for use in high–power feedforward loops.

Ultra–Linear – Class A (Silicon Bipolar Die)

Device	BW MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm/MHz	NF (Typ) dB	Case/ Style
MHL9128	800–960	28	400	20	0.5	31	43	7.5	448/1

Ultra–Linear – Class A (LDMOS Die) – Lateral MOSFETs

Device	BW MHz	V_{DD} (Nom.) Volts	I_{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm/MHz	NF (Typ) dB	Case/ Style
MHL9236[46a]	800–960	26	525	30	.1	34	47	4.5	301AP/1
MHL9236M[46a]	800–960	26	525	30	.1	34	47	4.5	301AP/2

Wideband Linear Amplifiers

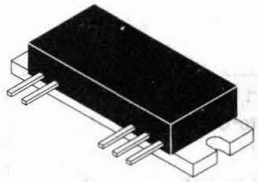
Table 1. Standard 50 Ohm Linear Hybrids

This series of RF linear hybrid amplifiers have been optimized for wideband, 50 ohm applications. These amplifiers were designed for multi–purpose RF applications where linearity, dynamic range and wide bandwidth are of primary concern. Each amplifier is available in various package options. The MHL series utilizes a new case style that provides microstrip input and output connections.

Device	BW MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain/Freq. (Typ) dB/MHz	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept Point/Freq. (Typ) dBm/MHz	NF/Freq. (Typ) dB/MHz	Case/ Style
CA2832C	1–200	28	435	35.5/100	0.5	33	47/200	5/200	714F/1
CA2830C	5–200	24	300	34.5/100	0.5	29	46/200	4.7/200	714F/1
CA2810C	10–450	24	310	34/50	1.5	30	43/300	5/300	714F/1
MHL8118	40–1000	28	400	17.5/900	1	30	41.5/1000	8.5/1000	448/1
MHL8115	40–1000	15	700	17.5/900	1	30	41.5/1000	8.5/1000	448/2
MHL8018	40–1000	28	210	18.5/900	1	26	38/1000	7.5/1000	448/1
MHL8015	40–1000	15	380	18.5/900	1	26	38/1000	7.5/1000	448/2

[46]To be introduced: a) 1Q98; b) 2Q98

RF Amplifier Modules Packages



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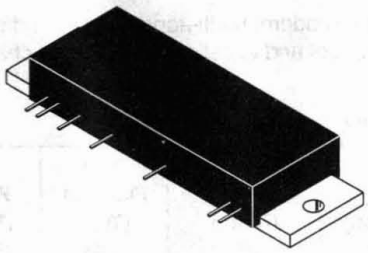

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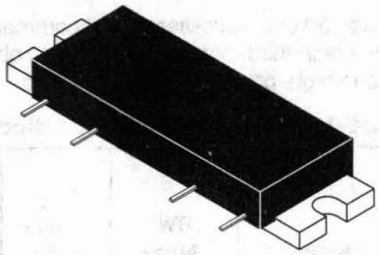

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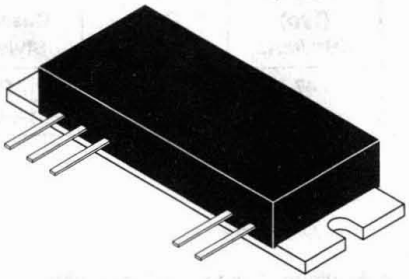

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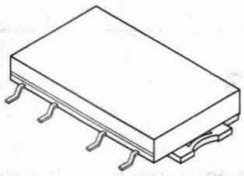

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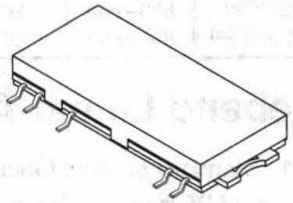

CASE 420AC
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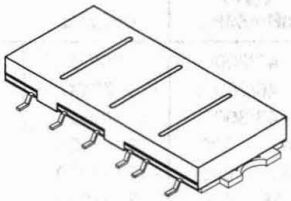

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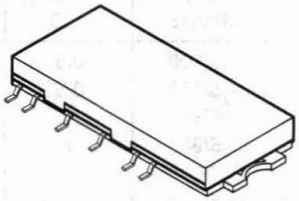

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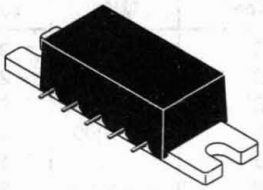

CASE 448
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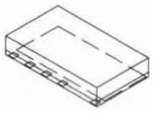

CASE 467A
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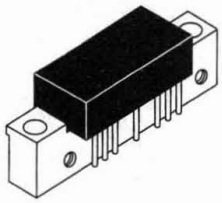

CASE 714F
STYLE 1

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

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Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifiers

40–1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
MHW9182	18	152	+38	−59(40)	−59	−59	8.0	714Y/1
MHW9242	24	152	+38	−59(40)	−58	−59	8	714Y/1

40–860 MHz Hybrids

Device	Gain dB Typ	Frequency MHz	V_{CC} Volts	2nd Order IMD @ V_{out} = 50 dBmV/ch Max	DIN45004B @ f=860 MHz dBμV Min	Noise Figure @ 860 MHz dB Max	Package/ Style
CA901	17	40 – 860	24	−60	120	8	714P/2
CA901A	17	40 – 860	24	−64	120	8	714P/2
Power Doubling Hybrids							
CA912	17	40 – 860	15	−63	123	9.5	714P/3
CA922	17	40 – 860	24	−63	123	9.5	714P/2
CA922A	17	40 – 860	24	−67	123	9.5	714P/2
Hybrid Jumper							
CATHRU	0	1 – 1000	75 Ohm Broadband Hybrid Jumper				714V

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
MHW8182	18	128	+38	−60(40)	− 60	− 60	7	714Y/1
MHW8182A ★	18.3	128	+38	−63(40)	− 62	− 64	8.0	714Y/1
MHW8222	22	128	+38	−60(40)	− 60	− 60	7.5	714Y/1
MHW8242	24	128	+38	−60(40)	− 60	− 60	7.5	714Y/1
MHW8242A★	24	128	+38	−62(40)	− 64	− 62	7.5	714Y/1
MHW8272	27	128	+38	−60(40)	− 60	− 60	7.0	714Y/1
MHW8272A ★	27.2	128	+38	−64(40)	− 64	− 62	7.0	714Y/1
MHW8292	29	128	+38	−56(40)	− 60	− 60	7.0	714Y/1

(40)Composite 2nd Order; V_{out} = +38 dBmV/ch

★New Product

CATV Distribution: Forward Amplifiers (continued)

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A (continued)

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
Power Doubling Hybrids								
MHW8185★	18.8	128	+40	–62[39]	– 64	– 64	8.0	714Y/1
MHW8185L[21,46b,52a]	18.9	128	+40	–62[39]	– 63	– 64	8.0	714Y/1
MHW8185R[14]★	18.8	128	+40	–62[39]	– 64	– 64	8.0	714Y/2
MHW8205★	19.8	128	+40	–60[39]	– 63	– 64	8.0	714Y/1
MHW8205L[22,46b,52a]	19.8	128	+40	–62[39]	– 63	– 64	8.0	714Y/1
Feedforward Hybrids								
MFF524B	24	128	+44	–68[36]	– 66	—	13.0	825A/2

40–750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Cross Modulation FM = 55.25 MHz dB 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
MHW7142	14	110	+40	–60[39]	– 62	– 66	8.0	714Y/1
MHW7182	18	110	+40	–62[39]	– 62	– 64	6.5	714Y/1
MHW7182A★	18.3	110	+40	–62[39]	– 62	– 64	6.5	714Y/1
MHW7222	22	110	+40	–55[39]	– 60	– 60	7	714Y/1
MHW7222A★	22	110	+40	–57[39]	– 60	– 60	7	714Y/1
MHW7242	24	110	+40	–60[39]	– 60	– 60	7	714Y/1
MHW7242A★	24	110	+40	–62[39]	– 63	– 61	7	714Y/1
MHW7272	27	110	+40	–60[39]	– 60	– 60	6.5	714Y/1
MHW7272A★	27.2	110	+40	–64[39]	– 64	– 60	6.5	714Y/1
MHW7292	29	110	+40	–60[39]	– 60	– 60	6.5	714Y/1
Power Doubling Hybrids								
MHW7185C★	18.8	110	+44	–64[36]	–62	–63	7.5	714Y/1
MHW7185CR[15]★	18.8	110	+44	–64[36]	–62	–63	7.5	714Y/2
MHW7185L[23,46b,52a]	18.9	110	+44	–64[36]	–61	–63	7.5	714Y/1
MHW7205C★	19.8	110	+44	–63[36]	–61	–62	7.5	714Y/1
MHW7205L[24,46b,52a]	19.8	110	+44	–63[36]	–61	–62	7.5	714Y/1
Feedforward Hybrids								
MFF424B	24	110	+44	–70[36]	–68	—	13	825A/2

[14]Forward Mirror Amplifier Version of MHW8185
[15]Forward Mirror Amplifier Version of MHW7185C
[21]Low DC Current Version of MHW8185
[22]Low DC Current Version of MHW8205
[23]Low DC Current Version of MHW7185C
[24]Low DC Current Version of MHW7205C
[36]Composite 2nd order; V_{out} = +44 dBmV/ch
[39] Composite 2nd order; V_{out} = +40 dBmV/ch
[46]To be introduced: a) 1Q98; b) 2Q98
[52]Engineering samples available: a) 2Q98
★New Product

CATV Distribution: Forward Amplifiers (continued)

40–600 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 87 CH	Cross Modulation dB 87 CH	Noise Figure @ 600 MHz dB Max	Package/ Style
MHW6182–6	18	87	+44	–56[36]	–57	–55	6	714Y/1
Feedforward Hybrids								
MFF324B	24	85	+44	–86[38]	–73	–68	12.5	825A/2

40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 77 CH	Cross Modulation dB 77 CH	Noise Figure @ 550 MHz dB Max	Package/ Style
MHW6142	14	77	+44	–72[35]	–59	–62	7.5	714Y/1
MHW6182	18	77	+44	–72[35]	–58	–62	7	714Y/1
MHW6222	22	77	+44	–66[35]	–57	–57	6	714Y/1
MHW6272	27	77	+44	–64[35]	–57	–57	6.5	714Y/1
MHW6342	34	77	+44	–64[35]	–57	–57	6.5	714Y/1
MHW6342T★	34	77	+44	–64[35]	–57	–57	6.5	714AA/1
Feedforward Hybrids								
MFF224B	24	77	+44	–86[35]	–75	–70	11	825A/2

40–450 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 60 CH	Cross Modulation dB 60 CH	Noise Figure @ 450 MHz dB Max	Package/ Style
MHW5182A	18	60	+46	–72[31]	–61	–59	6.5	714Y/1
MHW5222A	22	60	+46	–72[31]	–60	–59	5.5	714Y/1
MHW5342A	34	60	+46	–68[31]	–59	–59	6.0	714Y/1
MHW5342T★	34	60	+46	–68[31]	–59	–59	6.0	714AA/1
MHW5382A	38	60	+46	–64[31]	–59	–59	5.0	714Y/1
Power Doubling Hybrids								
MHW5185B	18	60	+46	–67[32]	–67	–67	7.0	714Y/1
Feedforward Hybrids								
MFF124B	24	60	+46	–84[31]	–79	–75	10	825A/2

[31]Channels 2 and M13 @ M22

[32]Composite 2nd order; V_{out} = +46 dBmV/ch

[35]Channels 2 and M30 @ M39

[36]Composite 2nd order; V_{out} = +44 dBmV/ch

[38]Channels 2 and M39 @ M48

★New Product

Reverse Amplifiers

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test[30] dB	Composite Triple Beat dB: 22 CH	Composite Triple Beat dB: 26 CH	Cross Modulation dB: 22 CH	Cross Modulation dB: 26 CH	Noise Figure @ 175 MHz dB Max	Package/ Style
MHW1134	13	22	+50	–72	–73	–71[19]	–65	–65[19]	7	714Y/1
MHW1184	18	22	+50	–72	–70	–70[19]	–64	–64[19]	5.5	714Y/1
MHW1224	22	22	+50	–72	–69	–68.5[19]	–62	–62[19]	5.5	714Y/1
MHW1244	24	22	+50	–72	–68	–67.5[19]	–61	–61[19]	5	714Y/1

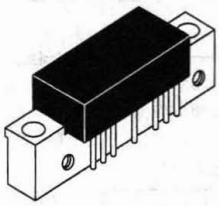
Low Current Amplifiers — 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test[30] dB	Composite Triple Beat dB: 4 CH	Cross Modulation dB: 4 CH	Noise Figure @ 50 MHz dB Max	Package/ Style
MHW1304L	30	4	135	+50	–70	–66	–57	4.5	714Y/1

[19]Typical

[30]Channels 2 and A @ 7

RF CATV Distribution Amplifiers



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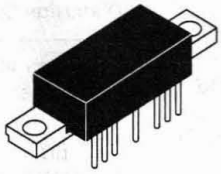

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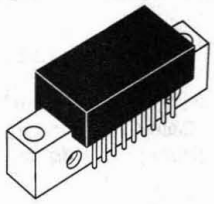

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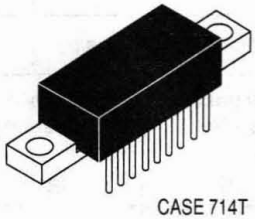

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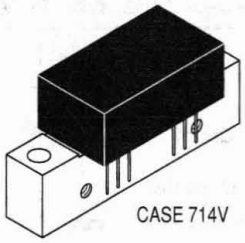

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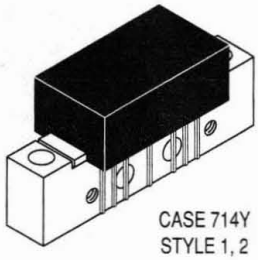

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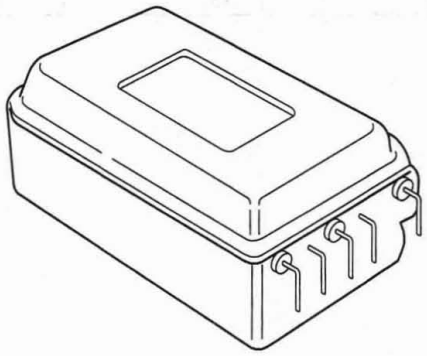

CASE 825A
STYLE 2

Chapter Two
RF Monolithic Integrated Circuits

Section One **2.1–0**
RF Monolithic Integrated Circuits – Selector Guide

Section Two **2.2–0**
RF Monolithic Integrated Circuits – Data Sheets

Section One
Selector Guide

Motorola RF Monolithic Integrated Circuits

Motorola's RF monolithic integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SOIC–8, SOIC–16, SOT–143, TSSOP–16, Micro–8, TSSOP–20, TSSOP–20HS, TQFP–48 or PFP–16 packages.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

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Motorola RF Monolithic Integrated Circuits

Switching

Antenna Switches/Local Oscillator Switches

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current μA (Typ)	P_{in}, 1 dB Compression dBm (Typ)	TX Insertion Loss dB (Typ)	Isolation dB (Typ)	Package	System Applicability
MRFIC1801[18b]	1500–2500	2.7–5.5	300	29	0.6	20	SO–8	DECT, PHS, PCS, ISM
MRFIC0903[18b]	100–2000	2.7–5.0	60	35.5	0.65	21	SO–8	AMPS, Class 4&5 GSM, DCS1800, PHS, PCS

Receiver Functions

General Purpose Integrated Circuits

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915[18c,46a]	100–2000	2.7–5.0	2.2	16.5	1.9	38	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS
MRFIC0916[18c]	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	Input Third Order Intercept	Package	System Applicability
MRF9820T1[18c]★	100–1500	2–5	1.0	16	–3	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS

900 MHz Front End

LNA + Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2001[18b]	500–1000	0–250	2.7–5.0	4.7	23	–10	SO–8	CT2, ISM

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

★New Product

Receiver Functions (continued)

1.5 – 2.2 GHz Front End

Integrated LNA

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC1501[18b] ★	1000–2000	3–5	5.7	18	1.1	26	SO–8	GPS
MRFIC1808[18b] ★	1700–2100	2.7–4.5	5.0	17	1.6	37	SO–8	DECT, PHS, PCS
MRFIC1808DM[18g,46a]	1700–2100	2.7–4.5	5.0	17	1.6	32	Micro–8	DECT, PHS, PCS

GPS Receiver

MRFIC1502★	1570–1580	4.5–5.5	50	65	9.5	—	TQFP–48	GPS

Integrated LNA/Downconverter

Device	RF Freq. Range GHz	IF Freq. Range GHz	Supply Volt. Range Vdc	Supply Current RX Mode mA (Typ)	Mixer Conv. Gain dB (Typ)	LNA Gain dB (Typ)	LNA Noise Figure dB (Typ)	Package	System Applicability
MRFIC1804[18b]	1.8–2.0	70–325	2.7–3.3	10	4	14	2.3	SO–16	DECT,PHS,PCS
MRFIC1814[18b] ★	1.8–2.0	70–325	2.7–4.5	13	8	17	2.5	TSSOP–16	DECT,PHS,PCS

2.4 GHz Front End

Integrated LNA/Downconverter

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	LNA Noise Figure dB (Typ)	Isolation Lo to RF, Lo to IF dB (Typ)	Package	System Applicability
MRFIC2401[18b]	2400–2500	100–350	4.75–5.25	9.5	21	1.9	20	SO–16	WLAN, MMDS, ISM

Transmitter Functions

General Purpose Integrated Circuits

Quadrature Modulator

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Gain Control dB (Typ)	Lo Leakage dBm (Typ)	SSB P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC0001[18b]	50–260	2.7–5.5	10	30	–55	–10	TSSOP–20	DCS1800, GSM, NADC PDC, PHS, PCS1900

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915[18c,46a]	100–2000	2.7–5.0	2.2	16.5	1.9	38	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS
MRFIC0916[18c]	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

★New Product

900 MHz Transmit Chain

Transmit Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2002[18b]	500–1000	0–250	2.7–5.0	5.5	0.1	10	–18	SO–8	AMPS,CT1,CT2, GSM, IS–54, ISM
MRFIC2101[18b]	800–1000	0–250	3–4.75	45	2	26.5	4.5	SO–16	AMPS,CT1,CT2, GSM, IS–54, ISM, USPCS, CDMA
MRFIC0931[18b]★	500–2000	0–250	2.7–4.8	38	—	25	1.0	SO–8	AMPS,CT1,CT2, GSM, IS–54, ISM, USPCS, CDMA

Driver Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Gain Control dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2004[18b]	800–1000	2.7–4.0	11	0.7	21.5	34	–1	SO–16	AMPS,CT1,CT2, GSM,ISM
MRFIC2006[18b]	500–1000	1.8–4.0	46	—	23	—	15.5	SO–8	AMPS,CT1,CT2, GSM,ISM
MRFIC0904[18b]	800–1000	2.7–5.0[47]	280	0.05	27	24.5	25.5	SO–16	AMPS,GSM,ISM

Integrated Power Amplifiers

Low Power 900 MHz Power Amplifiers

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Return Loss Input/Output dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2006[18b]	500–1000	1.8–4.0	46	23	15	15.5	SO–8	Silicon

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2101[18b]	800–1000	3 – 4.75	38	2	16	18	SO–16	Silicon

Analog Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0910[18e,46a]	824–905	4.8	50	17.8	–40	30.8/13	PFP–16	LDMOS
MRFIC0912[18e]★	824–905	4.6[47]	55	23.8	–25	30.8/7	PFP–16	GaAs

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

[47] Negative supply required

★New Product

Transmitter Functions: 900 MHz Transmit Chain: Integrated Power Amplifiers (continued)

GSM Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0913[18e]★	880–915	4.8[47]	48	24.5	–30	34.5/10	PFP–16	GaAs
MRFIC0917[18e]★	880–915	3.6[47]	43	22	–30	34/12	PFP–16	GaAs

DCS1800, PCS1900

Device	Freq. Range GHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC1818[18e]★	1.7–1.9	4.8[47]	35	30	–30	33/3	PFP–16	GaAs
MRFIC1817[18e]★	1.7–1.9	3.6[47]	35	27	–30	32/5	PFP–16	GaAs

Two–way Paging, ISM

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Typ)	Package	Semiconductor Technology
MRFIC0920[18b,46b]	890–950	3.4	35	28	–45	30.5/2.5	TSSOP–20HS	LDMOS

1.5 – 2.2 GHz Transmit Chain

Upconverter

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803[18b]	1.7–2.5	2.7–5.0	28	100	10	70–350	–2	SO–16	DECT,PHS, PCS
MRFIC1813[18b]★	1.7–2.5	2.7–4.5	25	100	15	70–350	3	TSSOP–16	CDMA,PCS
MRFIC0931[18b]★	0.5–2.0	2.7–4.8	38	—	20	0–250	–2	SO–8	CDMA,PCS

Power Amplifier

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc[47]	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}/P_{in} dBm (Typ)	1 dB Comp. dBm (Typ)	Pkg	System Applicability
MRFIC1805[18b]★	1.7–2.5	2.7–5.0	170	—	21	21.5/2	24	TSSOP–16	DECT,PHS, PCS
MRFIC1806[18b]	1.5–2.5	3.0–5.0	115	0.25	23	19.5/–3	21	SO–16	DECT,PHS, PCS
MRFIC1807[18b]	1.5–2.2	3.0–5.0	325	0.06	8	26.8/20	25	SO–16	DECT,PHS, PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 1Q98; b) 2Q98

[47]Negative supply required

★New Product

Transmitter Functions: 1.5 – 2.2 GHz Transmit Chain (continued)

Power Amplifier

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	PA Supply Current TX Mode mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Insertion Loss RX Mode dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC1807[18b] (Including TX/RX Switch)	1.5–2.2	3.0–5.0	325	0.06	8	1	25	SO–16	DECT, PHS, PCS

2.4 GHz Transmit Chain

Exciter Amplifier

Device	Freq. Range GHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2404[18b]	2.0–3.0	4.75–5.25	9	17	4.3	5	SO–8	WLAN, MMDS, ISM

Power Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Power Control Range dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2403[18b]	2200–2700	4.75–5.25	95	23	20	19	SO–16	WLAN, MMDS, ISM

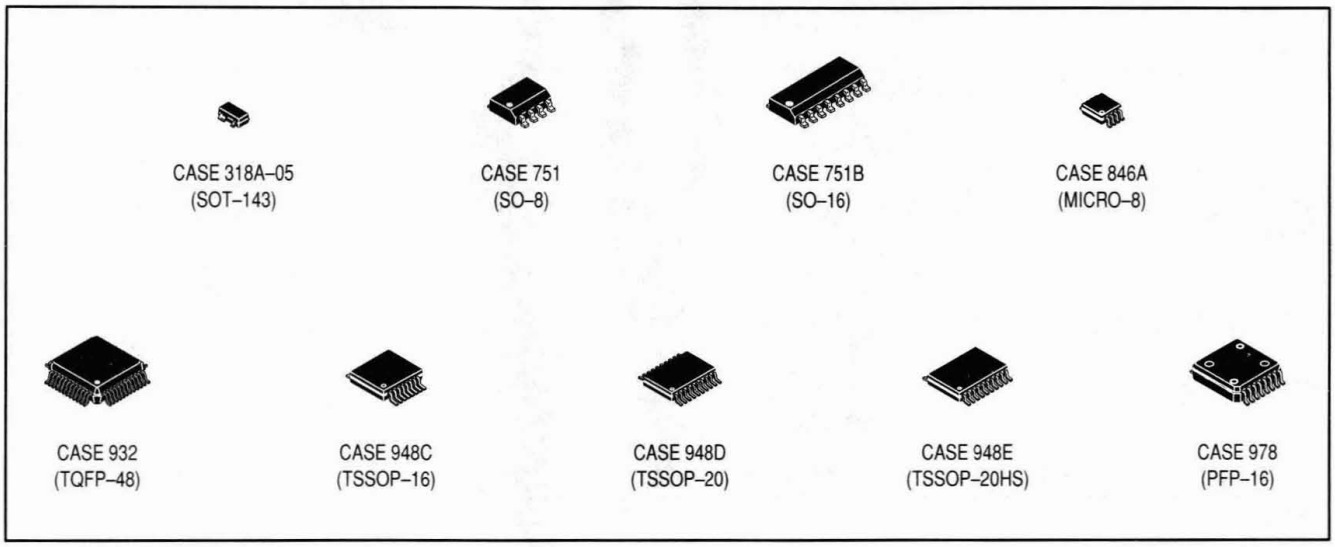
Upconverter

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803[18b]	1.7–2.5	2.7–5.0	28	100	10	70–350	–2	SO–16	WLAN, ISM
MRFIC1813[18b]★	1.7–2.5	2.7–4.5	25	100	15	70–350	3	TSSOP–16	WLAN, ISM
MRFIC2406[18b]	2.4 – 2.5	3.0–5.0	15	0.6	6	100–370	–10	SO–16	WLAN, MMDS,ISM

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

★New Product

RF Monolithic Integrated Circuit Packages



Section Two

Motorola RF Monolithic Integrated Circuits – Data Sheets

Device Number	Page Number
MRFIC0001	2.2–3
MRFIC0903	2.2–7
MRFIC0904	2.2–13
MRFIC0912	2.2–19
MRFIC0913	2.2–24
MRFIC0916	2.2–30
MRFIC0917	2.2–36
MRFIC0931	2.2–45
MRFIC1501	2.2–48
MRFIC1502	2.2–55
MRFIC1801	2.2–60
MRFIC1803	2.2–63
MRFIC1804	2.2–68
MRFIC1805	2.2–73
MRFIC1806	2.2–81
MRFIC1807	2.2–91
MRFIC1808	2.2–98
MRFIC1813	2.2–105
MRFIC1814	2.2–111
MRFIC1817	2.2–114
MRFIC1818	2.2–121
MRFIC2001	2.2–128
MRFIC2002	2.2–134
MRFIC2004	2.2–139
MRFIC2006	2.2–144
MRFIC2101	2.2–151
MRFIC2401	2.2–159
MRFIC2403	2.2–166
MRFIC2404	2.2–171
MRFIC2406	2.2–175

Advance Information

The MRFIC Line Quadrature Modulator

MRFIC0001

QUADRATURE MODULATOR INTEGRATED CIRCUIT

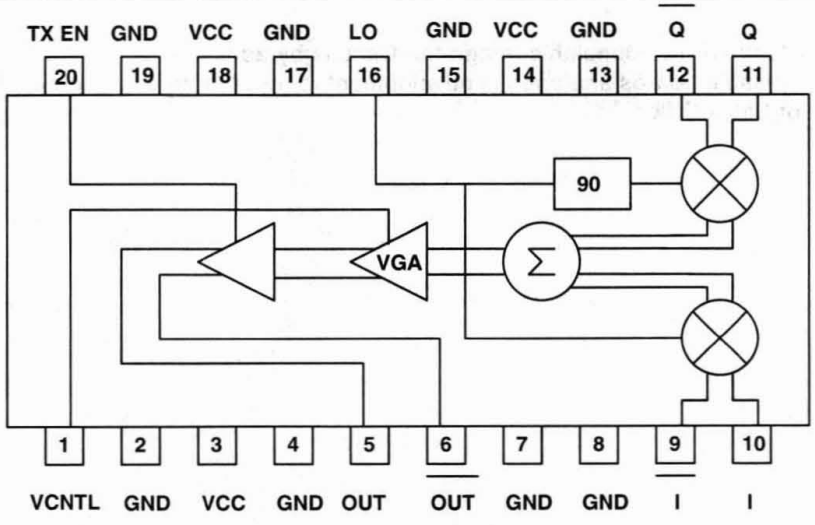
The MRFIC0001 is an integrated Quadrature Modulator designed for operation in the 50 to 260 MHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications include DQPSK for PDC, NADC, and PHS; GMSK for GSM and DCS1800; and QPSK for CATV.

- Linear I/Q Ports
- On Chip LO Phase Shifter
- I/Q Phase Imbalance = 2 degrees (Typ)
- I/Q Amplitude Imbalance = 0.3 dB (Typ)
- Gain Control = 30 dB (Typ)
- Single Source Low Operating Supply Voltage
- Low Power Consumption
- Low–Cost, Low Profile Plastic TSSOP Package
- Order MRFIC0001R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M001

CASE 948D–03
(TSSOP–20)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.5	Vdc
Control Voltages	TX EN, VCNTL	6.5	Vdc
LO Input Power	P_{LO}	0.0	dBm
Differential I/Q Input Voltage	V_D	2.0	V_{pp}
I, $\overline{I}$, Q, and $\overline{Q}$ DC Bias Voltage	V_B	2.0	Vdc
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



Pin Connections and Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 4

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.7 to 5.5	Vdc
LO Input Power	P_{LO}	–10	dBm
LO Frequency	f_{LO}	50 to 260	MHz
Differential I/Q Input Voltage	V_D	0 to 1.0	Vdc
I, $\overline{I}$, Q, and $\overline{Q}$ DC Bias Voltage	V_B	1.5 to 1.7	Vdc
Variable Gain Amplifier Control Voltage	V_{cntl}	0 to V_{CC}	Vdc
Transmit Enable Low Voltage	TX EN	0 to 0.2	Vdc
Transmit Enable High Voltage	TX EN	V_{CC} – 0.2 to V_{CC}	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, TX EN = 3.0 V, V_{cntl} = 0.0 V, V_D = 0.8 V_{PP}, V_B = 1.6 V, P_{LO} = –10 dBm, f_{LO} = 248 MHz, f_D = 100 kHz, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current	–	10	12	mA
Standby Current (TX EN = 0.0V)	–	40	100	µA
Single Sideband Output Power Level	–15	–13	–	dBm
Single Sideband Output Power 1dB Compression Point	–	–10	–	dBm
LO Leakage(2)	–	–55	–45	dBm
Undesired Sideband Level	–	–35	–30	dBc
Output Level Dynamic Range (V_{cntl} = 0 to 2.2V)(2)	–	30	–	dB
Turn–on/off Time	–	2	–	µs
I/Q Data				
Input 3dB Bandwidth	–	5	–	MHz
Amplitude Imbalance	–	0.3	–	dB
Phase Imbalance	–	2	–	degree

(1) All electrical characteristics measured in test circuit schematic shown in Figure 1.
V_B is the bias voltage on the input data ports.
V_D is the sinusoidal differential voltage on the input data ports when testing the part in a single sideband mode.
Above power levels are the single–ended output power.

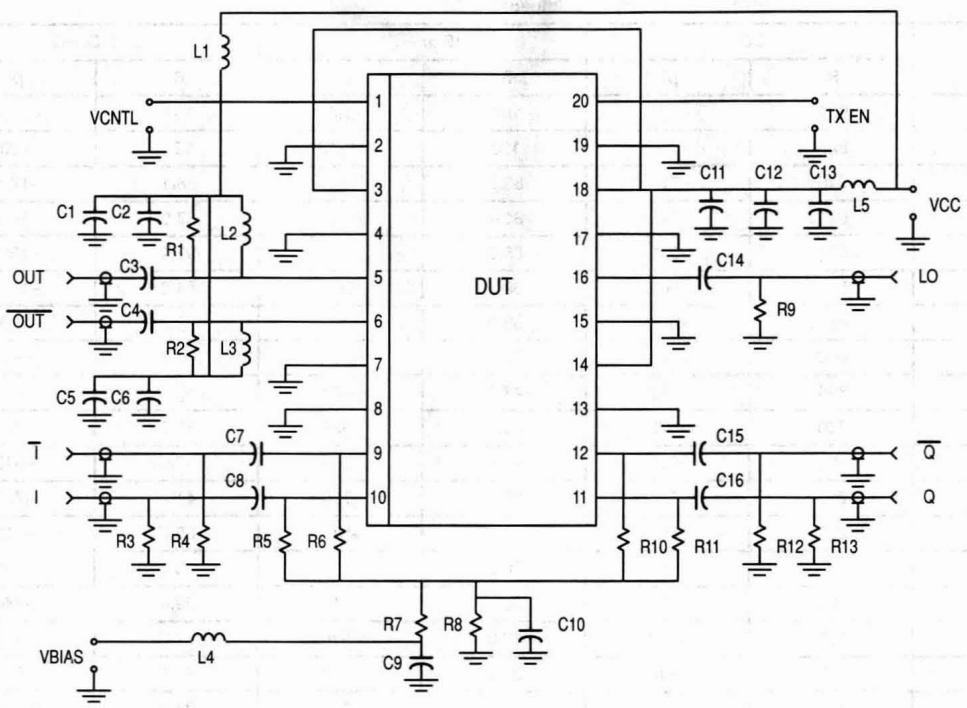
(2) LO leakage power is unaffected by V_{cntl} setting.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

Impedance Ω						
f MHz	LO		IF or –IF		I, –I, Q, –Q	
	R	jX	R	jX	R	jX
50	924	–694	164	–2330	181	–2448
60	825	–716	110	–1913	121	–2003
70	715	–713	83.2	–1661	88.1	–1709
80	635	–690	81.4	–1422	87.0	–1470
90	576	–691	86.8	–1312	93.4	–1361
100	509	–668	69.2	–1172	74.2	–1213
110	453	–651	56.0	–1055	72.2	–1091
120	400	–623	56.9	–969	60.3	–998
130	355	–595	47.3	–884	67.5	–913
140	330	–576	49.4	–835	38.3	–871
150	291	–551	49.8	–784	47.0	–815
160	259	–525	37.7	–730	41.2	–763
170	239	–509	32.5	–678	35.9	–712
180	225	–489	30.0	–651	33.0	–683
190	206	–473	30.4	–613	29.4	–644
200	187	–452	17.0	–579	22.7	–612
210	172	–440	33.1	–544	23.8	–580
220	158	–416	27.7	–521	24.5	–549
230	149	–402	20.5	–503	14.2	–530
240	137	–392	26.1	–482	18.3	–508
250	130	–375	19.5	–461	11.9	–485
260	119	–374	19.5	–437	17.1	–458
270	114	–353	20.1	–423	12.0	–443
280	105	–343	18.7	–408	11.1	–426
290	103	–332	20.7	–394	10.4	–412
300	93.5	–320	19.3	–380	9.65	–397
310	88.0	–312	17.9	–366	8.86	–380
320	84.8	–302	18.0	–354	6.91	–368
330	82.5	–296	19.4	–342	7.71	–354
340	76.1	–288	18.2	–332	6.02	–343
350	72.4	–282	15.0	–322	6.74	–331

Table 1. Selected Port Impedances



C1, C5, C9, C12 – 10000 pF, Chip Capacitor
C2, C6, C11 – 100 pF, Chip Capacitor
C3, C4 – 3.6 pF, Chip Capacitor
C7, C8, C10, C13, C15, C16 – 1 uF, Chip Capacitor
C14 – 10 pF, Chip Capacitor
L1, L4, L5 – 1.2 μH, Chip Inductor
L2, L3 – 68 nH, Chip Inductor

R1, R2 – 1000 Ω, Chip Resistor
R3, R4, R12, R13 – 510 Ω, Chip Resistor
R5, R6, R10, R11 – 2200 Ω, Chip Resistor
R7, R8, – 5100 Ω, Chip Resistor
R9 – 56 Ω, Chip Resistor

Figure 1. Typical Biasing Configuration

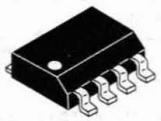
The MRFIC Line
Broadband GaAs Switch

MRFIC0903

ANTENNA SWITCH
GaAs MONOLITHIC
INTEGRATED CIRCUIT

The MRFIC0903 is an integrated GaAs SPDT switch designed for transceivers operating in the 100 MHz to 2.0 GHz frequency range. The design utilizes Motorola's advanced GaAs RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC0903 include Class 4 and 5 GSM, Class 1 and 2 DCS1800, DCS1900, DAMPS, PDC, digital cellular systems as well as analog cellular systems.

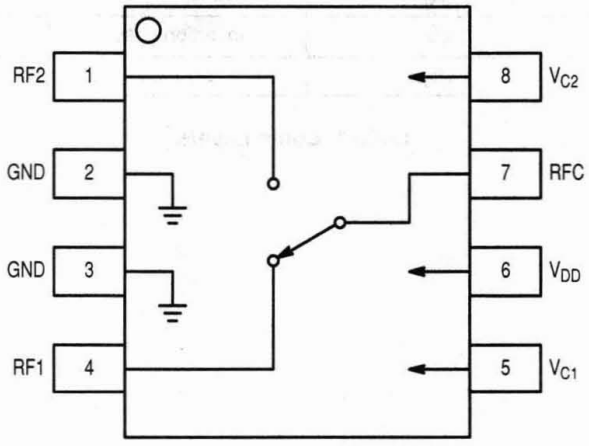
- 2.8 W Transmitting Capability through the Transmit Path with a 5.0 Volt Differential Control Signal
- 1.25 W Transmitting Capability through the Transmit Path with a 3.0 Volt Differential Control Signal
- Single Source Operating Supply Voltage
- Low Power Consumption
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC0903R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M0903



CASE 751–06
(SO–8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	10	Vdc
Control Voltage	V_{C1}, V_{C2}	V_{DD} + 0.8, V_{DD} – 12	Vdc
Power Dissipation	P_D	1.0	W
Power Input (Non–selected Port)	P_{in}	0.325	W
Ambient Operating Temperature	T_A	–35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C



Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	0 to 5.0	Vdc
Control Voltage Range	V_{C1}, V_{C2}	V_{DD} – 5.0 to V_{DD} + 0.5	Vdc
RF Frequency Range	f_{RF}	100 to 2000	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, P_{in} = 2.5 W (34 dBm), f = 900 MHz, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current				
I_{DD}	—	100	170	μA
$I_{Control}$	—	150	300	μA
VSWR	—	1.5:1	—	
Insertion Loss (RFC/RF1, RFC/RF2)	—	0.55	0.8	dB
Isolation (RFC/RF2, RFC/RF1)	18	20	—	dB
Output Power at 0.1 dB Compression	—	34.5	—	dBm

Electrical Characteristics at 900 MHz measured in test circuit schematic shown in Figure 1 with board losses removed.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, P_{in} = 2.0 W (33 dBm), f = 1800 MHz, T_A = 25°C unless otherwise noted)

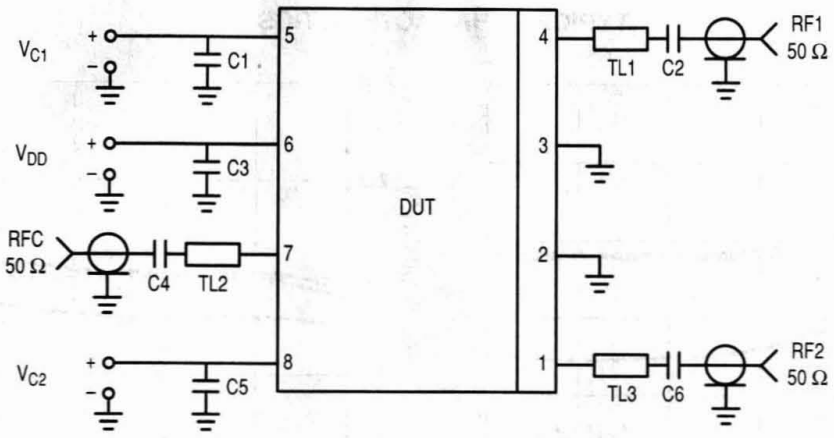
Characteristic	Min	Typ	Max	Unit
Supply Current				
I_{DD}	—	100	170	μA
$I_{Control}$	—	150	300	μA
VSWR	—	1.5:1	—	
Insertion Loss (RFC/RF1, RFC/RF2)	—	0.7	0.85	dB
Isolation (RFC/RF2, RFC/RF1)	18	20	—	dB
Output Power at 0.1 dB Compression	—	34	—	dBm

Electrical Characteristics at 1800 MHz measured in test circuit schematic shown in Figure 2 with board losses removed.

V_{C1} and V_{C2} Input Voltage	Min	Typ	Max	Unit
High	V_{DD}	—	V_{DD} + 0.5	Vdc
Low	V_{DD} – 10	—	V_{DD} – 5	Vdc

V_{C1}	V_{C2}	RFC – RF1	RFC – RF2
High	Low	Insertion Loss	Isolation
Low	High	Isolation	Insertion Loss

Table 1. Logic Levels

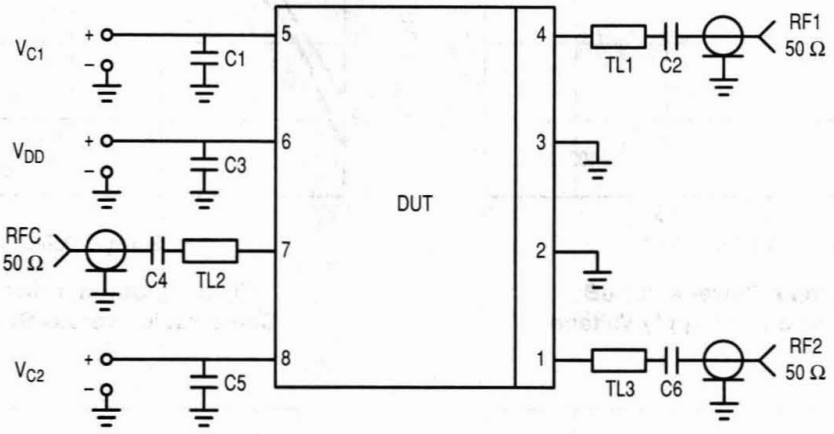


C1, C5 — 2.7 pF, Chip Capacitor
C2, C4, C6 — 100 pF, Chip Capacitor
C3 — 10 pF, Chip Capacitor

TL1, TL3 — 12 degrees of 50 Ω line at 1 GHz
TL2 — 15 degrees of 50 Ω line at 1 GHz

Note: Decoupling capacitors on pins 5, 6 and 8 must be as close as possible to the pins.

Figure 1. 300 MHz to 1600 MHz Test Circuit Configuration



C1, C5 — 1.3 pF, Chip Capacitor
C2, C3, C4, C6 — 8.2 pF, Chip Capacitor

TL1, TL3 — 12 degrees of 50 Ω line at 1 GHz
TL2 — 15 degrees of 50 Ω line at 1 GHz

Note: Decoupling capacitors on pins 5, 6 and 8 must be as close as possible to the pins.

Figure 2. 1600 MHz to 2000 MHz Test Circuit Configuration

TYPICAL CHARACTERISTICS

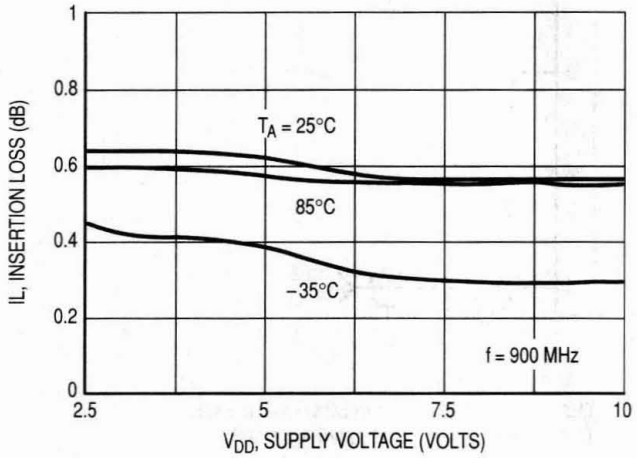


Figure 3. Insertion Loss at 0.1 dB Compression versus Supply Voltage

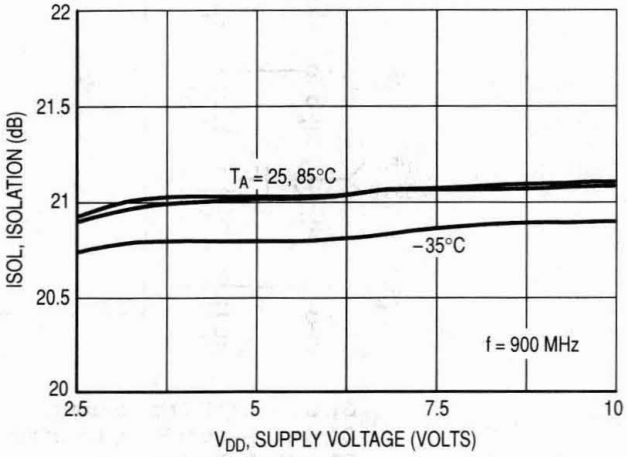


Figure 4. Isolation at 0.1 dB Compression versus Supply Voltage

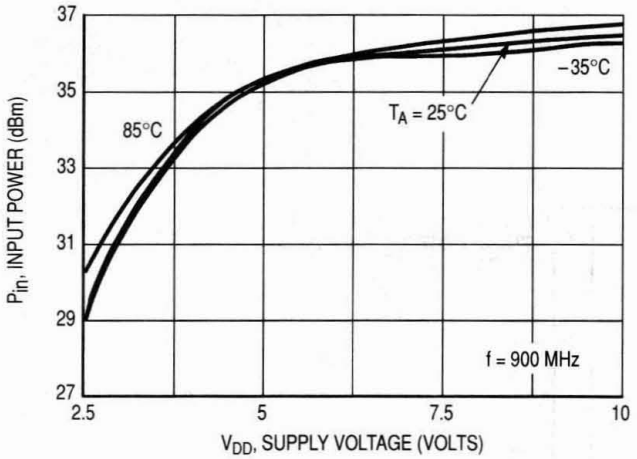


Figure 5. Input Power at 0.1 dB Compression versus Supply Voltage

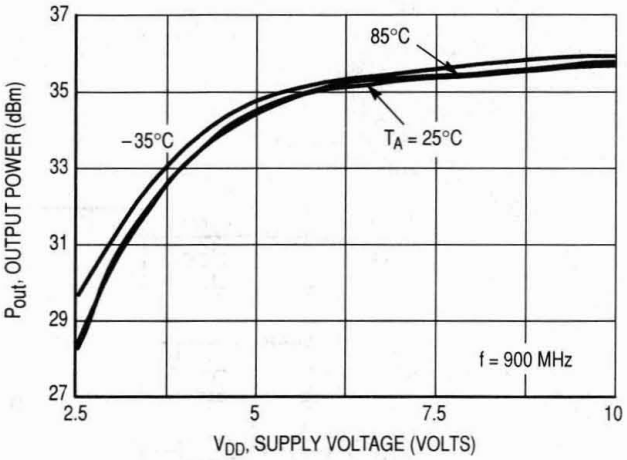


Figure 6. Output Power at 0.1 dB Compression versus Supply Voltage

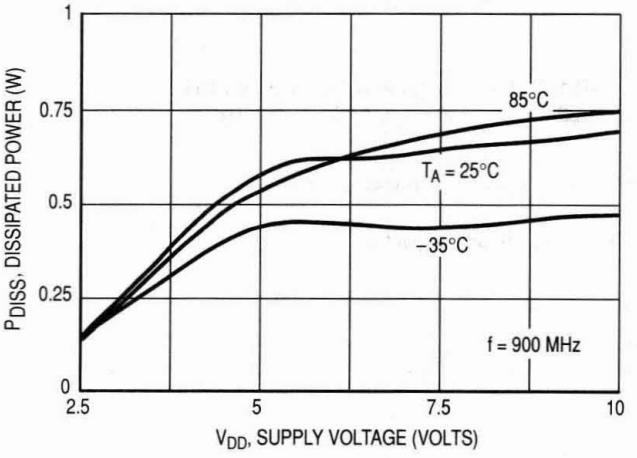


Figure 7. Dissipated Power at 0.1 dB Compression versus Supply Voltage

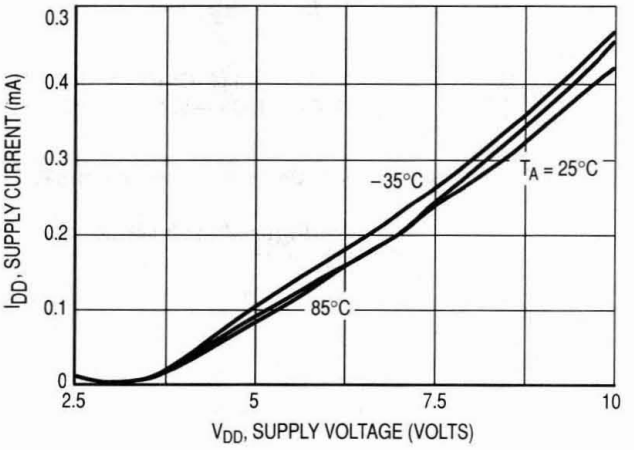


Figure 8. Supply Current at 0.1 dB Compression versus Supply Voltage

TYPICAL CHARACTERISTICS

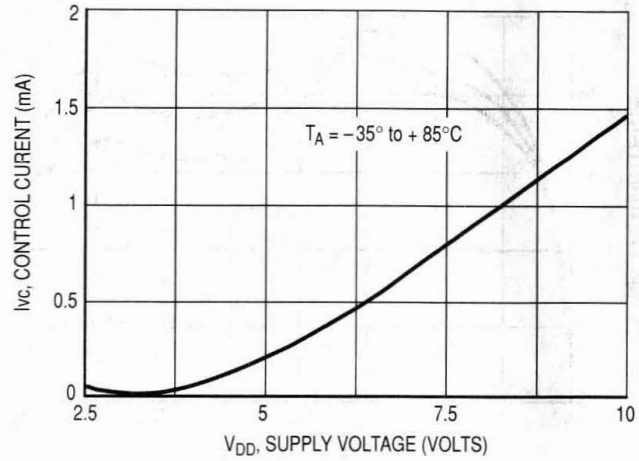


Figure 9. Control Current at Vc Pins at 0.1 dB Compression versus Supply Voltage

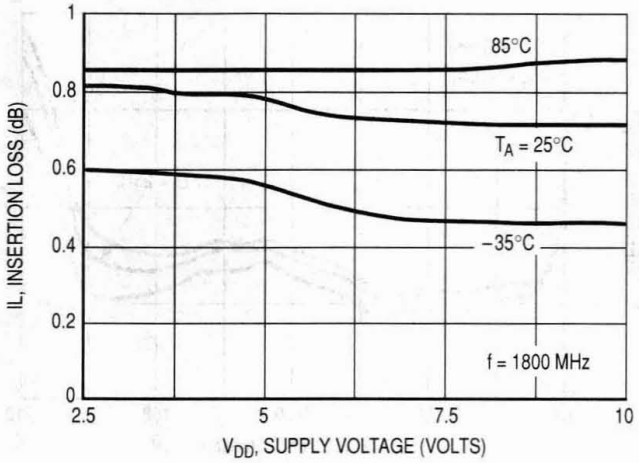


Figure 10. Insertion Loss at 0.1 dB Compression versus Supply Voltage

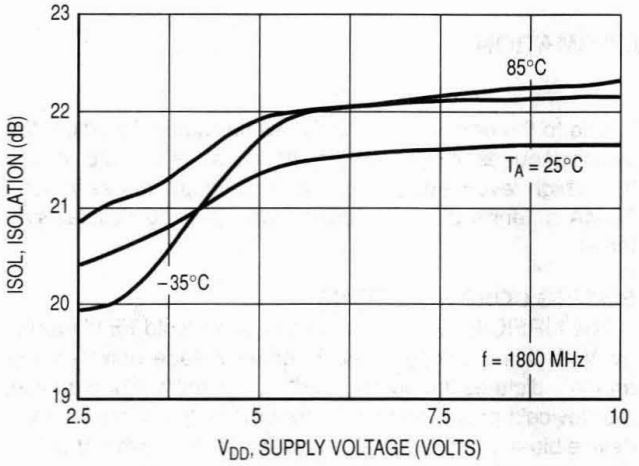


Figure 11. Isolation at 0.1 dB Compression versus Supply Voltage

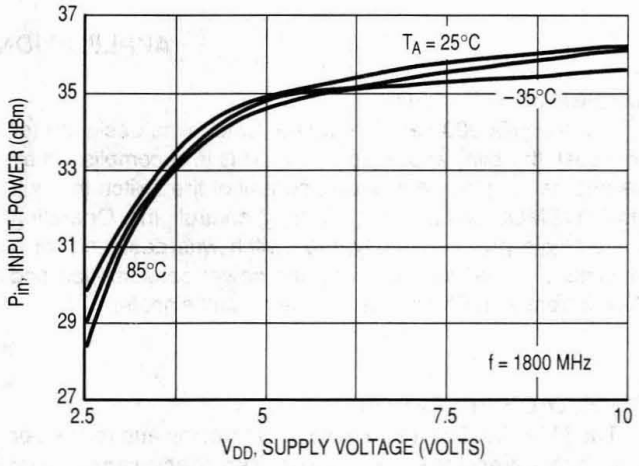


Figure 12. Input Power at 0.1 dB Compression versus Supply Voltage

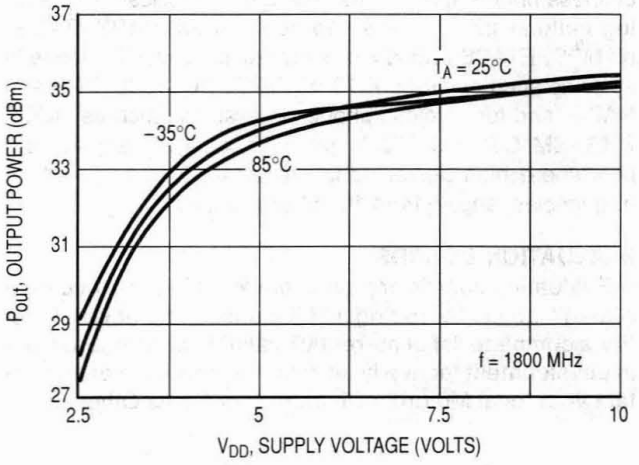


Figure 13. Output Power at 0.1 dB Compression versus Supply Voltage

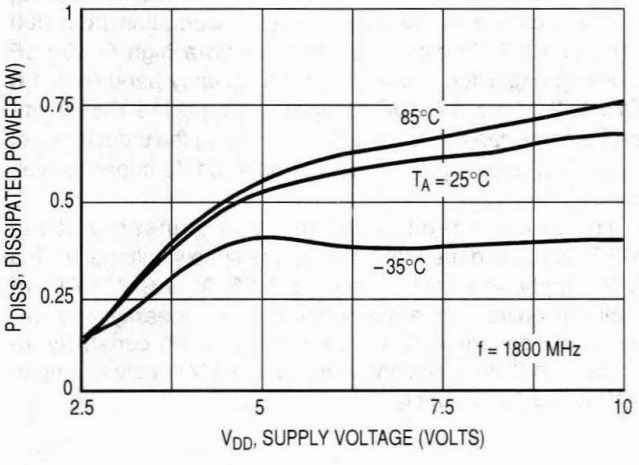


Figure 14. Dissipated Power at 0.1dB Compression versus Supply Voltage

TYPICAL CHARACTERISTICS

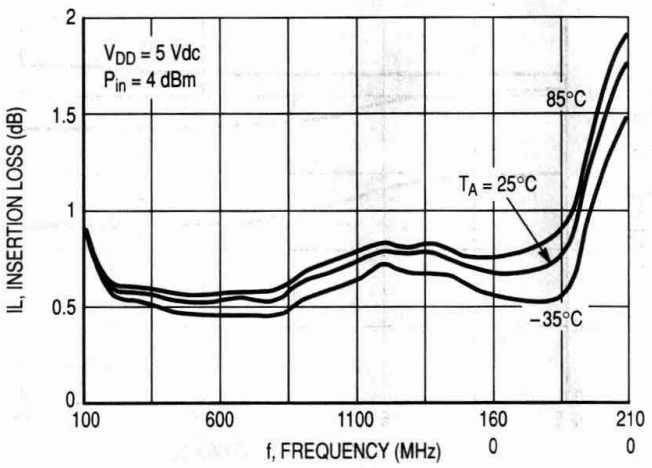


Figure 15. Insertion Loss versus Frequency

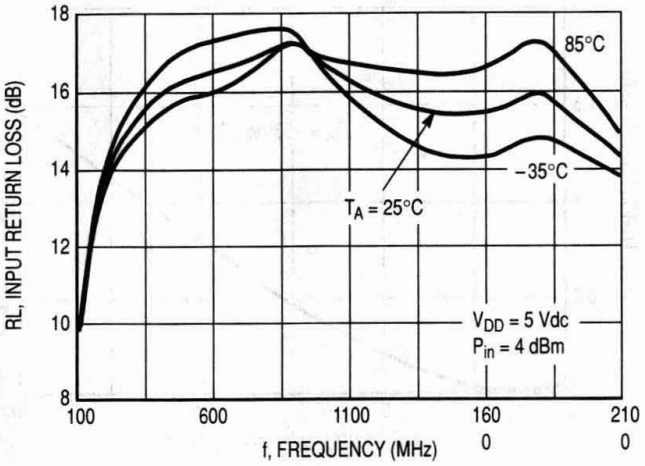


Figure 16. Input Return Loss versus Frequency

APPLICATIONS INFORMATION

DESIGN INFORMATION

The MRFIC0903 SPDT antenna switch was designed for low cost, flexibility and ease of use. This is accomplished by its internal topology that allows control of the switch through its TTL/CMOS compatible (0 to V_{DD}) control pins. Operating on a single positive supply, the switch was designed for a minimum supply voltage, minimum power consumption and low current TTL/CMOS compatible control signals.

THEORY OF OPERATION

The MRFIC0903 can be used as a transmit and receive or antenna diversity switch in the frequency range from 100 MHz to 2 GHz with incident power levels as high as 4 watts.

The frequency behavior can be optimized by resonating the DC blocking capacitor's position and value with the parasitic inductance of the package lead. Operation from 300 MHz to 1.6 GHz can be optimized with a high Q 100 pF blocking capacitor. For the higher frequency band from 1.6 GHz to 2.0 GHz, a 8.2 pF capacitor is suggested. Further improvements can be achieved by resonating the inductance of V_{DD}, V_{C1}, and V_{C2} pins with the appropriate capacitor values.

The power handling capability and linearity of the MRFIC0903 is dependent only on the supply voltage. With a 3 V supply, the device handles 1.25 W (1.6 W PEP) of incident power while maintaining good linearity and low harmonic distortion. The power transmitting capability increases to 3 W of incident power with a 5 V supply and up to 4 W with a 7.5 V supply.

Due to the device's inherently low harmonic distortion, the switch requires little harmonic filtering at its outputs. It also has a high reverse third–order intercept point for use in non–TDMA antenna diversity applications (analog cellular systems).

BIASING CONSIDERATIONS

The MRFIC0903 is based on a floating "cold FET" topology. With this topology, the differential voltage between V_{C1} and V_{C2} dictates the power handling capability. For example, the device's power handling capability is the same with the device biased with 5 V at V_{C1} and 0 V at V_{C2}, with 0 V at V_{C1} and –5 V at V_{C2}, or with 3 V at V_{C1} and –2 V at V_{C2}.

POSSIBLE APPLICATIONS

The MRFIC0903 can be used in a number of cellular and cordless phone applications. The part is applicable for analog cellular phones in systems such as AMPS, TACS, NAMPS, ETACS and NMT900; for digital cellular phones in systems such as GSM, PDC, DAMPS, DCS1800, PCS and NADC; and for cordless phones in systems such as DECT, PHS, ISM, CT1 and CT2. In general it can fit into any application where high power handling capability is required for frequencies ranging from 100 MHz to 2 GHz.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

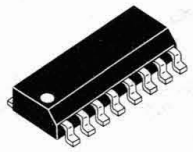
900 MHz GaAs Two-Stage Driver Amplifier

MRFIC0904

The MRFIC0904 is an integrated driver amplifier designed for class A/B operation in the 800 MHz to 1 GHz frequency range. The design utilizes Motorola's Advanced GaAs FET process to yield superior performance and efficiency in a cost effective monolithic device. Off–chip output matching provides maximum flexibility in design. Applications for the MRFIC0904 include GSM, AMPS, and ISM band transmitters.

- GSM Ramping/Gain Control of 45 dB with Power Control Function (PCNTRL)
- Class 4 P_{out} (1 dB Gain Compression) = 26 dBm @ 4.8 V (Typical)
- Class 4 Supply Current (1 dB) = 120 mA @ 4.8 V (Typical)
- Class 5 P_{out} (1 dB Gain Compression) = 24 dBm 3.6 V (Typical)
- Class 5 Supply Current (1 dB) = 120 mA @ 3.6 V (Typical)
- Low Cost Surface Mount Plastic Package
- Order MRFIC0904R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0904

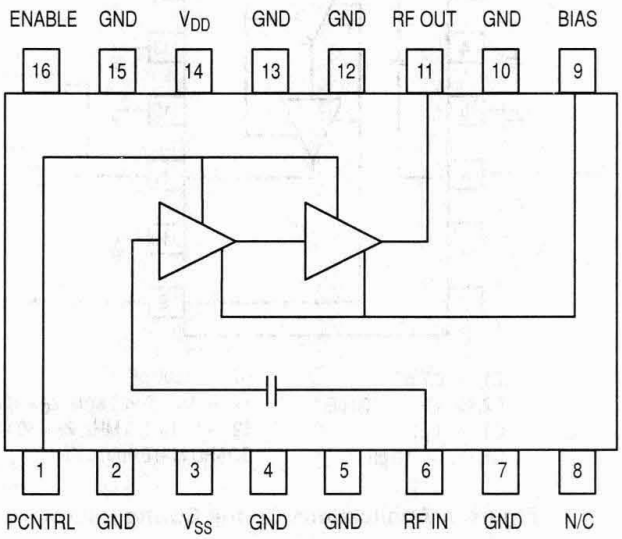
900 MHz GaAs
TWO STAGE DRIVER AMP
INTEGRATED CIRCUIT



CASE 751B–05
(SO–16)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD} V_{SS}	6.0 –3	Vdc
Power Control Voltage	PCNTRL	V_{DD}	Vdc
Enable Voltage	ENABLE	V_{DD}	Vdc
Input Power	P_{in}	5	dBm
Operating Ambient Temperature	T_A	– 35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	60	°C/W



Pin Connections and Functional Block Diagram

REV 2

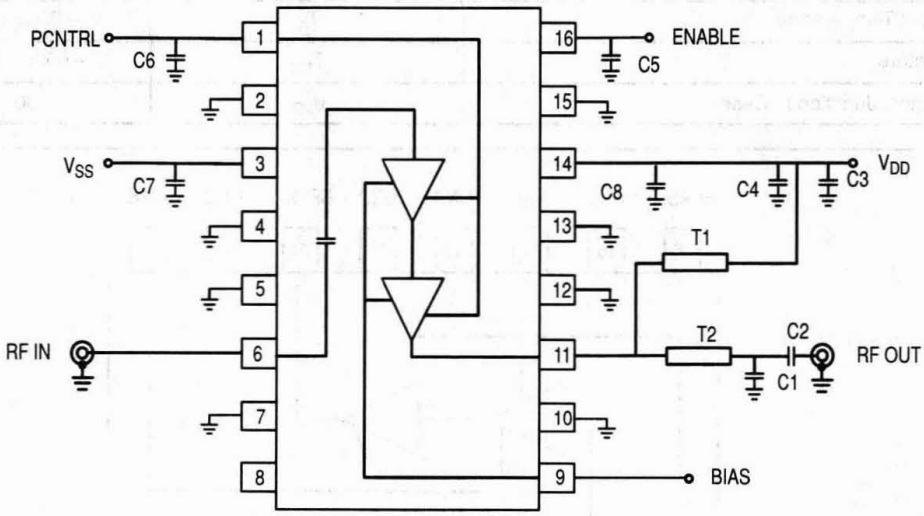
RECOMMENDED OPERATING RANGES (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD} V_{SS}	2.7 to 5.0 −2.75 to −2.25	Vdc
Bias Voltage Range	BIAS	0 to 1.0	Vdc
Power Control Voltage Range	PCNTRL	0 to 3.0	Vdc
Enable Voltage ON State	ENABLE	2.5	Vdc
Enable Voltage OFF State	ENABLE	0.5	Vdc
RF Frequency	f	800 to 1000	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.6 V, V_{SS} = −2.5 V, BIAS = 0.0 V, PCNTRL = 3.0 V, ENABLE = 3.0 V, P_{in} = −2 dBm, f = 900 MHz, Z_O = 50 Ω, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current				mA
I_{DD}	—	120	160	
I_{SS}	—	1.0	1.75	
Standby Current: Off–mode (ENABLE = 0 V)				µA
I_{DD}	—	50	130	
I_{SS}	—	60	360	
Output Power	22.5	24	—	dBm
Output Power at 1 dB Gain Compression	—	24.5	—	dBm
Input Return Loss	—	14	—	dB
PCNTRL Current	—	200	—	µA
ENABLE Current	—	200	—	µA
Gain Control Range	—	45	—	dB
Enable/Control Input 3 dB Bandwidth	—	1	—	MHz

(1) All electrical Characteristics are measured in test circuit schematic as shown in Figure 1.



C1 – 2.7 pF
C2, C4, C8 – 100 pF
C3 – 1 µF
C5, C6 – 10 pF
C7 – 1000 pF
T1 – 90° @ 900 MHz, Z_0 = 100 Ω
T2 – 9° @ 900 MHz, Z_0 = 50 Ω
BOARD MATERIAL = FR4

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

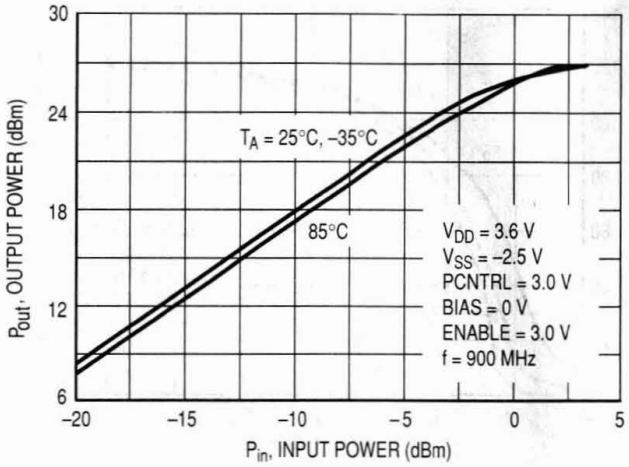


Figure 2. Output Power versus Input Power

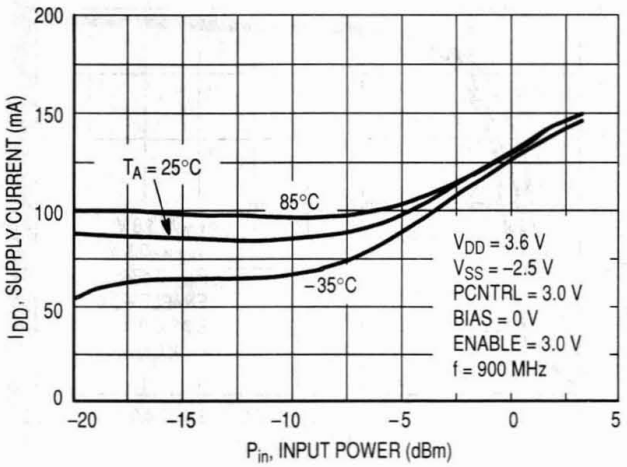


Figure 3. Supply Current versus Input Power

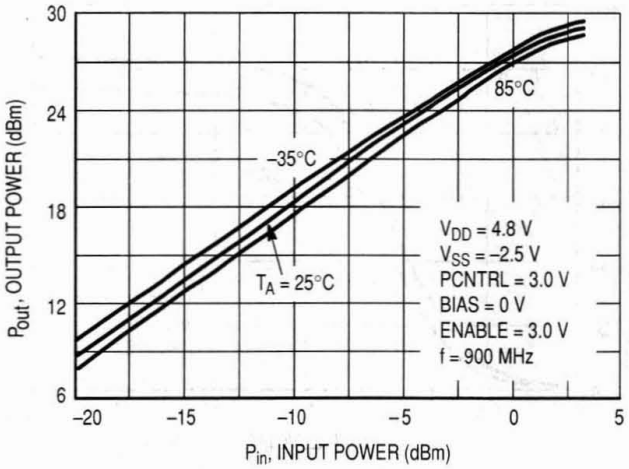


Figure 4. Output Power versus Input Power

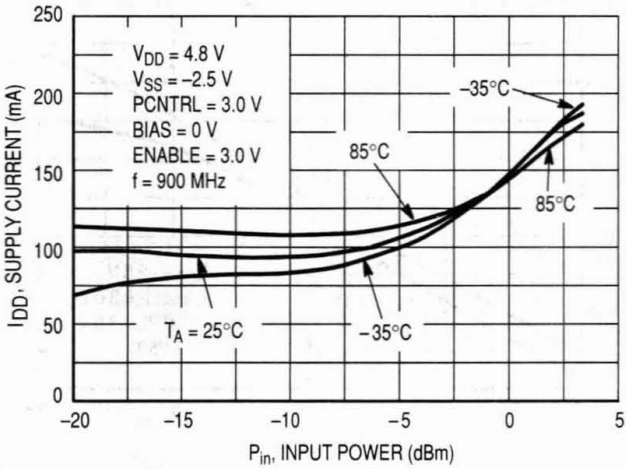


Figure 5. Supply Current versus Input Power

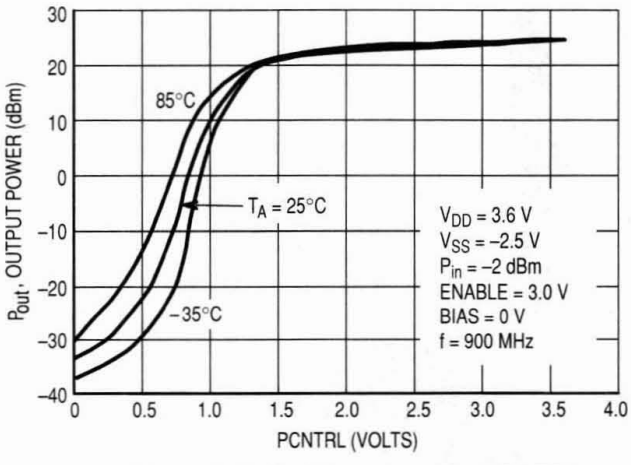


Figure 6. Output Power versus PCNTRL

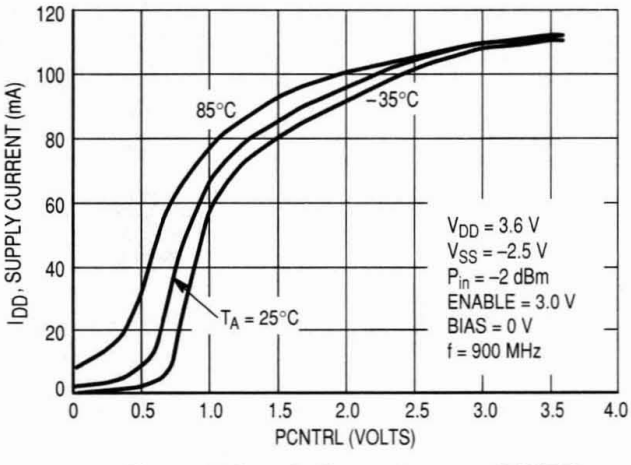


Figure 7. Supply Current versus PCNTRL

TYPICAL CHARACTERISTICS

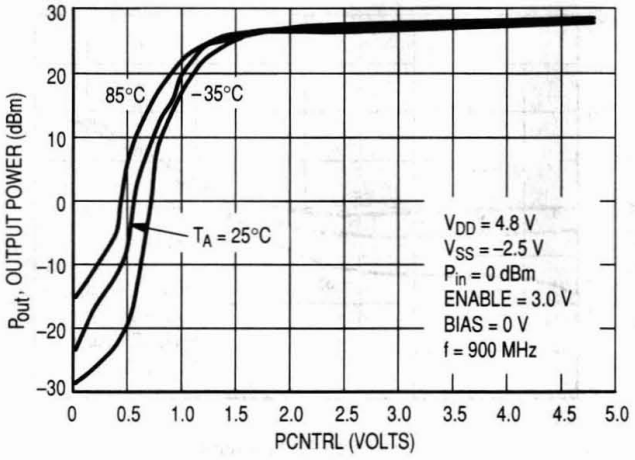


Figure 8. Output Power versus PCNTRL

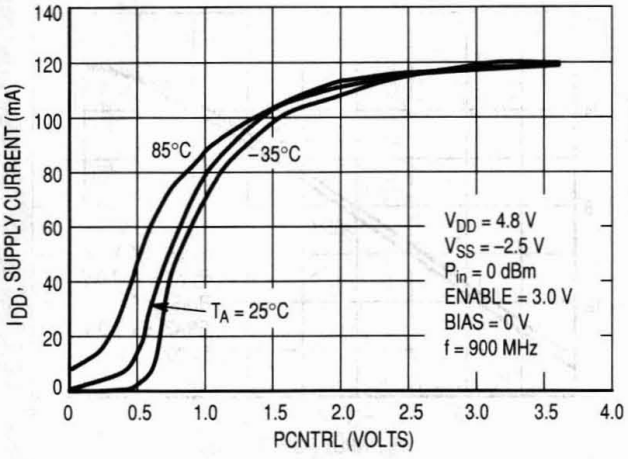


Figure 9. Supply Current versus PCNTRL

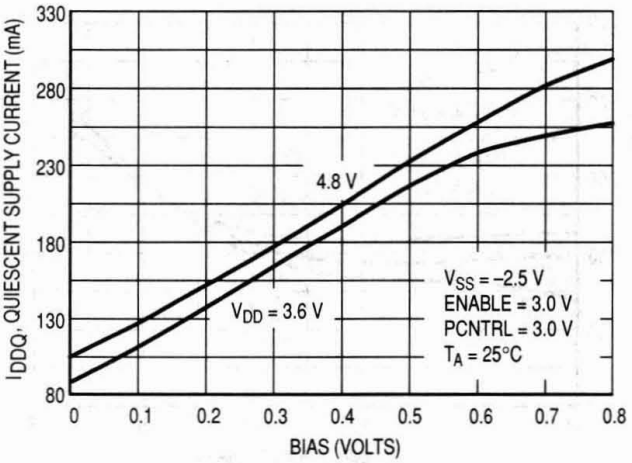


Figure 10. Quiescent Supply Current versus BIAS

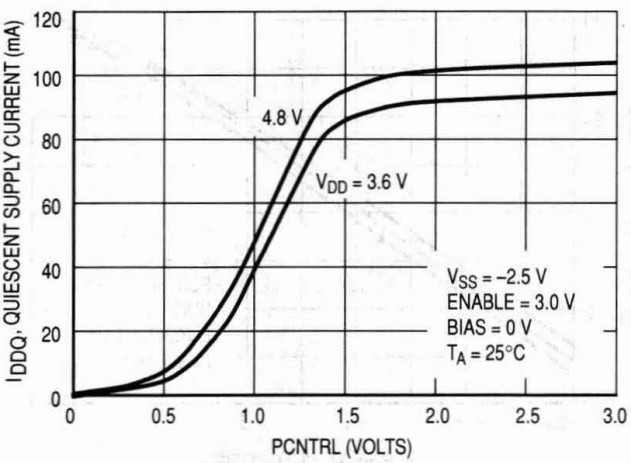


Figure 11. Quiescent Supply Current versus PCNTRL

Table 1. Scattering Parameters
(V_{DD} = 3.6 V, V_{SS} = –2.5 V, BIAS = 0.0 V, PCNTRL, ENABLE = 3 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\lvert S_{11}\rvert$	∠ϕ	$\lvert S_{21}\rvert$	∠ϕ	$\lvert S_{12}\rvert$	∠ϕ	$\lvert S_{22}\rvert$	∠ϕ
500	0.922	–40.93	12.201	–76.39	0.002	72.64	0.276	166.48
550	0.887	–52.05	16.242	–98.58	0.002	62.03	0.276	169.80
600	0.826	–65.21	21.133	–116.66	0.003	44.52	0.297	175.47
650	0.698	–81.22	28.039	–140.66	0.004	26.65	0.342	173.06
700	0.419	–99.95	33.973	174.46	0.004	6.35	0.360	169.94
750	0.206	–106.43	32.195	145.72	0.006	–9.10	0.393	163.65
800	0.073	–56.19	31.685	121.12	0.006	–31.13	0.392	154.83
850	0.146	–4.45	29.419	85.45	0.006	–47.59	0.351	146.93
900	0.170	–1.59	25.996	64.50	0.006	–61.44	0.305	145.90
950	0.183	10.82	24.115	45.18	0.007	–80.54	0.276	152.91
1000	0.232	27.47	22.091	16.72	0.007	–107.22	0.287	162.87
1050	0.302	34.19	19.995	–5.08	0.007	–116.06	0.310	167.00
1100	0.395	34.85	17.411	–26.64	0.006	–125.77	0.337	170.51
1150	0.522	29.21	14.15	–52.28	0.006	–146.60	0.380	169.57
1200	0.607	23.25	11.961	–71.38	0.005	–154.46	0.403	167.34
1250	0.675	17.30	9.76	–88.04	0.005	–177.16	0.419	163.73
1300	0.743	9.17	7.951	–108.01	0.004	160.61	0.436	159.33

Table 2. Scattering Parameters
(V_{DD} = 4.8 V, V_{SS} = –2.5 V, BIAS = 0.0 V, PCNTRL, ENABLE = 3 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\lvert S_{11}\rvert$	∠ϕ	$\lvert S_{21}\rvert$	∠ϕ	$\lvert S_{12}\rvert$	∠ϕ	$\lvert S_{22}\rvert$	∠ϕ
500	0.910	–41.17	12.58	–78.69	0.0012	65.66	0.228	168.72
550	0.873	–51.75	17.09	–99.91	0.0024	43.49	0.232	172.87
600	0.807	–64.98	22.33	–118.28	0.0032	48.13	0.252	177.75
650	0.671	–81.03	29.24	–142.97	0.0041	17.29	0.293	174.31
700	0.409	–100.12	35.95	172.30	0.0040	–10.22	0.326	172.83
750	0.200	–104.83	34.04	143.18	0.0055	–14.65	0.349	164.57
800	0.080	–53.72	33.08	118.78	0.0056	–28.05	0.345	156.12
850	0.142	–6.52	30.64	83.58	0.0057	–45.38	0.307	147.87
900	0.165	0.32	27.22	62.36	0.0065	–62.81	0.248	146.40
850	0.187	14.68	24.95	41.95	0.0066	–86.95	0.226	146.72
1000	0.252	28.28	22.30	14.13	0.0062	–100.71	0.257	167.95
1050	0.323	32.92	20.06	–7.52	0.0057	–113.16	0.279	172.05
1100	0.409	32.35	17.37	–28.14	0.0049	–121.71	0.310	173.62
1150	0.527	26.77	14.03	–53.24	0.0051	–152.49	0.349	171.86
1200	0.606	21.18	11.89	–71.66	0.0051	–159.64	0.365	169.36
1250	0.669	15.59	9.74	–87.41	0.0043	–155.55	0.381	163.46
1300	0.735	8.10	7.96	–107.51	0.0039	171.99	0.397	161.81

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC0904 is a versatile driver amplifier designed to operate in the 800 MHz to 1 GHz frequency range for cellular phone and Industrial, Scientific, and Medical (ISM) applications. The amplifier is designed using depletion mode GaAs MESFETs to perform at high efficiency at battery voltages of 3.6 and 4.8 Volts. While designed as a driver amplifier for a discrete transistor final stage, the device can act as a power amplifier for lower power systems such as ISM applications in telemetry and cordless telephones.

THEORY OF OPERATION

The MRFIC0904 has various control features making it versatile and applicable to both linear and saturated applications. The BIAS pin allows the setting of drain quiescent current. For non–linear applications such as GSM cellular, the pin can be grounded. For better gain and linearity, a positive voltage up to about 0.6 Volts can be applied. The PCNTRL pin allows the control of the output power over a wide dynamic range with low AM to AM distortion such as is required in GSM and other cellular systems. As shown in Figures 6 through 9, PCNTRL affects both the output power and the drain current thus maintaining good efficiency over a range of output power. The ENABLE pin is used to control the on–off state of the device and is useful as a reduced current standby control. A logic high signal of more than 2.5 Volts turns the device on. A logic low signal of less than 0.5 Volts reduces total supply current to typically less than 200 μA.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

900 MHz GaAs Integrated Power Amplifier

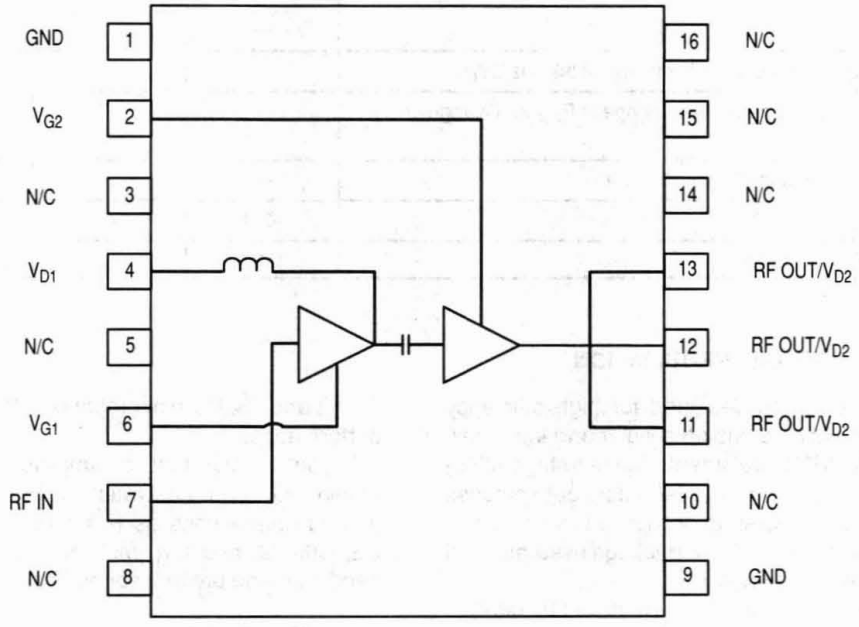
MRFIC0912

900 MHz
GaAs INTEGRATED
POWER AMPLIFIER

Designed primarily for use in high efficiency Analog Cellular applications, the MRFIC0912 is a two–stage power amplifier in Motorola's proprietary Power Flat Pack 16–lead package. This integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility in optimizing gain and efficiency. The design employs Motorola's planar, self–aligned GaAs MESFET IC process to give the highest efficiency possible.

- Usable Frequency Range = 800–1000 MHz, Specified for 824–905 MHz
- 30.8 dBm Minimum Output Power
- 470 mA Maximum Supply Current at 30.8 dBm Output
- 23.8 dB Minimum Gain
- Simple Off–chip Matching for Maximum Power/Efficiency Flexibility
- 4.6 Volt Supply
- 45 dB/Volt Typical Power Output Control
- Order MRFIC0912R2 for Tape and Reel Option. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0912

CASE 978–02
(PFP–16)



Pin Connections and Functional Block Diagram

REV 1

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Limit	Unit
Supply Voltage	V_{D1}, V_{D2}	8	Vdc
RF Input Power	P_{RF}	20	dBm
Gate Voltage	V_{G1}, V_{G2}, V_{GG}	–5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Case Temperature	T_C	– 35 to +100	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	18	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	824–905	MHz
Supply Voltage	V_{D1}, V_{D2}	4.0–6.0	Vdc
Gate Voltage	V_{G1}, V_{G2}	–2.3 to –1.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 4.6 V, T_A = 25°C, f_{RF} = 840 MHz, P_{in} = 7 dBm, V_{GG} set for I_{D2Q} = 200 mA, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Output Power	30.8	31.2	—	dBm
Power Slump (V_{D1}, V_{D2} = 4.0 V, T_C = 100°C)	28.5	—	—	dBm
Load Mismatch Survival (V_{D1}, V_{D2} = 7 V, Load VSWR = 10:1, all phases, 10 sec)	No Degradation			
Spurious Output (V_{D1},V_{D2} = 0 to 7 V, P_{in} = 5 to 9 dBm, Load VSWR = 10:1)	—	—	–60	dBc
Input Return Loss	—	10	—	dB
Harmonic Output (P_{out} = 30.8 dBm) $2f_0$ $3f_0$ $4f_0$	 — — —	 — — —	dBc –25 –40 –40	
Noise Power (V_{DD} = 0 to 7 V, 45 MHz Above f_{RF} at 30 kHz BW)	—	—	–93	dBm
Maximum Power Control Voltage Slope (Change in P_{out} for Change on V_{D1})	—	45	—	dB/V
Total Supply Current (V_{D1} set for P_{out} = 30.8 dBm)	—	430	470	mA
V_{GG} Required for I_{D2Q} = 200 mA	–2.3	–2.0	–1.7	Vdc
Gate Current during RF Operation	–2	—	2	mA

DESIGN AND APPLICATIONS INFORMATION

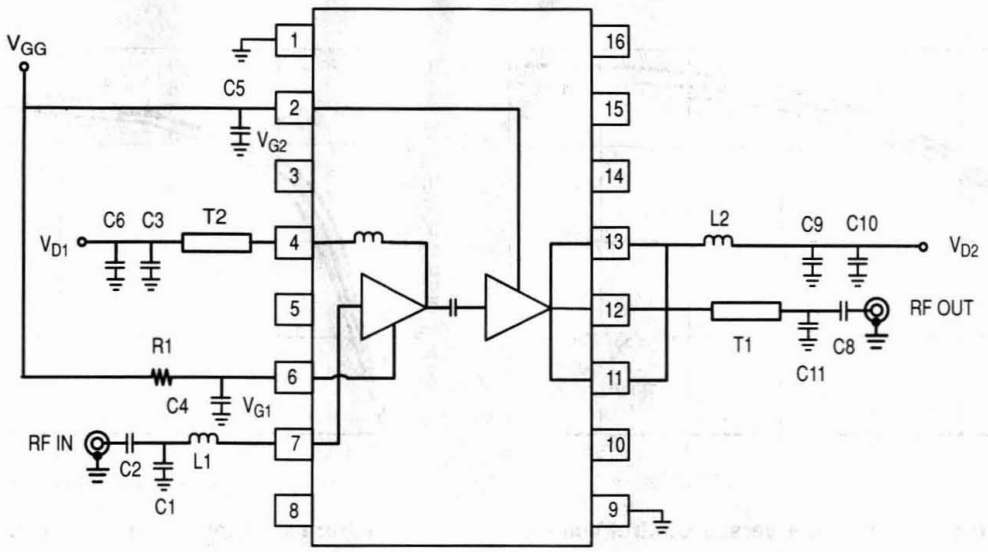
The MRFIC0912 has been designed for high efficiency 900 MHz applications such as analog cellular and Industrial, Medical and Scientific (ISM) equipment. The two stage MESFET design utilizes Motorola's planar refractory gate process to allow high performance GaAs to be applied to consumer applications. The proprietary PFP–16 package assures good grounding and low thermal resistance.

As shown in Figure 1, the gate voltage pins can be ganged together and one voltage applied to both gates to set the quiescent operating current. Alternatively, V_{G1} and V_{G2} can be set separately. V_{D1} can be used as power control with a 45 dB per volt sensitivity. The placement of C3 in the V_{D1} supply line can be varied to optimize RF performance since T2 is part of a shunt L matching section. On the output, pins 11, 12 and 13, the placement of C11 is adjusted for best RF performance.

Layout is important for amplifier stability and RF performance. Ground vias must be located as close to circuit ground connections as possible. Power supply bypassing C3, C6, C9, and C10 must be included to reduce out–of–band gain and prevent spurious output.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.



R1	1 kΩ	C6	0.01 µF	L2	22 nH
C1	3.3 pF	C10	1 µF	T1	50 Ω, 13° @ 840 MHz
C2, C3, C8, C9	100 pF	C4, C5	1000 pF	T2	50 Ω, 8° @ 840 MHz
C11	8.2 pF	L1	10 nH	BOARD MATERIAL — GLASS/EPOXY, ε_r = 4.45, THICKNESS = 18 MIL	

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

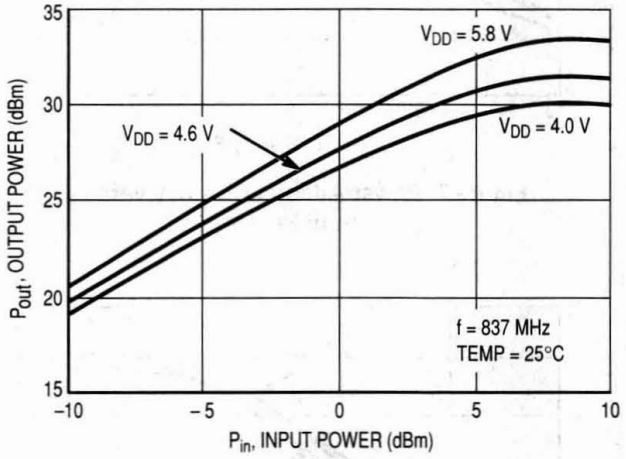


Figure 2. Output Power versus Input Power

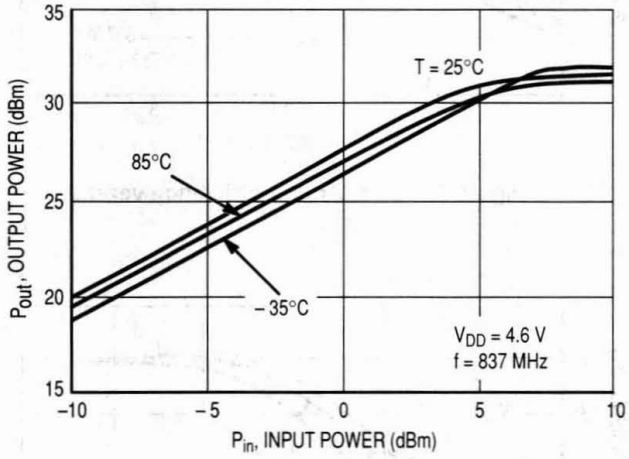


Figure 3. Output Power versus Input Power

TYPICAL CHARACTERISTICS

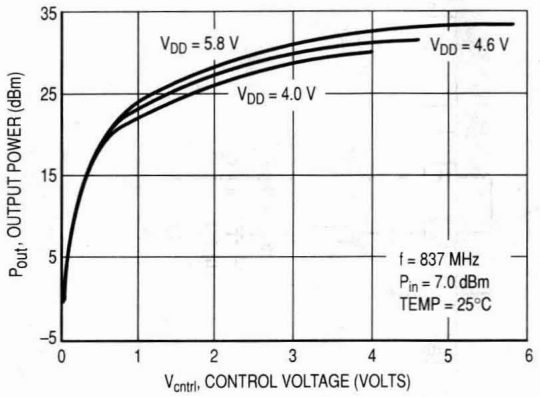


Figure 4. Output Power versus Control Voltage

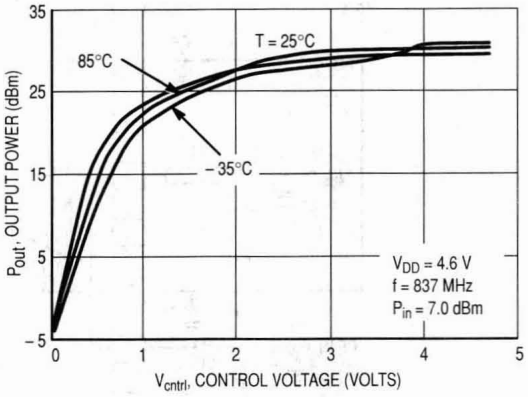


Figure 5. Output Power versus Control Voltage

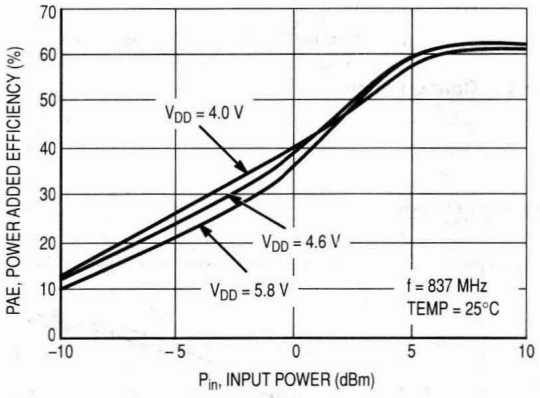


Figure 6. Power Added Efficiency versus Input Power

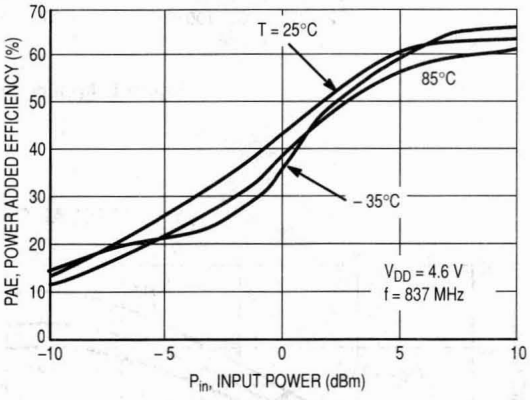


Figure 7. Power Added Efficiency versus Input Power

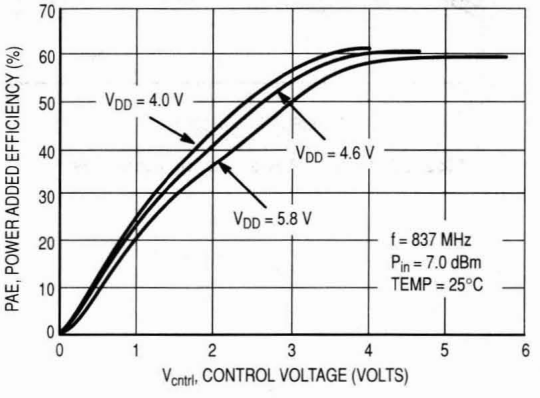


Figure 8. Power Added Efficiency versus Control Voltage

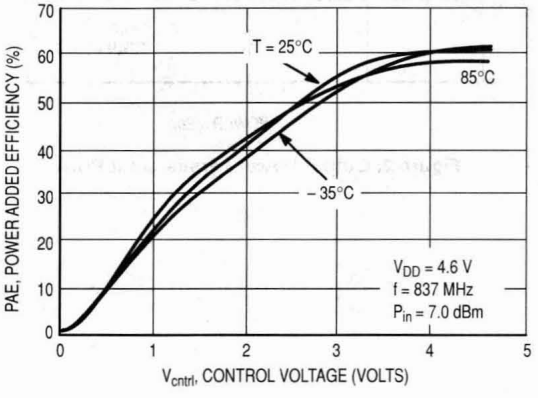


Figure 9. Power Added Efficiency versus Control Voltage

TYPICAL CHARACTERISTICS

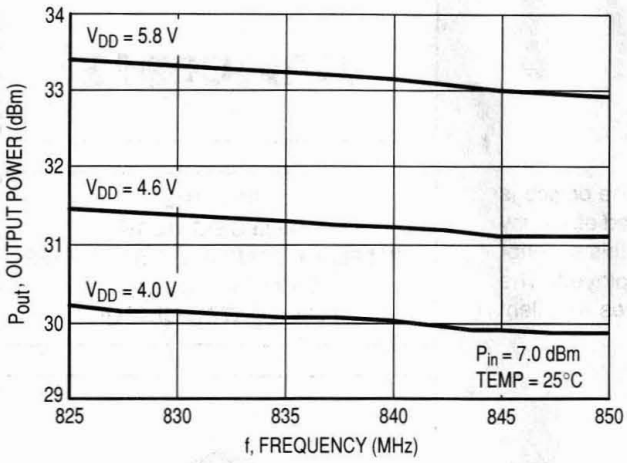


Figure 10. Output Power versus Frequency

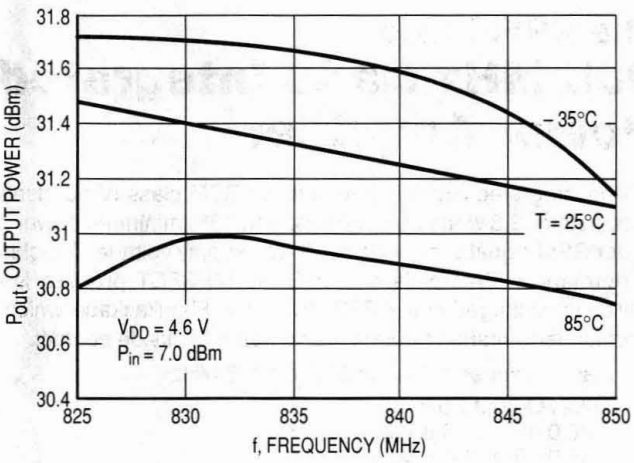


Figure 11. Output Power versus Frequency

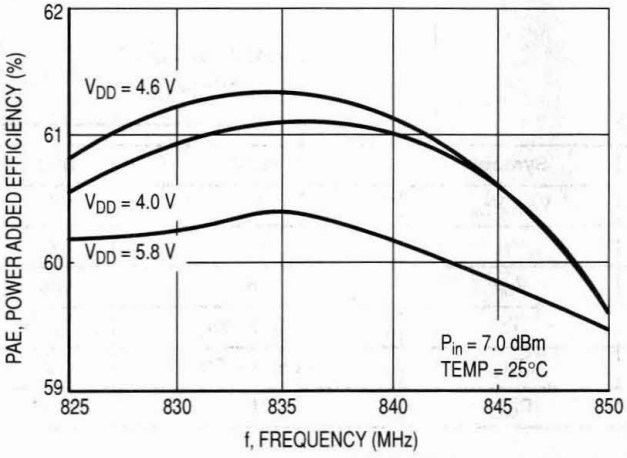


Figure 12. Power Added Efficiency versus Frequency

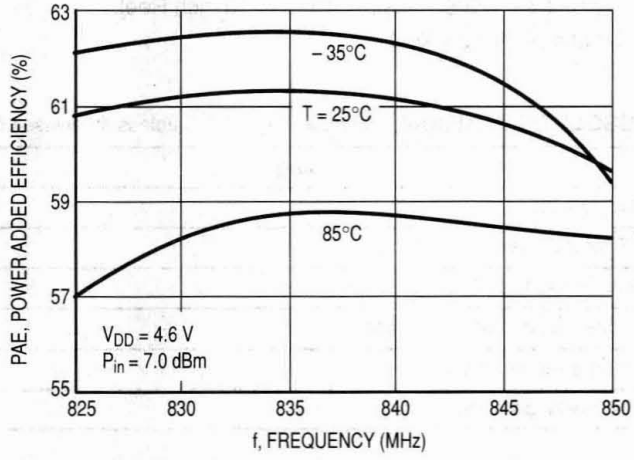


Figure 13. Power Added Efficiency versus Frequency

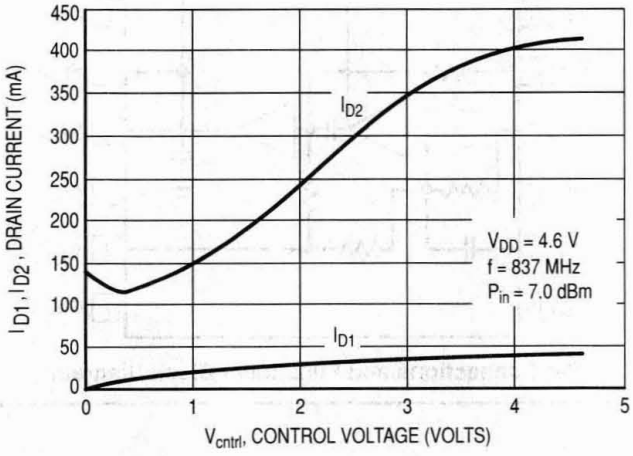


Figure 14. Drain Current versus Control Voltage

The MRFIC Line

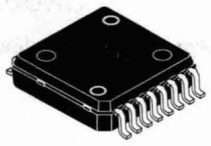
900 MHz GaAs Integrated Power Amplifier

MRFIC0913

900 MHz
GSM CELLULAR
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

This integrated circuit is intended for GSM class IV handsets. The device is specified for 2.8 watts output power and 48% minimum power added efficiency under GSM signal conditions at 4.8 Volt supply voltage. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal performance through a solderable backside contact.

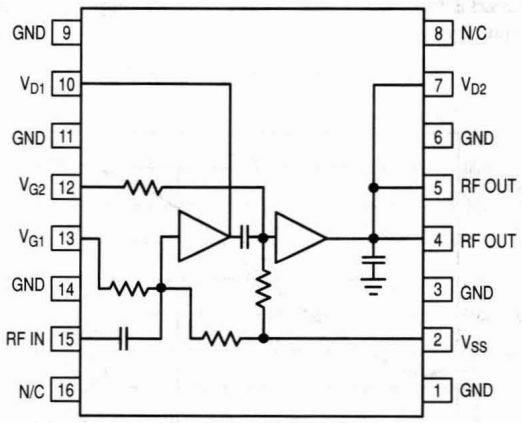
- Usable Frequency Range 800 to 1000 MHz
- Typical Output Power:
  36.0 dBm @ 5.8 Volts
  35.0 dBm @ 4.8 Volts
  31.5 dBm @ 3.6 Volts
- 48% Minimum Power Added Efficiency
- Low Parasitic, High Thermal Dissipation Package
- Order MRFIC0913R2 for Tape and Reel Option.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0913



CASE 978–02
(PFP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	9	Vdc
RF Input Power	P_{in}	15	dBm
Gate Voltage	V_{SS}	–6	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W



Pin Connections and Functional Block Diagram

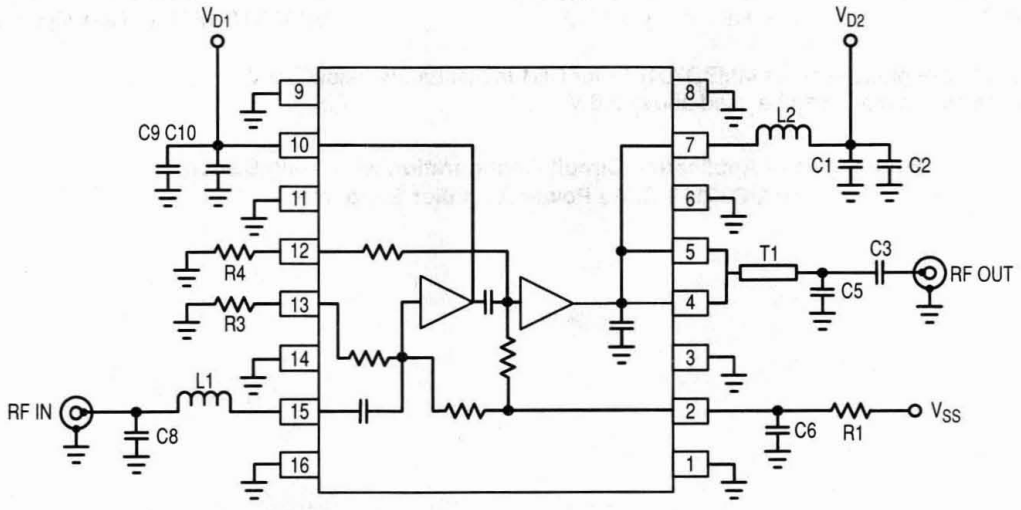
REV 1

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	2.7 to 7.5	Vdc
Gate Voltage	V_{SS}	–5 to –3	Vdc
RF Frequency Range	f_{RF}	800 to 1000	MHz
RF Input Power	P_{RF}	6 to 13	dBm

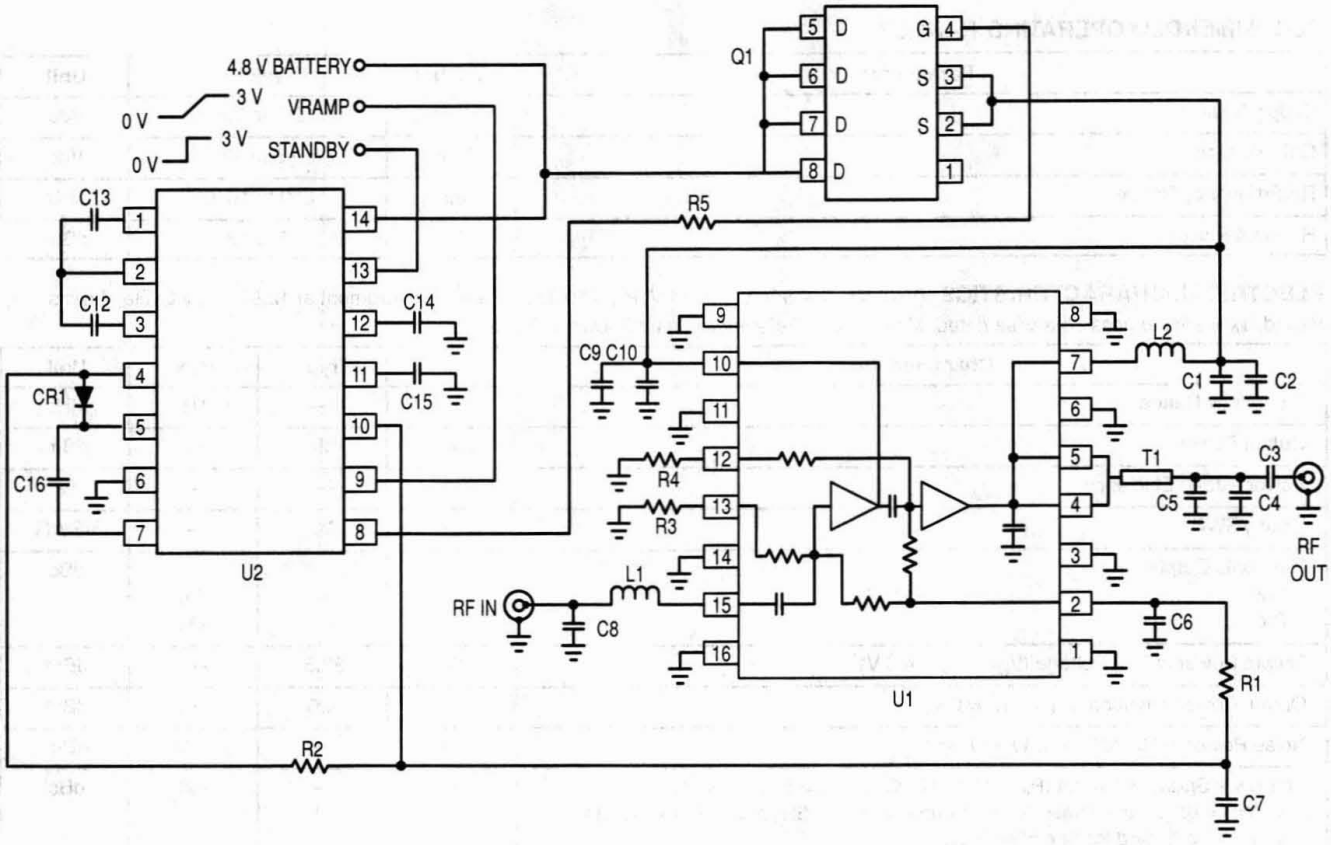
ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 4.8 V, V_{SS} = –4 V, P_{in} = 10 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	880	—	915	MHz
Output Power	34.5	35	—	dBm
Power Added Efficiency	48	—	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output 2nd 3rd	 — —	 — —	 –30 –35	dBc
Output Power at Low voltage (V_{D1}, V_{D2} = 4.0 V)	33.3	33.5	—	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	—	–20	–15	dBm
Noise Power in 100 kHz, 925 to 960 MHz	—	—	–90	dBm
Stability – Spurious Output (P_{in} = 10 to 13 dBm, P_{out} = 5 to 35 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle, V_{D1}, V_{D2} adjusted for Specified P_{out})	—	—	–60	dBc
Load Mismatch stress (P_{in} = 10 to 13 dBm, P_{out} = 5 to 35 dBm, Load VSWR = 10:1 at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 6 V)	1	—	—	MHz
Negative Supply Current	—	—	1.25	mA



C1, C3, C10	47 pF, ATC	L1	8.2 nH, 0805 Toko	R3	1.8 kΩ
C2, C9	47 nF, Vitramon	L2	10 Turn MicroSpring,	R4	2.7 kΩ
C5	10 pF, ATC		Coilcraft 1606–10	T1	5 mm 30 Ω Microstrip Line
C6	22 nF, Vitramon	R1	330 Ω	BOARD MATERIAL	Glass/Epoxy, ε_r = 4.45
C8	6.8 pF, ATC				

Figure 1. 900 MHz Reference Circuit



C1	33 pF, 0603 NPO/COG	CR1	MMBD701LT1	R2	100 Ω
C2, C9	33 nF	L1	8.2 nH, 0805 Toko	R3	1.8 kΩ
C3	47 pF, 0603 NPO/COG	L2	10 Turn MicroSpring,	R4	2.7 kΩ
C4, C5, C8	6.8 pF, 0603 NPO/COG		Coilcraft 1606–10 (for	R5	470 Ω
C6	33 nF		improved harmonic rejection	T1	5 mm 30 Ω Microstrip Line
C7	220 nF		only)	U1	MRFIC0913
C10	33 pF, 0603 NPO/COG	Q1	MMSF4N01HD	U2	MC33169 (–4 V Version)
C12 – C16	1 μF	R1	330 Ω	BOARD MATERIAL	Glass/Epoxy, ε_r = 4.45

Note: Use of a Schottky diode such as MMBD701LT1 for CR1 is mandatory below 3.6 V.
A general purpose silicon diode can be used above 3.6 V.

Figure 2. GSM Application Circuit Configuration with Drain Switch and MC33169 GaAs Power Amplifier Support IC

TYPICAL CHARACTERISTICS

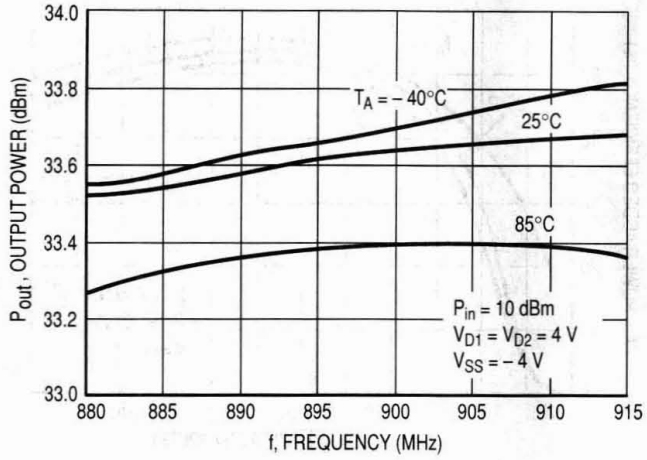


Figure 3. Output Power versus Frequency

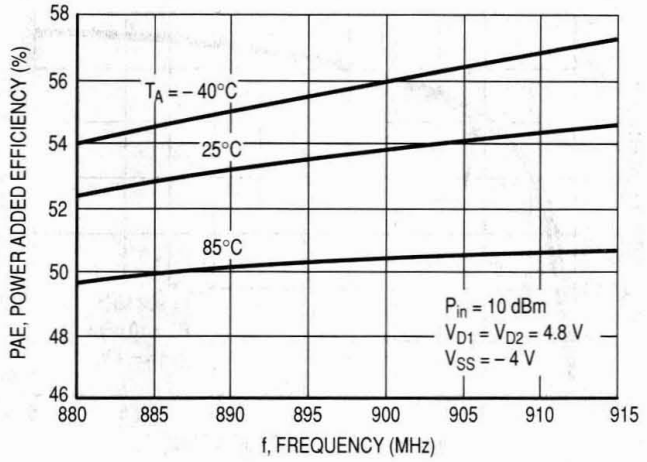


Figure 4. Power Added Efficiency versus Frequency

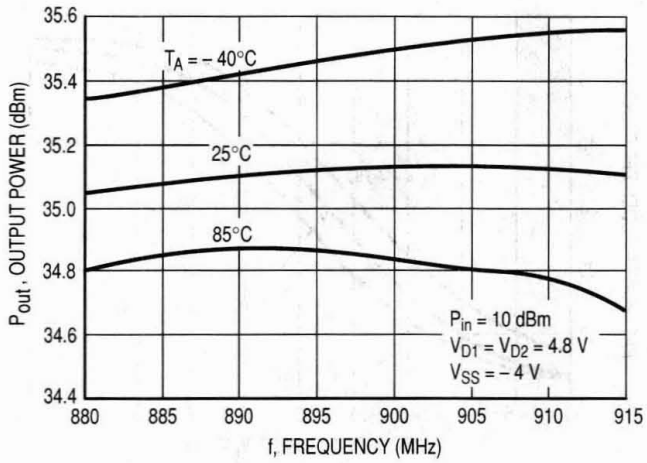


Figure 5. Output Power versus Frequency

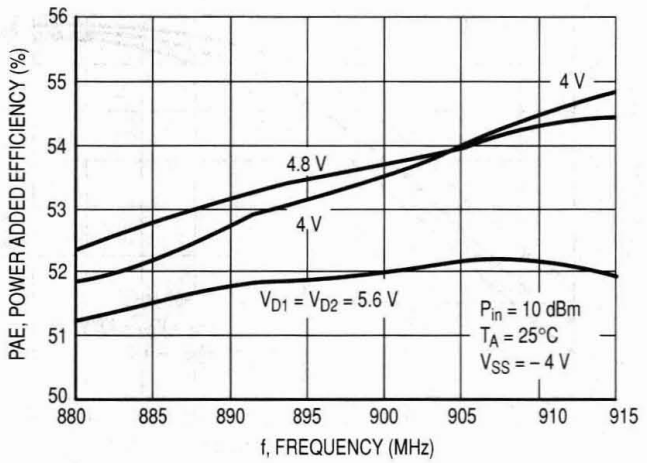


Figure 6. Power Added Efficiency versus Frequency

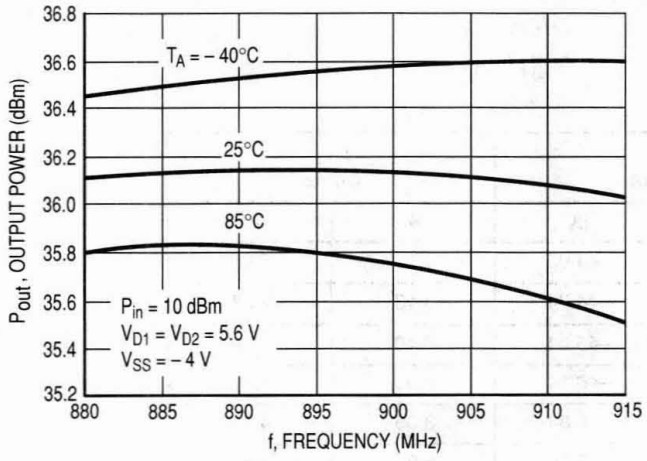


Figure 7. Output Power versus Frequency

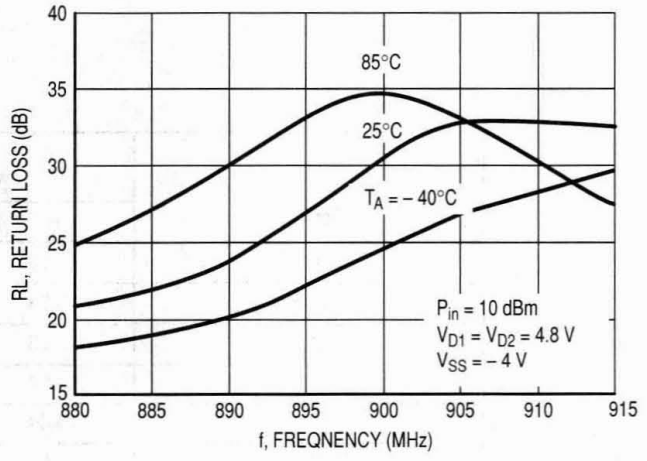


Figure 8. Input Return Loss versus Frequency

TYPICAL CHARACTERISTICS

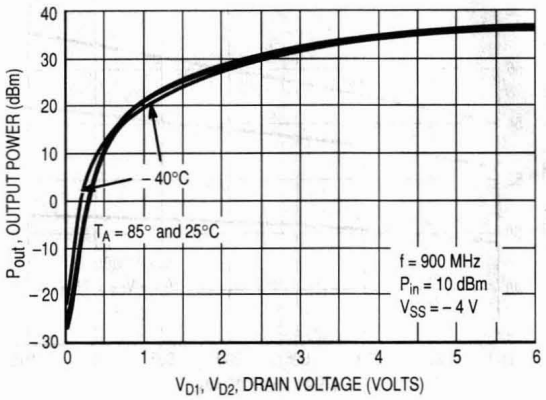


Figure 9. Output Power versus Drain Voltage

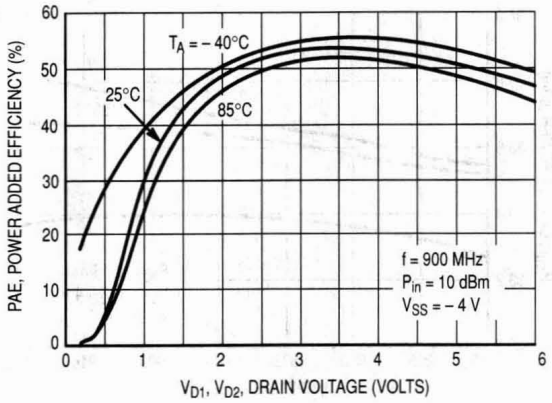


Figure 10. Power Added Efficiency versus Drain Voltage

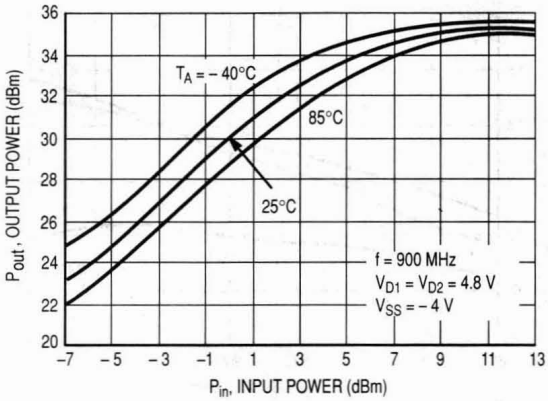


Figure 11. Output Power versus Input Power

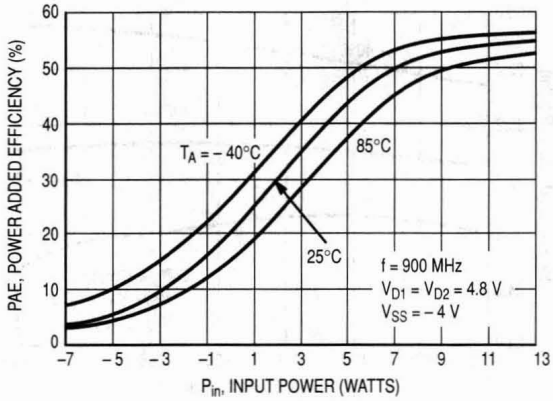


Figure 12. Power Added Efficiency versus Input Power

f	Z_{in} Ohms		Z_{OL}^* Ohms	
(MHz)	R	jX	R	jX
880	13.65	–44.05	3.15	5.06
885	13.64	–44.74	3.13	4.97
890	13.65	–45.44	3.10	4.89
895	13.64	–46.14	3.08	4.80
900	13.64	–46.84	3.06	4.71
905	13.65	–47.55	3.04	4.63
910	13.66	–48.27	3.02	4.54
915	13.66	–49.00	3.00	4.45

Table 1. Device Impedances Derived from Circuit Characterization

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC0913 is a two–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in GSM Class IV, 4.8 V operation. With matching circuit modifications, it is also applicable for use in GSM Class IV 6 V and Class V 3.6 V equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 800 to 1000 MHz frequency range. Typical performance at different battery voltages is:

- 36.0 dBm @ 5.8 V
- 35.0 dBm @ 4.8 V
- 31.5 dBm @ 3.6 V

This capability makes the MRFIC0913 suitable for portable cellular applications such as:

- 6 and 4.8 V GSM Class IV
- 3.6 V GSM Class V
- 3.6 V, 1.2 W Analog Cellular

RF Circuit Considerations

The MRFIC0913 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical GSM Class IV applications circuit.

The input match is a shunt–C, series–L, low–pass structure and can be retuned as desired with the only limitation being the on–chip 12 pF blocking capacitor. For saturated applications such as GSM and analog cellular, the input match should be optimized at the rated RF input power.

Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} supply line. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin.

Output matching is accomplished with a one–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50Ω microstrip transmission line. Values and positions are chosen to present a 3Ω loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. When low–Q commercial chip capacitors are used for the shunt capacitors, loss can be reduced by mounting two capacitors in parallel, as shown in Figure 2, to achieve the total value needed.

Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes. The bias supply line which supplies the output should include an RF choke of at least 8 nH, surface mount solenoid inductors or equivalent length of microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

The DC blocking capacitor required at the output of the device is best mounted at the 50Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Biasing Considerations

Gate bias is supplied to each stage separately through resistive division of the V_{SS} voltage. The top of each divider is brought out through pins 12 and 13 (V_{G2} and V_{G1} respectively) allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of each stage separately.

For applications where the amplifier is operated close to saturation, such as GSM and analog cellular, the gate bias can be set with resistors. Variations in process and temperature will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 80 to 160 mA for the first stage and 400 to 800 mA for the second stage.

For linear modes of operation which are required for PDC, DAMPS and CDMA, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1.25 mA is required in the divider network so a DAC can be used as the voltage source. Typical settings for 6 V linear operation are 100 mA ±5% for the first stage, and 500 mA ±5% for the second stage.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_D^2. This provides a very linear and repeatable power control transfer function. This technique can be used open–loop to achieve 20–25 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for GSM phase II control where 29 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control.

The transmit waveform ramping function required for systems such as GSM can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for GSM, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power.

For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC0913 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 300 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

The MRFIC0913 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as GSM where saturated amplifier operation is used.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

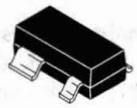
General Purpose RF Cascode Amplifier

MRFIC0916

SILICON GENERAL PURPOSE RF CASCODE AMPLIFIER

The MRFIC0916 is a cost–effective, high isolation cascode silicon monolithic amplifier in the industry standard SOT–143 surface mount package designed for general purpose RF applications. On chip bias circuitry sets the bias point while matching is accomplished off chip affording the maximum in application flexibility.

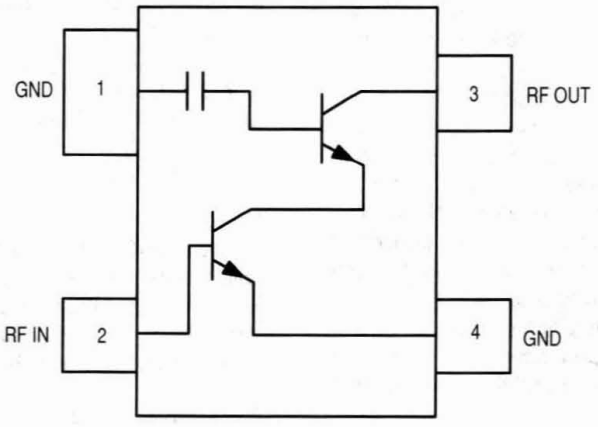
- Usable Frequency Range = 100 to 2500 MHz
- 18.5 dB typical gain at 850 MHz, V_{CC} = 2.7 Volts
- 2.3 dBm typical Output Power at 1 dB Gain Compression at 850 MHz, V_{CC} = 2.7 Volts
- 44 dB Typical Reverse Isolation at 850 MHz
- 5.6 mA Max Bias Current at V_{CC} = 2.7 Volts
- 2.7 to 5 Volt Supply
- Available in Tape and Reel by Adding T1 Suffix to Part Number. T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel.
- Device Marking = 16



CASE 318A–05
(SOT–143)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{CC}	6	Vdc
RF Input Power	P_{RF}	10	dBm
Power Dissipation	P_{DIS}	100	mW
Supply Current	I_{CC}	20	mA
Thermal Resistance, Junction to Case	$R_{\theta JC}$	250	°C/W
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Case Temperature	T_C	– 35 to +100	°C



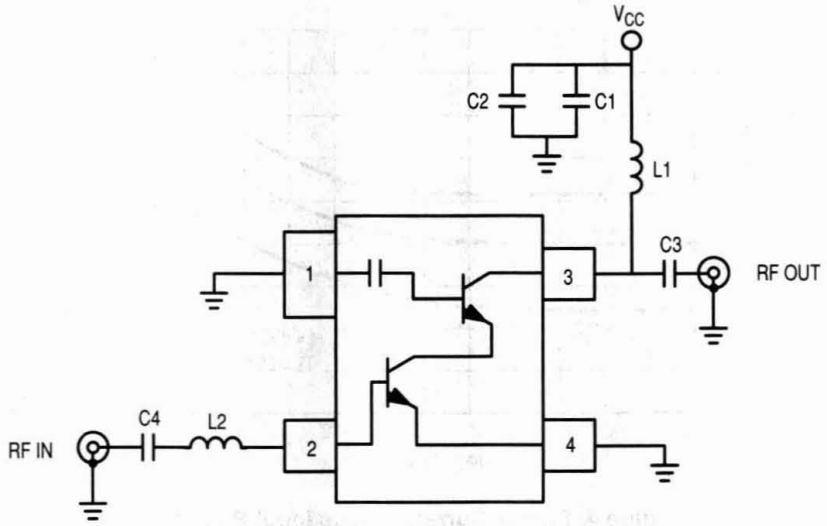
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	100 to 2500	MHz
Supply Voltage	V_{CC}	2.7 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, T_A = 25°C, f_{RF} = 850 MHz, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain	16.5	18.5	20.5	dB
Noise Figure	—	1.9	—	dB
Power Output at 1dB Gain Compression	0	2.3	—	dBm
Output 3rd Order Intercept Point	—	11	—	dBm
Reverse Isolation	—	44	—	dB
Supply Current	3.8	4.7	5.6	mA



C1 – 100 pF
C2 – 0.01 µF
C3 – 1.4 pF
C4 – 100 pF
L1 – 8.2 nH
L2 – 6.8 nH

Figure 1. 850 MHz Applications Circuit Configuration

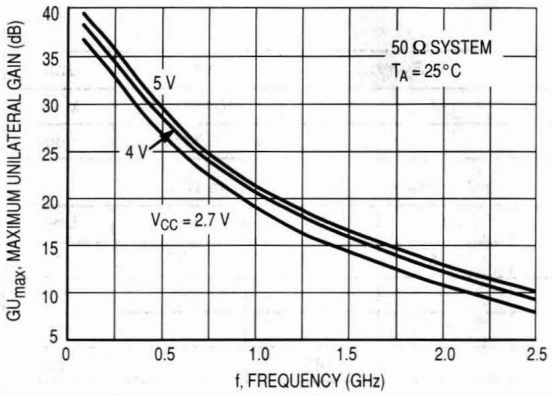


Figure 2. GU_{max} versus Frequency

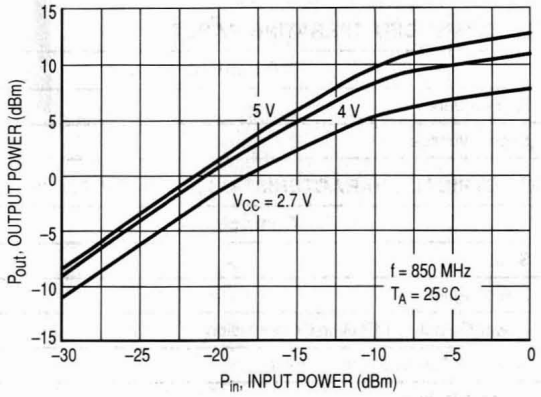


Figure 3. Output Power versus Input Power

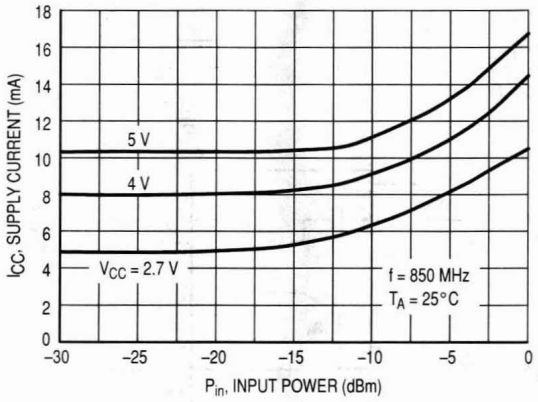


Figure 4. Supply Current versus Input Power

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
100	0.806	–17.01	12.03	162.32	0.001	–0.14	0.956	–4.69
200	0.765	–33.28	11.18	145.74	0.001	71.58	0.948	–8.69
300	0.713	–47.99	10.18	130.99	0.002	69.67	0.945	–13.23
400	0.652	–61.35	9.06	118.01	0.003	64.61	0.930	–17.35
500	0.574	–70.94	8.06	106.50	0.003	62.93	0.904	–20.85
600	0.533	–81.00	7.09	96.50	0.003	61.94	0.891	–24.71
700	0.493	–89.33	6.36	87.60	0.003	63.16	0.875	–28.18
800	0.469	–97.65	5.62	79.57	0.003	66.33	0.857	–31.89
900	0.432	–103.64	5.16	72.38	0.002	80.79	0.845	–35.21
1000	0.409	–110.68	4.70	65.39	0.002	100.33	0.831	–38.86
1100	0.396	–116.17	4.29	58.75	0.002	127.72	0.815	–42.52
1200	0.383	–122.20	3.91	52.55	0.003	152.57	0.799	–45.77
1300	0.373	–126.00	3.66	46.34	0.004	164.39	0.789	–49.49
1400	0.369	–131.29	3.38	40.61	0.006	169.63	0.776	–53.23
1500	0.366	–134.46	3.14	35.29	0.008	172.81	0.762	–56.86
1600	0.366	–140.07	2.93	29.63	0.011	172.47	0.751	–60.74
1700	0.364	–143.07	2.75	23.86	0.013	172.79	0.738	–64.66
1800	0.368	–147.48	2.58	18.42	0.016	171.54	0.727	–68.29
1900	0.377	–148.91	2.42	13.15	0.020	170.15	0.719	–72.29
2000	0.381	–153.42	2.27	7.58	0.023	167.89	0.707	–76.58
2100	0.394	–155.23	2.15	2.46	0.027	165.86	0.695	–80.50
2200	0.396	–158.91	2.03	–3.00	0.032	163.46	0.685	–84.85
2300	0.416	–160.43	1.90	–8.32	0.037	161.00	0.672	–88.93
2400	0.424	–162.98	1.81	–13.30	0.042	158.00	0.662	–93.38
2500	0.434	–166.35	1.68	–18.45	0.047	155.58	0.654	–97.89

Table 1. Scattering Parameters (V_{CC} = 2.7 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
100	0.744	–17.43	16.979	160.38	0.001	–2.89	0.955	–4.40
200	0.691	–33.58	15.442	142.46	0.001	83.36	0.950	–8.33
300	0.627	–47.53	13.633	127.28	0.002	76.39	0.946	–12.79
400	0.558	–59.50	11.851	114.52	0.002	70.12	0.931	–16.75
500	0.482	–67.02	10.284	103.51	0.002	67.02	0.907	–20.11
600	0.440	–75.50	8.957	94.12	0.002	66.00	0.895	–23.85
700	0.401	–81.87	7.930	85.95	0.002	68.71	0.880	–27.22
800	0.377	–88.89	7.003	78.57	0.002	73.50	0.863	–30.83
900	0.348	–93.11	6.348	71.96	0.002	90.55	0.852	–34.06
1000	0.328	–98.88	5.747	65.59	0.002	113.74	0.838	–37.62
1100	0.317	–103.27	5.223	59.57	0.002	146.45	0.822	–41.18
1200	0.306	–108.54	4.765	53.98	0.003	165.49	0.808	–44.34
1300	0.301	–111.30	4.425	48.39	0.004	175.51	0.798	–47.95
1400	0.297	–116.30	4.082	43.18	0.006	177.46	0.785	–51.59
1500	0.298	–118.89	3.790	38.32	0.008	179.45	0.771	–55.11
1600	0.298	–124.58	3.531	33.13	0.011	178.69	0.760	–58.88
1700	0.301	–127.19	3.300	28.02	0.014	178.02	0.748	–62.66
1800	0.305	–131.73	3.093	23.10	0.016	176.25	0.737	–66.16
1900	0.319	–133.16	2.901	18.34	0.020	174.44	0.729	–70.03
2000	0.324	–137.94	2.724	13.33	0.023	172.03	0.717	–74.16
2100	0.339	–140.09	2.575	8.67	0.027	169.82	0.706	–77.92
2200	0.342	–143.98	2.434	3.79	0.032	166.99	0.696	–82.07
2300	0.367	–146.00	2.278	–0.98	0.036	164.37	0.684	–86.04
2400	0.375	–148.75	2.166	–5.56	0.042	161.35	0.674	–90.25
2500	0.387	–152.75	2.020	–10.12	0.046	158.69	0.666	–94.64

Table 2. Scattering Parameters (V_{CC} = 4 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
100	0.707	–17.56	20.04	159.03	0.001	–7.95	0.954	–4.25
200	0.648	–33.40	17.93	140.29	0.001	86.24	0.950	–8.15
300	0.579	–46.60	15.53	124.94	0.002	78.79	0.946	–12.54
400	0.509	–57.44	13.31	112.38	0.002	72.27	0.931	–16.42
500	0.438	–63.51	11.40	101.70	0.002	69.34	0.908	–19.68
600	0.397	–70.90	9.87	92.70	0.002	69.55	0.896	–23.35
700	0.363	–76.05	8.69	84.92	0.002	71.59	0.882	–26.64
800	0.340	–82.18	7.67	77.89	0.002	79.44	0.865	–30.20
900	0.316	–85.44	6.91	71.60	0.002	95.59	0.855	–33.36
1000	0.298	–90.52	6.24	65.56	0.001	121.55	0.841	–36.86
1100	0.290	–94.44	5.67	59.82	0.002	152.13	0.826	–40.37
1200	0.280	–99.17	5.17	54.53	0.003	169.84	0.811	–43.48
1300	0.277	–101.65	4.79	49.25	0.005	177.80	0.802	–47.02
1400	0.274	–106.49	4.42	44.27	0.006	–179.84	0.790	–50.59
1500	0.278	–109.07	4.10	39.65	0.008	–179.19	0.776	–54.04
1600	0.276	–114.88	3.82	34.68	0.011	–179.68	0.765	–57.73
1700	0.281	–117.46	3.56	29.88	0.013	179.47	0.753	–61.43
1800	0.285	–122.11	3.34	25.21	0.016	177.73	0.742	–64.85
1900	0.300	–123.94	3.14	20.70	0.019	175.80	0.734	–68.66
2000	0.305	–128.93	2.95	15.91	0.023	173.47	0.723	–72.71
2100	0.322	–131.48	2.78	11.50	0.027	171.04	0.712	–76.37
2200	0.324	–135.50	2.63	6.84	0.031	168.25	0.703	–80.42
2300	0.351	–138.04	2.47	2.33	0.036	165.47	0.691	–84.31
2400	0.358	–140.88	2.34	–2.05	0.041	162.71	0.681	–88.42
2500	0.371	–145.28	2.19	–6.40	0.046	160.19	0.674	–92.74

Table 3. Scattering Parameters (V_{CC} = 5 V, 50 Ω System)

The MRFIC Line

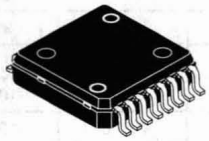
900 MHz GaAs Integrated Power Amplifier

MRFIC0917

900 MHz
GSM CELLULAR
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

This integrated circuit is intended for GSM class IV handsets. The device is specified for 2.5 Watts output power and 43% minimum power added efficiency under GSM signal conditions at 3.6 Volt supply voltage. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Pack package which gives excellent thermal performance through a solderable backside contact.

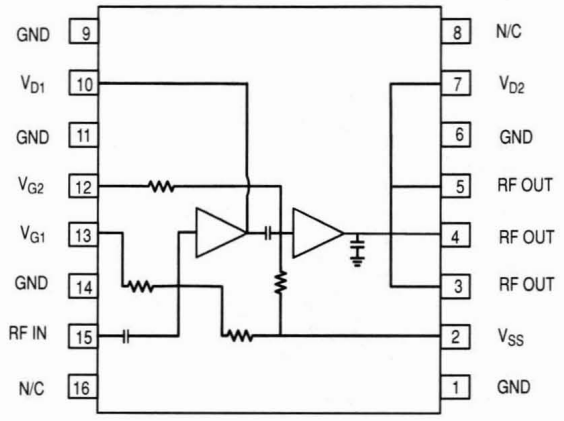
- Usable Frequency Range 800 to 1000 MHz
- Typical Output Power: 34.5 dBm @ 3.6 Volts
- 43% Minimum Power Added Efficiency
- Low Parasitic, High Thermal Dissipation Package
- Order MRFIC0917R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0917



CASE 978–02
(PFP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage, Normal Conditions	V_{D1}, V_{D2}	6	Vdc
Supply Voltage under Load Stress	V_{D1}, V_{D2}	4.5	Vdc
RF Input Power	P_{in}	15	dBm
Gate Voltage	V_{SS}	–6	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	15	°C/W



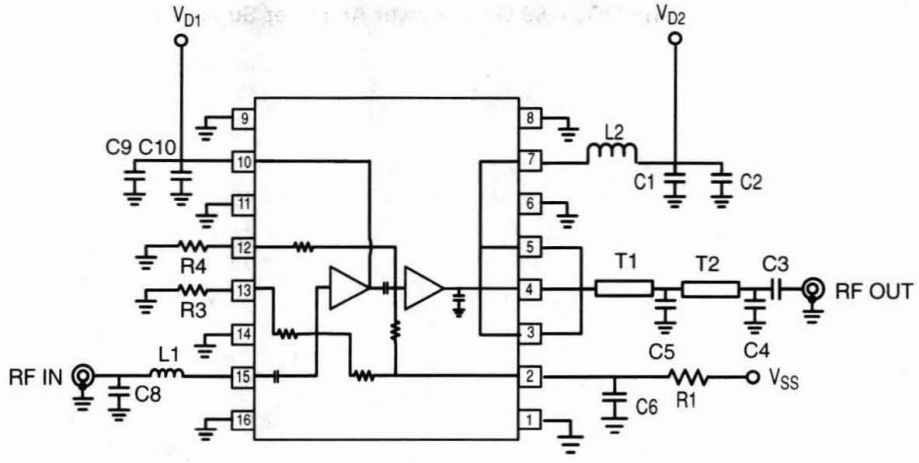
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	2.7 to 5.5	Vdc
Gate Voltage	V_{SS}	–5 to –3	Vdc
RF Frequency Range	f_{RF}	800 to 1000	MHz
RF Input Power	P_{RF}	6 to 13	dBm

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 3.6 V, V_{SS} = –4 V, P_{in} = 12 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Circuit Configuration Shown in Figure 1.)

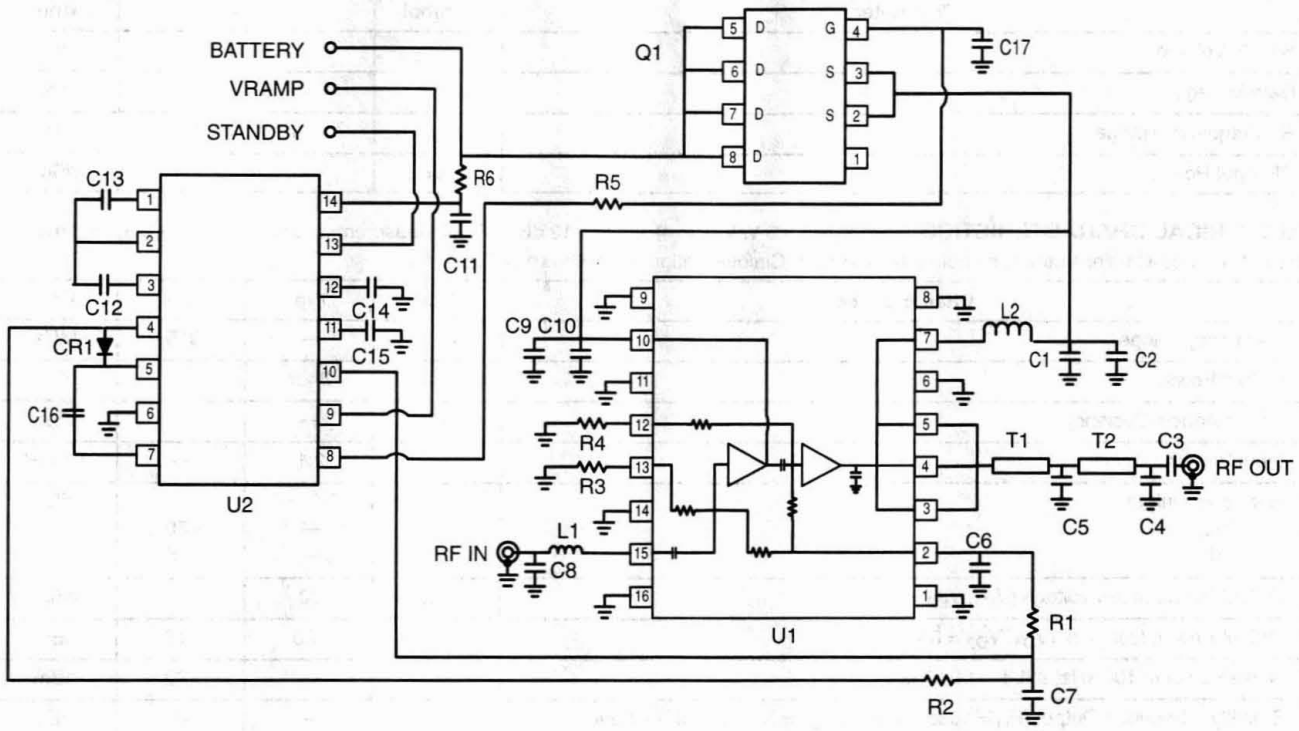
Characteristic	Min	Typ	Max	Unit
Frequency Range	880	—	915	MHz
Output Power	34	34.5	—	dBm
Power Added Efficiency	43	—	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output 2nd 3rd	 — —	 — —	 –30 –35	dBc
Output Power at low voltage (V_{D1}, V_{D2} = 3.0 V)	32.5	33	—	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	—	–20	–15	dBm
Noise Power in 100 kHz, 925 to 960 MHz	—	—	–90	dBm
Stability – Spurious Output (P_{in} = 10 to 13 dBm, P_{out} = 5 to 34.5 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	—	—	–60	dBc
Load Mismatch Stress (P_{in} = 10 to 13 dBm, P_{out} = 5 to 34.5 dBm, Load VSWR = 10:1 at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 4.5 V)	1	—	—	MHz
Negative Supply Current	—	—	1	mA



C1, C3, C10	33 pF	C8	6.8 pF
C2, C6, C9	33 nF	L1	5.6 nH
C4	4.7 pF	L2	10 Turn MicroSpring, Coilcraft 1606–10 or 18 mm 50 Ω MICROSTRIP
C5	10 pF		

R1, R3	330 Ω
R4	1 kΩ
T1	2 mm 30 Ω MICROSTRIP
T2	3.5 mm 30 Ω MICROSTRIP
BOARD MATERIAL	FR4

Figure 1. 900 MHz Reference Circuit



C1, C3, C10	33 pF	CR1	MMBD701LT1	R4	1 kΩ
C2, C6, C9	33 nF	L1	5.6 nH	R5	470 Ω
C4	4.7 pF	L2	10 Turn MicroSpring,	R6	22 Ω
C5	10 pF		Coilcraft 1606–10 or 18 mm	T1	2 mm 30 Ω MICROSTRIP
C7	220 nF		50 Ω MICROSTRIP	T2	3.5 mm 30 Ω MICROSTRIP
C8	6.8 pF	Q1	MMSF4N01HD	U1	MRFIC0917
C11 to C16	1 μF	R1, R3	330 Ω	U2	MC33169 (–4 V Version)
C17	0 to 5 nF Depending on control bandwidth	R2	100 Ω	BOARD MATERIAL	FR4

Figure 2. GSM Application Circuit Configuration with Drain Switch and MC33169 GaAs Power Amplifier Support IC

TYPICAL CHARACTERISTICS

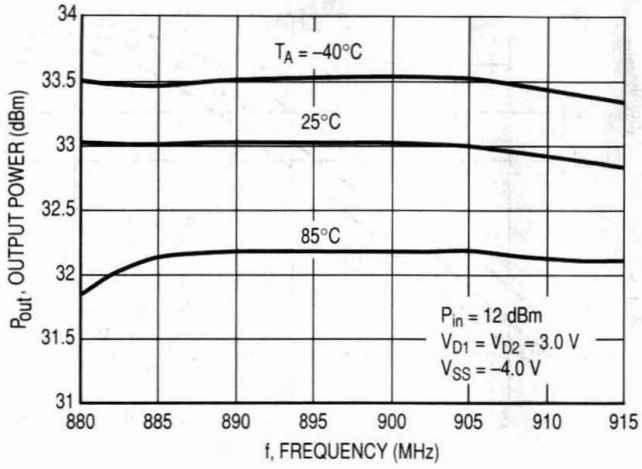


Figure 3. Output Power versus Frequency

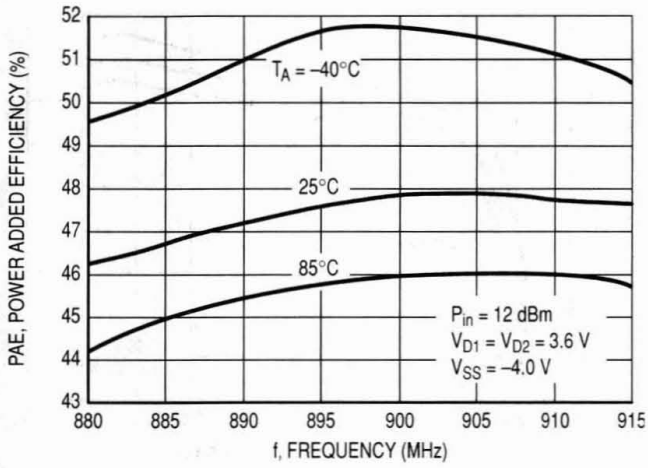


Figure 4. Power Added Efficiency versus Frequency

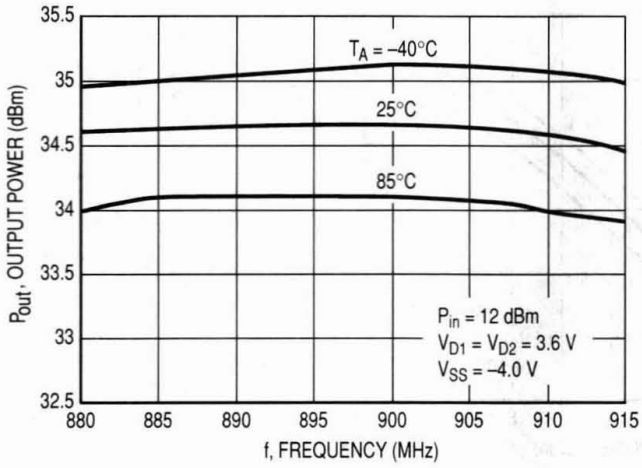


Figure 5. Output Power versus Frequency

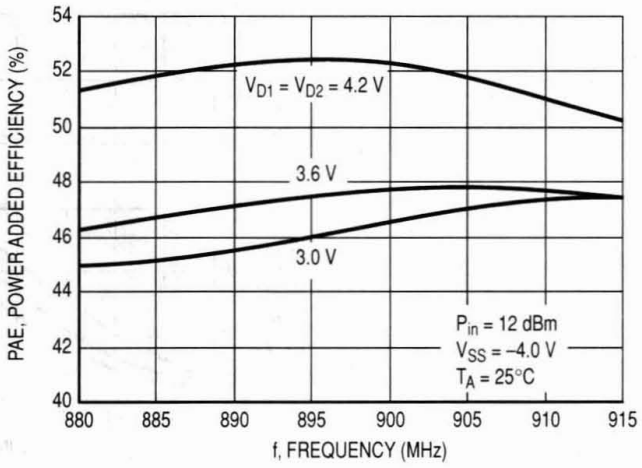


Figure 6. Power Added Efficiency versus Frequency

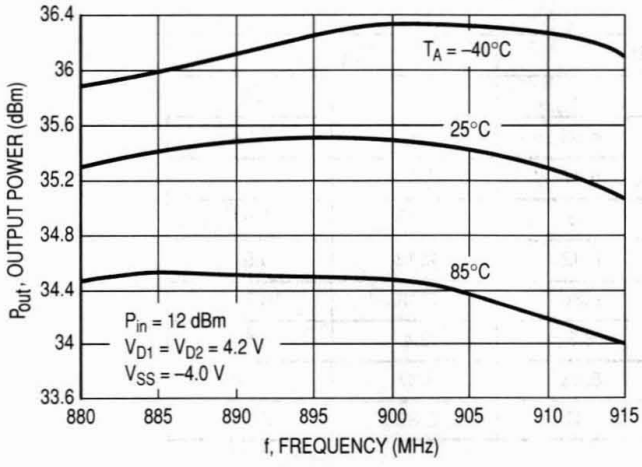


Figure 7. Output Power versus Frequency

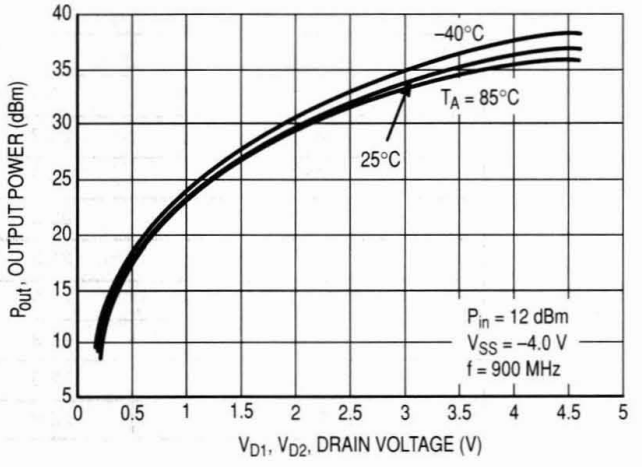


Figure 8. Output Power versus Drain Voltage

TYPICAL CHARACTERISTICS

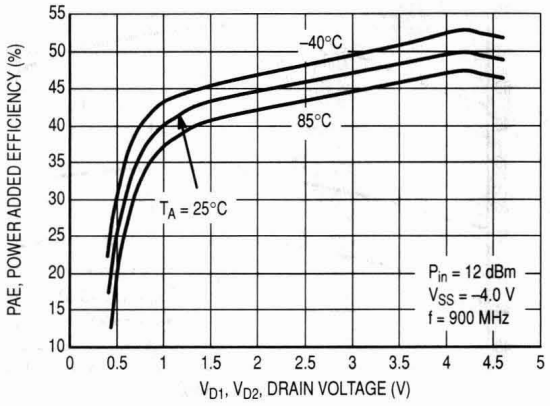


Figure 9. Power Added Efficiency versus Drain Voltage

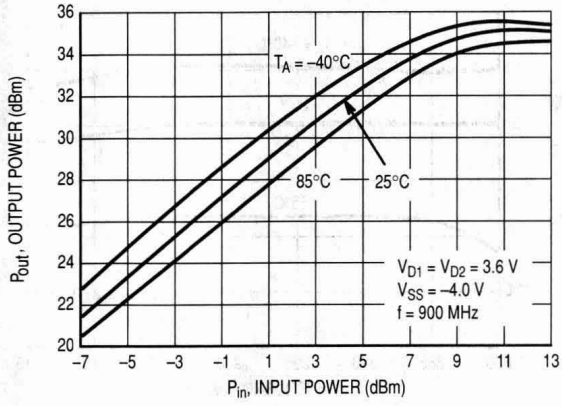


Figure 10. Output Power versus Input Power

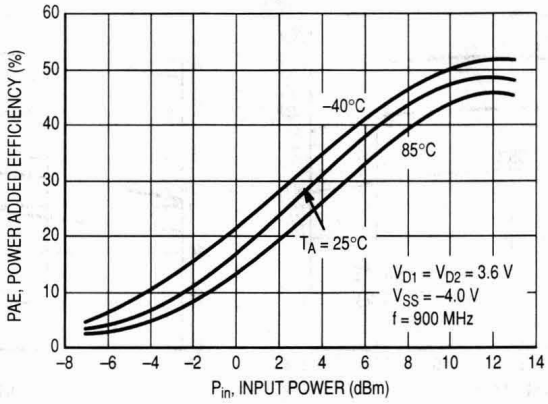


Figure 11. Power Added Efficiency versus Input Power

f	Z_{in} (Ω)		Z_{OL}^* (Ω)	
MHz	R	jX	R	jX
880	20.2	8.63	2.49	7.04
885	20.5	8.57	2.48	6.98
890	20.8	8.5	2.45	6.91
895	21.2	8.42	2.43	6.81
900	21.5	8.36	2.42	6.74
905	21.9	8.3	2.4	6.64
910	22.3	8.23	2.37	6.58
915	22.6	8.17	2.36	6.51

Table 1. Device Impedances Derived from Circuit Characterization

Table 2. Scattering Parameters

(V_{DD} = 3 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\lvert S_{11}\rvert$	∠ ϕ	$\lvert S_{21}\rvert$	∠ ϕ	$\lvert S_{12}\rvert$	∠ ϕ	$\lvert S_{22}\rvert$	∠ ϕ
500	0.738	–86	12.71	–82	0.002	147	0.891	173
600	0.786	–83	5.05	–102	0.003	132	0.874	170
700	0.799	–113	11.56	–79	0.004	153	0.858	173
800	0.681	–115	8.44	–113	0.005	138	0.885	171
820	0.671	–116	7.93	–115	0.005	138	0.887	170
840	0.669	–117	7.54	–117	0.005	133	0.885	170
860	0.668	–118	7.30	–119	0.005	130	0.888	170
880	0.673	–119	7.18	–121	0.006	129	0.885	169
900	0.672	–120	7.07	–123	0.006	131	0.883	169
920	0.672	–122	6.90	–127	0.006	130	0.883	168
940	0.672	–123	6.65	–130	0.006	130	0.882	168
960	0.673	–124	6.37	–133	0.007	127	0.881	168
980	0.682	–126	6.10	–136	0.007	130	0.88	168
1000	0.679	–127	5.83	–138	0.006	123	0.881	167
1100	0.685	–134	4.81	–145	0.007	120	0.874	166
1200	0.705	–143	4.67	–152	0.008	121	0.868	165
1300	0.703	–152	4.06	–165	0.010	113	0.855	164
1400	0.704	–161	3.69	–175	0.011	106	0.838	163
1500	0.646	–174	3.19	160	0.011	86	0.826	166

Table 3. Scattering Parameters

(V_{DD} = 3.6 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\lvert S_{11}\rvert$	∠ϕ	$\lvert S_{21}\rvert$	∠ϕ	$\lvert S_{12}\rvert$	∠ϕ	$\lvert S_{22}\rvert$	∠ϕ
500	0.737	–85	14.12	–84	0.002	135	0.887	174
600	0.792	–83	5.47	–103	0.002	130	0.866	170
700	0.799	–112	12.69	–80	0.004	157	0.853	174
800	0.687	–115	9.13	–115	0.005	131	0.881	171
820	0.681	–116	8.56	–117	0.005	131	0.882	171
840	0.680	–117	8.12	–119	0.005	132	0.882	170
860	0.678	–118	7.83	–121	0.005	131	0.883	170
880	0.680	–119	7.69	–123	0.005	129	0.882	170
900	0.681	–120	7.53	–125	0.006	133	0.882	169
920	0.680	–122	7.36	–129	0.006	127	0.879	169
940	0.681	–123	7.09	–132	0.006	130	0.878	169
960	0.681	–125	6.77	–135	0.006	121	0.878	168
980	0.688	–126	6.47	–137	0.006	123	0.878	168
1000	0.684	–128	6.18	–139	0.006	123	0.876	168
1100	0.690	–135	5.08	–147	0.007	116	0.870	166
1200	0.707	–143	4.90	–153	0.007	123	0.862	165
1300	0.701	–153	4.24	–167	0.009	112	0.852	164
1400	0.704	–162	3.83	–176	0.010	107	0.833	164
1500	0.643	–174	3.26	160	0.010	84	0.828	167

Table 4. Scattering Parameters

(V_{DD} = 4.2 V, V_{SS}, V_{G1}, V_{G2} Set for I_{DQ1}= 150 mA and I_{DQ2} = 750 mA, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\lvert S_{11}\rvert$	∠ϕ	$\lvert S_{21}\rvert$	∠ϕ	$\lvert S_{12}\rvert$	∠ϕ	$\lvert S_{22}\rvert$	∠ϕ
500	0.740	–85	15.59	–86	0.002	139	0.880	174
600	0.798	–84	5.71	–103	0.002	135	0.859	171
700	0.802	–112	13.82	–81	0.004	154	0.851	174
800	0.694	–116	9.82	–116	0.005	137	0.879	171
820	0.688	–116	9.20	–119	0.005	132	0.883	171
840	0.684	–117	8.70	–121	0.004	137	0.877	171
860	0.688	–119	8.37	–123	0.005	133	0.879	170
880	0.684	–120	8.20	–125	0.005	129	0.879	170
900	0.686	–121	8.03	–127	0.005	127	0.879	169
920	0.685	–123	7.82	–131	0.006	130	0.879	169
940	0.682	–124	7.53	–134	0.005	127	0.875	169
960	0.687	–126	7.18	–137	0.006	126	0.874	169
980	0.694	–127	6.84	–139	0.006	124	0.875	168
1000	0.686	–129	6.53	–141	0.006	123	0.873	168
1100	0.692	–137	5.34	–149	0.006	116	0.866	167
1200	0.704	–145	5.12	–155	0.007	122	0.861	165
1300	0.698	–154	4.41	–168	0.009	113	0.847	165
1400	0.695	–163	3.94	–178	0.010	104	0.835	164
1500	0.638	–175	3.34	159	0.009	84	0.828	167

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC0917 is a two–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in GSM Class IV, 3.6 V operation. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 800 to 1000 MHz frequency range.

This capability makes the MRFIC0917 suitable for portable cellular applications such as:

- 3.6 V 900 MHz DAMPS
- 3.6 V 900 MHz PDC

RF Circuit Considerations

The MRFIC0917 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical GSM Class IV applications circuit.

The input match is a shunt–C, series–L, low–pass structure and can be retuned as desired with the only limitation being the on–chip 12 pF blocking capacitor. For saturated applications such as GSM and analog cellular, the input match should be optimized at the rated RF input power.

Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} supply line. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin.

Output matching is accomplished with a two–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50Ω microstrip transmission line. Values and positions are chosen to present a 2Ω loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. When low–Q commercial chip capacitors are used for the shunt capacitors, loss can be reduced by mounting two capacitors in parallel to achieve the total value needed.

Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes. The bias supply line which supplies the output should include an RF choke of at least 8 nH, surface mount solenoid inductors or equivalent length of microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

The DC blocking capacitor required at the output of the device is best mounted at the 50Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_D^2. This provides a very linear and repeatable power control transfer function. This technique can be used open–loop to achieve 20–25 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for GSM phase II control where 29 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control.

The transmit waveform ramping function required for systems such as GSM can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for GSM, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power.

For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC0917 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Biasing Considerations

Gate bias is supplied to each stage separately through resistive division of the V_{SS} voltage. The top of each divider is brought out through pins 12 and 13 (V_{G2} and V_{G1} respectively) allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of each stage separately.

For applications where the amplifier is operated close to saturation, such as GSM and analog cellular, the gate bias can be set with resistors. Variations in process and temperature will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 100 to 200 mA for the first stage and 600 to 1200 mA for the second stage.

For linear modes of operation, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1.0 mA is required in the divider network so a DAC can be used as the voltage source. Typical settings for 3.6 V linear operation are 150 mA ±5% for the first stage, and 750 mA ±5% for the second stage.

Conclusion

The MRFIC0917 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as GSM where saturated amplifier operation is used.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

Advance Information

The MRFIC Line

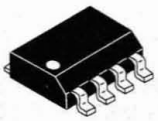
Balanced Transmit Mixer

MRFIC0931

BALANCED TRANSMIT MIXER SILICON MONOLITHIC INTEGRATED CIRCUIT

The MRFIC0931 is a balanced Gilbert cell mixer with LO buffer amplifier intended for transmit upmixer application. The device is usable for Industrial, Scientific and Medical (ISM), Cellular and PCS applications and is packaged in a low–cost surface mount package.

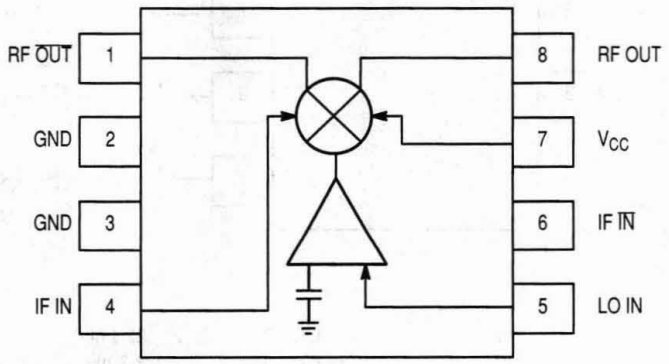
- Usable 500–2000 MHz
- High Output Power @ 1 dB Gain Compression, 3.6 Volts
  0.9 dBm (Typ) @ 900 MHz
  –2 dBm (Typ) @ 1800 MHz
- 2.7–4.8 Volts Operation
- Balanced Design for Good LO Rejection
- 47 mA (Max) Current @ 4.5 Volts
  45 mA (Max) Current @ 3.6 Volts
- Low Cost Surface Mount Package
- Order MRFIC0931R2 for Tape and Reel.
  R2 suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M0931



CASE 751-06
(SO-8)

ABSOLUTE MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	5	Vdc
Input Power, IF and LO	P_{IF}, P_{LO}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C



Pin Connections and Functional Block Diagram

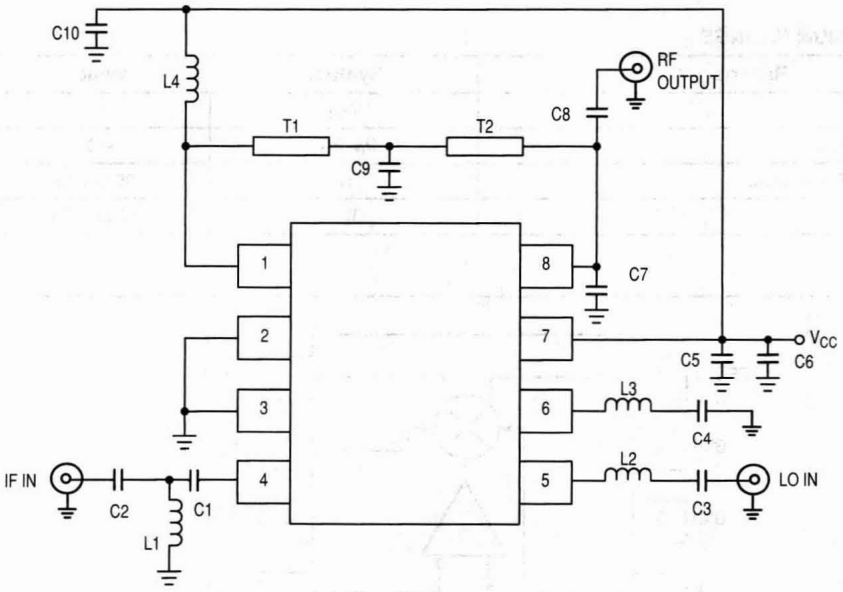
REV 2

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltages	V_{CC}	2.7 to 4.5	Vdc
RF Frequency Range	f_{RF}	500 to 2000	MHz
IF Frequency Range	f_{IF}	0 to 250	MHz

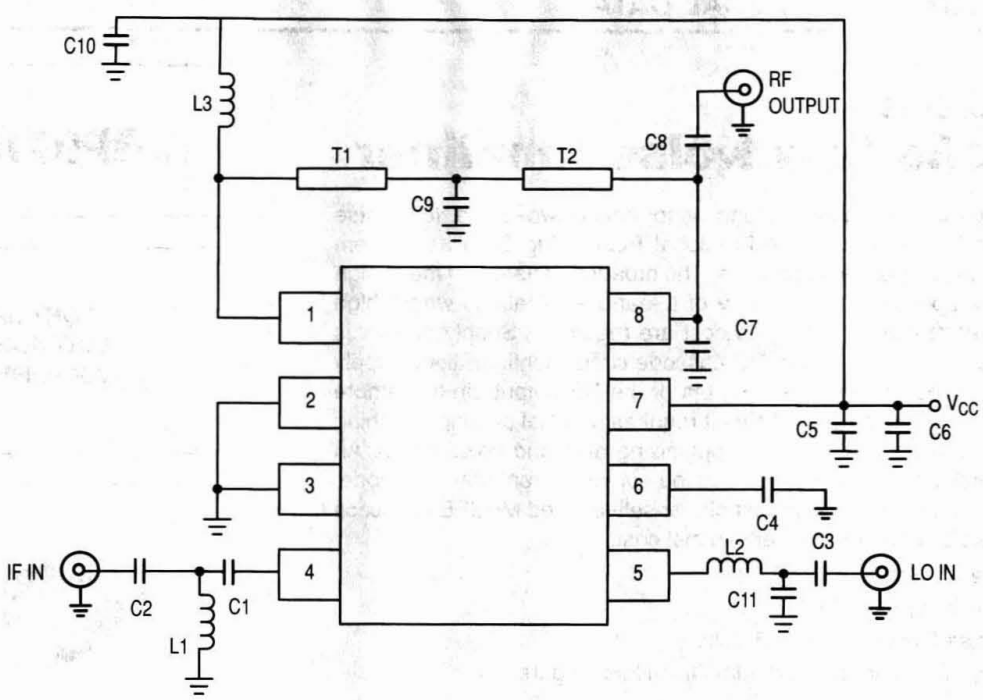
ELECTRICAL CHARACTERISTICS (T_A = 25°C, measured in circuit shown in Figure 1 or 2 as frequency indicates)

Parameter	Min	Typ	Max	Unit
RF Output Power (f_{IF} = 88 MHz, f_{LO} = 815 MHz, P_{LO} = –10 dBm, P_{IF} = –20 dBm, V_{CC} = 4.5 V)	2	4	8	dBm
LO Feed Through (f_{IF} = 88 MHz, f_{LO} = 815 MHz, P_{LO} = –10 dBm, P_{IF} = –20 dBm, V_{CC} = 4.5 V)	—	—	–16	dBc
Undesired Sideband Output (f_{IF} = 88 MHz, f_{LO} = 815 MHz, P_{LO} = –10 dBm, P_{IF} = –20 dBm, V_{CC} = 4.5 V)	—	—	– 25	dBc
Small Sigal Conversion Gain (f_{IF} = 100 MHz, P_{IF} = –25 dBm, V_{CC} = 3.6 V) 900 MHz (P_{LO} = –10 dBm) 1800 MHz (P_{LO} = –5 dBm)	 — —	 25 20	 — —	 dB dB
Power Output at 1 dB Gain Compression (f_{IF} = 100 MHz, P_{IF} = –25 dBm, V_{CC} = 3.6 V) 900 MHz (P_{LO} = –10 dBm) 1800 MHz (P_{LO} = –5 dBm)	 — —	 0.9 –2	 — —	 dBm dBm
Supply Current V_{CC} = 4.5 V V_{CC} = 3.6 V	 — —	 38 30	 47 45	 mA mA



C1, C4, C6, C10	1000 pF	L1, L3	220 nH
C2	13 pF	L2	3.3 nH
C3, C9	10 pF	L4	12 nH
C5	100 pF	T1, T2	1/8 λ 50 Ω Microstrip
C7	2.4 pF	Board Material	Epoxy/Glass ε_r = 4.45
C8	2 pF		

Figure 1. 903 MHz Configuration Test Circuit



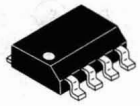
C1, C6, C10	1000 pF
C2	10 pF
C3, C4, C5, C8	100 pF
C7	1.2 pF
C9	2.7 pF
C11	1 pF
L1,	180 nH
L2	3.3 nH
L3	2.7 nH
T1, T2	1/8 λ 50 Ω Microstrip
Board Material	Epoxy/Glass ε_r = 4.45

Figure 2. 1800 MHz Applications Circuit

The MRFIC Line
GPS GaAs Low Noise Amplifier

MRFIC1501

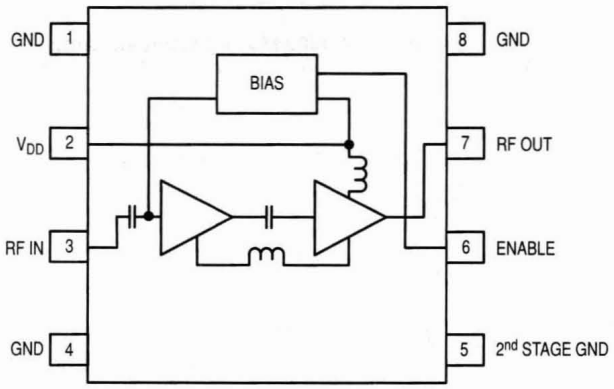
1.6 GHz GaAs LOW NOISE AMPLIFIER



CASE 751–06 (SO-8)

The MRFIC1501 is a low cost yet high performance two–stage, low–noise amplifier designed primarily for use in Global Positioning Satellite System (GPS) and other L–band satellite receivers. The broadband nature of the design makes the device applicable to a variety of L–band applications where high performance at reasonable current and cost are required. Supply current is minimized through a current sharing DC cascode circuit configuration. Supply voltage can be applied to either the V_{DD} pin or the RF output pin for remote antenna applications. The integrated circuit requires minimal off-chip matching while allowing for maximum flexibility in optimizing gain and noise figure. An ENABLE pin is provided to allow for a reduced supply current standby mode. The design employs Motorola's low cost planar self–aligned MESFET process to assure repeatable characteristics at minimal cost.

- Usable Frequency Range = 1 to 2 GHz
- 18 dB Typ Gain at V_{DD} = 5 Volts
- 1.1 dB Typ Noise Figure at V_{DD} = 5 Volts
- Simple Off-chip Matching for Maximum Gain/Noise Figure Flexibility
- Single Bias Supply = 3 to 5 Volts
- Low Power Consumption = 30 mW (Typ) at 5 Volts
- Low Cost Surface Mount Plastic Package
- Order MRFIC1501R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M1501



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

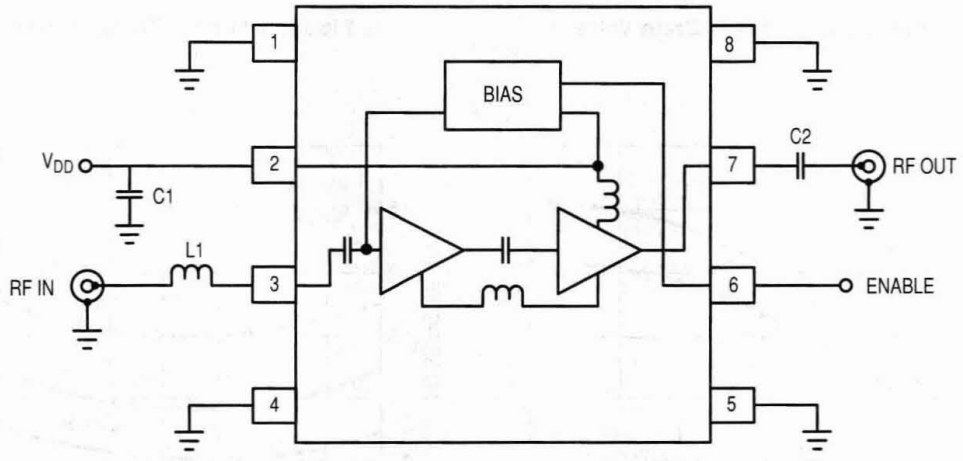
Ratings	Symbol	Limit	Unit
Supply Voltage	V_{DD}	6	Vdc
RF Input Power	P_{RF}	3	dBm
ENABLE Voltage	ENABLE	6	Vdc
V_{DD} Current Sourcing (With Supply Connected to Pin 7)	I_{PIN2}	20	mA
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to + 100	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	1 to 2	GHz
ENABLE "ON" (Device Operational) Voltage	ENABLE	$V_{DD} \pm 0.5$	Vdc
ENABLE "OFF" (Device in Standby Mode) Voltage	ENABLE	0 to 0.5	Vdc
Supply Voltage	V_{DD}	3 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, RF = 1.575 GHz, ENABLE = 5 V, Circuit Configuration Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Gain	17	18	—	dB
SSB Noise Figure	—	1.1	—	dB
RF Output 3rd Order Intercept Point	—	10	—	dBm
Output 1 dB Gain Compression	—	0	—	dBm
Reverse Isolation (s_{12})	—	30	—	dB
Input Return Loss	—	10	—	dB
Output Return Loss	—	10	—	dB
Supply Current	—	5.9	7.5	mA



C1, C2 – 22 pF
L1 – 11 nH (Implemented in Microstrip)

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

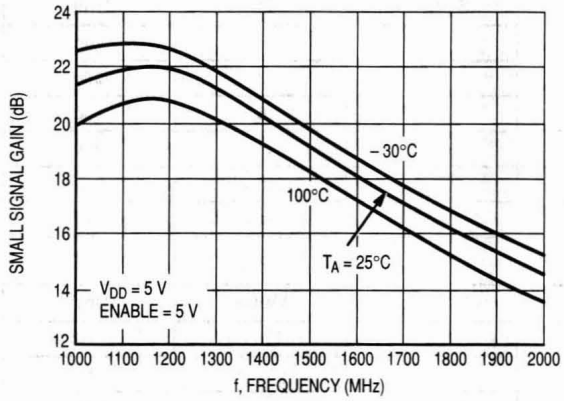


Figure 2. Small Signal Gain versus Frequency

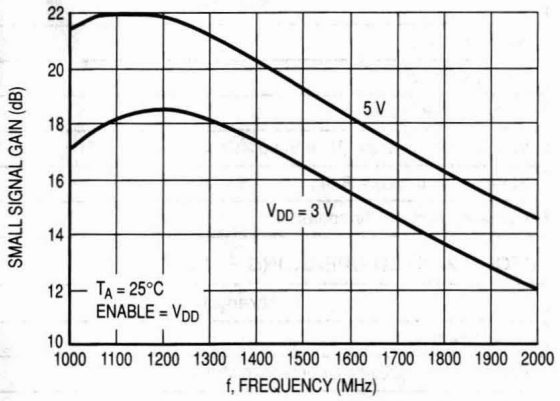


Figure 3. Small Signal Gain versus Frequency

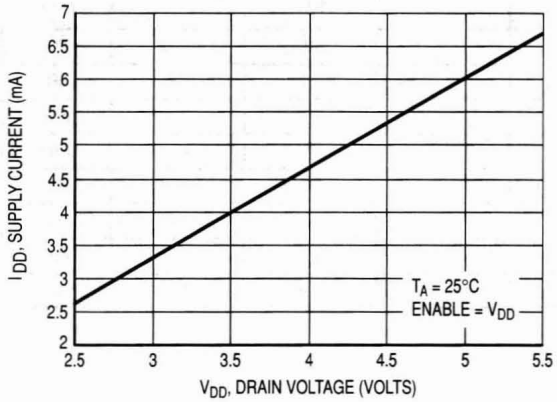


Figure 4. Drain Current versus Drain Voltage

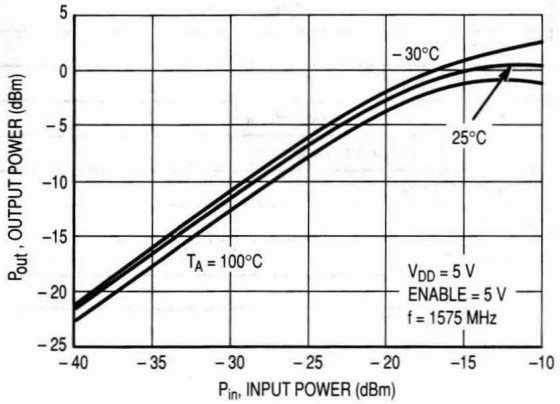


Figure 5. Output Power versus Input Power

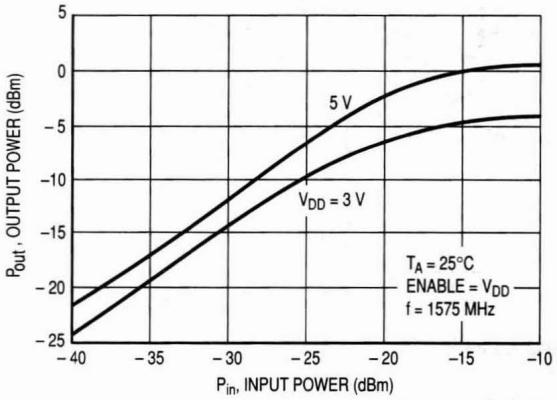


Figure 6. Output Power versus Input Power

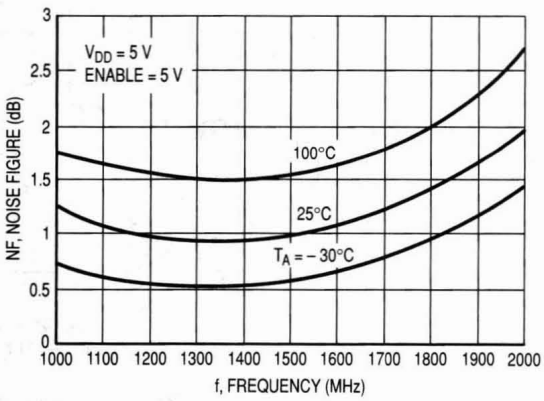


Figure 7. Noise Figure versus Frequency

TYPICAL CHARACTERISTICS

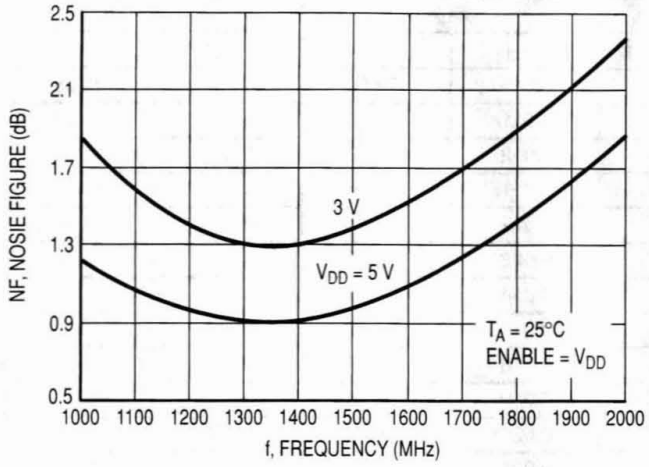


Figure 8. Noise Figure versus Frequency

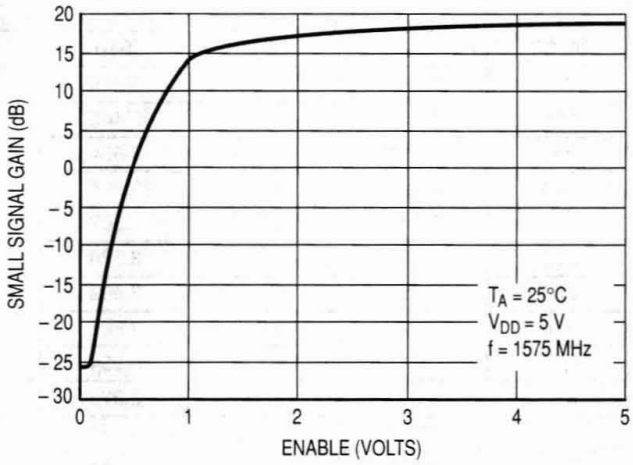


Figure 9. Gain versus ENABLE Voltage

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The circuit configuration employs a DC cascode arrangement which allows current sharing between two FETs. This gives excellent noise figure at reduced supply current. Since GPS applications often require the downconverter to be remotely mounted at the antenna, the output is DC coupled so that the drain voltage can be supplied through the coax feed. The V_{DD} pin can actually supply other components in the equipment at less than 20 mA of current. On–chip bias circuitry tracks changes in device threshold voltage and temperature and is externally controlled through the ENABLE pin. This feature allows for a low current standby mode or for gain reduction. Refer to Figure 9 for control characteristics.

CIRCUIT CONSIDERATIONS

As shown in Figure 1, impedance matching of the MRFIC1501 is quite simple. Through use of an on–chip source inductor in the first stage, Γ_{opt} and and Γ_{in}^{*} are approximately equal. A single inductor at the input will give good input match and noise figure. This inductor can be implemented with a high impedance microstrip line or a chip inductor.

As with all RF active circuit designs, bypassing the supply pin is recommended. Layout and ground via location is important. Vias should be located as close as possible to ground pins and the ground side of off–chip components.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" to the device type. For a complete list of currently available boards and ones in development for newly introduced products, please consult your local Motorola Distributor or Sales Office.

Table 1. Scattering Parameters (V_{DD} = 3 Volts, ENABLE = 3 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
795	0.958	–28.07	3.218	28.76	0.011	179.98	0.358	21.08
825	0.959	–29.71	3.448	23.95	0.011	176.45	0.336	15.36
855	0.954	–31.16	3.534	18.42	0.012	172.43	0.311	9.65
870	0.951	–32.04	3.535	16.03	0.011	171.06	0.297	6.67
900	0.945	–33.63	3.502	11.26	0.012	166.26	0.273	1.19
930	0.935	–35.48	3.528	6.47	0.013	166.48	0.250	–5.16
960	0.932	–37.28	3.689	2.07	0.014	164.19	0.227	–11.04
990	0.921	–39.03	3.867	–2.41	0.016	163.33	0.203	–18.26
1020	0.912	–40.69	3.954	–7.56	0.018	160.39	0.181	–25.17
1050	0.901	–42.28	3.975	–12.01	0.019	158.58	0.158	–33.18
1080	0.892	–44.16	4.039	–16.73	0.020	154.26	0.138	–40.98
1110	0.879	–46.05	4.154	–21.72	0.021	151.91	0.119	–49.98
1140	0.865	–47.91	4.296	–27.64	0.022	147.91	0.101	–58.85
1170	0.846	–49.35	4.320	–32.73	0.022	147.32	0.086	–71.10
1200	0.825	–51.34	4.224	–36.64	0.022	147.46	0.077	–87.14
1230	0.800	–51.92	4.125	–40.14	0.026	152.91	0.070	–118.39
1260	0.798	–52.57	4.224	–42.75	0.029	141.81	0.053	–155.35
1290	0.782	–53.50	4.371	–47.81	0.030	135.50	0.051	169.35
1320	0.775	–55.70	4.554	–53.11	0.031	132.76	0.049	140.94
1350	0.758	–57.05	4.525	–57.58	0.030	128.85	0.052	126.02
1380	0.742	–58.70	4.501	–61.64	0.031	125.89	0.061	114.60
1410	0.721	–60.03	4.511	–66.70	0.030	123.70	0.073	105.25
1440	0.703	–60.76	4.538	–71.38	0.031	121.40	0.083	97.32
1470	0.686	–61.48	4.553	–75.65	0.030	119.75	0.095	89.55
1500	0.668	–62.72	4.497	–79.44	0.031	116.74	0.107	82.70
1530	0.652	–63.71	4.436	–83.00	0.031	115.52	0.119	77.82
1560	0.633	–63.91	4.437	–87.36	0.030	115.29	0.132	72.37
1575	0.629	–64.01	4.458	–89.76	0.030	114.23	0.139	69.33
1590	0.621	–63.94	4.474	–91.54	0.030	112.50	0.147	66.71
1620	0.604	–64.46	4.477	–95.21	0.031	112.56	0.159	62.76
1650	0.586	–63.98	4.425	–98.51	0.030	111.63	0.172	58.00
1680	0.576	–64.45	4.330	–102.11	0.031	108.93	0.185	54.00
1710	0.559	–64.36	4.264	–105.61	0.030	106.34	0.198	50.85
1740	0.549	–64.02	4.227	–108.90	0.030	106.33	0.208	47.46
1770	0.538	–63.89	4.219	–112.08	0.030	106.56	0.222	43.54
1800	0.527	–63.69	4.172	–114.95	0.029	104.83	0.233	40.56
1830	0.523	–63.58	4.046	–118.53	0.030	104.72	0.244	37.76
1860	0.511	–62.83	3.965	–121.26	0.028	102.55	0.256	34.88
1890	0.503	–62.92	3.925	–124.29	0.029	103.12	0.266	32.47
1920	0.495	–62.26	3.917	–126.71	0.029	102.20	0.275	29.95
1950	0.485	–60.97	3.843	–129.24	0.029	102.70	0.283	27.89
1980	0.479	–60.47	3.759	–132.13	0.029	101.50	0.290	25.95
2010	0.474	–59.93	3.631	–135.13	0.027	98.87	0.300	24.27

Table 2. Scattering Parameters (V_{DD} = 4 Volts, ENABLE = 4 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
900	0.927	–34.45	4.901	4.43	0.011	167.24	0.210	–4.75
930	0.915	–36.30	4.962	–0.21	0.012	166.66	0.185	–12.35
960	0.908	–38.22	5.164	–4.86	0.013	165.06	0.160	–20.80
990	0.895	–39.78	5.383	–9.68	0.015	161.65	0.135	–30.56
1020	0.883	–41.42	5.485	–14.72	0.016	158.86	0.112	–42.22
1050	0.869	–43.05	5.514	–19.31	0.017	158.43	0.092	–55.71
1080	0.858	–44.69	5.573	–24.34	0.018	155.12	0.078	–73.31
1110	0.840	–46.48	5.695	–29.10	0.019	151.63	0.068	–94.03
1140	0.822	–48.23	5.813	–35.10	0.020	149.83	0.063	–115.86
1170	0.804	–49.58	5.817	–40.03	0.020	149.25	0.066	–136.79
1200	0.783	–51.19	5.741	–43.83	0.020	149.99	0.077	–153.70
1230	0.750	–51.37	5.625	–47.36	0.023	155.59	0.102	–172.32
1260	0.753	–51.39	5.762	–49.92	0.026	144.73	0.114	165.51
1290	0.747	–52.29	5.894	–55.24	0.028	137.19	0.122	150.89
1320	0.741	–54.09	6.078	–60.53	0.028	134.63	0.123	139.00
1350	0.727	–55.80	5.998	–65.01	0.028	131.72	0.129	131.12
1380	0.709	–57.17	5.957	–68.70	0.028	128.11	0.137	124.50
1410	0.692	–58.13	5.921	–73.18	0.027	126.13	0.144	117.65
1440	0.676	–59.05	5.928	–77.75	0.027	126.40	0.153	111.32
1470	0.661	–59.68	5.909	–81.80	0.028	122.94	0.162	105.05
1500	0.641	–60.62	5.821	–85.30	0.027	122.00	0.169	98.79
1530	0.628	–61.62	5.715	–88.81	0.028	119.28	0.179	93.52
1560	0.613	–61.52	5.686	–93.11	0.028	119.11	0.190	87.97
1575	0.606	–61.90	5.667	–95.29	0.028	119.48	0.196	85.31
1590	0.599	–61.76	5.667	–97.03	0.029	117.97	0.201	82.57
1620	0.587	–62.04	5.635	–100.45	0.028	117.17	0.209	78.01
1650	0.570	–61.74	5.550	–103.32	0.027	117.04	0.222	73.51
1680	0.560	–62.07	5.423	–106.67	0.028	114.76	0.233	69.07
1710	0.543	–62.20	5.318	–110.16	0.028	112.28	0.243	65.48
1740	0.534	–61.92	5.250	–113.26	0.028	113.29	0.253	61.42
1770	0.527	–61.70	5.212	–116.15	0.028	112.91	0.264	58.10
1800	0.516	–61.84	5.146	–118.66	0.029	113.11	0.274	54.22
1830	0.511	–61.24	4.991	–121.89	0.027	112.07	0.285	50.97
1860	0.501	–60.19	4.848	–124.80	0.027	111.64	0.295	47.95
1890	0.491	–60.35	4.783	–127.80	0.027	110.45	0.304	45.16
1920	0.484	–59.86	4.747	–130.12	0.028	109.45	0.315	42.60
1950	0.474	–58.58	4.697	–132.44	0.028	109.35	0.323	40.11
1980	0.471	–58.40	4.605	–134.97	0.028	111.10	0.329	38.15
2010	0.462	–57.51	4.407	–138.30	0.026	108.25	0.339	35.69

Table 3. Scattering Parameters (V_{DD} = 5 Volts, ENABLE = 5 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
900	0.909	–35.17	6.271	–1.16	0.011	168.82	0.163	–11.03
930	0.892	–37.01	6.337	–6.08	0.011	165.10	0.137	–21.39
960	0.882	–38.73	6.583	–10.74	0.012	163.68	0.109	–33.61
990	0.869	–40.38	6.808	–15.88	0.014	161.24	0.088	–49.68
1020	0.855	–41.71	6.927	–21.01	0.015	160.19	0.072	–71.47
1050	0.840	–43.22	6.925	–25.76	0.016	157.93	0.065	–98.66
1080	0.828	–44.84	6.996	–30.74	0.017	156.01	0.067	–124.50
1110	0.807	–46.50	7.081	–35.59	0.018	152.69	0.076	–144.89
1140	0.791	–47.98	7.172	–41.40	0.019	151.04	0.088	–161.86
1170	0.769	–49.03	7.150	–45.93	0.019	150.32	0.103	–174.42
1200	0.745	–50.40	7.082	–49.82	0.018	149.54	0.120	178.54
1230	0.716	–49.79	6.940	–53.44	0.021	156.21	0.149	168.88
1260	0.726	–49.58	7.070	–56.18	0.024	146.99	0.165	154.85
1290	0.724	–50.16	7.183	–61.43	0.025	140.13	0.175	144.80
1320	0.721	–52.48	7.285	–66.39	0.027	136.54	0.177	136.23
1350	0.707	–54.20	7.176	–70.78	0.025	133.27	0.183	130.59
1380	0.690	–55.55	7.102	–74.39	0.026	131.27	0.191	124.77
1410	0.675	–56.53	7.006	–78.73	0.026	129.73	0.198	119.51
1440	0.660	–57.13	6.962	–82.74	0.026	127.44	0.204	113.76
1470	0.646	–57.73	6.936	–86.50	0.026	126.66	0.212	108.23
1500	0.629	–58.40	6.822	–89.92	0.026	124.54	0.219	102.92
1530	0.618	–59.69	6.687	–93.31	0.026	122.48	0.227	98.15
1560	0.601	–59.69	6.606	–97.38	0.026	121.63	0.235	93.28
1575	0.594	–59.80	6.573	–99.55	0.027	122.68	0.243	90.64
1590	0.592	–59.78	6.548	–101.29	0.027	122.13	0.246	88.16
1620	0.577	–60.13	6.477	–104.22	0.027	120.48	0.254	84.10
1650	0.562	–59.69	6.366	–106.82	0.027	119.01	0.263	79.24
1680	0.552	–60.13	6.218	–110.11	0.027	118.15	0.272	75.16
1710	0.543	–60.34	6.094	–113.45	0.026	117.67	0.282	71.64
1740	0.529	–59.65	6.000	–116.40	0.027	118.05	0.291	67.99
1770	0.523	–59.54	5.945	–119.10	0.026	116.25	0.301	64.28
1800	0.515	–59.87	5.845	–121.60	0.027	117.55	0.311	60.73
1830	0.507	–59.61	5.676	–124.69	0.027	116.91	0.320	57.22
1860	0.497	–58.77	5.488	–127.65	0.027	115.88	0.330	54.18
1890	0.491	–58.79	5.414	–130.43	0.027	114.66	0.339	51.39
1920	0.478	–58.39	5.376	–132.53	0.028	117.05	0.348	48.34
1950	0.472	–57.29	5.324	–134.66	0.029	114.84	0.356	45.85
1980	0.466	–56.94	5.193	–137.20	0.028	114.82	0.363	43.87
2010	0.461	–56.18	4.972	–140.40	0.027	114.81	0.372	41.56

Table 4. Noise Parameters (V_{DD} = 5 Volts, ENABLE = 5 Volts, 50 Ω System)

f (MHz)	NF_{min} (dB)	Γ_0		R_N
		MAG	∠ ϕ	
1.000	0.8	0.859	26.36	0.98
1.575	1.0	0.793	43.87	0.70
2.000	1.3	0.713	55.80	0.56

The MRFIC Line
Integrated GPS Downconverter

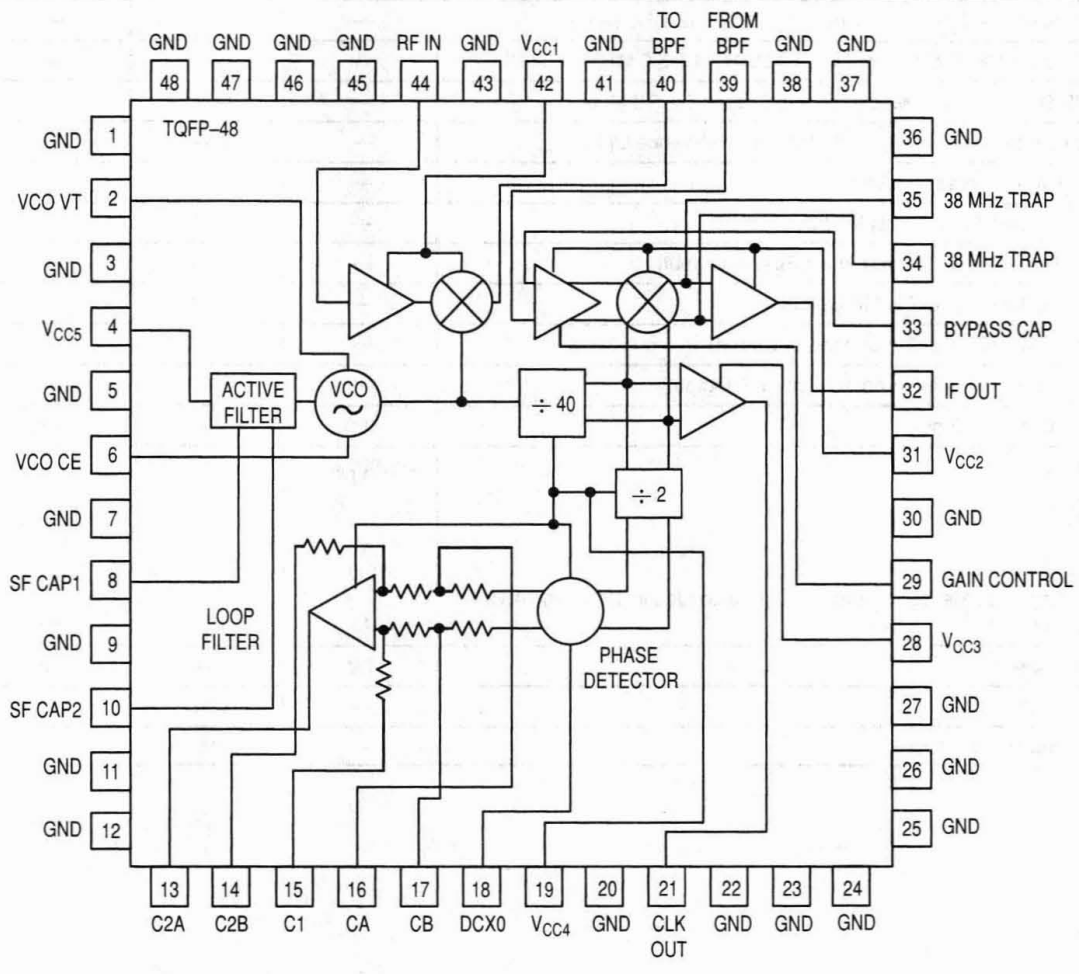
MRFIC1502

1.575 GHz GPS DOWNCONVERTER

This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Motorola's low–cost high performance MOSAIC 3 silicon bipolar process and is packaged in a low–cost surface mount TQFP–48 package. In addition to the mixers, a VCO, a PLL and a loop filter are integrated on–chip. Output IF is nominally 9.5 MHz.

- 65 dB Minimum Conversion Gain
- 5 Volts Operation
- 50 mA Typical Current Consumption
- Low–Cost, Low Profile Plastic TQFP Package
- Order MRFIC1502R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1502

CASE 932–02
(TQFP–48)



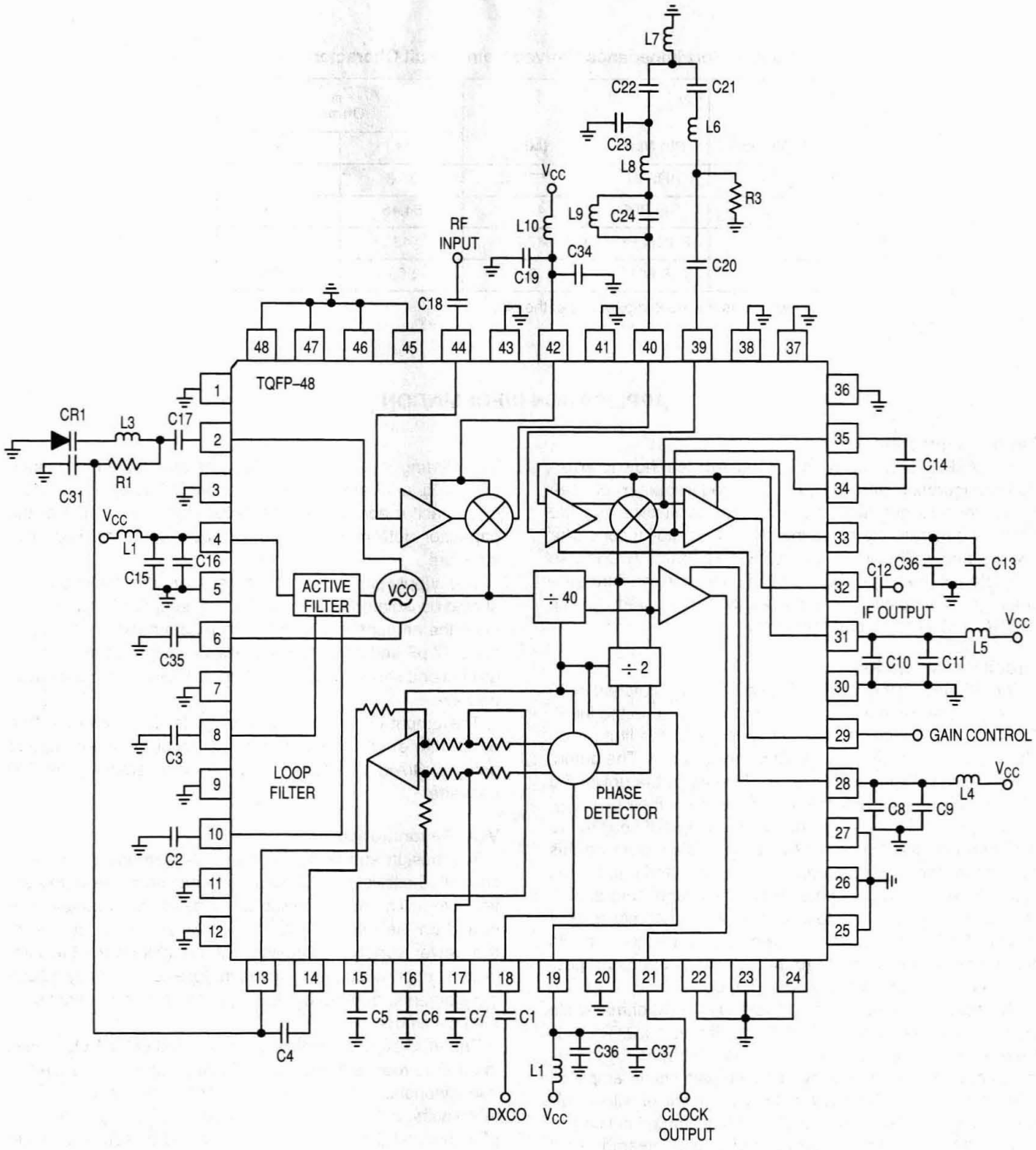
Pin Connections and Functional Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Limit	Unit
DC Supply Voltage	V_{DD}	+6.0	Vdc
DC Supply Current	I_{DD}	60	mA
Operating Ambient Temperature	T_A	– 40 to +100	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Lead Soldering Temperature Range (10 seconds)	—	+260	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, and V_{CC} = 5 V, Tested in Circuit shown in Figure 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Voltage	4.75	—	5.25	Vdc
Supply Current	—	—	60	mA
L–Band Gain (Measured from L–Band Input to 47 MHz Output)	—	20	—	dB
IF Gain (Measured from 47 MHz Input to 9.5 MHz Output with Gain Control at Maximum)	—	45	—	dB
Conversion Gain (Measured from L–Band Input to 9.5 MHz Output with Gain Control at Maximum)	65	—	—	dB
Gain Control (Externally Adjustable 0 to 5.0 V, Maximum at 0 V)	—	40	—	dB
Noise Figure (Double Sideband)	—	9.5	—	dB
L–Band Input VSWR (Measured into 50 Ω; 1575.42 ± 5.0 MHz)	—	2:1	—	—
First IF Output VSWR (Measured into 50 Ω; 47.74 ± 5.0 MHz)	—	2:1	—	—
Second IF Output VSWR (Measured into 50 Ω; 9.5 ± 5.0 MHz)	—	2:1	—	—
Input Impedance @ 1st IF 47.7 ± 5 MHz (For Reference Only)	—	2000	—	Ω
Output 1.0 dB Compression Point	—	–7	—	dBm
First LO (Measured at the First IF Output)	—	–20	—	dBm
All Other Harmonics (Measured at the First IF Output)	—	–45	—	dBm
38.1915 MHz Leakage at First IF Output	—	–50	—	dBm
Second LO (Measured at the Second IF Output)	—	–25	—	dBm
All Other Harmonics (Measured at Second IF Output)	—	–45	—	dBm
Reference Oscillator Input	400	—	4500	mVpp
Clock Output Frequency Amplitude Low High (Clock Amplitude Measured with the Output Loaded in 15 pF and 40 kΩ) Duty Cycle	$2Xf_{ref}$ — 2.0 45	—	$2Xf_{ref}$ 0.8 — 55	 V V %
VCO Lock Voltage	1.2	—	3.0	V
Phase Detector Gain	—	0.16	—	V/Radian
VCO Modulation Sensitivity	—	15	—	MHz/V



C1, C8, C10, C12, C13, C15, C19, C20, C37	10,000 pF	C24	68 pF, ATC
C4, C5	5600 pF	C35	0.4 pF, ATC
C6, C7, C31	1000 pF	CR1	2.7 pF, MA45233–123, MACOM
C2, C3	1.0 μF	L1, L4, L5, L10	2.2 μH, 1008CS–222XKBC, COILCRAFT
C14	3.9 pF, ATC	L3	2.2 nH, LL2012–F2N2S, TOKO
C16, C18, C36	27 pF, ATC	L6	2.2 μH
C17	15 pF, ATC	L7	220 nH
C21	5.6 pF, ATC	L8	0.56 μH
C9, C11, C34, C36	47 pF, ATC	L9	0.27 μH
C22, C23	120 pF, ATC	R1	10 kΩ
		R3	220 Ω

Figure 1. Test Circuit Configuration

Table 1. Port Impedance Derived from Circuit Characterization

Pin Number	Pin Name	f (MHz)	Z_{in} Ohms	
			R	jX
44	RF IN	1575.42	38.3	–16.09
40	TO BPF	47.74	54.45	11.3
39	FROM BPF	47.74	43	1.5
32	IF OUT	9.5	560	–850

Z_{in} represents the input impedance of the pin.

APPLICATION INFORMATION

Design Philosophy

The MRFIC1502 design is a standard dual downconversion configuration with an integrated fixed frequency phase–locked loop to generate the two local oscillators and the buffer to generate the sampling clock for a digital correlator and decimator. The active device for the L–band VCO is also integrated on the chip. This chip is designed in the third generation of Motorola's Oxide Self Aligned Integrated Circuits (MOSAIC 3) silicon bipolar process.

Circuit Considerations

The RF input to the MRFIC1502 is internally matched to 50 ohms. Therefore, only AC coupling is required on the input. The output of the amplifier is fed directly into the first mixer. This mixer is an active Gilbert Cell configuration. The output of the mixer is brought off–chip for filtering of the unwanted mixer products. The amplifier and mixer have their own V_{CC} supply (pin 42) in order to reduce the amount of coupling to the other circuits. There are two bypass capacitors on this pin, one for the high frequency components and one for the lower frequency components. These two capacitors should be placed physically as close to the bias pin as possible to reduce the inductance in the path. The capacitors should also be grounded as close to the ground of the IC as possible, preferably through a ground plane.

The output impedance of the first mixer is 50 ohms, while the input impedance to the first IF amplifier is 1 kΩ. There is a trap (zero) designed in at the second LO frequency to limit the amount of LO leakage into the high gain first IF amplifier.

The first IF amplifier is a variable gain amplifier with 25 dB of gain and 40 dB of gain control. The gain control pin can be grounded to provide the maximum gain out of the amplifier. If the baseband design utilizes a multi–bit A/D converter in the digital signal processing chip, this amplifier could be used to control the input to the A/D converter. The amplifier has an external bypassing capacitor. This capacitor should be on the order of 0.01 μF, and again should be located near the package pin.

The second mixer design is also a Gilbert Cell configuration. The interface between the mixer and the second IF amplifier is differential in order to increase noise immunity. This differential interface is also brought off–chip so that some additional filtering could be added in parallel between the output of the mixer and input to the amplifier. This filtering is primarily to reduce the amount of LO leakage into the final IF amplifier and is achieved using a single 3.9 pF capacitor across the differential ports. The value of the capacitor determines the high frequency of the low pass structure.

The supply pin for the IF circuits is pin 33. This supply pin should be isolated from the other chip supplies in order to reduce the amount of coupling. The recommended capacitors are a 47 pF and a 0.01 μF, in parallel to bypass the supply to ground and should be placed physically as close to the pin as possible.

The output of the second IF amplifier is 50 ohms with a bandwidth of ±5.0 MHz. This signal must be filtered before being digitized in order to limit the noise entering the A/D converter.

VCO Resonator Design

The design and layout of the circuits around the voltage controlled oscillator (VCO) are the most sensitive of the entire layout. The active device and biasing resistors are integrated on the MRFIC1502. The external circuits consist of the power supply decoupling, the capacitors for the integrated supply superfilter, the resonator and frequency adjusting elements, and the bypassing capacitor on the emitter of the active device.

The VCO supply is isolated from the rest of the PLL circuits in order to reduce the amount of noise that could cause frequency/phase noise in the VCO. The supply should be filtered using a 22 μH inductor in series and a 27 pF and 0.01 μF in parallel. The 27 pF capacitor should be series resonant at least as high as the VCO frequency to get the most L–band bypassing as possible. The on–chip supply filter requires two capacitors off–chip to filter the supply. The capacitors on the input (pin 8) and output (pin 10) of the filter are 1.0 μF, and the output also has a high frequency bypass capacitor in parallel. The input capacitor should not be smaller than a 1.0 μF to insure stability of the supply filter.

The VCO design is a standard negative resistance cell with a buffer amplifier. The resonating structure is connected to the base of the active device and consists of a coupling capacitor, a hyper–abrupt varactor diode, and a wire wound chip inductor. With the values shown on the application

circuit, the VCO is centered at 1527.7 MHz, and the gain of the VCO is approximately 20 MHz/Volt.

The above performance is heavily dependent on the capacitive structure that is used as the emitter bypass on pin 6. The total capacitance should be approximately 1.0 pF; that can be achieved using either a discrete element or a microstrip open circuited stub. The evaluation circuit shown uses a 0.4 pF capacitor.

Phase–locked Loop Design

The VCO signal at 1527.68 MHz is divided by 40 to get the second LO frequency of 38.19 MHz. In addition to providing the LO to the second mixer, the 38 MHz signal is output through a translator and is used as the sampling clock for the digital correlator and decimator circuits. There is an additional divide by two so the signal used by the phase detector is at 19.096 MHz. The reference input to the phase detector (pin 18) has an input sensitivity of 400 mVpp minimum and 2.5 Vpp maximum.

The loop filter design is the standard op–amp loop filter, resulting in a type 2 second order loop. The layout of the discrete components around the loop filter and VCO is very critical to the performance of the phase–locked loop. Care should be taken in routing the VCO control voltage line from the output of the loop filter to the varactor diode.

The output of the divide by 40 is buffered by a clock translator that converts the low level sine wave into a TTL level square wave. The loading on the buffer is high so the peak currents can reach as high as 50 mA with the maximum load of 1.0 kΩ in parallel with 40 pF on the output. Therefore, the translator has a dedicated V_{CC} supply, pin 28, which requires external bypassing and isolation. The recommended bypassing uses two capacitors in parallel, a 47 pF and a 0.01 μF capacitor.

Conclusion

The MRFIC1502 offers a highly integrated downconverter solution for GPS receivers. For more detailed applications information on GPS system design refer to application note AN1610, "Using Motorola's MRFIC1502 in Global Positioning System Receivers."

The MRFIC Line
1.8 GHz Antenna Switch

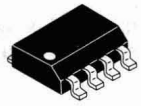
Designed primarily for use in DECT, Japan Personal Handy System (PHS), other wireless Personal Communication Systems (PCS) applications, and 2.4 GHz ISM band applications. The MRFIC1801 is a single pole, double throw reflective antenna switch featuring low insertion loss and high power handling capability in a low-cost SOIC-8 package. The integrated circuit requires no off-chip matching and provides for easy control circuit interface. The high power handling capability allows application in higher power wireless systems than traditional GaAs antenna switches.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

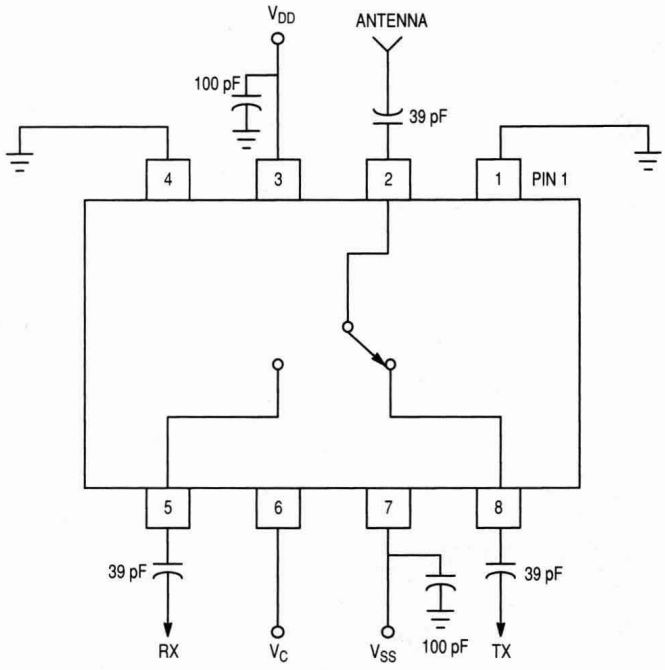
- Usable Frequency Range 1.5 to 2.5 GHz
- High 1.0 dB Compression Point = 29 dBm (Typ)
- Low Transmit Insertion Loss = 0.75 dB (Typ)
- High Transmit to Receive Isolation = 22 dB (Typ)
- Single Control Pin for Easy Switching Signal Interface
- Low Current Drain = 300 μA (Typ) in TX, 45 μA (Typ) in RX
- Low Cost Surface Mount Plastic Package
- Order MRFIC1801R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M1801

MRFIC1801

1.8 GHz
TRANSMIT/RECEIVE
ANTENNA SWITCH
GaAs MONOLITHIC
INTEGRATED CIRCUIT



CASE 751–06
(SO-8)



Functional Block Diagram and Pin Assignment

MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	10	Vdc
Supply Voltage Difference	$V_{DD} - V_{SS}$	8	Vdc
RF Input Power	P_{in}	33	dBm
Switch Control Voltage	V_C	V_{DD} +1, V_{SS} –1	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to + 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	2.7 to 5.5	Vdc
Supply Voltage Difference	$V_{DD} - V_{SS}$	5.5	Vdc
Switch Control Voltage	V_C	V_{DD} to V_{SS}	Vdc
Operating Frequency	f	1.5 to 2.5	GHz

ELECTRICAL CHARACTERISTICS ($V_{DD} - V_{SS}$ = 5.5 V, T_A = 25°C, f = 1.9 GHz)

Characteristic	Min	Typ	Max	Unit
Antenna to Receive Insertion Loss (RX Mode, P_{IN} = 0 dBm)	—	0.8	1	dB
Transmit to Antenna Insertion Loss (TX Mode, P_{IN} = +27 dBm)	—	0.6	1	dB
Transmit to Receive Isolation in TX Mode (P_{IN} = +27 dBm)	—	22	—	dB
Antenna to Transmit Isolation in RX Mode (P_{IN} = 0 dBm)	—	18	—	dB
Input Return Loss, all ports	—	15	—	dB
Transmit to Antenna Input 1.0 dB Compression	—	29	—	dBm
Leakage Current (RX Mode)	—	45	—	μA
Total Supply Current (TX Mode)	—	300	—	μA

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

APPLICATIONS INFORMATION

The MRFIC1801 is a SPDT switch. A series–shunt pair of FETs are used in each path for improved isolation. The power handling capability of the MRFIC1801 is determined by the difference between V_{DD} and V_{SS}. Typical operating conditions are V_{DD} = 3.0 V and V_{SS} = –2.5 V, but a negative V_{SS} is not required. V_{SS} can be grounded.

Mode	V_C
RX	V_{SS}
TX	V_{DD}

Table 1. Logic Table

TYPICAL CHARACTERISTICS
($V_{DD} - V_{SS} = 5.5$ V)

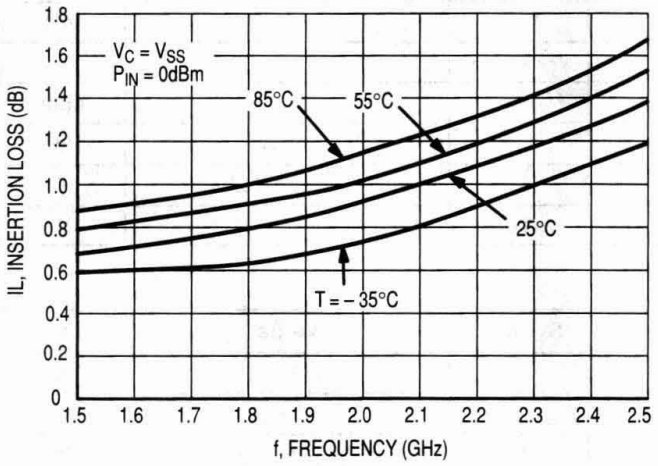


Figure 1. Antenna to Receive Insertion Loss

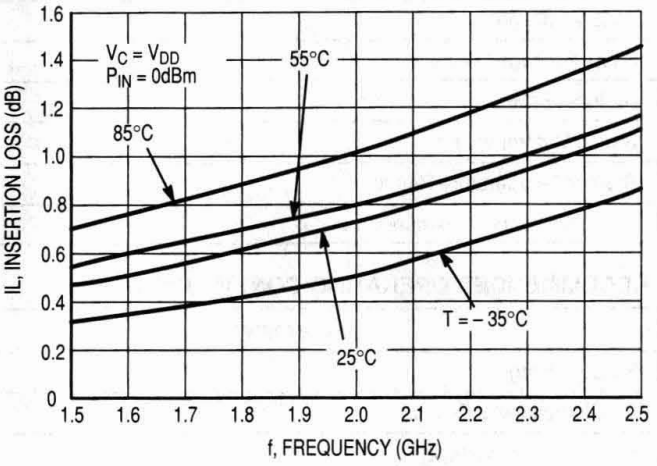


Figure 2. Transmit to Antenna Insertion Loss (Small Signal)

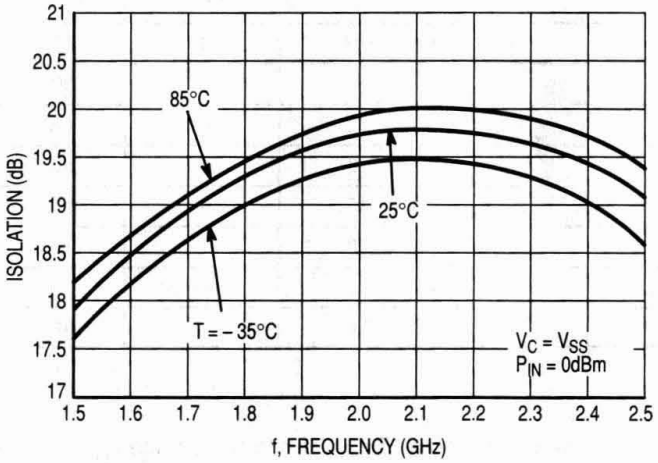


Figure 3. Antenna to Transmit Isolation in RX Mode

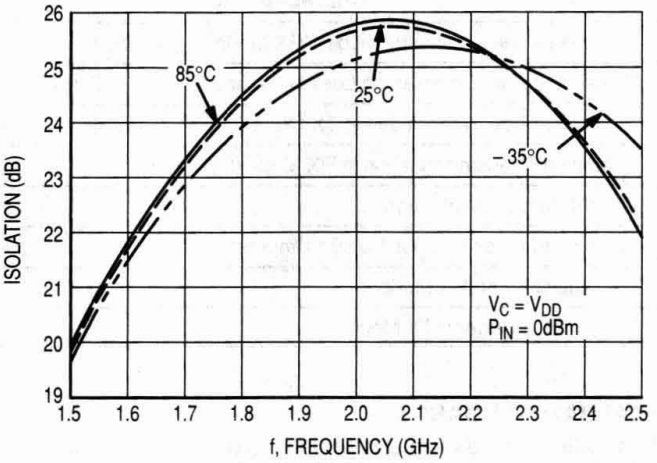


Figure 4. Transmit to Receive Isolation in TX Mode

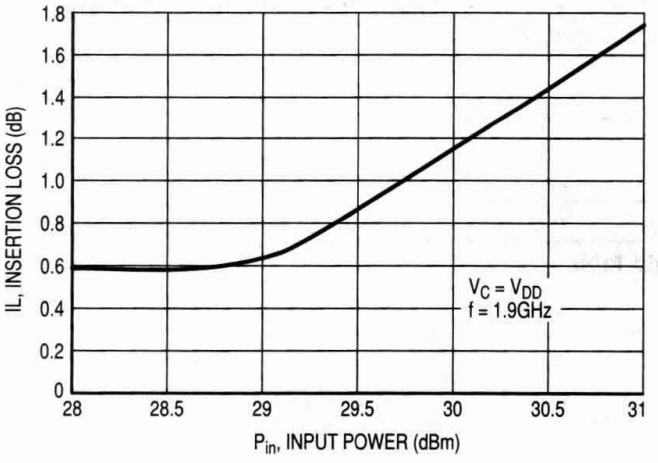


Figure 5. Antenna Switch Insertion Loss versus Input Power (Large Signal)

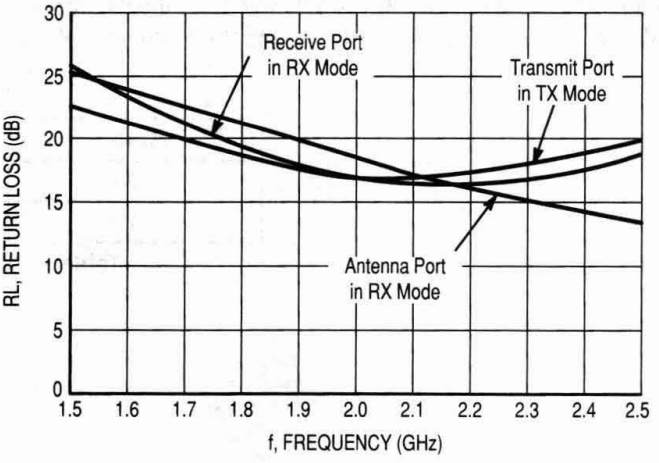
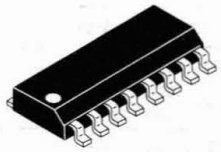


Figure 6. Return Loss

The MRFIC Line
1.8 GHz Upconverter

MRFIC1803

1.8 GHz UPMIXER, EXCITER AND LO AMP GaAs MONOLITHIC INTEGRATED CIRCUIT



CASE 751B-05 (SO–16)

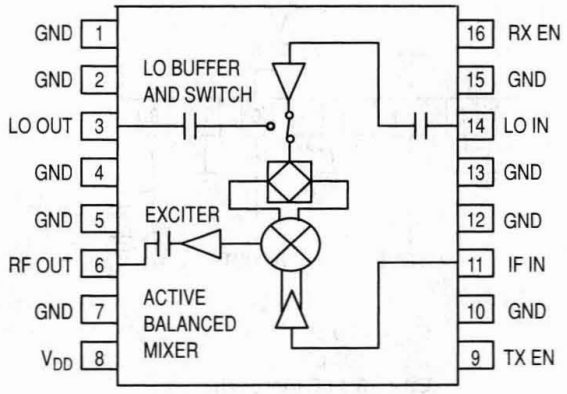
Designed primarily for use in DECT, Japan's Personal Handy System (PHS), and other wireless Personal Communication Systems (PCS) applications at 1.8 GHz, but also applicable to Industrial, Scientific and Medical (ISM) applications at 2.5 GHz. The MRFIC1803 is a complete active upmixer, exciter amplifier, and LO buffer amplifier in a low-cost SOIC-16 package. The low power consumption design includes a single balanced active mixer, CMOS compatible receive and transmit enable inputs, a buffer/exciter amplifier, and a buffered LO output capable of driving the MRFIC1804 downconverter. IF, LO and RF ports are matched to 50 Ω and no off-chip baluns are required. With both TX and RX enable pins low, the device is in standby mode and draws less than 0.3 mA.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- 10 dB IF to RF Conversion Gain
- Usable Frequency Range = 1.7 to 2.5 GHz
- Low Power Consumption = 80 mW (Typ)
- Single Bias Supply = 2.7 to 3.3 V
- No External Baluns Required
- IF, LO and RF Ports Matched to 50 Ω
- Low LO Power Requirement = –10 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1803R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1803

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	5.5	Vdc
IF Input Power	P_{IF}	3	dBm
LO Input Power	P_{LO}	3	dBm
Transmit and Receive Enable Voltage	TX EN, RX EN	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to + 85	°C



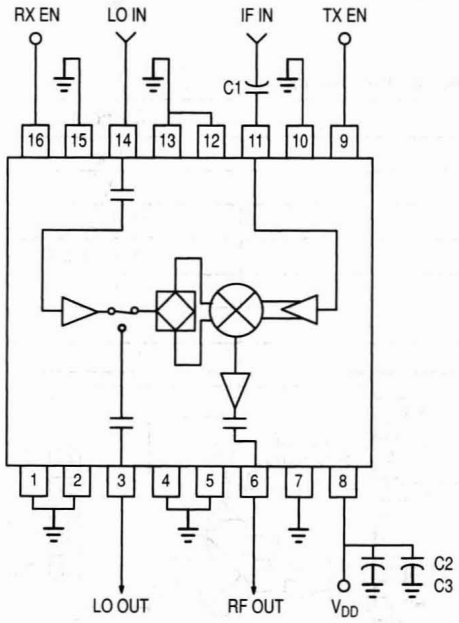
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
LO Input Frequency	f_{LO}	1.5 to 2.4	GHz
LO Input Power	P_{LO}	–10	dBm
IF Input Frequency	f_{IF}	70 to 350	MHz
RF Output Frequency	f_{RF}	1.7 to 2.5	GHz
Transmit and Receive Enable Voltage	TX EN, RX EN	2.7 to V_{DD}	Vdc
Supply Voltage	V_{DD}	2.7 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, LO = 1790 MHz @ –10 dBm, IF = 110 MHz @ –15 dBm, TX EN = 3.0 V, RX EN = 0 V, unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
IF to RF Conversion Gain	8	10	—	dB
RF Output 1 dB Compression	—	– 2	—	dBm
RF Output 3rd Order Intercept	—	9	—	dBm
LO Feed Through to RF Port	—	–19	—	dBm
Auxiliary LO Output Power (TX EN = 0 V, RX EN = 3 Vdc)	—	– 4	—	dBm
Supply Current, TX Mode	—	28	50	mA
Supply Current, RX Mode (TX EN = 0 V, RX EN = 3 Vdc)	—	3	—	mA
Standby Mode Current (TX EN = 0 V, RX EN = 0 Vdc)	—	0.1	0.3	mA



C1 470 pF
C2 100 pF
C3 0.1 µF (optional)

Figure 1. Applications Circuit Configuration

Typical Characteristics

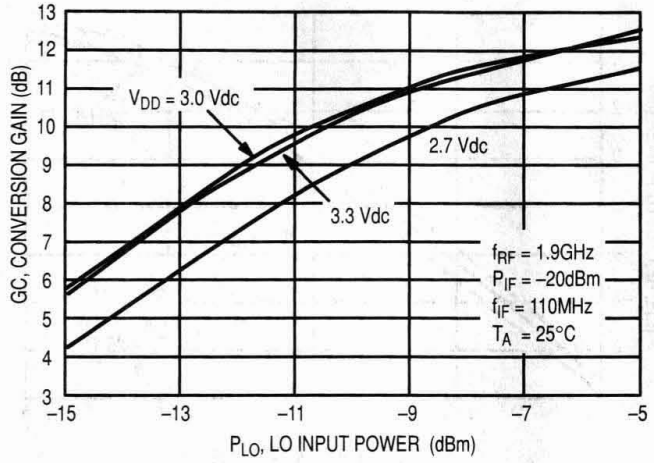


Figure 2. Conversion Gain versus LO Power

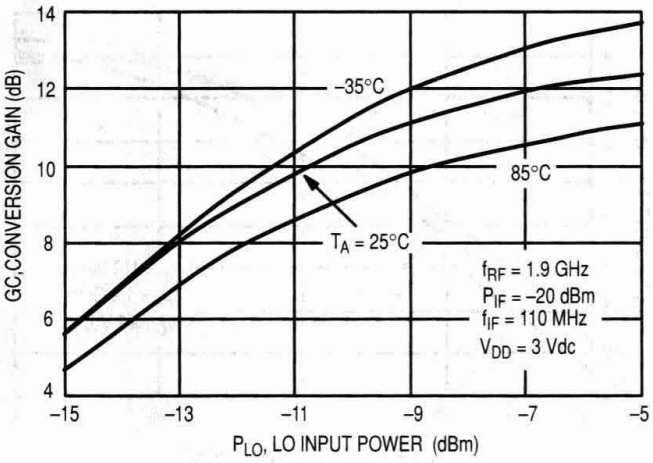


Figure 3. Conversion Gain versus LO Power

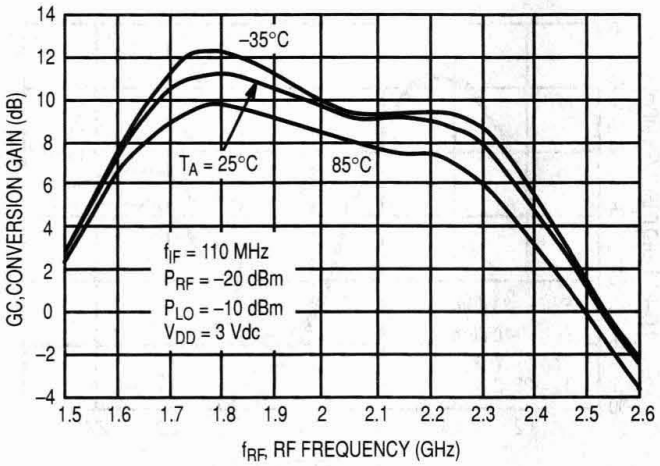


Figure 4. Conversion Gain versus RF Frequency

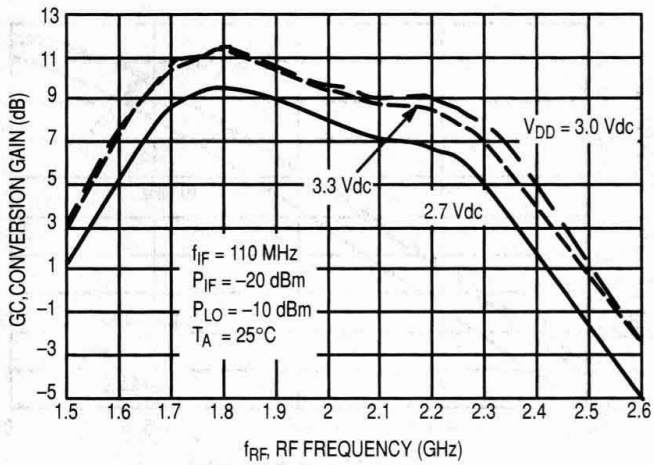


Figure 5. Conversion Gain versus RF Frequency

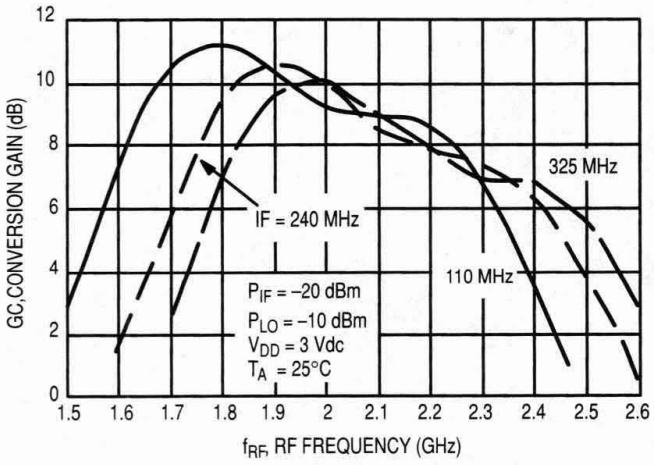


Figure 6. Conversion Gain versus RF Frequency

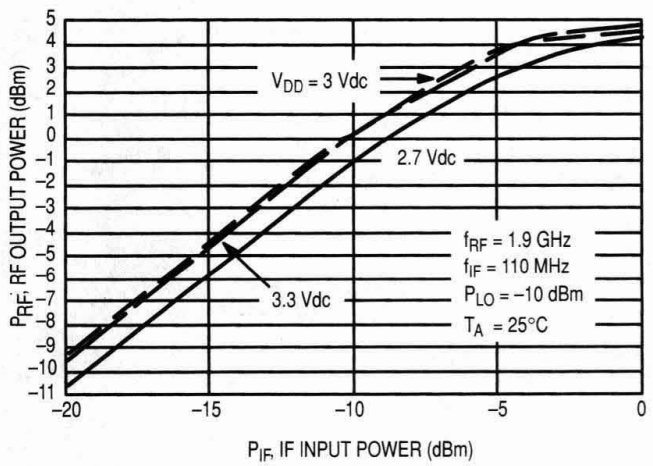


Figure 7. Output Power versus IF Input Power

Typical Characteristics

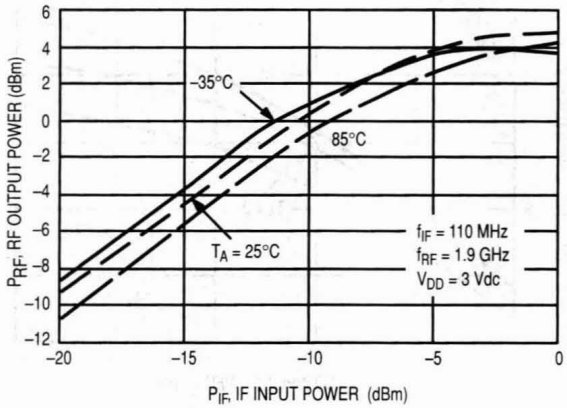


Figure 8. RF Output Power versus IF Input Power

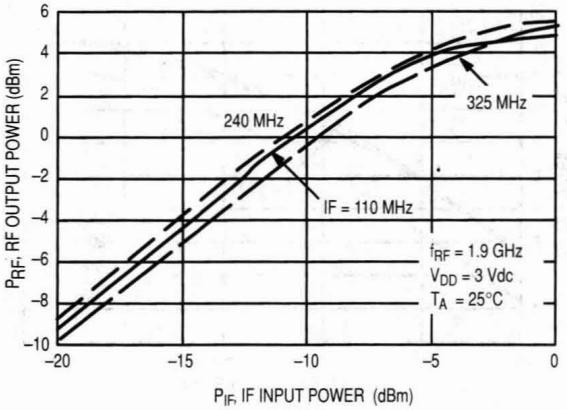


Figure 9. RF Output Power versus IF Input Power

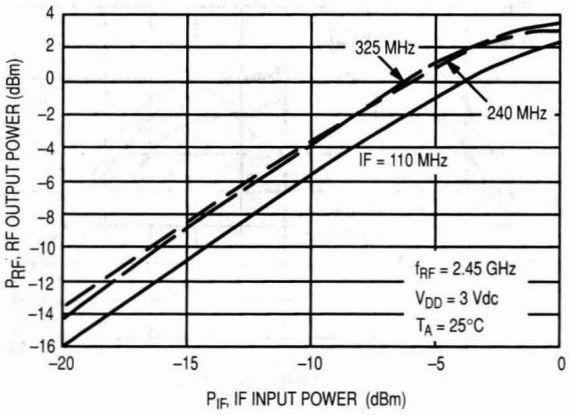


Figure 10. RF Output Power versus IF Input Power at 2.45 GHz

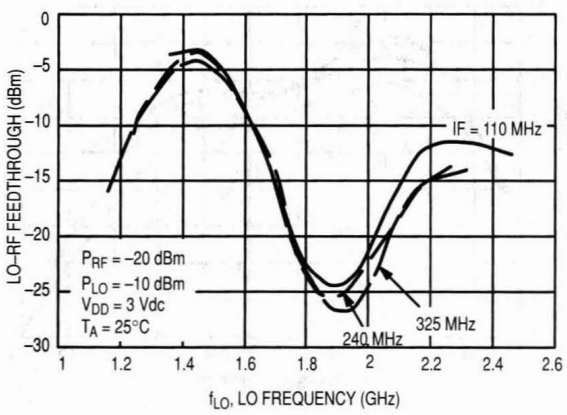


Figure 11. LO to RF Feedthrough versus LO Frequency

Frequency (MHz)	RF Output	LO Input	LO Output
1500	22.07 –j11.36	41.98 +j22.31	20.09 +j31.15
1550	21.74 –j4.69	50.60 +j9.80	26.39 +j40.79
1600	22.28 +j2.16	41.93 –j0.07	37.63 +j52.47
1650	24.01 +j8.25	32.74 +j3.32	56.16 +j63.47
1700	26.64 +J14.13	28.78 +j11.39	87.97 +j67.31
1750	30.83 +j20.11	28.98 +j21.04	131.33 +j40.34
1800	36.39 +j25.30	32.13 +j30.26	137.85 –j16.48
1850	43.92 +j29.26	37.68 +j40.38	103.88 –j50.81
1900	54.37 +j30.98	48.31 +j54.15	69.58 –j53.97
1950	65.34 +j28.57	68.80 +j70.87	50.13 –j46.24
2000	75.30 +j21.12	118.18 +j86.46	38.97 –j36.86
2050	81.19 +j8.43	220.83 +j17.19	32.08 –j27.58
2100	80.22 –j4.24	148.91 –j120.77	28.43 –j19.86
2150	74.20 –j14.00	58.50 –j105.11	26.56 –j12.82
2200	65.50 –j19.72	27.23 –j71.51	26.03 –j5.89
2250	57.40 –j21.38	17.22 –j50.26	26.73 –j0.03
2300	50.59 –j20.61	13.00 –j35.19	28.46 +j5.10
2350	44.53 –j18.16	10.95 –j22.96	30.88 +j9.86
2400	40.24 –j14.78	10.23 –j13.58	33.75 +j13.92
2450	37.73 –j10.54	10.20 –j5.32	37.50 +j17.32
2500	36.38 –j6.72	10.62 +j2.90	42.00 +j20.34

Table 1. Selected Device Impedances

DESIGN AND APPLICATIONS INFORMATION

The MRFIC1803 combines a single–balanced FET mixer with an LO pre–amp and an exciter amplifier to form a self–contained upconverter. The device is usable from RF frequencies of 1.7 to 2.5 GHz and at IF frequencies of 70 to 325 MHz. The design is optimized for low side injection in hetrodyne transmitter applications. In the upconversion process, modulation is imparted to an IF carrier which is converted to the RF transmit frequency by a mixer. By DC coupling the IF input, the device can be used for simple on–off keying (OOK) or bi–phase shift keying (BPSK) applications with no IF.

The MRFIC1803 design minimizes the need for off–chip components. An active balun is employed at the IF input and provides an excellent broadband 50Ω match over the full range of IF frequencies. The LO quadrature divider is passive and internal to the device. The LO buffer amplifier is equipped with a diversity switch which switches the amplified LO signal to the LO output pin during RECEIVE mode. The –5 dBm LO output is the appropriate level to drive the MRFIC1804 for 1.8 GHz applications or the MRFIC2401 for 2.4 GHz applications.

As shown in Figure 1, the device is easy to use with minimal off–chip components. More or less bypassing of the control and supply lines may be required depending on board layout and shielding. Careful layout of the RF frequency portions of the board is critical to successful implementation. Controlled impedance lines must be used and any off–chip components must be mounted as close to the IC as possible. The applications circuit was used to gather the information displayed in the typical characteristics curves. Since the MRFIC1803 design was optimized for the 1.7 to 1.9 GHz frequency range, improved performance can be had with some off–chip matching at frequencies outside this range. In particular, matching of the LO port will supply higher LO drive and improve conversion gain. At the RF output, either better gain or better 1dB compression can be had with external matching.

Filtering is generally required in the upconversion process to reduce image and LO radiation. To minimize pin count, this filtering is accomplished external to the device at the exciter output. For the frequency ranges of application, two and three pole ceramic surface filters are available at reasonable cost and with less than 2 dB of loss.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line
1.8 GHz LNA/Downmixer

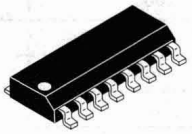
MRFIC1804

1.8 GHz LOW NOISE AMPLIFIER AND DOWNMIXER GaAs MONOLITHIC INTEGRATED CIRCUIT

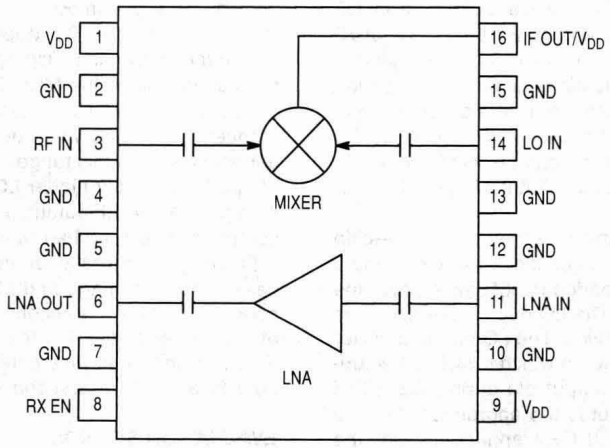
Designed primarily for use in DECT, Japan Personal Handy Phone (JPHP), and other wireless Personal Communication Systems (PCS) applications. The MRFIC1804 includes a low noise amplifier and downmixer in a low-cost SOIC-16 package. The integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility and efficiency. The mixer is optimized for low side injection and offers reasonable intercept point as well as high efficiency and 4 dB of conversion gain. Image filtering is implemented off-chip to allow maximum flexibility. With both TX and RX enable pins low, the device is in standby mode and draws less than 0.5 mA.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable Frequency Range = 1.5 to 2.2 GHz
- 14 dB Gain, 2.3 dB Noise Figure LNA
- 4 dB Gain, 13 dB Noise Figure Mixer
- 0.9 dB Mixer Input Intercept Point
- Simple LO/IF Off-Chip Matching for Maximum Flexibility
- Low Power Consumption = 24 mW (Typ)
- Single Bias Supply = 2.7 to 3.3 V
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1804R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1804



CASE 751B-05
(SO–16)



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

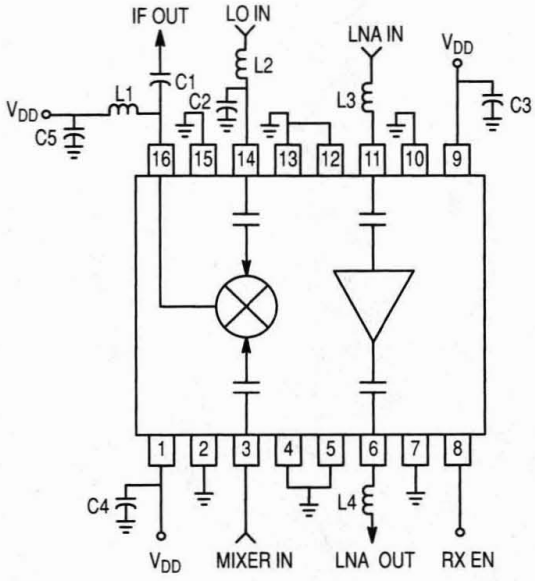
Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	5	Vdc
LNA Input Power (Standby Mode)	LNA_{in}	10	dBm
LO Input Power	P_{LO}	0	dBm
Receive Enable Voltage	RX EN	5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.8 to 1.925	GHz
Mixer LO Frequency	f_{LO}	1.5 to 1.9	GHz
IF Output Frequency	f_{IF}	70 to 325	MHz
Supply Voltage	V_{DD}	2.7 to 3.3	Vdc
Receive Enable Voltage	RX EN	2.7 to 3.3	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, LO = 1790 MHz @ – 5 dBm, RF = 1.9 GHz , RX EN = 3 V)

Characteristic	Min	Typ	Max	Unit
LNA Gain	—	14	—	dB
LNA Noise Figure	—	2.3	—	dB
LNA Input 3rd Order Intercept	—	–11	—	dBm
Mixer Conversion Gain (into 50 Ω)	—	4	—	dB
Mixer Noise Figure	—	13	—	dB
Mixer Input 3rd Order Intercept	—	0.9	—	dBm
Downconverter Gain (Less Image Filter Loss)	16	—	—	dB
Supply Current, RX Mode (RX EN = 3 V, LO_{off})	—	7	10	mA
Standby Mode Current (RX EN = 0 V, LO off)	—	—	0.5	mA



C1 12 pF (110 MHz) or 7.5 pF (240 MHz)
C2 0.8 pF
C3, C4 100 pF
C5 1000 pF
L1 82 nH (110 MHz) or 15 nH (240 MHz)
L2 8.2 nH
L3, L4 3.0 nH (Microstrip)

Figure 1. Applications Circuit Configuration (for 110 MHz and 240 MHz IF)

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.801	–64.71	5.65	–63.77	0.025	139.08	0.685	–62.55
1.6	0.741	–70.03	6.07	–80.96	0.033	128.21	0.622	–74.44
1.7	0.641	–73.54	6.63	–98.00	0.038	123.07	0.622	–83.36
1.8	0.559	–72.72	6.70	–113.87	0.047	113.17	0.560	–92.40
1.82	0.533	–71.10	6.58	–117.42	0.046	111.66	0.543	–93.20
1.84	0.512	–71.20	6.32	–120.25	0.046	109.36	0.530	–94.40
1.86	0.494	–69.93	5.92	–123.27	0.049	107.72	0.513	–95.19
1.88	0.478	–68.86	5.79	–126.51	0.052	106.52	0.498	–95.56
1.9	0.467	–67.50	5.88	–129.49	0.054	104.49	0.486	–96.35
1.92	0.452	–66.18	5.98	–132.33	0.055	103.55	0.476	–97.14
2.0	0.383	–57.10	5.57	–143.54	0.055	97.41	0.412	–96.10
2.1	0.326	–47.69	5.06	–155.69	0.058	92.26	0.344	–90.55
2.2	0.271	–35.10	4.61	–167.78	0.063	86.81	0.276	–83.89
2.3	0.205	–15.07	4.12	175.72	0.072	83.78	0.192	–63.78
2.4	0.708	–12.53	1.84	–155.83	0.073	45.03	0.406	–48.22
2.5	0.462	–34.07	3.18	–178.63	0.055	58.37	0.292	–66.60

Table 1. LNA S–Parameters

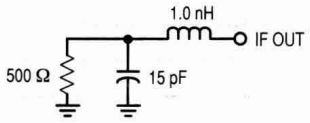


Figure 2. Equivalent IF Output Circuit

TYPICAL CHARACTERISTICS
(V_{DD} = 3 V)

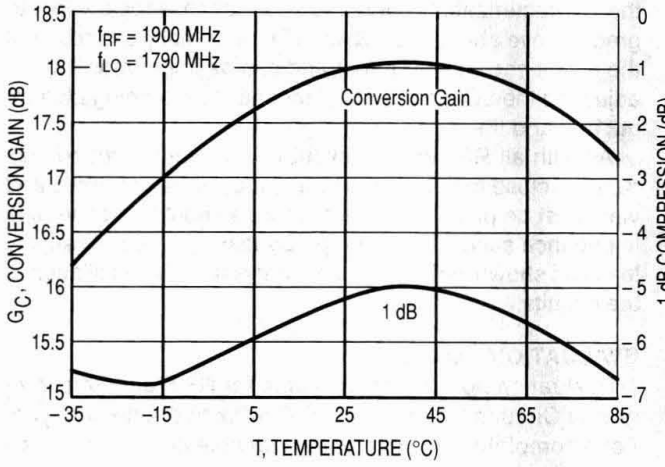


Figure 3. Downconverter Conversion Gain (less Image Filter) and 1 dB Compression versus Temperature

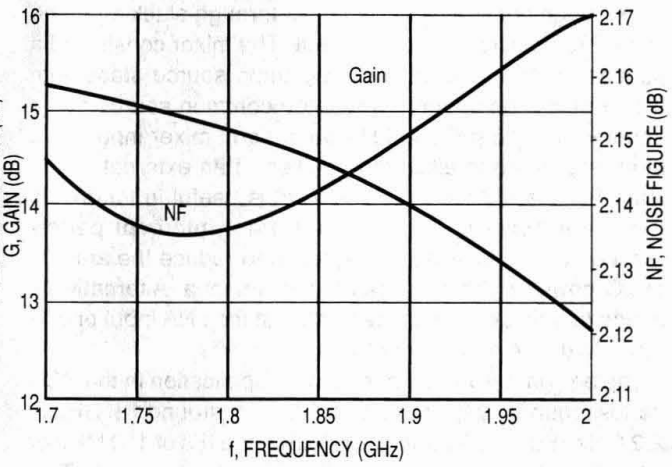


Figure 4. LNA Gain and Noise Figure versus Frequency

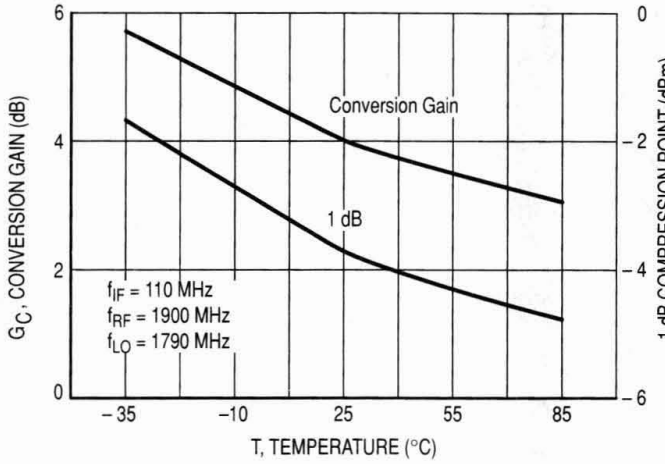


Figure 5. Mixer Conversion Gain and 1 dB Compression versus Temperature

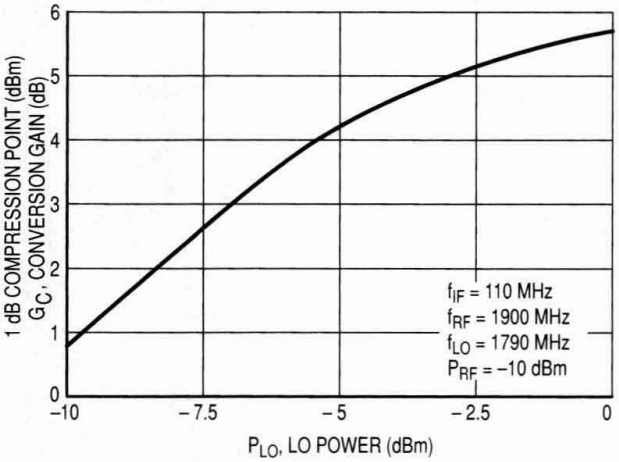


Figure 6. Mixer RF to IF Conversion Gain versus LO Power

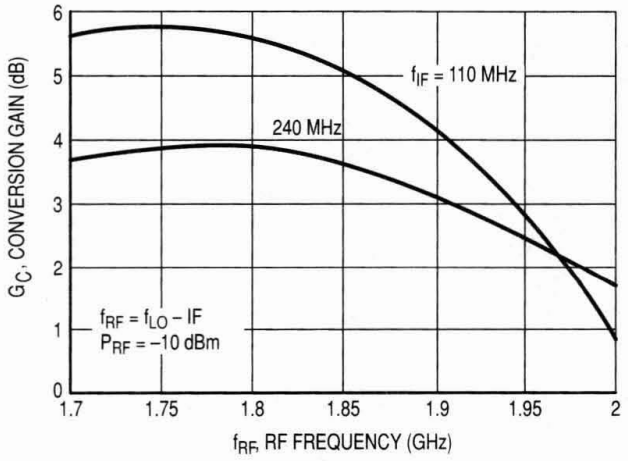


Figure 7. Mixer RF to IF Conversion Gain versus RF Frequency

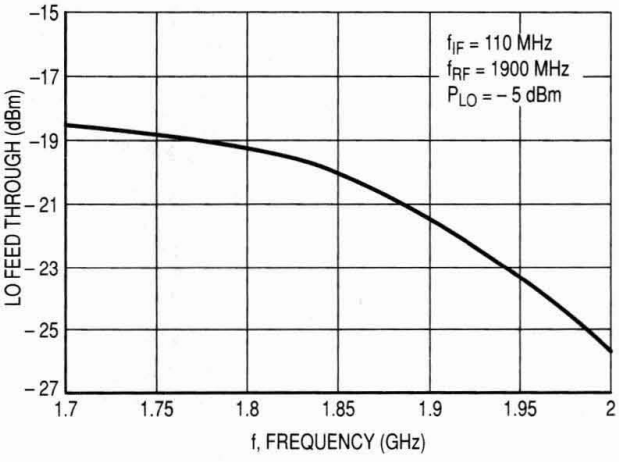


Figure 8. Mixer LO to IF Feed Through versus RF Frequency

DESIGN AND APPLICATIONS INFORMATION

The MRFIC1804 consists of a two–stage GaAs MESFET low noise amplifier and a single ended MESFET mixer. The LNA design conserves bias current through stacking of the two FETs, thus reusing the current. The mixer consists of a common gate stage driving a common source stage with the IF output being the drain of the common source stage shunted with 15 pF. The LNA output and mixer input have been separated to allow the addition of an external image filter. Such a filter, usually ceramic, is useful in improving the mixer noise figure and third order intercept performance. It also provides LO rejection to reduce the amount of LO power which may leak to the antenna. Alternatively, image trapping can be implemented at the LNA input or output with discrete or distributed components.

The design has been optimized for application in the PCS bands around 1.9 GHz but is usable from around 1.5 GHz to 2.2 GHz. For applications at 1.9 GHz and IFs of 110 MHz or 240 MHz, the circuit shown in Figure 1 can be used. This circuit was used to derive the characterization data shown in Figures 3 through 8. For other IF frequencies in the 100 MHz to 350 MHz range, use the IF equivalent circuit shown in Figure 2 for matching network design. As can be seen in the characterization curves, performance appears to degrade above about 1.85 GHz. This is partially a function of the circuit shown in Figure 1 and can be improved, first, by adjusting the LO input match, second, by matching LNA input and and the mixer input off chip.

As with all RF circuits, layout is important. Ground vias must be close to the component or lead to be grounded and vias must be plentiful. RF signal lines should be controlled impedance such as microstrip. Bypassing of power supply leads as shown in Figure 1 is essential to avoid oscillation of the circuits.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

1.9 GHz GaAs Power Amplifier

MRFIC1805

1.9 GHz
POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

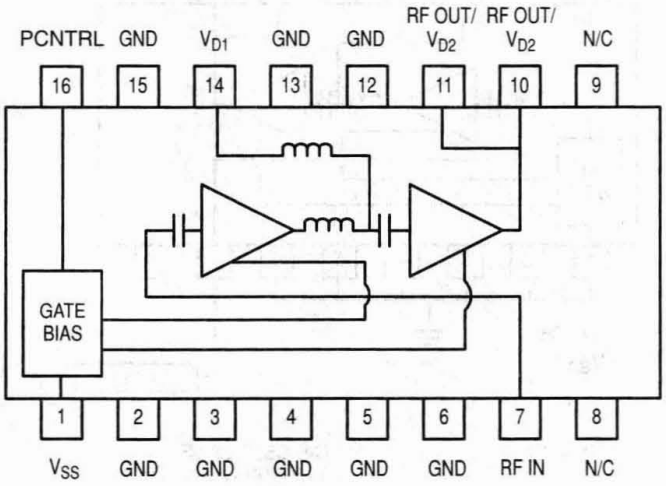
This two–stage class AB monolithic GaAs amplifier in a low–cost 16 lead plastic package is designed for output or driver applications in 1.9 GHz PCS handsets and basestations. The design is optimized for 3.0 Volt operation in systems such as Japan's PHS, Europe's DECT and the emerging North American PCS services. With modifications to the simple off–chip matching, the device can be used in other applications from 1.5 to 2.5 GHz.

- High Output Capability = 27 dBm Typical P_{sat}
  21.5 dBm Typical with PHS Format
- High Gain = 21 dB Typical Small Signal, 20 dB at P_{out} = 22 dBm
- Low Current Drain = 170 mA Typical with PHS Format
  250 mA Typical with DECT Format
- Low–Cost, Low Profile Plastic TSSOP Package
- Order MRFIC1805R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1805

CASE 948C–03
(TSSOP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{D1}, V_{D2}	6	Vdc
Supply Voltage	V_{SS}	–4	Vdc
RF Input Power	RF_{in}	+10	dBm
Drain Current	I_{DD}	500	mA
Thermal Resistance, Junction to Air	$R_{\theta JA}$	240	/W
Operating Junction Temperature	T_J	+175	°C
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



Pin Connections and Functional Block Diagram

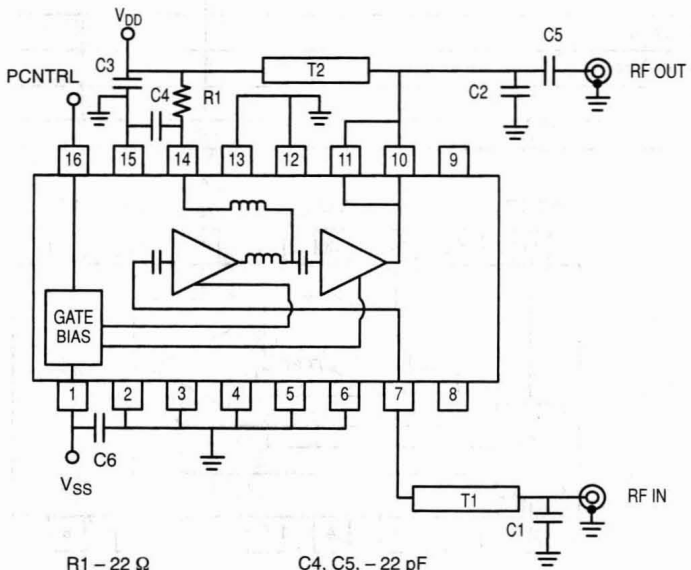
REV 1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{D1}, V_{D2}	2.7 to 5	Vdc
Supply Voltage	V_{SS}	–2.5	Vdc
PA Control Voltage	PCNTRL	0.0 to V_{DD}	Vdc
RF Input Power	P_{in}	–20 to +10	dBm
Operating Frequency Range	f_{OP}	1500 to 2200	MHz

ELECTRICAL CHARACTERISTICS ($V_{D1} = V_{D2} = 3$ Vdc, $V_{ss} = -2.5$ Vdc, $T_A = 25°C$, f = 1.9 GHz, P_{in} = +2 dBm, PCNTRL set for I_{DQ} = 125 mA, circuit configuration as shown in Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Output, Saturation	P_{SAT}	23	25	–	dBm
RF Output Power	P_{out}	20	21.5	–	dBm
Adjacent Channel Power Ratio (384 Kbps π/4 DQPSK Signal, 600 kHz Offset, P_{out} = 21 dBm	P_{ACP}	–	–58	–55	dBc
RF Output 1 dB Compression	P_{1dB}	22	24	–	dBm
2nd Harmonic Output	–	–	–40	–	dBc
3rd Harmonic Output	–	–	–40	–	dBc
Supply Current	I_{DD}	–	170	210	mA
Supply Current	I_{SS}	–	200	300	μA
Supply Current	I_{PCNTRL}	–	220	300	μA
Input Return Loss	–	–	13	–	dB
Reverse Isolation	–	–	31	–	dB
Output Third Intercept	–	–	34	–	dBm
Turn On Time	–	–	1	–	μs



R1 – 22 Ω
C1 – 1.2 pF
C2 – 2.2 pF
C3, C6 – 330 pF

C4, C5, – 22 pF
T1 – 100 Ω Line, 7 mm
T2 – 100 Ω Line, 20 mm
Board Material – 30 MIL FR4
Connectors – SMA Type

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

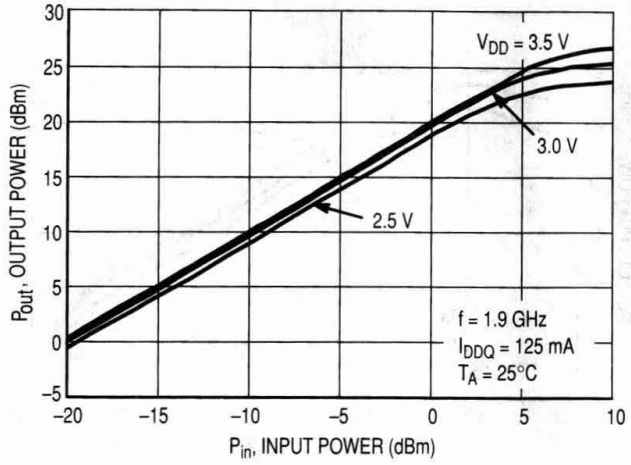


Figure 2. Output Power versus Input Power

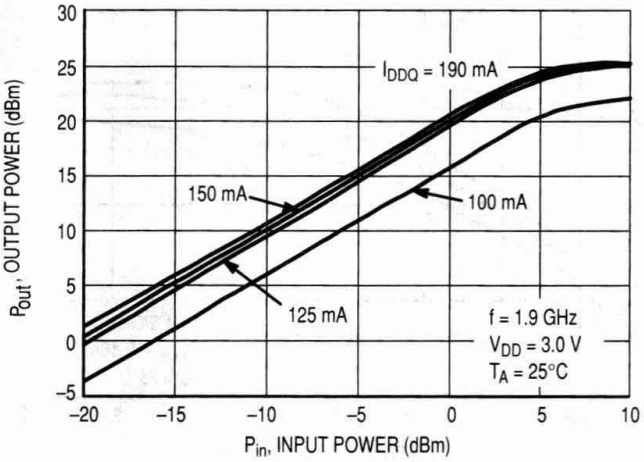


Figure 3. Output Power versus Input Power

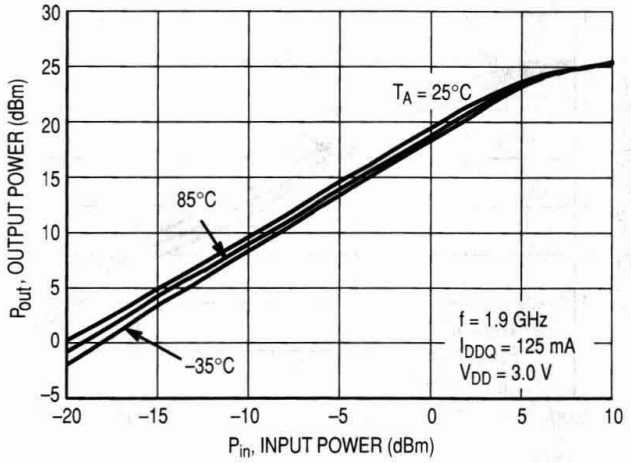


Figure 4. Output Power versus Input Power

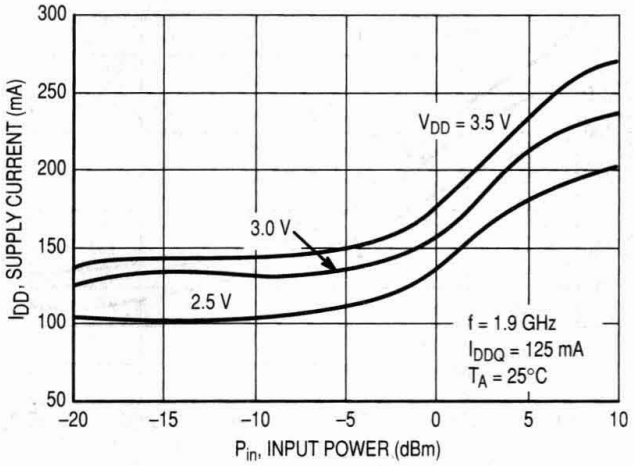


Figure 5. Supply Current versus Input Power

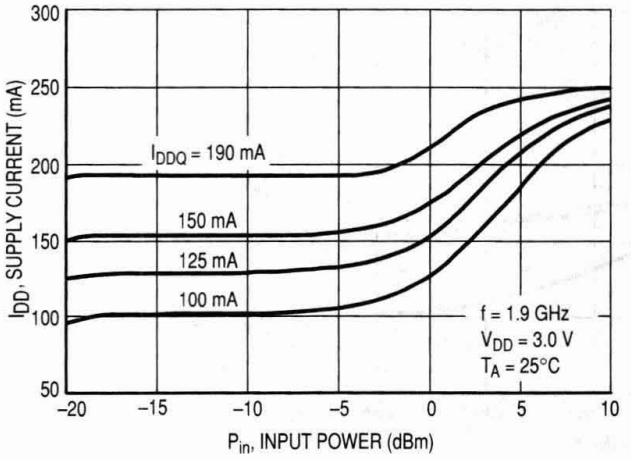


Figure 6. Supply Current versus Input Power

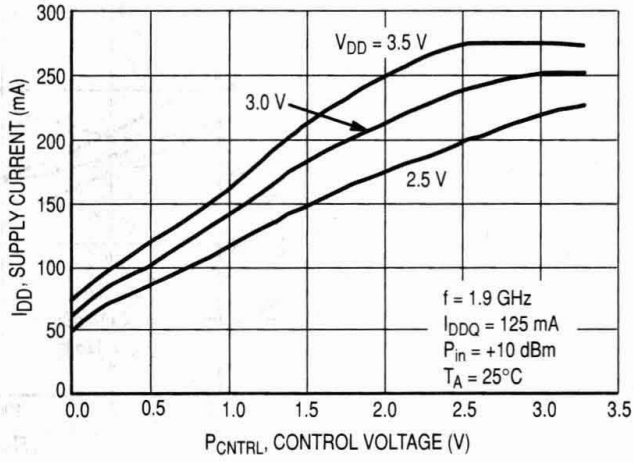


Figure 7. Supply Current versus Control Voltage

TYPICAL CHARACTERISTICS

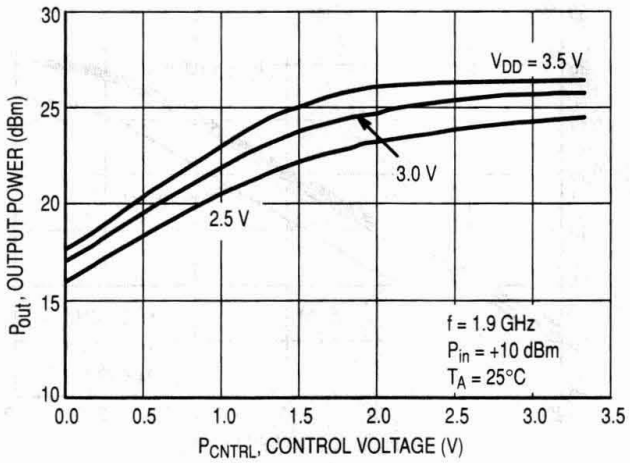


Figure 8. Output Power versus Control Voltage

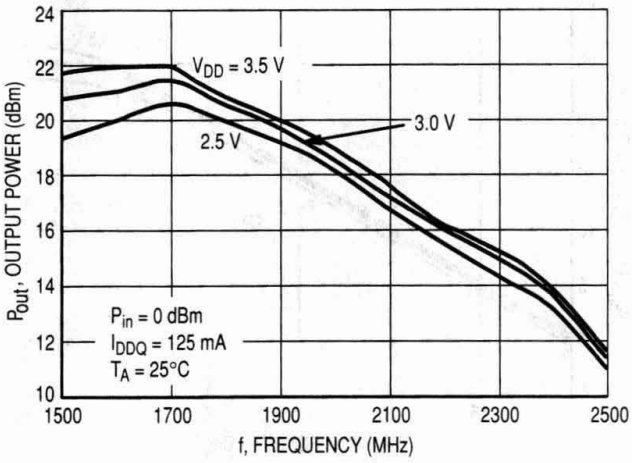


Figure 9. Output Power versus Frequency

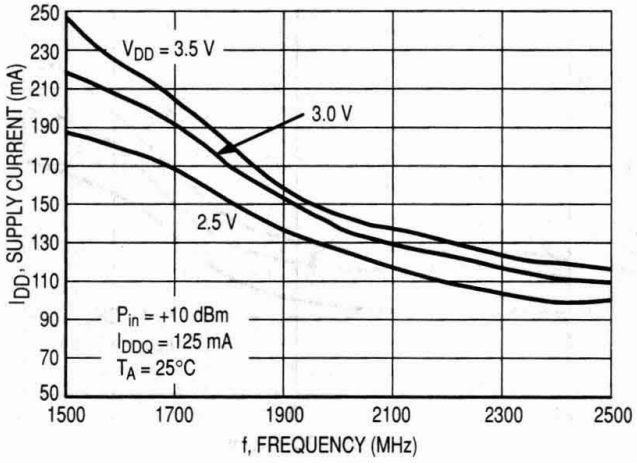


Figure 10. Supply Current versus Frequency

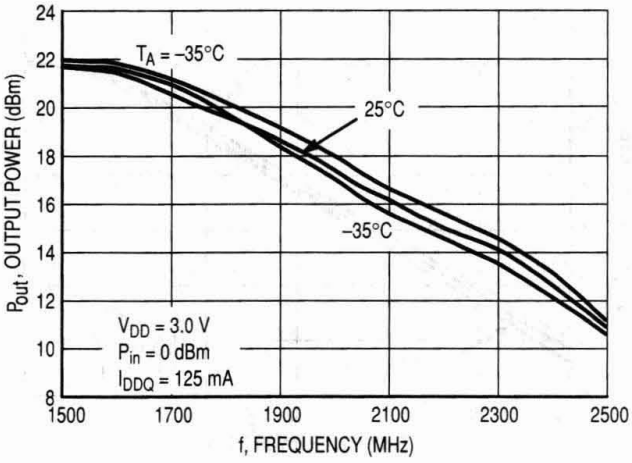


Figure 11. Output Power versus Freqency

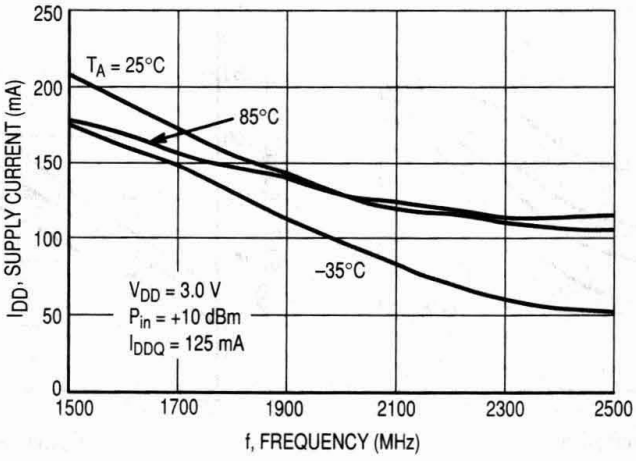


Figure 12. Supply Current versus Frequency

Table 1. Small Signal S–Parameters

(V_{D1} = V_{D2} = 3 Vdc, T_A = 25°C, f = 1.9 GHz, PCNTRL set for I_{DQ} = 125 mA, no matching circuit)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1.50	0.744	–76	10.99	–104	0.013	167	0.494	–177
1.55	0.697	–76	11.01	–114	0.014	164	0.520	179
1.60	0.662	–75	10.39	–124	0.015	163	0.533	174
1.65	0.645	–75	9.22	–132	0.015	160	0.528	170
1.70	0.636	–75	8.93	–135	0.016	157	0.522	167
1.75	0.623	–75	8.90	–141	0.017	157	0.515	164
1.80	0.617	–75	8.24	–148	0.018	158	0.506	161
1.85	0.612	–76	7.70	–152	0.018	155	0.497	159
1.90	0.602	–76	7.06	–158	0.019	154	0.489	156
1.95	0.599	–78	6.41	–160	0.019	154	0.481	154
2.00	0.590	–79	6.16	–160	0.021	154	0.475	152
2.05	0.581	–80	6.12	–165	0.022	152	0.469	150
2.10	0.570	–81	5.83	–170	0.022	150.	0.461	148
2.15	0.562	–83	5.57	–174	0.023	151.	0.458	146
2.20	0.548	–84	5.27	–178	0.024	152	0.455	144
2.25	0.538	–86	5.00	–179	0.025	152	0.450	142
2.30	0.527	–88	4.81	–179	0.027	151	0.448	141
2.35	0.512	–90	4.60	175	0.027	149	0.447	139
2.40	0.499	–92	4.43	171	0.027	146	0.447	137
2.45	0.485	–94	4.27	169	0.028	149	0.449	136
2.50	0.471	–97	4.00	163	0.030	150	0.449	134

Table 2. Small Signal S–Parameters

(V_{D1} = V_{D2} = 3 Vdc, T_A = 25°C, f = 1.9 GHz, PCNTRL set for I_{DQ} = 150 mA, no matching circuit)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1.50	0.752	–75	11.90	–104	0.012	169	0.480	–178
1.55	0.699	–75	11.90	–114	0.013	167	0.509	178
1.60	0.662	–75	11.19	–124	0.014	165	0.520	174
1.65	0.643	–74	9.94	–132	0.015	162	0.519	170
1.70	0.628	–74	9.60	–135	0.016	160	0.514	167
1.75	0.616	–74	9.55	–141	0.017	159	0.507	163
1.80	0.607	–74	8.81	–148	0.018	158	0.498	160
1.85	0.598	–75	8.23	–152	0.018	156	0.490	158
1.90	0.590	–75	7.54	–157	0.019	156	0.483	156
1.95	0.584	–77	6.82	–159	0.020	156	0.476	154
2.00	0.573	–78	6.55	–159	0.021	156	0.471	152
2.05	0.564	–79	6.50	–164	0.022	153	0.463	149
2.10	0.550	–81	6.17	–170	0.022	152	0.458	147
2.15	0.541	–82	5.88	–173	0.023	154	0.453	146
2.20	0.529	–84	5.56	–178	0.024	153	0.448	143
2.25	0.518	–86	5.26	–179	0.026	154	0.447	141
2.30	0.507	–88	5.04	–179	0.027	153	0.444	140
2.35	0.492	–90	4.82	176	0.028	150	0.443	138
2.40	0.481	–93	4.62	172	0.028	149	0.442	136
2.45	0.468	–95	4.45	170	0.028	152	0.444	135
2.50	0.454	–97	4.17	165	0.030	152	0.445	133

Table 3. Small Signal S–Parameters

(V_{D1} = V_{D2} = 3.3 Vdc, T_A = 25°C, f = 1.9 GHz, PCNTRL set for I_{DQ} = 125 mA, no matching circuit)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
1.50	0.764	–73	11.50	–104	0.013	169	0.492	–177
1.55	0.711	–74	11.49	–114	0.014	166	0.518	179
1.60	0.674	–73	10.82	–124	0.014	164	0.528	174
1.65	0.652	–73	9.60	–132	0.016	162	0.524	170
1.70	0.641	–73	9.27	–135	0.016	158	0.519	167
1.75	0.628	–73	9.24	–141	0.017	158	0.507	164
1.80	0.616	–73	8.54	–148	0.017	158	0.495	161
1.85	0.607	–74	7.99	–152	0.019	155	0.489	159
1.90	0.598	–75	7.33	–157	0.019	155	0.480	157
1.95	0.590	–76	6.63	–160	0.020	156	0.471	154
2.00	0.580	–77	6.35	–160	0.021	154	0.461	153
2.05	0.569	–79	6.30	–165	0.021	152	0.454	150
2.10	0.556	–80	5.98	–170	0.023	151	0.445	148
2.15	0.546	–82	5.70	–174	0.022	154	0.439	147
2.20	0.534	–84	5.39	–178	0.024	152	0.436	144
2.25	0.523	–86	5.11	–179	0.025	153	0.430	142
2.30	0.510	–88	4.90	–179	0.026	150	0.427	141
2.35	0.499	–90	4.70	175	0.027	149	0.424	139
2.40	0.486	–93	4.48	171	0.027	148	0.422	137
2.45	0.473	–95	4.31	169	0.027	150	0.422	135
2.50	0.463	–98	4.05	164	0.029	151	0.420	133

Table 4. Small Signal S–Parameters

(V_{D1} = V_{D2} = 3.3 Vdc, T_A = 25°C, f = 1.9 GHz, PCNTRL set for I_{DQ} = 150 mA, no matching circuit)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
1.50	0.756	–74	12.03	–105	0.012	168	0.483	–178
1.55	0.702	–75	12.02	–115	0.013	168	0.509	178
1.60	0.663	–74	11.33	–125	0.014	162	0.519	174
1.65	0.644	–73	10.03	–133	0.015	161	0.518	170
1.70	0.628	–73	9.69	–136	0.016	160	0.514	167
1.75	0.614	–73	9.62	–142	0.016	160	0.502	164
1.80	0.603	–74	8.88	–149	0.018	159	0.494	161
1.85	0.596	–74	8.30	–153	0.018	157	0.485	159
1.90	0.584	–75	7.59	–158	0.019	156	0.476	157
1.95	0.577	–76	6.87	–160	0.020	156	0.466	154
2.00	0.567	–77	6.58	–160	0.021	155	0.458	152
2.05	0.559	–79	6.50	–165	0.022	152	0.450	150
2.10	0.545	–80	6.17	–171	0.022	152	0.443	148
2.15	0.536	–82	5.87	–175	0.022	152	0.436	147
2.20	0.524	–84	5.54	–179	0.024	153	0.429	145
2.25	0.512	–86	5.25	–180	0.025	153	0.424	143
2.30	0.500	–88	5.03	180	0.026	152	0.422	141
2.35	0.486	–90	4.78	174	0.027	149	0.418	139
2.40	0.477	–93	4.58	170	0.027	149	0.414	137
2.45	0.462	–95	4.40	168	0.027	150	0.413	136
2.50	0.452	–98	4.13	163	0.029	151	0.412	134

The MRFIC Line
1.8 GHz PA Driver/Ramp

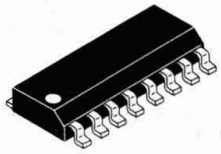
MRFIC1806

1.8 GHz DRIVER AMPLIFIER AND RAMP CIRCUIT GaAs MONOLITHIC INTEGRATED CIRCUIT

Designed primarily for use in DECT, Japan Personal Handy System (PHS), and other wireless Personal Communication Systems (PCS) applications. The MRFIC1806 includes a two stage driver amplifier and transmit waveform shaping circuitry in a low–cost SOIC–16 package. The amplifier portion employs depletion mode power GaAs MESFETs to produce +21 dBm output with 0 dBm input. The ramping circuit controls the burst–mode transmit rise and fall time and is adjustable through external components. This circuitry also places the amplifier in standby during TDMA receive mode. The MRFIC1806 is sized to drive the MRFIC1807 PA/Switch.

Together with the rest of the MRFIC1800 GaAs ICs, this family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable 1500–2500 MHz
- 23 dB Typical Gain
- +21 dBm Typical 1.0 dB Compression
- Simple Off–Chip Matching for Maximum Flexibility
- 3.0 to 5.0 Volt Supply
- Low Cost Surface Mount Plastic Package
- Order MRFIC1806R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1806



CASE 751B–05
(SO–16)

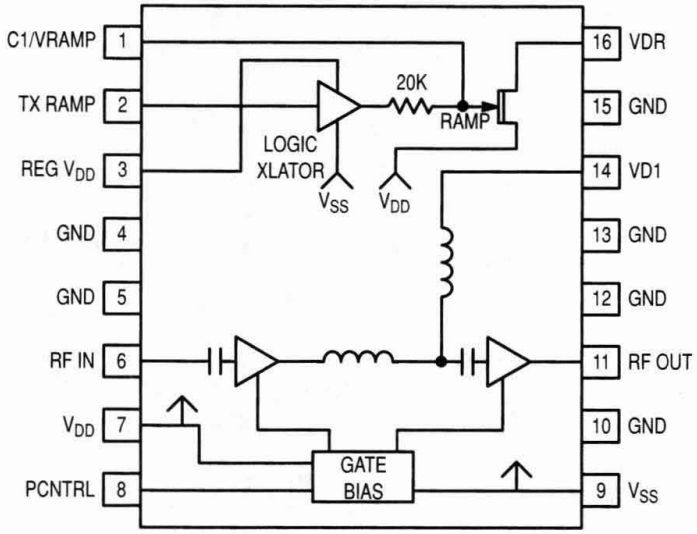


Figure 1. Pin Connections and Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Supply Voltage	V_{SS}	−4.0	Vdc
Supply Voltage	REG V_{DD}	4.5	Vdc
Bias Control Voltage	PCNTRL	3.0	Vdc
RF Input Power	P_{IN}	10	dBm
Ramp Circuit Input Voltage (High)	TX RAMP	6.0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Ambient Operating Temperature	T_A	−10 to +70	°C
Thermal Resistance, Junction to Case	θ_{JC}	100	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.5−2.5	GHz
Supply Voltage	V_{DD}	3.0 to 5.0	Vdc
Supply Voltage	V_{SS}	−2.75 to −2.25	Vdc
Supply Voltage	REG V_{DD}	2.9 to 3.1	Vdc
Bias Control Voltage	PCNTRL	0.5 to 1.5	Vdc
RF Input Power	P_{IN}	−20 to +5	dBm
Transmit Burst Enable Voltage (High)	TX RAMP	2.8 to 3.5	Vdc
Transmit Burst Enable Voltage (Low)	TX RAMP	−0.2 to +0.2	Vdc

ELECTRICAL CHARACTERISTICS

DECT Application with Internal Logic Translator (See Figure 2. V_{DD} = 3.5 V, REG V_{DD} = 3.0 V, T_A = 25°C, V_{SS} = −2.5 V, TX RAMP = 3.0 V, PCNTRL set for Quiescent I_{DD} = 120 mA, P_{IN} = −3.0 dBm @ 1.9 GHz unless otherwise stated.)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = −7.0 dBm)	21	23	—	dB
Input Return Loss	—	12	—	dB
Reverse Isolation	—	36	—	dB
Output Power	18	19.5	—	dBm
Harmonic Output	—	−36	—	dBc
Output Third Order Intercept	—	33	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.35	0.6	mA
Supply Current, I_{DD} (Pin 7)	—	115	135	mA
Supply Current, REG I_{DD} (Pin 3)	—	0.6	0.9	mA
Ramp Circuit Dynamic Range	40	44	—	dB

STANDBY MODE (TX RAMP = 0 V)

Characteristic	Min	Typ	Max	Unit
Output Power	—	−25	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.4	0.6	mA
Supply Current, REG I_{DD} (Pin 3)	—	0.25	0.4	mA

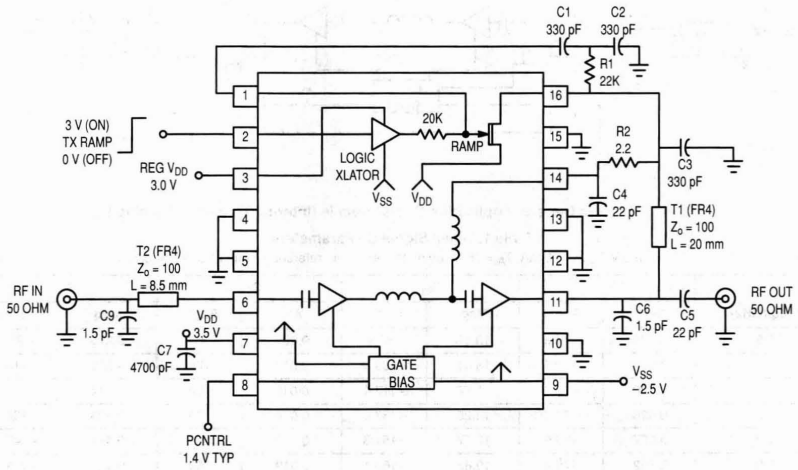


Figure 2. Applications Circuit Details for DECT using Internal Logic Translator

DESIGN AND APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC1806 is designed to drive the MRFIC1807 Power Amplifier and Transmit/Receive Switch IC in Personal Communications System (PCS) applications such as Europe's DECT and Japan's Personal Handy System (PHS). The design incorporates not only a two–stage GaAs MESFET driver/exciter amplifier, but also externally controllable bias and ramping circuitry. The IC is designed to drive the MRFIC1807 with about +19 dBm which will, in turn, produce +26 dBm output, suitable for DECT. To reduce chip size (and cost) and to allow for flexibility of application, the amplifier has limited on–chip matching. The ramp circuitry is used to shape the drain voltage to the FETs for Time Domain Multiple Access (TDMA) applications and is comprised of a depletion mode pass device driven by a logic translator. Attack and release times are controllable through the use of external components. The IC is configured such that all, part or none of the ramping circuitry can be used, depending on the application.

AMPLIFIER CIRCUIT APPLICATION

As can be seen in Figures 2 and 3, the off–chip matching is straight forward. At frequencies near 1.9 GHz, the input requires 4.7 nH in series and 1.5 pF in shunt. The 4.7 nH series inductance may be implemented with a high–impedance transmission line as shown. The output, being close to 25 Ω, requires only a shunt 1.5 pF capacitor. Drain voltage for stage 1 is supplied through pin 14 and for stage 2 through pin 11, the RF output. Pin 8, PCNTRL is used to set the quiescent bias point for both stages. While nominal I_{DDQ} is 120 mA, it can be set as high as 180 mA for better linearity circuits, board layout and grounding are important. All RF signal paths must be controlled impedance structures. RF chip components must be high quality. Bypassing capacitors must be close to the IC and to ground vias. Pins which are designated as ground connections must be as close as possible to ground vias.

RAMPING CIRCUIT OPTIONS

The on–chip ramp circuit can be used to control the amplifier attack and release time for DECT applications through the use of a few external components as shown in Figure 2. This ramping is required to control the burst signal rise and fall time to avoid adjacent channel interference. At the same time, system specifications require the transmitter to reach full power in a minimum time. For DECT, it has been shown that a rise time of not greater than 2 microseconds will produce acceptable adjacent channel performance. The system requires full power in not greater than 10 microseconds. A good compromise, and the timing implemented in Figure 2, is 7 microseconds.

The on–chip logic translator can be bypassed as shown in Figure 3 by applying a ramp voltage to Pin 1 through a 1.0 kΩ resistor. This configuration allows flexibility in ramping the amplifier. The regulated V_{DD} voltage is not required so current consumption can be reduced. −2.3 V at Pin 1 turns the pass transistor, and the amplifier, off while a positive voltage will turn the pass transistor on. For full on state it is recommended that V_{RAMP} be close to V_{DD}. V_{RAMP} can also be used to on–off key the amplifier for simple telemetry applications or as transmit/receive control.

ELECTRICAL CHARACTERISTICS

General Application without Internal Logic Translator (See Figure 3. V_{DD} = 3.5 V, REG V_{DD} (Pin 2) open, V_{SS} = −2.5 V, TX RAMP (Pin 2) grounded, V_{RAMP} = 3.0 V, PCNTRL set for Quiescent I_{DD} = 120 mA, P_{IN} = 0 dBm @ 1.9 GHz, T_A = 25°C unless otherwise stated.)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = −7.0 dBm)	21	23	—	dB
Output Power (P_{IN} = 0 dBm)	20	22	—	dBm
Output Power (P_{IN} = +4.0 dBm)	—	23	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.3	0.5	mA
Supply Current, I_{DD} (Pin 7)	—	130	145	mA

STANDBY MODE (V_{RAMP} = −2.4 V)

Characteristic	Min	Typ	Max	Unit
Output Power	—	−25	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.4	0.6	mA

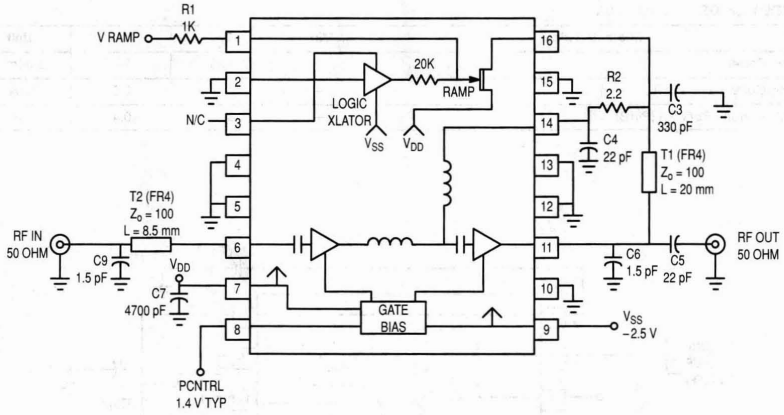


Figure 3. 1.9 GHz General Application Circuit Details (Internal Translator Disabled)

Table 1. Small Signal S−Parameters

(V_{DD} = 3.5 V, I_{DQ} = 120 mA, T_A = 25°C, no matching circuit, reference plane at pins 6 and 11.)

	S_{11}		S_{21}		S_{12}		S_{22}	
Freq (GHz)	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.734	−76.8	13.11	−87.9	0.009	−176	0.278	−98.9
1.6	0.654	−82.4	13.01	−109.4	0.012	178	0.326	−116.4
1.7	0.620	−72.6	11.17	−117.4	0.011	152	0.344	−109.8
1.8	0.636	−79.8	12.25	−137.0	0.014	170	0.423	−134.1
1.9	0.607	−80.6	10.77	−151.3	0.017	169	0.421	−147.7
2.0	0.592	−79.4	10.88	−165.1	0.019	163	0.427	−161.8
2.1	0.581	−79.4	9.64	−174.9	0.024	163	0.432	−172.3
2.2	0.571	−78.9	9.30	174.1	0.026	158	0.429	178.8
2.3	0.560	−79.1	7.95	166.9	0.029	157	0.432	171.1
2.4	0.541	−79.8	7.80	155.7	0.033	153	0.442	164.6
2.5	0.521	−80.1	6.90	147.2	0.042	154	0.445	161.7

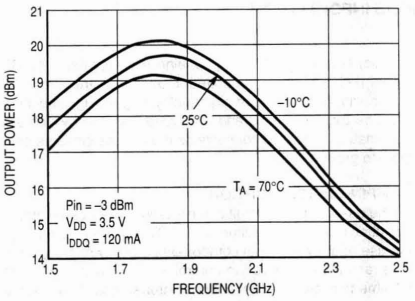


Figure 4. Output Power versus Frequency With Internal Logic Translator

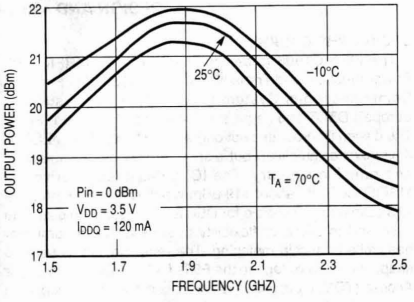
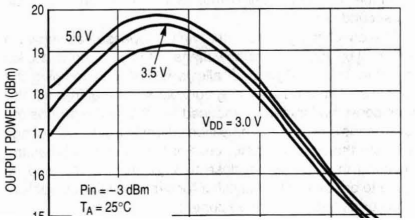
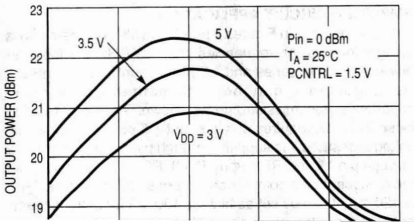


Figure 5. Output Power versus Frequency Without Internal Logic Translator





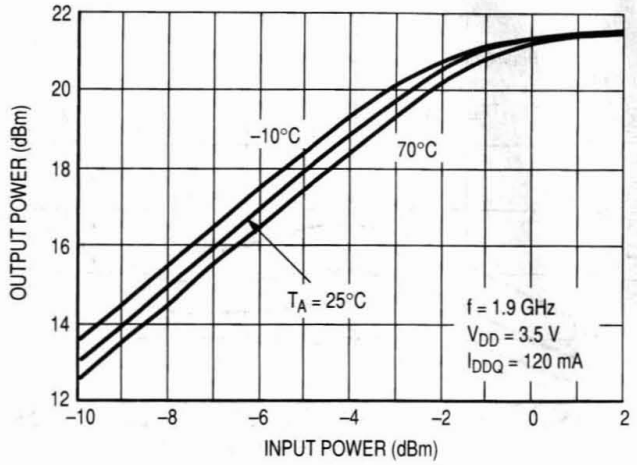


Figure 10. Output Power versus Input Power With Internal Logic Translator

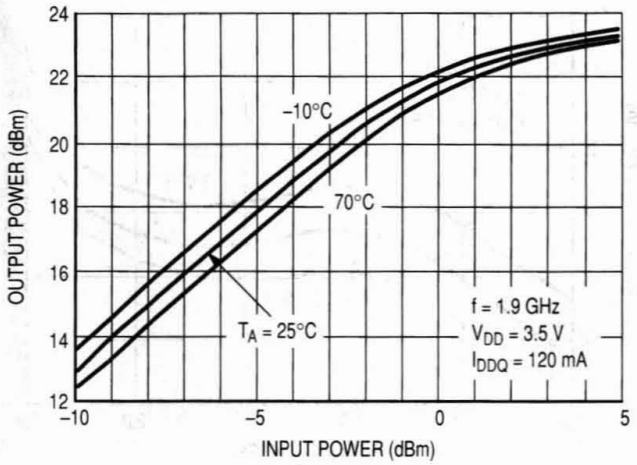


Figure 11. Output Power versus Input Power Without Internal Logic Translator

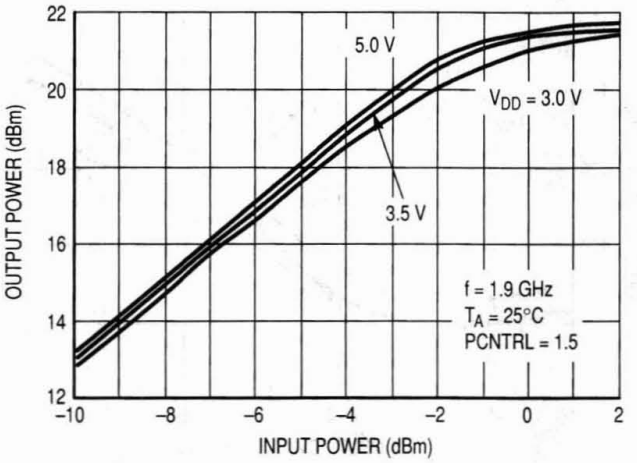


Figure 12. Output Power versus Input Power With Internal Logic Translator

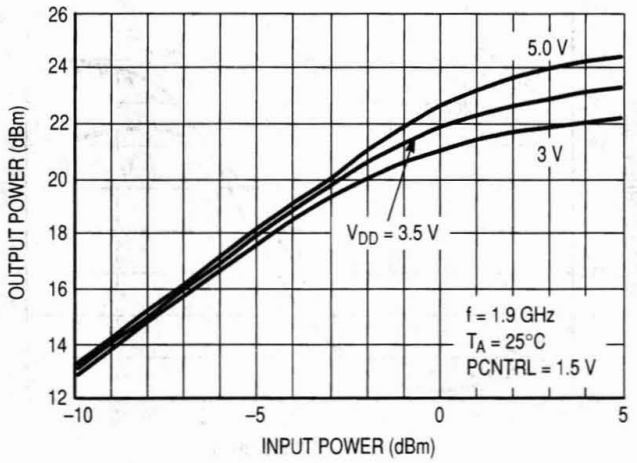


Figure 13. Output Power versus Input Power Without Internal Logic Translator

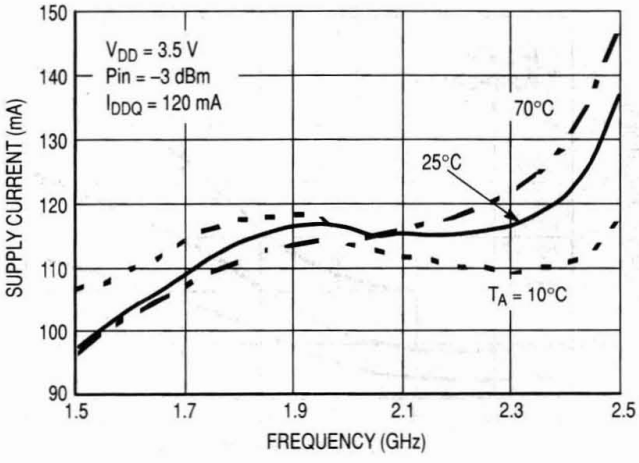


Figure 14. Supply Current versus Frequency With Internal Logic Translator

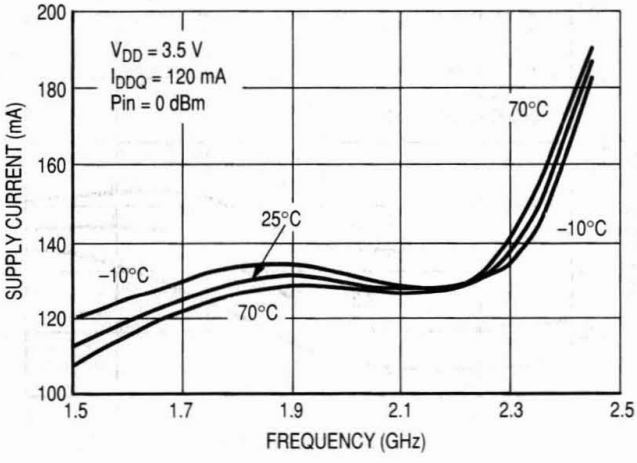


Figure 15. Supply Current versus Frequency Without Internal Logic Translator

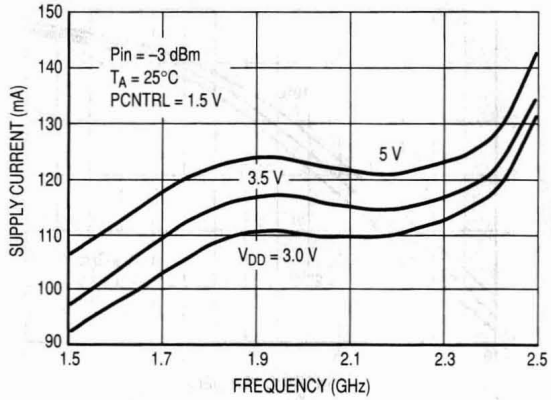


Figure 16. Supply Current versus Frequency With Internal Logic Translator

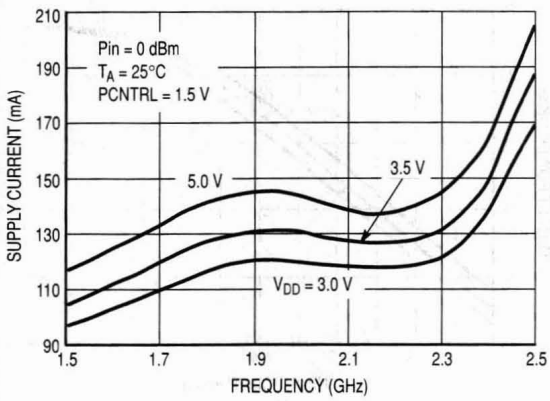


Figure 17. Supply Current versus Frequency Without Internal Logic Translator

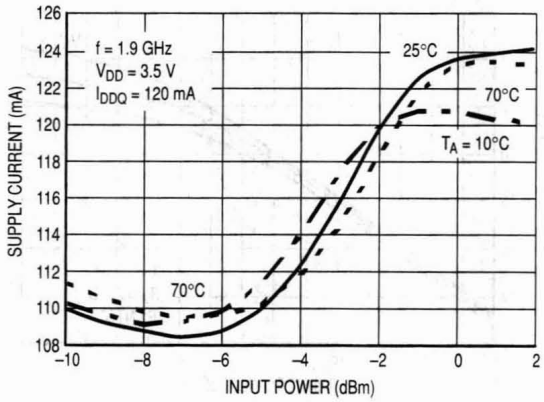


Figure 18. Supply Current versus Input Power With Internal Translator

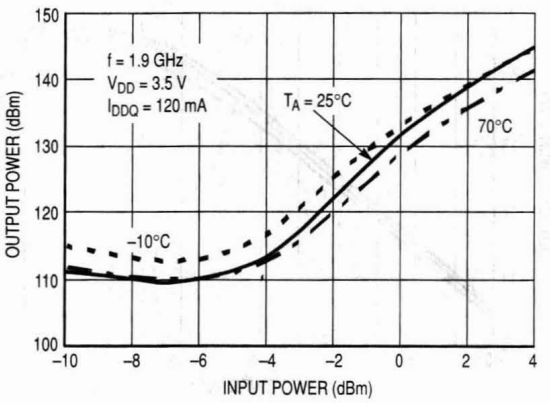


Figure 19. Supply Current versus Input Power Without Internal Translator

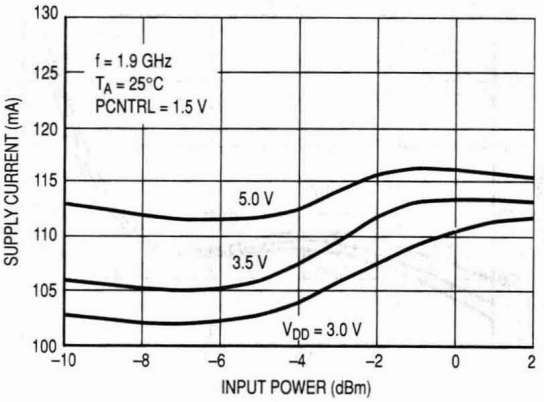


Figure 20. Supply Current versus Input Power With Internal Translator

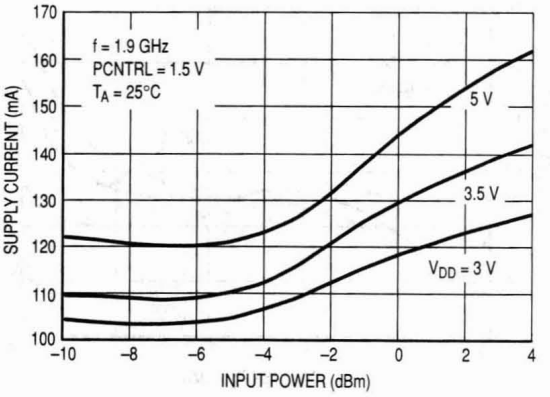


Figure 21. Supply Current versus Input Power Without Internal Logic Translator

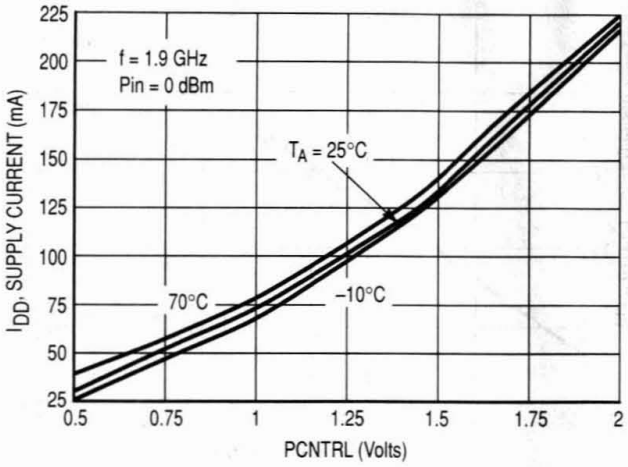


Figure 22. Supply Current versus PCNTRL Without Internal Logic Translator

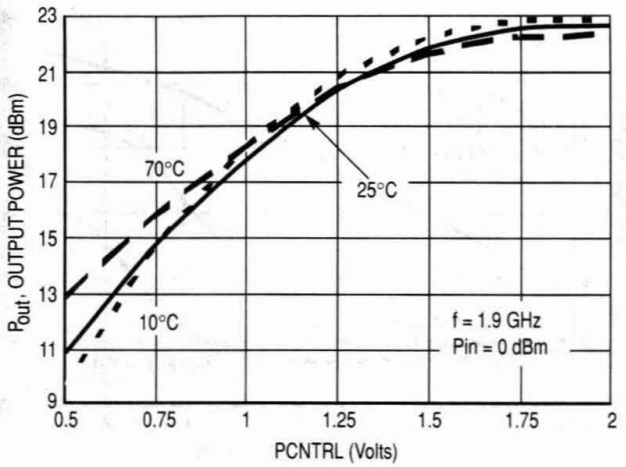


Figure 23. P_{out} versus PCNTRL Without Internal Logic Translator

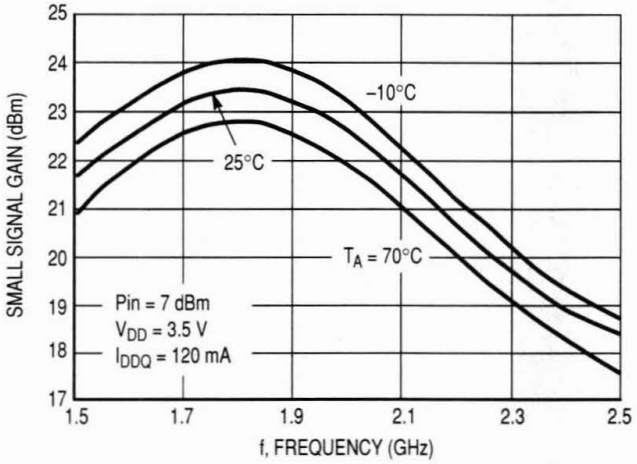


Figure 24. Small Signal Gain versus Frequency With Internal Logic Translator

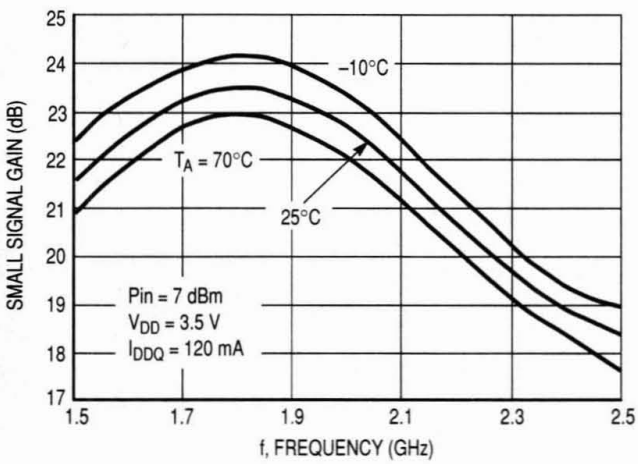


Figure 25. Small signal Gain versus Frequency Without Internal Logic Translator

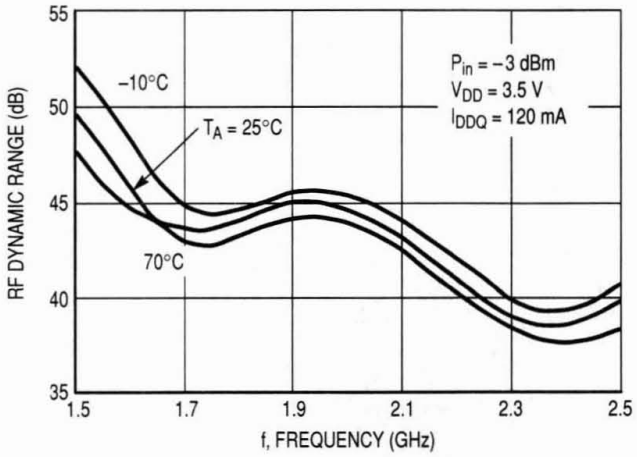


Figure 26. Dynamic Range versus Frequency With Internal Logic Translator

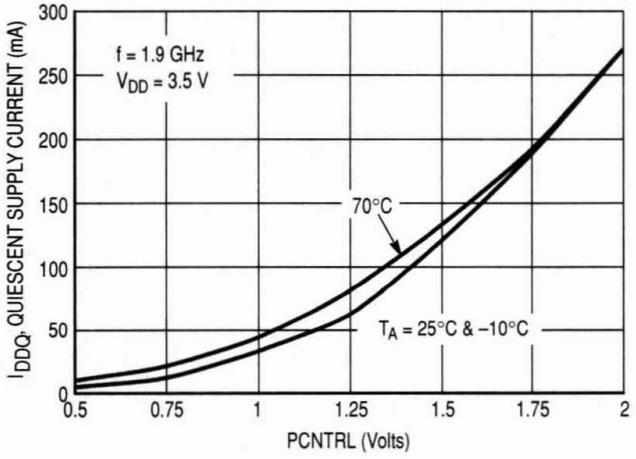


Figure 27. Quiescent Supply Current versus PCNTRL With Internal Logic Translator

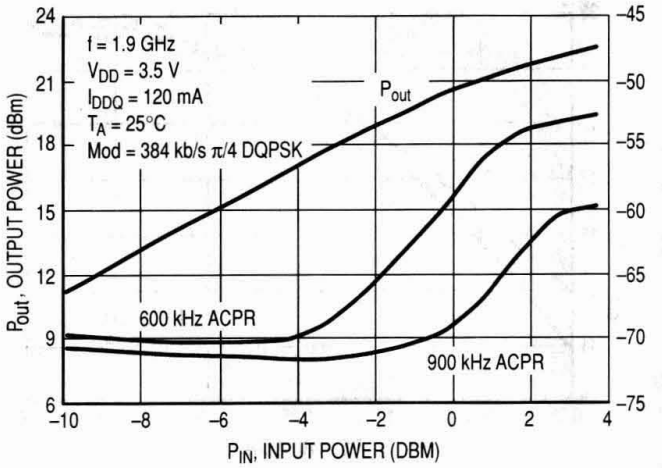


Figure 28. Output Power and Adjacent Channel Power Ratio versus Input Power Without Internal Logic Translator

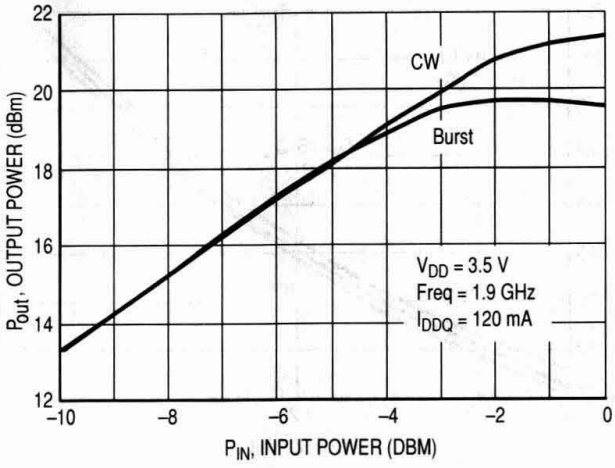
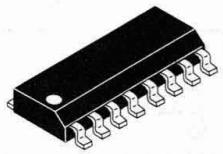


Figure 29. Continuous and Burst Mode Output Power versus Input Power With Internal Logic Translator

MRFIC1807

The MRFIC Line
1.8 GHz Power Amp/Switch

1.8 GHz POWER AMPLIFIER AND TRANSMIT/RECEIVE SWITCH GaAs MONOLITHIC INTEGRATED CIRCUIT



CASE 751B–05 (SO–16)

Designed primarily for use in DECT, Japan Personal Handy System (PHS) and other wireless Personal Communication Systems (PCS) applications. The MRFIC1807 includes a single–stage power amplifier and transmit/receive switch in a low–cost SOIC–16 package. The amplifier portion employs a depletion mode power GaAs MESFET and produces up to +27 dBm output with +19 dBm input. On–chip power control circuitry allows bias adjustment for optimum performance. The T/R switch is capable of handling up to +28 dBm through the transmit path without significant increase in insertion loss. The switch is controlled by CMOS logic level signals — no negative control voltage required. The MRFIC1807 is sized to be driven by the MRFIC1806 Driver/ Ramp IC.

Together with the rest of the MRFIC1800 GaAs ICs, this family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable 1500–2200 MHz
- 8.0 dB Gain Including Switch
- +26 dBm Minimum Output Power at Antenna Port
- 1.0 dB Typ RX Path Insertion Loss
- Simple Off–Chip Matching for Maximum Flexibility
- 3.0 to 5.0 V Supply
- No Spurious Outputs for Load VSWR up to 8:1
- CMOS Level Switching Signal for T/R Switch
- Order MRFIC1807R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1807

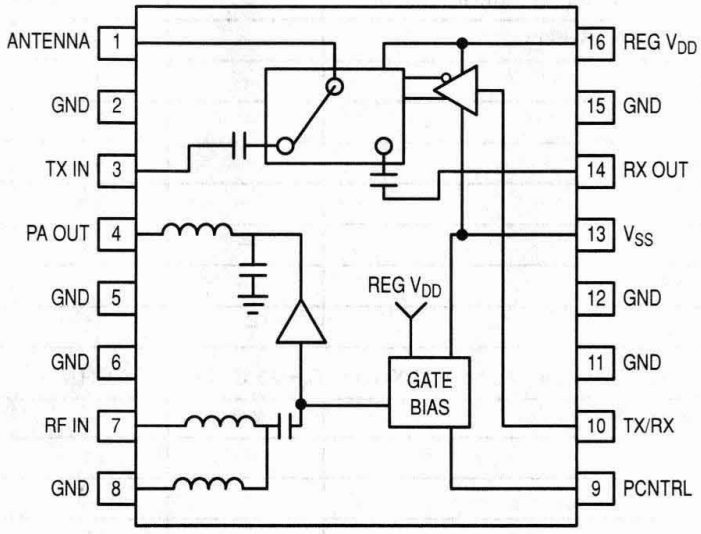


Figure 1. Pin Connection and Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise noted)

Rating	Symbol	Limit	Unit
PA Supply Voltage	V_{DD}	6.0	Vdc
Supply Voltage	REG V_{DD}	4.5	Vdc
Supply Voltage	V_{SS}	−4.0	Vdc
RF Input Power	P_{in}	+25	dBm
Switch Control Voltage	TX/RX	6.0	Vdc
PA Control Voltage	PCNTRL	3.0	Vdc
Ambient Operating Temperature	T_A	−10 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	24	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.5 to 2.2	GHz
PA Supply Voltage	V_{DD}	3.0 to 5.0	Vdc
Supply Voltage	REG V_{DD}	2.9 to 3.1	Vdc
Supply Voltage	V_{SS}	−2.75 to −2.25	Vdc
RF Input Power	P_{IN}	+5.0 to +23	dBm
Switch Control Voltage, High (TX Mode)	TX/RX	2.8 to 3.5	Vdc
Switch Control Voltage, Low (RX Mode)	TX/RX	−0.2 to 0.2	Vdc
PA Control Voltage	PCNTRL	0.0 to 2.5	Vdc

ELECTRICAL CHARACTERISTICS (1)

Transmit Mode (V_{DD} = 3.5 V, REG V_{DD} = 3.0 V, T_A = 25°C, V_{SS} = −2.5 V, PCNTRL 0 V to 2.5 V, P_{IN} = 20 dBm @ 1.9 GHz, TX/RX = 3 V, P_{OUT} Measured at ANT Port)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = 0 dBm, PCNTRL set for I_{DDQ} = 180 mA)	7.0	8.0	—	dB
Output Power (PCNTRL adjusted for efficiency ≥ 35%)	26	26.8	—	dBm
Output 1.0 dB Compression (PCNTRL set for I_{DDQ} = 180 mA)	—	25	—	dBm
Harmonic Output (PCNTRL set for P_{OUT} = 26 dBm)	—	−40	—	dBc
Switch RX to TX Switching Time	—	0.1	—	μsec
TX/RX Control Input Current, Pin 10	—	0.2	—	mA
Drain Efficiency (P_{out} = 26 dBm) (2)	—	40	—	%
Supply Current, I_{SS}	—	0.8	1.2	mA
Supply Current, REG I_{DD}	—	0.8	1.2	mA
PCNTRL Control Input Current (Pin 9)	—	15	—	μA
Leakage Power at RX Port	—	−1	+ 6	dBm

Receive Mode (V_{DD} = 0 V, REG V_{DD} = 3.0 V, V_{SS} = −2.5 V, TX/RX = 0 V, T_A = 25°C, Freq = 1.9 GHz)

Characteristic	Min	Typ	Max	Unit
ANT to RX Insertion Loss	—	1.0	1.3	dB
Switch TX to RX Switching Time	—	1.0	—	μsec
Supply Current, REG I_{DD}	—	60	250	μA
Supply Current, I_{SS}	—	60	250	μA

NOTES:
1. Measured with circuit configuration shown in Figure 2.
2. Includes switch loss.

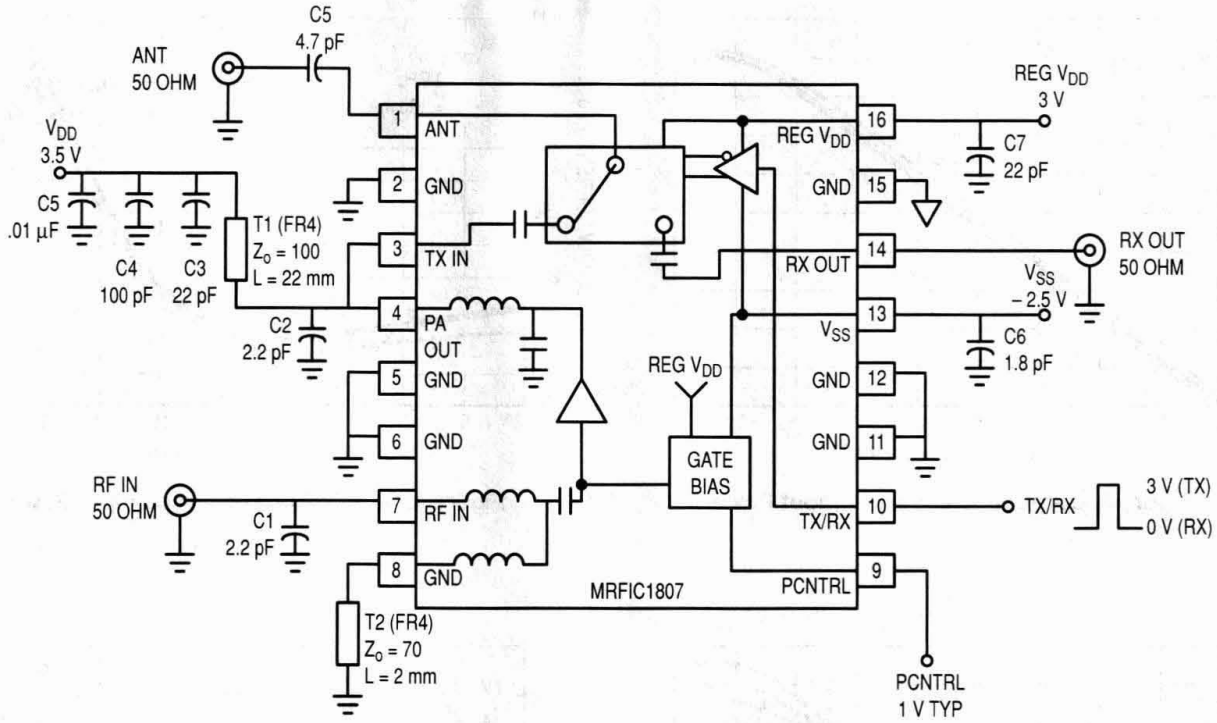


Figure 2. 1.9 GHz Applications Circuit Configuration

Table 1. Small Signal S–Parameters

(V_{DD} = 3.5 V, I_{DDQ} = 180 mA, T_A = 25°C, no input or output matching)

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.614	–171.5	2.203	82.6	0.104	74.5	0.741	175.4
1.6	0.695	175.7	1.871	71.7	0.110	69.2	0.746	171.5
1.7	0.747	167.3	1.647	63.4	0.108	64.0	0.745	167.4
1.8	0.777	160.3	1.473	56.2	0.106	58.7	0.746	163.0
1.9	0.799	154.2	1.341	49.2	0.120	54.0	0.753	158.9
2.0	0.814	148.3	1.230	43.0	0.118	49.6	0.758	154.8
2.1	0.826	142.5	1.128	36.8	0.114	45.2	0.764	150.6
2.2	0.835	137.0	1.041	31.2	0.120	40.6	0.767	146.7
2.3	0.842	131.4	0.959	26.4	0.127	37.0	0.780	143.4
2.4	0.856	126.6	0.895	21.1	0.124	33.8	0.796	139.8
2.5	0.870	121.7	0.840	16.0	0.126	30.4	0.808	136.4

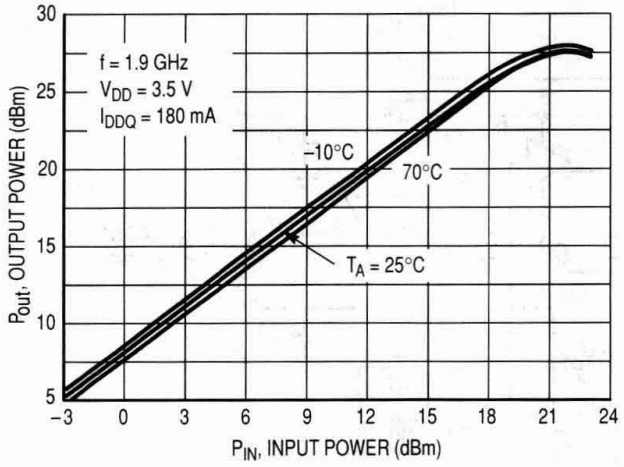


Figure 3. Output Power versus Input Power

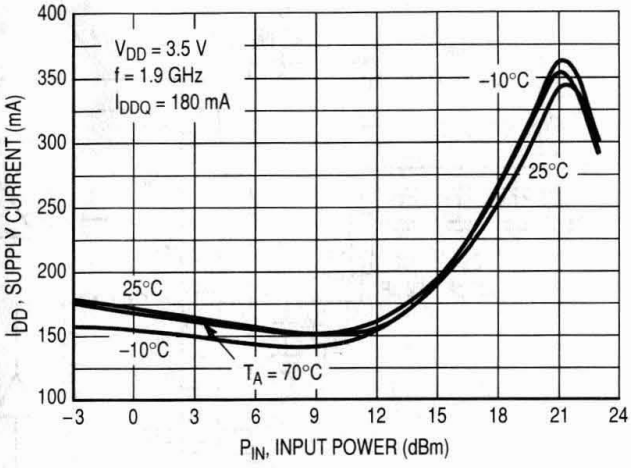


Figure 4. Supply Current versus Input Power

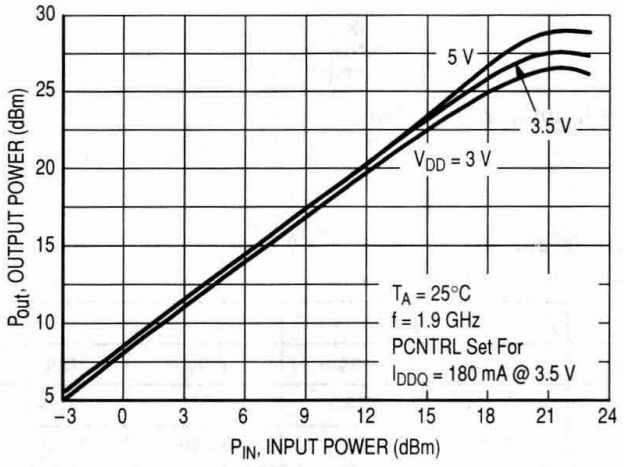


Figure 5. Output Power versus Input Power

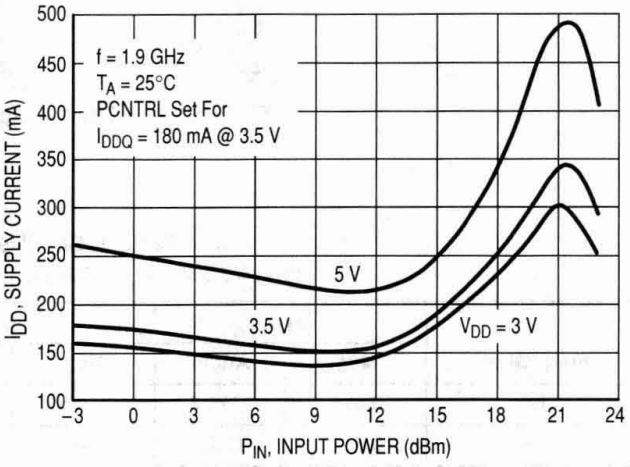


Figure 6. Supply Current versus Input Power

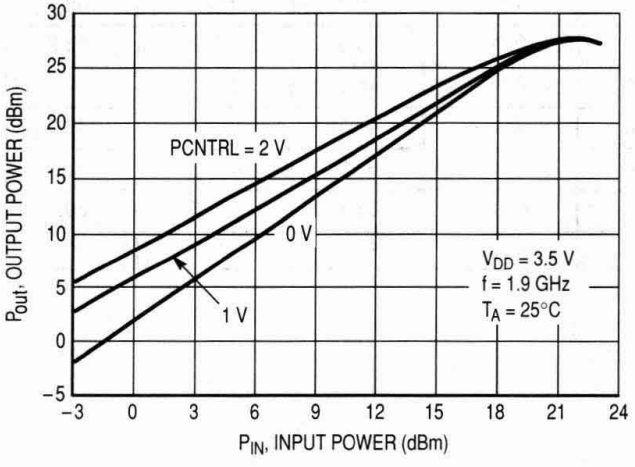


Figure 7. Output Power versus Input Power

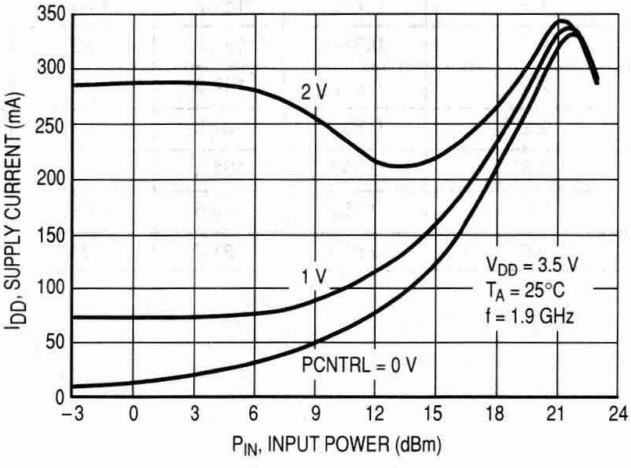


Figure 8. Supply Current versus Input Power

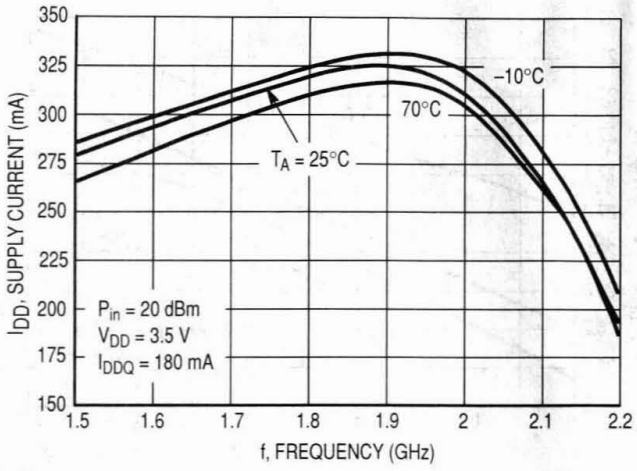


Figure 9. Supply Current versus Frequency

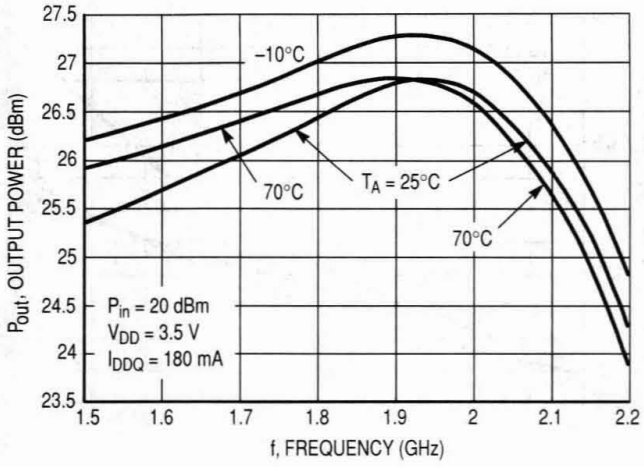


Figure 10. Output Power versus Frequency

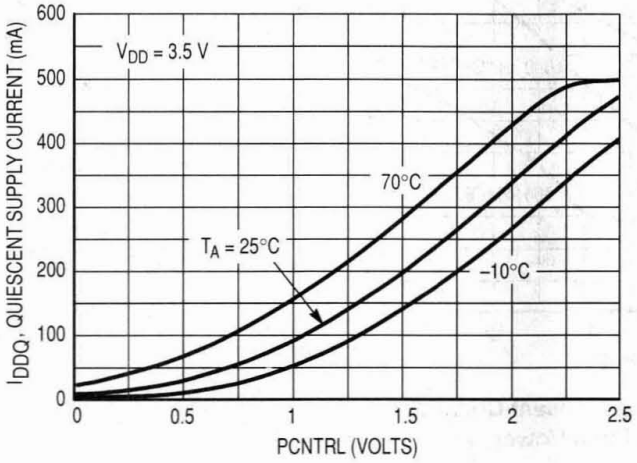


Figure 11. Quiescent Supply Current versus PCNTRL

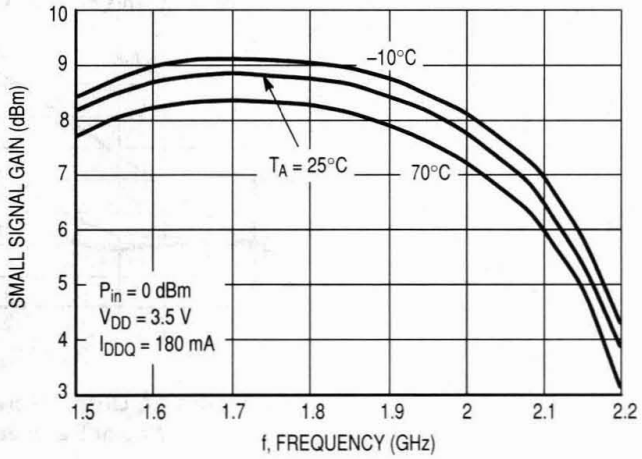


Figure 12. Small Signal Gain versus Frequency

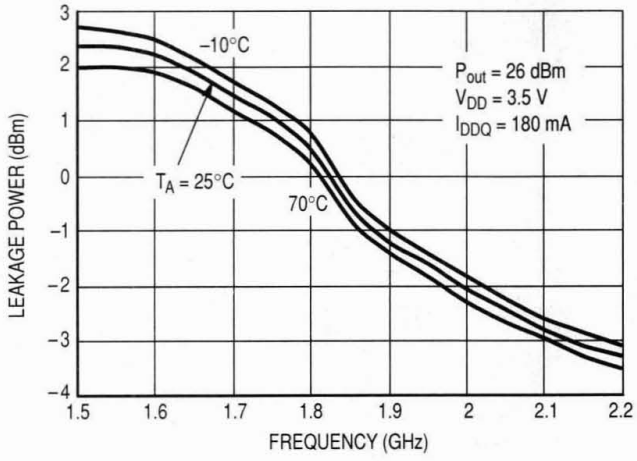


Figure 13. Leakage Power at RX Port in TX Mode versus Frequency

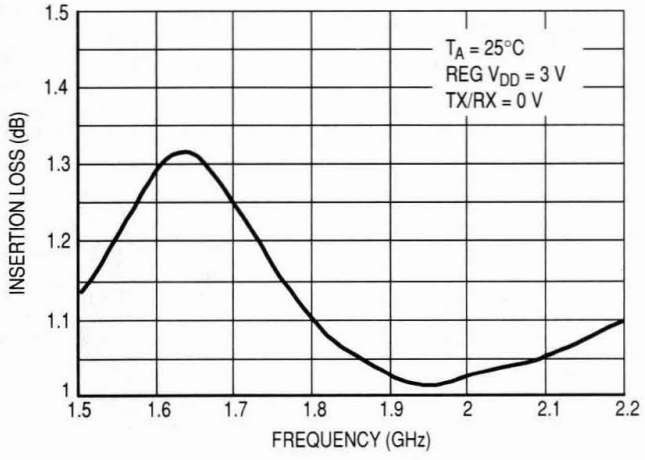


Figure 14. RX Path Insertion Loss in RX Mode versus Frequency

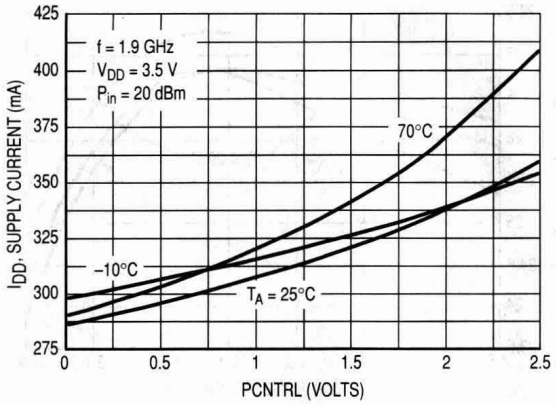


Figure 15. Supply Current versus PCNTRL

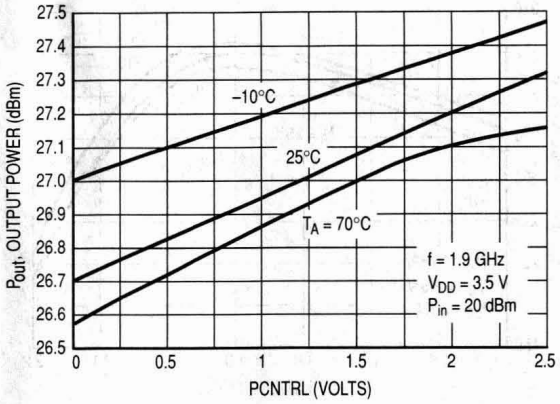


Figure 16. Output Power versus PCNTRL

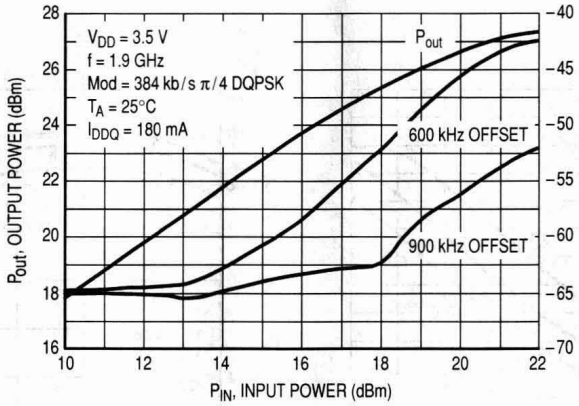


Figure 17. Output Power and Adjacent Channel Power Ratio versus Input Power

DESIGN AND APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC1807 is designed to operate with the MRFIC1806 Driver/Ramp IC in 1.9 GHz Personal Communication System (PCS) applications such as Europe's DECT and Japan's PHS. The design incorporates a depletion mode GaAs power MESFET with a high–power transmit/receive switch and associated bias circuitry in one low–cost SOIC–16 package.

The power MESFET is sized to produce at least 27 dBm saturated output power, including switch loss, from a 3.5 V supply, but the output power can be controlled using the PCNTRL input. This control voltage also allows setting of the quiescent current of the FET. PCNTRL can be set to give best efficiency or linearity for the particular system application. The TX/RX control pin allows fast switching of the T/R switch for TDMA applications. When switching from transmit to receive, the battery supply voltage should be removed from the PA (Pin 4), to avoid excessive current drain. This is usually accomplished using an external pass transistor controlled by the TX/RX signal. Alternatively, if PCNTRL is reduced to 0 V during RX mode, the bias current is reduced to nearly zero.

The Transmit/Receive switch is a reflective MESFET design which is optimized for low loss and power handling in transmit mode. The design can handle 28 dBm of transmit power without significant increase in insertion loss. A regulated 3.0 Volt supply is required at pin 16 for the T/R switch and the bias and control circuitry.

DECT APPLICATIONS

Figure 2 shows the component values for a DECT implementation of the MRFIC1807. For use in equipment designed for DECT, the power amplifier is operated close to saturation to improve device efficiency. Maximum power output at the antenna connector is 24 dBm during a burst. The constant envelope characteristics of the GMSK modulation allow non–linear amplification without spectral regrowth. The transmit signal must be shaped or "ramped" to meet system transmit turn on time requirements of 10 μsec minimum while not splattering into adjacent channels. A turn on time on greater than 2.0 μsec has been shown to give adequate adjacent channel power performance. Most DECT realizations have the modulation applied to the transmit VCO so the most straight forward way of implementing this ramping function is at the power amplifier. The MRFIC1806 Driver/Ramp IC has an on–chip ramping circuit specifically designed for DECT. When ramped in this manner, the MRFIC1806 will supply the appropriately ramped RF signal to the MRFIC1807 which only has to be turned on and off with TX/RX. Alternate off–chip ramping can be implemented either with external components or at baseband. Consult the MRFIC1806 datasheet for more information.

PHS APPLICATIONS

For Japan's Personal Handy System applications, the modulation is $\pi/4$ DQPSK. When amplified with a non–linear amplifier, the signal will regrow the sidebands which have been carefully filtered at baseband, resulting in adjacent channel interference. To avoid this spectral regrowth, the amplifier must be operated "backed off" from saturation. The amount of backoff required has been shown to be a function of amplifier saturated output capability and may be as high as 5.0 dB. The PHS specification calls for a maximum average power during a burst to be 19 dBm. This is consistent with 5.0 dB backoff from the DECT operating point so the same DECT operating condition could be used. Alternatively, PCNTRL can be adjusted for a lower bias point to improve efficiency or higher bias for better linearity. With $\pi/4$ DQPSK modulation, ramping can be accomplished in the encoder so no external ramp circuit is needed. See the MRFIC1806 data sheet for further details.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

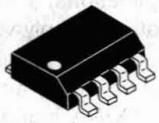
1.9 GHz GaAs Low Noise Amplifier

MRFIC1808

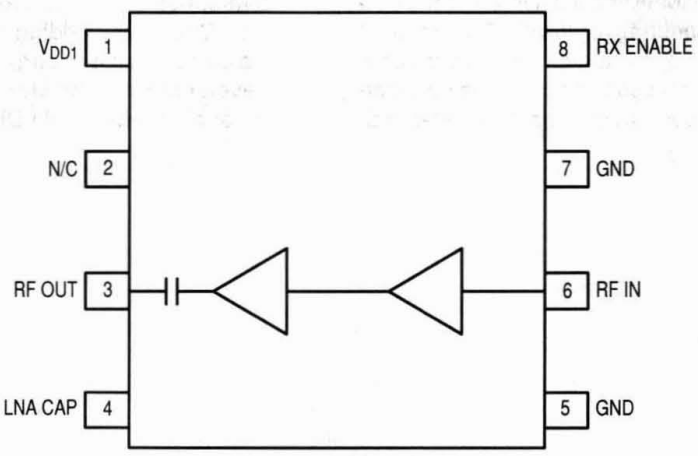
1.9 GHz GaAs LOW NOISE AMPLIFIER

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS) and the emerging North American systems as a preamp for discrete or integrated downmixers. The MRFIC1808 is a two–stage low noise amplifier in a low–cost SO–8 package. The amplifier can be matched to optimize gain or noise figure with simple off–chip input matching. The design employs a novel stacked MESFET design which reuses bias current for the highest gain at minimal current. A CMOS compatible RECEIVE ENABLE pin allows for very low standby current while the system is in transmit mode.

- Usable Frequency Range = 1.7 to 2.1 GHz
- 19 dB Typ Gain
- 1.6 dB Typ Noise Figure
- Simple Off–chip Matching for Maximum Gain/Noise Figure Flexibility
- High Reverse Isolation = –34 dB (Typ)
- Low Power Consumption = 13 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 Volts
- Low Standby Current = 8 μA (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1808R2 forTape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M1808



CASE 751–06
(SO–8)



Pin Connections and Functional Block Diagram

REV 2

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

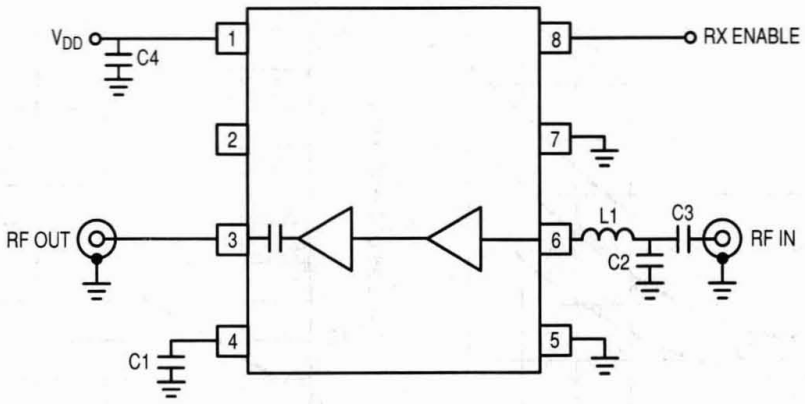
Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	5.5	Vdc
RF Input Power	P_{RF}	3	dBm
Enable Voltage	RX ENABLE	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	1.7 to 2.1	GHz
Supply Voltage	V_{DD}	2.7 to 4.5	Vdc
RX Enable Voltage, ON	RX ENABLE	2.7 to V_{DD}	Vdc
RX Enable Voltage, OFF	RX ENABLE	0 to 0.2	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, RF = 1.9 GHz, RX ENABLE = 3 V, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Gain	16.0	19	—	dB
SSB Noise Figure	—	1.6	—	dB
RF Output 3rd Order Intercept Point	—	13	—	dBm
Output 1 dB Gain Compression	–3.0	1	—	dBm
Reverse Isolation (s_{12})	—	–34	—	dB
Input Return Loss	—	–12	—	dB
Output Return Loss	—	–15	—	dB
Supply Current RX Mode	—	4.2	6.5	mA
Supply Current Standby Mode (RX ENABLE = 0 V)	—	8	25	μA



C1 2 pF
C2 1.8 pF
C3, C4 22 pF
L1 5.6 nH

Figure 1. Applications Circuit Configuration

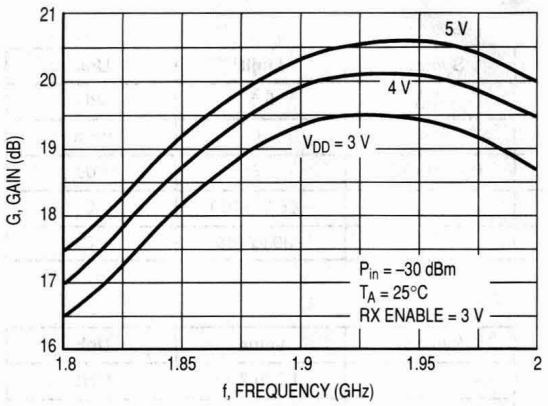


Figure 2. Gain versus Frequency

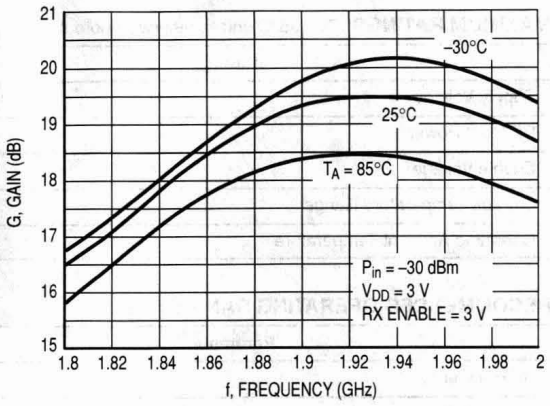


Figure 3. Gain versus Frequency

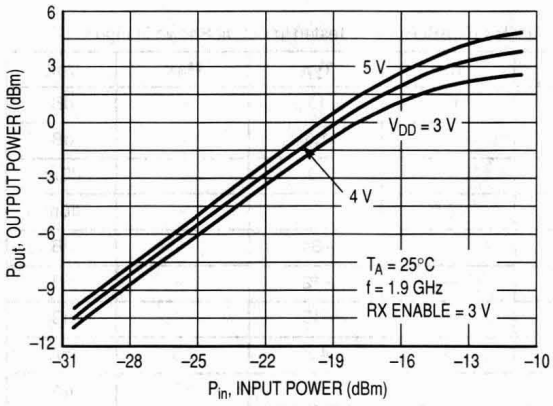


Figure 4. Output Power versus Input Power

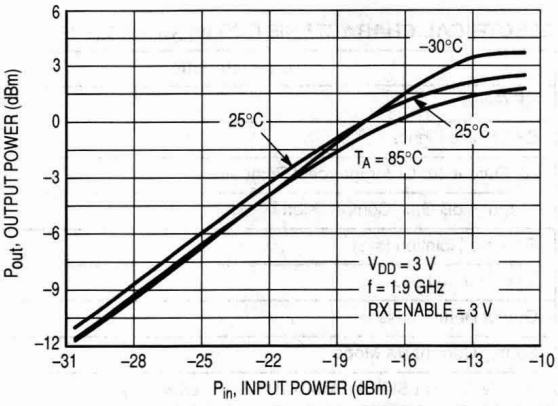


Figure 5. Output Power versus Input Power

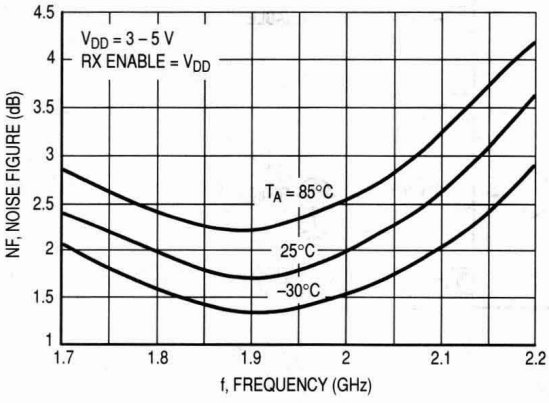


Figure 6. Noise Figure versus Frequency

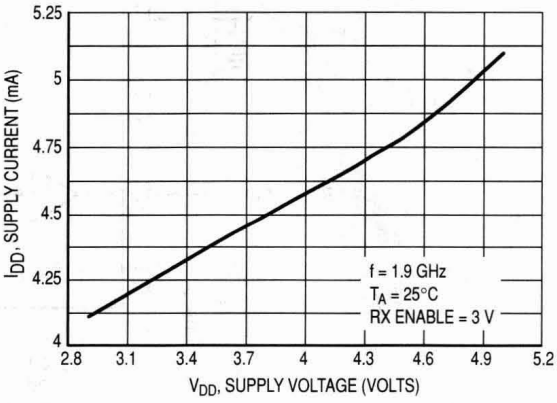


Figure 7. Supply Current versus Voltage

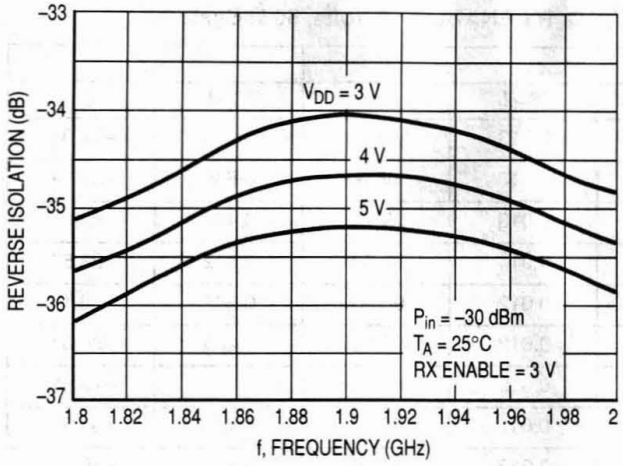


Figure 8. Reverse Isolation versus Frequency

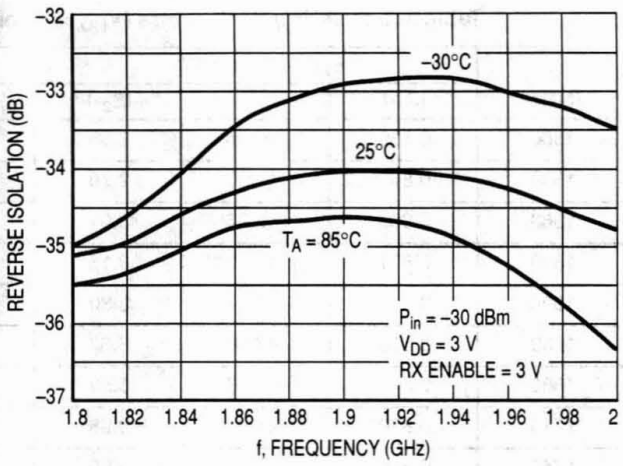


Figure 9. Reverse Isolation versus Frequency

Table 1. Scattering Parameters (V_{DD} = 3 Volts, T_A = 25°C, RX ENABLE = 3 Volts, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\lvert S_{11}\rvert$	$\angle\phi$	$\lvert S_{21}\rvert$	$\angle\phi$	$\lvert S_{12}\rvert$	$\angle\phi$	$\lvert S_{22}\rvert$	$\angle\phi$
1500	0.859	–40.95	2.58	139.07	0.013	103.72	0.583	–79.05
1530	0.870	–41.50	2.79	134.79	0.013	105.63	0.530	–80.94
1560	0.866	–42.06	3.01	130.60	0.013	99.14	0.474	–82.85
1590	0.871	–42.92	3.18	125.11	0.014	98.40	0.412	–83.57
1620	0.873	–43.47	3.30	118.70	0.012	98.00	0.348	–83.11
1650	0.876	–43.60	3.37	112.85	0.012	97.39	0.285	–80.54
1680	0.877	–44.86	3.52	106.23	0.012	92.68	0.229	–73.01
1710	0.880	–45.35	3.68	100.77	0.011	93.90	0.186	–60.35
1740	0.876	–46.03	3.80	94.40	0.012	93.12	0.168	–40.74
1770	0.876	–47.22	3.87	88.75	0.011	88.55	0.182	–20.50
1800	0.885	–48.69	3.98	82.96	0.010	88.40	0.221	–6.82
1830	0.879	–48.55	3.98	76.83	0.010	89.46	0.272	–0.29
1860	0.881	–49.87	3.98	71.11	0.009	94.75	0.324	3.05
1890	0.885	–50.71	4.00	66.38	0.009	97.00	0.376	4.39
1920	0.878	–51.81	4.09	61.64	0.009	88.22	0.425	4.25
1950	0.873	–52.42	4.19	56.66	0.008	87.57	0.474	3.79
1980	0.860	–52.98	4.15	51.32	0.007	88.75	0.522	2.22
2010	0.866	–54.24	3.98	44.93	0.006	100.17	0.564	0.85
2040	0.859	–56.12	3.85	40.93	0.005	87.86	0.599	–0.87
2070	0.861	–56.69	3.89	37.99	0.004	99.30	0.634	–3.01
2100	0.850	–57.79	4.04	35.71	0.004	98.94	0.661	–4.59
2130	0.844	–58.53	4.18	31.89	0.004	118.15	0.691	–6.96
2160	0.834	–60.21	4.21	26.88	0.003	137.84	0.714	–8.94
2190	0.834	–61.26	4.15	22.38	0.003	141.53	0.734	–11.49
2220	0.830	–62.53	4.17	18.75	0.004	–164.13	0.760	–13.48
2250	0.817	–63.84	4.22	14.85	0.004	–172.30	0.776	–15.27
2280	0.812	–64.69	4.21	9.17	0.005	–165.76	0.787	–17.20
2310	0.811	–66.64	4.14	4.09	0.006	–148.57	0.805	–19.42
2340	0.800	–67.89	3.95	1.20	0.007	–153.96	0.808	–21.63
2370	0.794	–69.40	3.83	0.29	0.008	–144.49	0.819	–23.38
2400	0.791	–72.05	3.88	0.33	0.009	–133.12	0.822	–26.10
2430	0.784	–73.59	4.09	–2.06	0.012	–138.06	0.826	–28.21
2460	0.774	–75.60	4.30	–8.63	0.014	–138.55	0.824	–30.43
2490	0.769	–78.81	4.33	–16.94	0.015	–146.05	0.821	–32.72
2520	0.751	–80.46	4.31	–23.37	0.018	–148.25	0.815	–35.42
2550	0.737	–83.20	4.23	–27.46	0.021	–149.08	0.798	–37.56
2580	0.707	–86.12	4.08	–32.67	0.024	–155.44	0.767	–39.31

Table 2. Scattering Parameters (V_{DD} = 4 Volts, T_A = 25°C, RX ENABLE = 3 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
1500	0.849	–40.63	2.83	138.31	0.013	101.12	0.592	–78.76
1530	0.854	–41.00	3.07	134.02	0.012	99.54	0.537	–80.92
1560	0.852	–41.65	3.30	129.90	0.012	97.89	0.482	–82.91
1590	0.855	–42.76	3.50	124.44	0.013	103.09	0.421	–84.04
1620	0.861	–43.15	3.63	118.09	0.013	104.42	0.357	–84.20
1650	0.862	–43.22	3.73	112.01	0.012	95.75	0.293	–82.14
1680	0.861	–44.49	3.89	106.04	0.012	95.43	0.233	–75.91
1710	0.861	–44.93	4.07	100.17	0.011	99.73	0.187	–63.54
1740	0.869	–45.60	4.19	94.14	0.011	94.00	0.164	–43.94
1770	0.864	–46.48	4.30	87.75	0.011	95.67	0.173	–22.19
1800	0.870	–48.17	4.41	82.13	0.011	88.56	0.210	–7.42
1830	0.860	–48.09	4.41	75.97	0.010	88.92	0.258	0.31
1860	0.866	–49.28	4.41	70.37	0.010	96.31	0.313	3.91
1890	0.870	–50.19	4.46	65.24	0.009	93.39	0.367	5.28
1920	0.861	–50.75	4.54	60.65	0.008	90.74	0.417	5.60
1950	0.852	–51.77	4.66	55.96	0.008	89.58	0.468	4.75
1980	0.849	–52.40	4.56	50.46	0.007	84.42	0.518	3.22
2010	0.847	–53.50	4.40	44.25	0.006	94.48	0.561	1.68
2040	0.847	–55.19	4.25	39.96	0.005	88.62	0.597	–0.03
2070	0.847	–55.75	4.29	37.08	0.004	109.85	0.633	–2.25
2100	0.842	–56.92	4.47	34.67	0.005	103.26	0.664	–3.78
2130	0.830	–57.36	4.61	30.80	0.004	125.77	0.694	–6.23
2160	0.823	–59.26	4.66	26.03	0.004	122.00	0.717	–8.30
2190	0.820	–60.09	4.57	21.27	0.004	152.31	0.742	–10.87
2220	0.820	–61.37	4.57	17.70	0.002	160.02	0.762	–13.04
2250	0.812	–63.01	4.63	13.81	0.003	176.88	0.778	–14.80
2280	0.801	–63.88	4.61	8.47	0.004	–165.16	0.792	–17.00
2310	0.802	–65.68	4.54	2.90	0.005	–156.21	0.807	–19.20
2340	0.789	–67.07	4.32	0.38	0.007	–141.83	0.815	–21.21
2370	0.781	–68.28	4.21	–1.24	0.008	–144.89	0.821	–23.34
2400	0.775	–70.61	4.23	–0.61	0.010	–143.18	0.826	–25.75
2430	0.771	–72.01	4.47	–2.85	0.012	–140.04	0.829	–28.07
2460	0.764	–74.59	4.70	–9.44	0.012	–144.28	0.829	–30.56
2490	0.759	–77.25	4.72	–17.93	0.015	–149.63	0.826	–32.63
2520	0.743	–78.88	4.69	–24.28	0.017	–148.60	0.820	–35.12
2550	0.730	–81.98	4.58	–28.44	0.021	–148.70	0.802	–37.38
2580	0.700	–85.55	4.45	–33.64	0.022	–157.99	0.772	–39.29

Table 3. Scattering Parameters (V_{DD} = 5 Volts, T_A = 25°C, RX ENABLE = 3 Volts, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
1500	0.830	–40.58	3.12	137.17	0.011	98.73	0.600	–78.51
1530	0.839	–41.24	3.39	132.69	0.011	101.93	0.548	–80.73
1560	0.836	–41.75	3.64	128.74	0.012	96.66	0.492	–82.85
1590	0.842	–42.35	3.85	123.33	0.013	99.33	0.433	–84.11
1620	0.848	–42.88	4.02	116.83	0.012	101.06	0.370	–84.63
1650	0.843	–43.41	4.11	110.95	0.012	95.15	0.306	–82.83
1680	0.844	–44.37	4.30	104.87	0.012	96.02	0.243	–77.32
1710	0.849	–45.07	4.49	99.42	0.012	96.86	0.193	–66.79
1740	0.852	–45.25	4.64	93.23	0.010	99.66	0.163	–48.45
1770	0.848	–46.18	4.75	87.02	0.012	88.90	0.164	–26.11
1800	0.856	–47.76	4.88	81.25	0.011	93.18	0.200	–9.04
1830	0.850	–47.99	4.87	75.09	0.010	90.25	0.247	–0.08
1860	0.850	–48.93	4.90	69.14	0.009	88.62	0.301	3.73
1890	0.849	–49.88	4.96	64.08	0.009	93.94	0.355	5.69
1920	0.846	–50.72	5.02	59.31	0.009	93.67	0.407	6.01
1950	0.837	–51.45	5.15	54.55	0.007	90.89	0.459	5.70
1980	0.830	–52.33	5.07	48.85	0.008	98.84	0.511	4.17
2010	0.831	–52.97	4.89	42.81	0.006	90.07	0.557	2.40
2040	0.831	–55.08	4.72	38.38	0.004	100.73	0.593	0.51
2070	0.829	–55.58	4.74	35.43	0.005	96.39	0.631	–1.55
2100	0.823	–56.53	4.95	32.95	0.004	122.68	0.661	–3.57
2130	0.815	–57.23	5.10	29.26	0.004	112.15	0.691	–5.96
2160	0.805	–58.81	5.14	24.21	0.004	132.80	0.718	–7.96
2190	0.802	–59.57	5.04	19.45	0.004	136.20	0.739	–10.56
2220	0.801	–60.70	5.05	15.80	0.003	178.25	0.762	–12.60
2250	0.791	–62.24	5.11	12.01	0.004	170.40	0.780	–14.52
2280	0.781	–62.95	5.08	6.42	0.005	–172.19	0.793	–16.63
2310	0.786	–64.98	4.97	1.09	0.006	–169.11	0.811	–18.96
2340	0.773	–66.05	4.74	–1.76	0.006	–150.31	0.818	–21.10
2370	0.766	–67.23	4.60	–2.91	0.008	–143.53	0.821	–23.29
2400	0.763	–69.83	4.64	–2.54	0.009	–146.46	0.827	–25.81
2430	0.757	–71.49	4.89	–4.89	0.011	–141.36	0.832	–27.88
2460	0.750	–73.61	5.12	–11.49	0.012	–147.16	0.832	–30.37
2490	0.742	–76.17	5.17	–19.88	0.014	–145.27	0.827	–32.68
2520	0.726	–78.01	5.10	–26.09	0.016	–145.14	0.820	–35.26
2550	0.712	–81.26	5.01	–30.13	0.018	–150.98	0.805	–37.48
2580	0.686	–84.54	4.81	–35.31	0.022	–155.55	0.771	–39.32

The MRFIC Line

1.9 GHz GaAs Upconverter

MRFIC1813

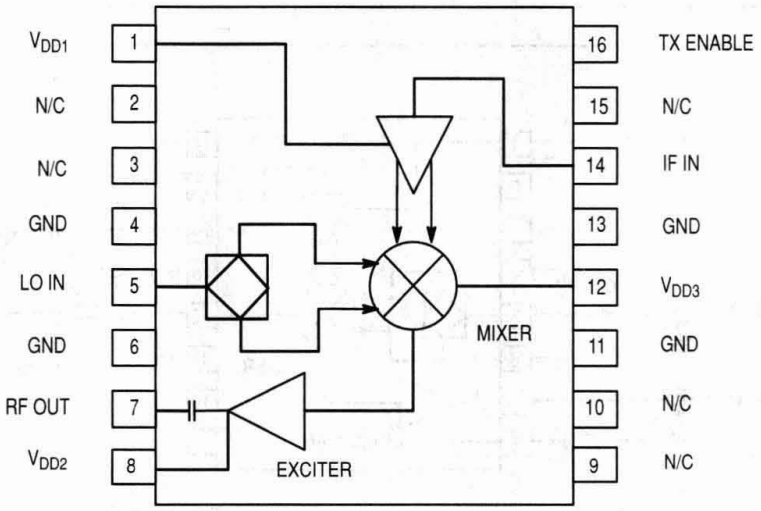
1.9 GHz UPMIXER AND EXCITER AMPLIFIER

CASE 948C–03
(TSSOP–16)

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS) and the emerging North American systems. The MRFIC1813 is also applicable to 2.4 GHz ISM equipment. The device combines a balanced upmixer and a transmit exciter amplifier in a low-cost TSSOP–16 package. Minimal off-chip matching is required while allowing for maximum flexibility and efficiency. The mixer is optimized for low–side injection and provides more than 12 dB of conversion gain with over 0 dBm output at 1 dB gain compression. Image filtering is implemented off-chip to allow maximum flexibility. A CMOS compatible ENABLE pin allows standby operation where the current drain is less than 250 μA.

Together with other devices from the MRFIC180X or the MRFIC240X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone or 2.4 GHz ISM band equipment.

- Usable Frequency Range = 1.7 to 2.5 GHz
- 15 dB Typ IF to RF Conversion Gain
- 3 dBm Power Output Typ, 0 dBm Minimum at 1 dB Gain Compression
- Simple Off-chip Matching for Maximum Flexibility
- Low Power Consumption = 75 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 Volts
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1813R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1813



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

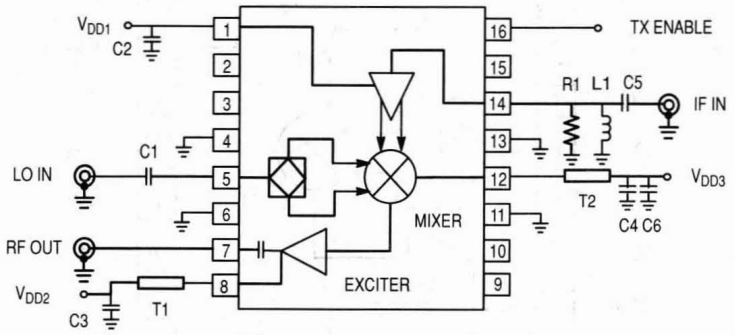
Ratings	Symbol	Limit	Unit
Supply Voltage	V_{DD1}, V_{DD2}, V_{DD3}	5.5	Vdc
IF Input Power	P_{IF}	3	dBm
LO Input Power	P_{LO}	3	dBm
Enable Voltage	TX ENABLE	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Output Frequency	f_{RF}	1.7 to 2.5	GHz
LO Input Frequency	f_{LO}	1.5 to 2.4	GHz
IF Input Frequency	f_{IF}	70 to 350	MHz
Supply Voltage	V_{DD}	2.7 to 4.5	Vdc
TX Enable Voltage, ON	TX ENABLE	2.7 to V_{DD}	Vdc
TX Enable Voltage, OFF	TX ENABLE	0 to 0.2	Vdc

ELECTRICAL CHARACTERISTICS ($V_{DD1,2,3}$, TX ENABLE= 3 V, T_A = 25°C, f_{LO} = 1.65 GHz @ – 5 dBm, f_{IF} = 250 MHz @ –15 dBm)

Characteristic	Min	Typ	Max	Unit
IF to RF Small Signal Conversion Gain (P_{RF} = –35 dBm)	12	15	—	dB
RF Output 1 dB Gain Compression	0	3	—	dBm
RF Output 3rd Order Intercept	—	11	—	dBm
LO Feedthrough to RF Port	—	–15	–10	dBm
Noise Figure	—	11	—	dB
Lower Sideband Output Power at RF Port	—	–10	–6	dBm
Supply Current TX Mode	—	25	35	mA
Supply Current Standby Mode (TX ENABLE = 0 V, LO Off)	—	100	250	μA
TX Enable Current	—	3	—	μA



C1, C2, C3, C4 15 pF
C6 1 μF
R1 300 Ω
T1, T2 MICROSTRIP, Z_0 = 73 Ω, θ = 29° @ 1.9 GHz
BOARD MATERIAL – GLASS/EPOXY, ε_r = 4.45,
DIELECTRIC THICKNESS = 0.018 INCH

IF Frequency	L1	C5
110 MHz	180 nH	12 pF
250 MHz	68 nH	5.6 pF
350 MHz	39 nH	3.9 pF

Figure 1. Applications Circuit Configuration

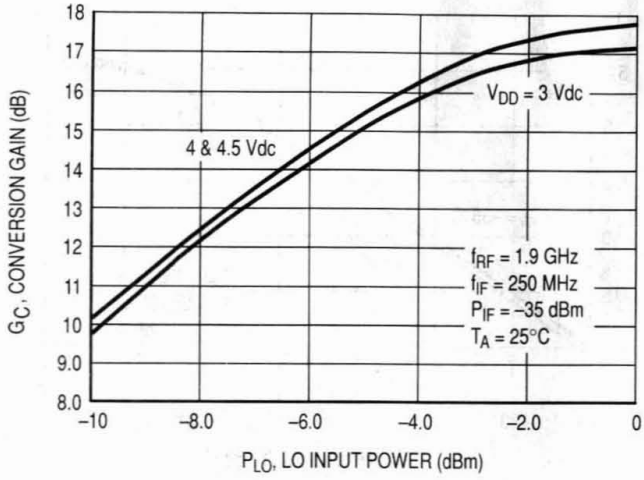


Figure 2. Conversion Gain versus LO Power

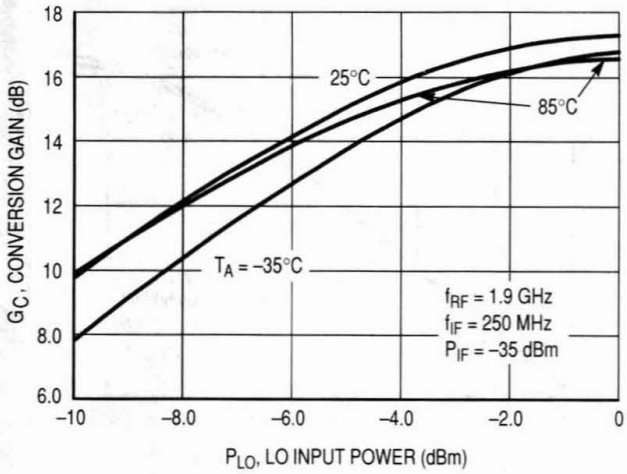


Figure 3. Conversion Gain versus LO Power

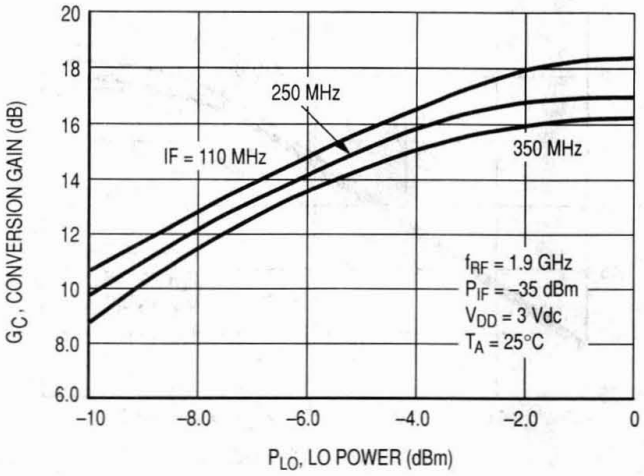


Figure 4. Conversion Gain versus LO Power

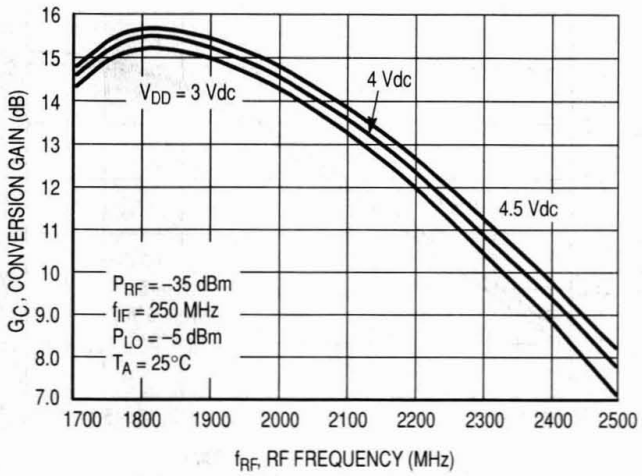


Figure 5. Conversion Gain versus RF Frequency

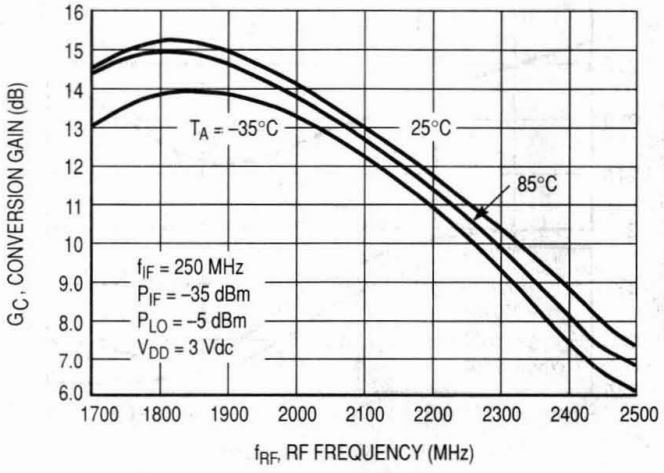


Figure 6. Conversion Gain versus RF Frequency

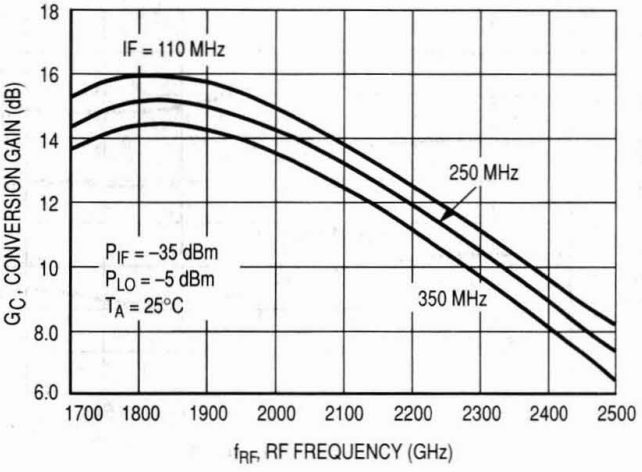


Figure 7. Conversion Gain versus RF Frequency

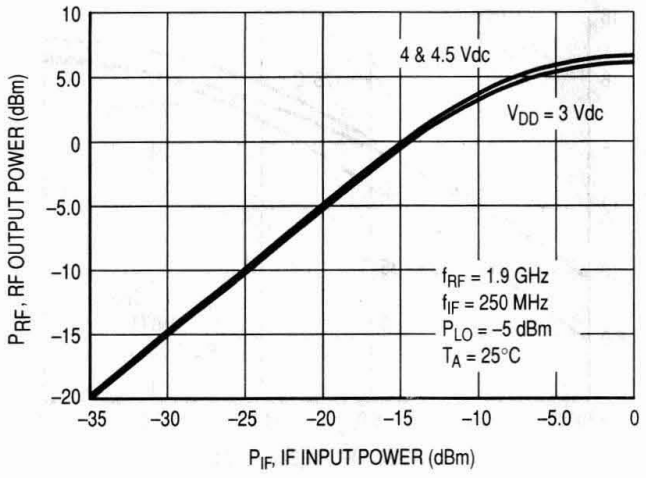


Figure 8. RF Output versus Input Power

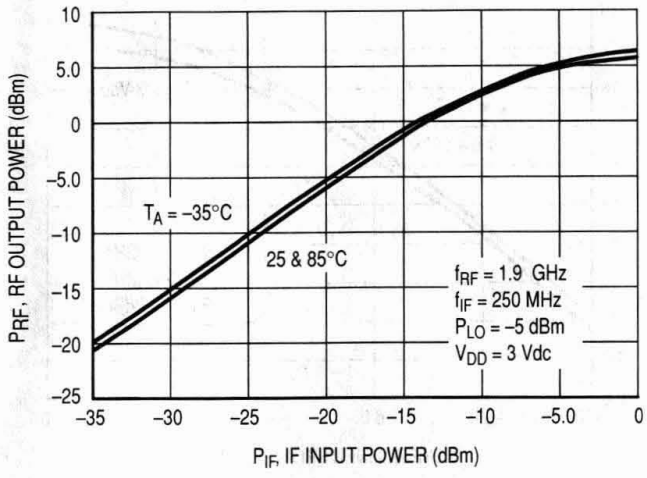


Figure 9. RF Output Power versus IF Input Power

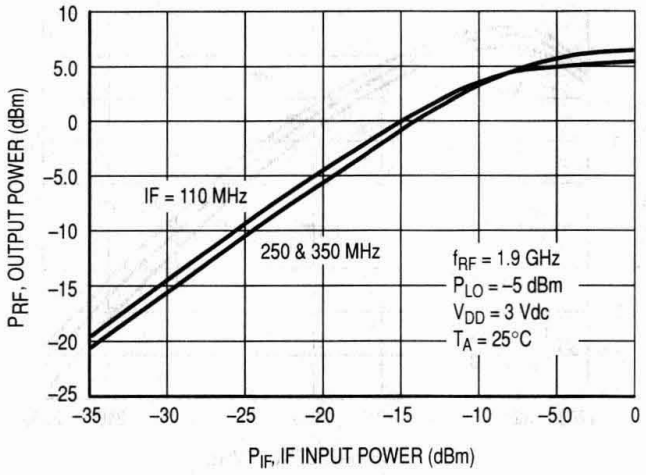


Figure 10. RF Output versus IF Input Power

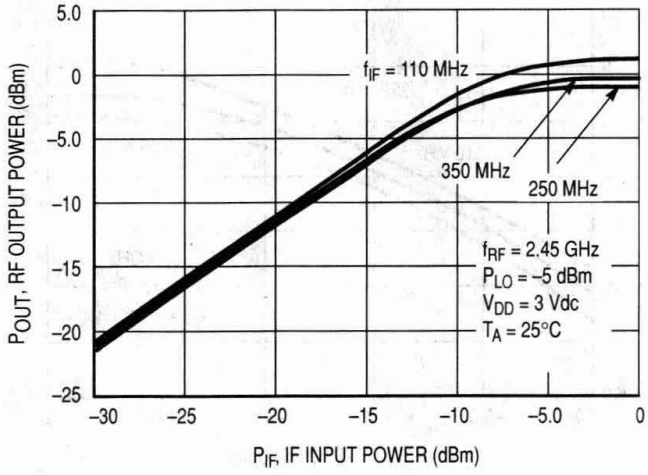


Figure 11. Output Power versus IF Input Power

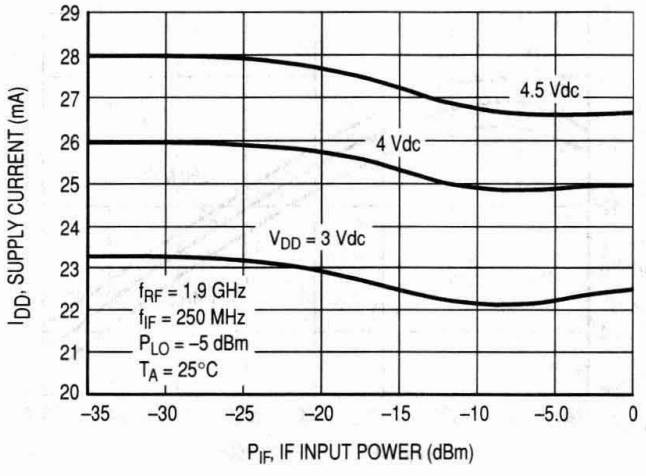


Figure 12. Supply Current versus IF Input Power

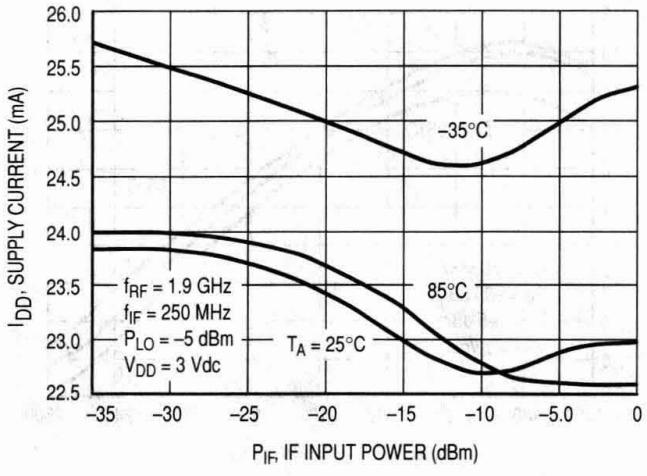


Figure 13. Supply Current versus IF Input Power

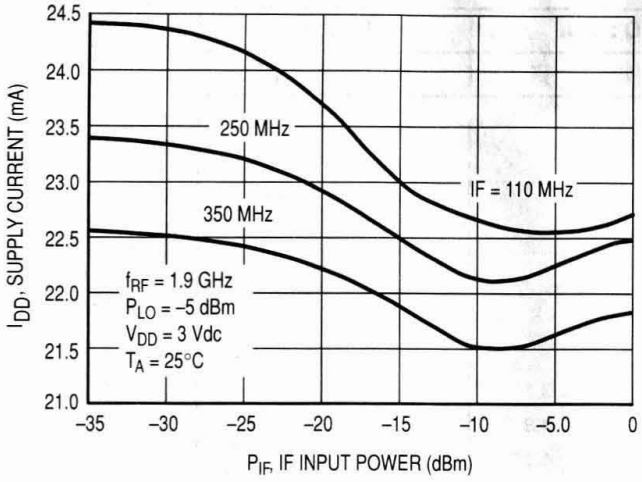


Figure 14. Supply Current versus IF Input Power

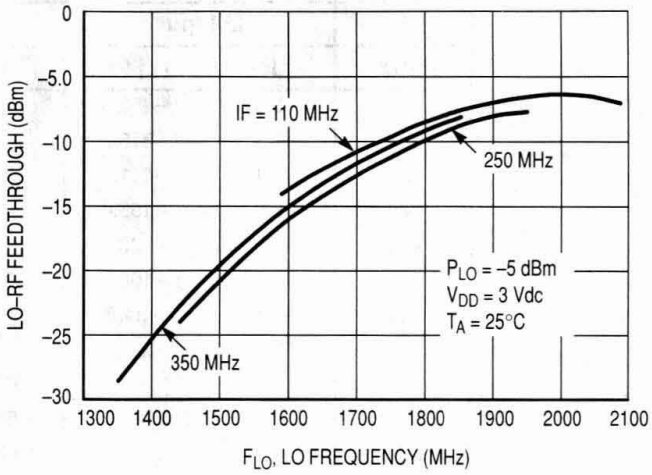


Figure 15. LO to RF Feedthrough versus LO Frequency

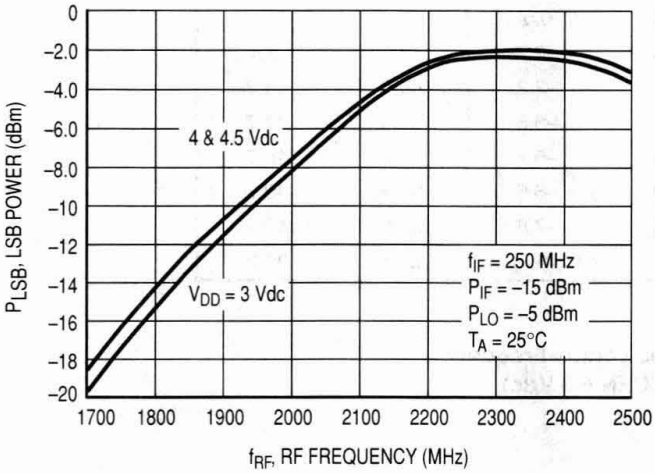


Figure 16. Lower Side Band Power versus RF Frequency

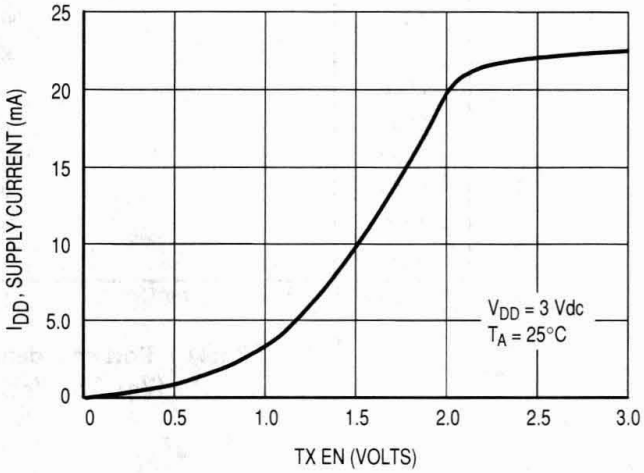


Figure 17. Supply Current versus Transmit Enable Voltage

f	IF Input		LO Input		RF Output (1)	
(MHz)	R	jX	R	jX	R	jX
70	8.3	–452.4				
100	7.3	–318.5				
150	7.1	–211.3				
200	6.6	–156.4				
250	6.5	–123.1				
300	6.1	–100.7				
350	5.7	–84.2				
1100			62.5	3.1		
1200			58.1	4.3		
1300			53.7	4.7		
1400			50.2	4.2		
1500			47.3	3.9		
1600			44.4	3.2		
1700			42.0	1.6	30.4	33.6
1800			40.6	0.5	42.6	16.9
1900			39.6	–0.7	49.1	2.3
2000			38.7	–2.2	40.6	14.2
2100			38.2	–3.6	33.8	17.7
2200			38.4	–5.1	33.3	15.7
2300			38.9	–6.5	32.9	13.7
2400			39.5	–7.8	29.6	13.2
2500					27.4	11.9

(1) Includes T1 shown in Figure 1.

Table 1. Port Impedances versus Frequency (V_{D1}, V_{D2}, V_{D3}, TX EN = 3 Vdc)

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MRFIC1813 combines a single–balanced MESFET mixer with an exciter amplifier. It is usable for transmit frequencies from 1.7 to 2.5 GHz and IF frequencies from 70 to 350 MHz. The design is optimized for low–side local oscillator injection in hetrodyne transmit applications.

Minimal off–chip matching is required while allowing for flexibility and performance optimization. An active balun is employed at the IF port which gives good balance down to at least 70 MHz. A passive splitter is used at the LO input to complete the single–balanced configuration.

CIRCUIT CONSIDERATIONS

Figure 1 shows the application circuit used to gather the data presented in the characterization curves. As shown in Table 1, the IF port impedance is very high. Three hundred ohms was chosen for R1 to shunt the IF port as a compromise of gain and bandwidth. A 50 Ω resistor can be used and L1 and C5 eliminated to provide a broadband match. The conversion gain is reduced to about 8 dB. Microstrip inductors T1 and T2 combine with inductance internal to the device to form RF chokes. Some tuning of the RF output can be achieved with T1.

As with all RF devices, circuit layout is important. Controlled impedance lines should be used for all RF and IF interconnects. As shown in Figure 1, power supply by–passing should be used to avoid device instability. Ground vias should be included near all ground connections indicated in the schematic. Off–chip components should be mounted as close to the IC leads as possible.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" to the device type. For a complete list of currently available boards and one in development for newly introduced products, please contact your local Motorola Distributor or Sales Office.

Advance Information

The MRFIC Line

1.9 GHz GaAs Downconverter

MRFIC1814

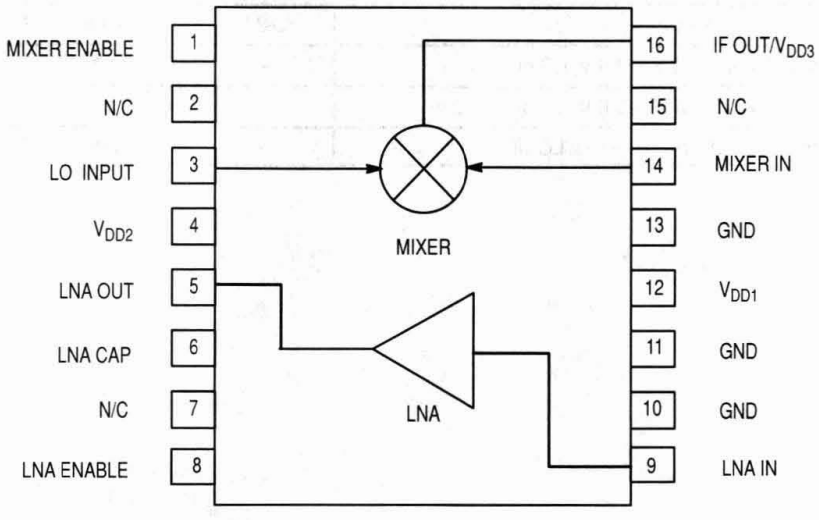
1.8 GHz LOW NOISE AMPLIFIER AND DOWNMIXER

CASE 948C–03
(TSSOP–16)

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS), and the emerging North American systems. The MRFIC1814 includes a low noise amplifier and downmixer in a low-cost TSSOP–16 package. The integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility and efficiency. The mixer is optimized for low–side injection and offers reasonable intercept point as well as high efficiency with 9 dB of conversion gain. Image filtering is implemented off-chip to allow maximum flexibility. CMOS compatible ENABLE pins allow standby operation where the current drain is less than 0.1 mA.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable Frequency Range = 1.8 to 2.0 GHz
- 17 dB Typ Gain, 2.5 dB Typ Noise Figure LNA
- 8 dB Typ Gain, 10 dB Typ Noise Figure Mixer
- –5.5 dBm Typ Mixer Input Intercept Point
- Simple LO/IF Off-chip Matching for Maximum Flexibility
- Low Power Consumption = 39 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 Volts
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1814R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1814



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

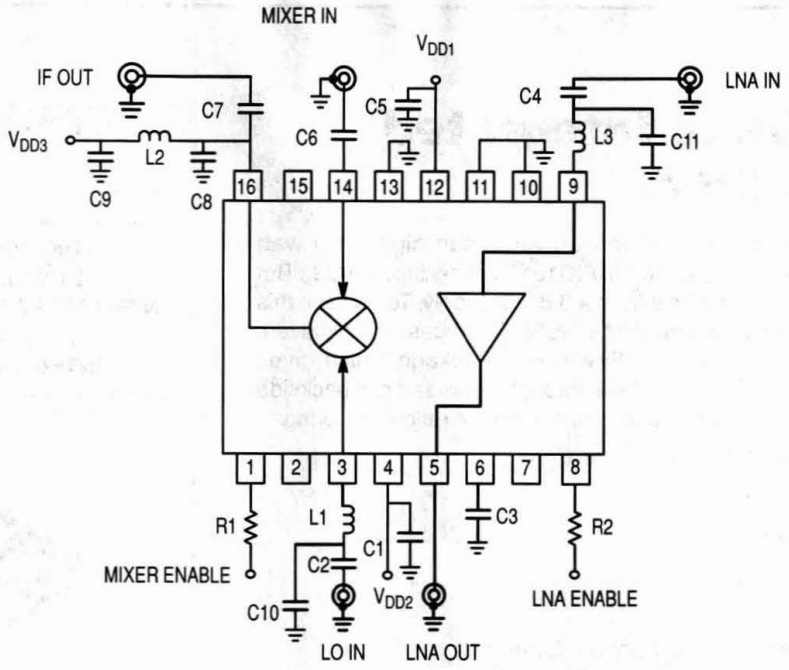
Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	5.5	Vdc
LNA Input Power	LNA_{in}	10	dBm
LO Input Power	P_{LO}	10	dBm
Enable Voltage	ENABLE	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.8 to 2.0	GHz
Mixer LO Frequency	f_{LO}	1.5 to 1.8	GHz
IF Output Frequency	f_{IF}	70 to 300	MHz
Supply Voltage	V_{DD}	2.7 to 4.5	Vdc
Enable Voltage, ON	MIXER, LNA ENABLE	2.7 to V_{DD}	Vdc
Enable Voltage, OFF	MIXER, LNA ENABLE	0 to 0.2	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, LO = 1.65 GHz @ – 5 dBm, RF = 1.9 GHz @ –30 dBm, MIXER & LNA ENABLE = 3 V)

Characteristic	Min	Typ	Max	Unit
LNA Gain (LNA ENABLE = 3 V)	14	17	—	dB
LNA Gain (LNA ENABLE = 0 V)	—	–19	—	dB
LNA Noise Figure	—	2.5	—	dB
LNA Input 3rd Order Intercept	—	–7	—	dBm
LNA Output 1 dB Gain Compression Point	–6	–3	—	dBm
Mixer Conversion Gain (into 50 Ω)	5	8	—	dB
Mixer Noise Figure	—	10	—	dB
Mixer Input 3rd Order Intercept	—	–5	—	dBm
Mixer Output 1 dB Gain Compression Point	–8.5	–5.5	—	dBm
Total Supply Current (ENABLE VOLTAGES = 3.0 V, LO off)	—	10	17	mA
Total Supply Current (ENABLE VOLTAGES = 3.0 V, LO on)	—	13	—	mA
Standby Mode Current (ENABLE VOLTAGES = 0 V, LO off)	—	0.05	0.25	mA



C1, C2, C4	15 pF	C11	1.6 pF
C3	3 pF	L1	4.7 nH
C5	30 pF	L2	10 nH
C6, C8	10 pF	L3	3.9 nH
C7	12 pF	R1, R2	10 kΩ
C9	560 pF	BOARD MATERIAL GLASS/EPOXY, ε_r = 4.45,	
C10	3.6 pF	0.018 INCH DIELECTRIC THICKNESS	

Figure 1. Applications Circuit Configuration for 250 MHz IF

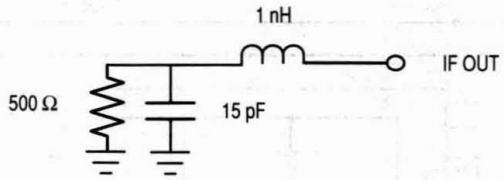


Figure 2. Equivalent IF Output Circuit

The MRFIC Line

1800 MHz GaAs Integrated Power Amplifier

MRFIC1817

1700–1900 MHz MMIC
DCS1800/PCS1900
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

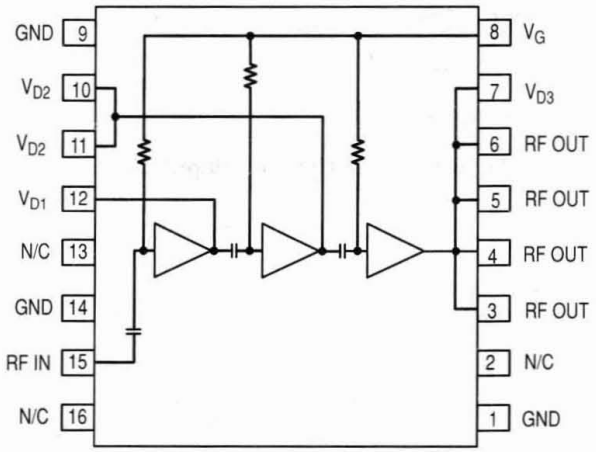
Designed specifically for application in Pan European digital 1.0 watt DCS1800/PCS1900 handheld radios, the MRFIC1817 is specified for 32 dBm output power with power gain over 27 dB from a 3.6 volt supply. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal and electrical performance through a solderable backside contact while allowing the convenience and cost benefits of reflow soldering.

- Minimum Output Power Capabilities
  32 dBm @ 3.6 Volts
  30 dBm @ 3.0 Volts
- Typical Volt Characteristics
  RF Input Power = 5.0 dBm
  RF Output Power = 33.5 dBm
  Typical PAE = 42%
- Low Current required from Negative Supply – 2 mA max
- Guaranteed Stability and Ruggedness
- Order MRFIC1817R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1817

CASE 978–02
(PFP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Z_O = 50 Ω, unless otherwise noted)

Rating	Symbol	Value	Unit
DC Positive Supply Voltage	$V_{D1, 2, 3}$	6	Vdc
DC Negative Supply Voltage	V_{SS}	–5	Vdc
RF Input Power	P_{in}	10	dBm
RF Output Power	P_{out}	35	dBm
Operating Case Temperature Range	T_C	–35 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W



Pin Connections and Functional Block Diagram

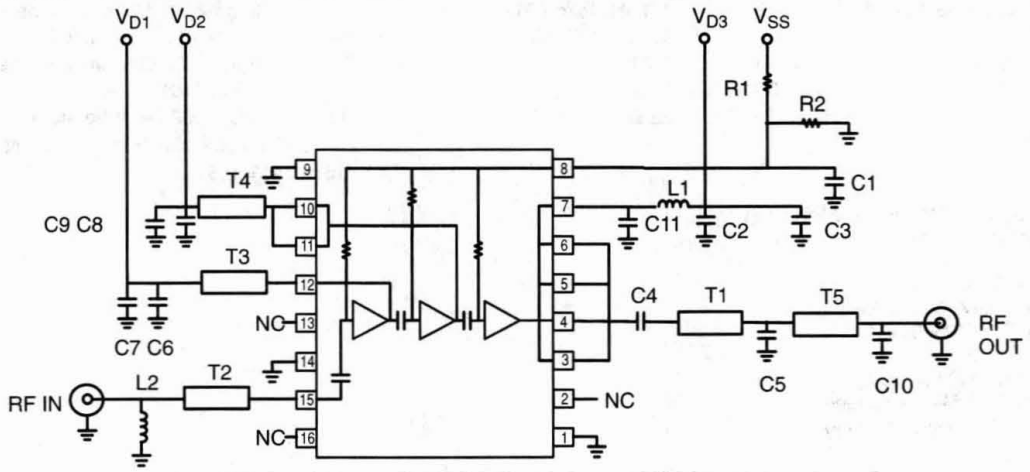
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{D1, 2, 3}$	2.7 to 5	Vdc
Gate Voltage	V_{SS}	–3.5 to –4.5	Vdc
RF Frequency Range	f_{RF}	1700 to 1900	MHz
RF Input Power	P_{RF}	0 to 6	dBm

ELECTRICAL CHARACTERISTICS ($V_{D1, 2, 3}$ = 3.6 V, V_{SS} = –4 V, P_{in} = 5 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
Frequency Range	1710	—	1785	MHz
Output Power	32	33.5	—	dBm
Power Added Efficiency	35	42	—	%
Output Power (PCS 1900 Tuning f = 1850 to 1910 MHz)	—	33.5	—	dBm
Power Added Efficiency (PCS 1900 Tuning f = 1850 to 1910 MHz)	—	42	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output (2nd and 3rd)	—	–35	–30	dBc
Output Power at Low voltage (V_{D1}, V_{D2}, V_{D3} = 3.0 V)	30	32	—	dBm
Output Power Isolation (V_{D1}, V_{D2}, V_{D3} = 0 V)	—	–40	–30	dBm
Noise Power (In 100 kHz, 1805 to 1880 MHz)	—	–85	–80	dBm
Stability – Spurious Output (P_{in} = 5 dBm, P_{out} = 0 to 33 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle) (1)	—	—	–60	dBc
Load Mismatch stress (P_{out} = 33 dBm, Load VSWR = 10:1 at any Phase Angle) (1)	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth	—	2	—	MHz
Negative Supply Current	—	0.7	2	mA

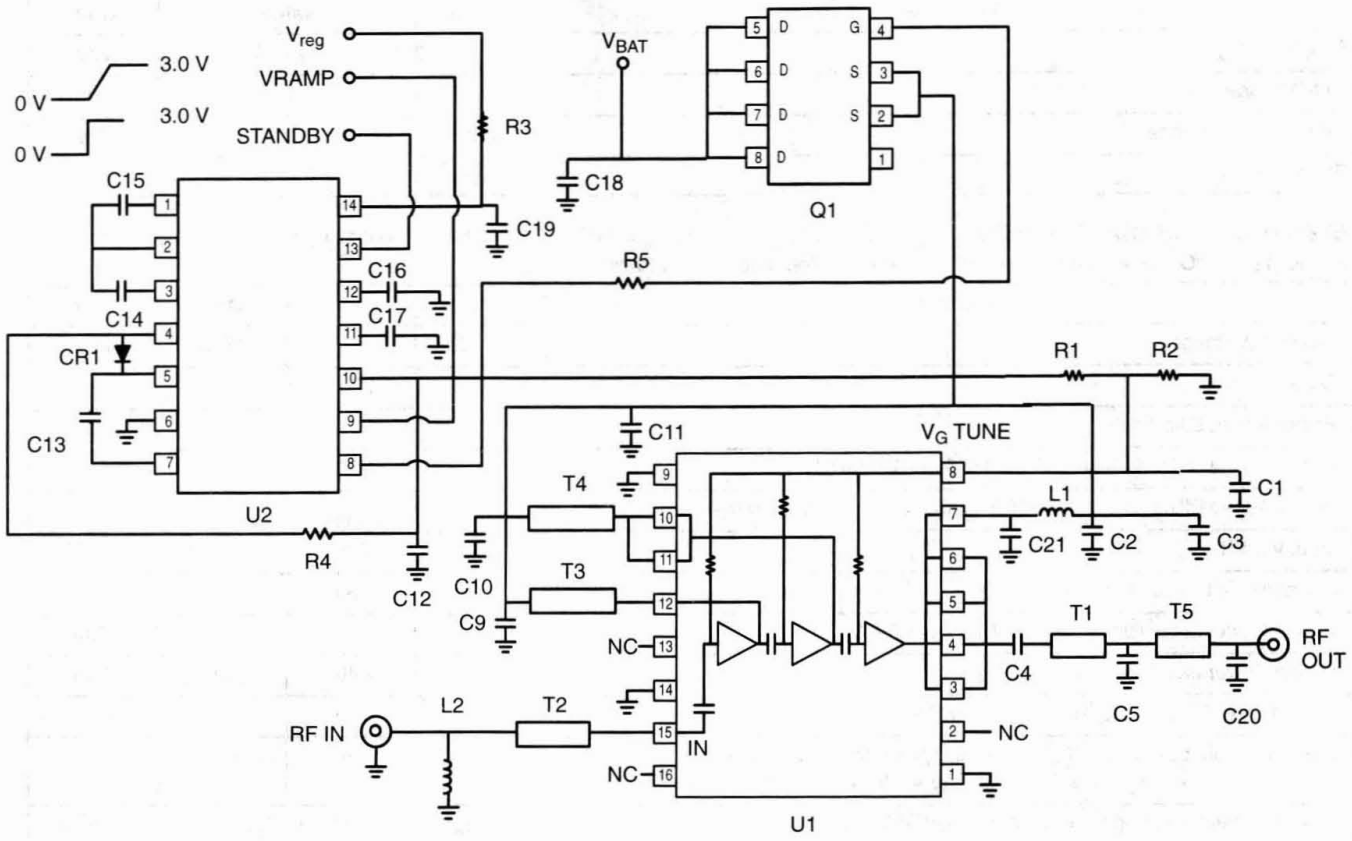
(1) Adjust $V_{D1, 2, 3}$ (0 to 3.6 V) for specified P_{out}; Duty Cycle = 12.5%, Period = 4.6 ms.



C1	1 nF	L1	18 nH, Coilcraft or 20 mm 50 Ω Microstrip Line	T2	6 mm 50 Ω Microstrip Line
C2, C6, C8	22 pF, NPO/COG			T3	5 mm 40 Ω Microstrip Line
C3, C7, C9	47 nF	L2	1.8 nH, Toko 2012	T4	1 mm 40 Ω Microstrip Line
C4	5.6 pF, AVX0603 ACCUF	R1	2.7 KΩ	T5	5.5 mm 50 Ω Microstrip Line
C5	3.9 pF, AVX0603 ACCUF	R2	2.2 KΩ	Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	
C10, C11	1 pf	T1	2.5 mm 50 Ω Microstrip Line		

NOTE: For PCS 1900 tuning the following values are changed.
C5 = 2.7 pF, AVX0603 ACCUF
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 1. Reference Circuit Configuration



C1	6.8 nF	C20, C21	1 pF	R4	100 Ω
C2, C9, C10	22 pF, 0603 NPO/COG	CR1	MMBD701LT1	R5	470 Ω
C3, C11	47 nF	L1	18 nH, Coilcraft or 20 mm 50 Ω Microstrip Line	T1	0.5 mm 30 Ω Microstrip Line
C4	5.6 pF, AVX0603 ACCUF			T2	5 mm 50 Ω Microstrip Line
C5	3.9 pF, AVX0603 ACCUF	L2	1.8 nH, Toko 2012	T3	8 mm 50 Ω Microstrip Line
C12	220 nF	Q1	MMSF4N01HD	T4	1 mm 50 Ω Microstrip Line
C13, C16, C17, C19	1 μF	R1	2.7 KΩ	T5	5.5 mm 50 Ω Microstrip Line
C14, C15	1 μF	R2	3 KΩ	U1	MRFIC1817
C18	1 μF	R3	22 Ω	U2	MC33169 (–4 V Version)
				Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	

NOTE: For PCS1900 applications, the following component values are changed

L2 = 1.5 nH Toko 2012
C4 = 6.8 pF, AVX0603 ACCUF
C5 = 2.7 pF, AVX0603 ACCUF
C20 = Not Used
T1 = 0.5 mm 50 Ω Microstrip Line
T2 = 5 mm 50 Ω Microstrip Line
T3 = 1 mm 40 Ω Microstrip Line

Figure 2. DCS1800/PCS1900 Applications Circuit Configuration

Typical Characteristics

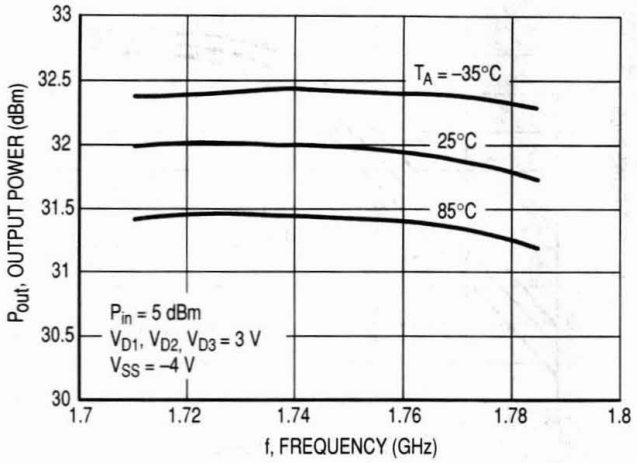


Figure 3. Output Power versus Frequency

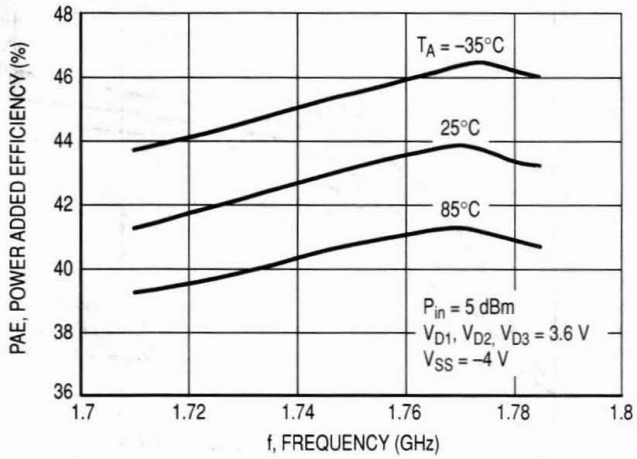


Figure 4. Power Added Efficiency versus Frequency

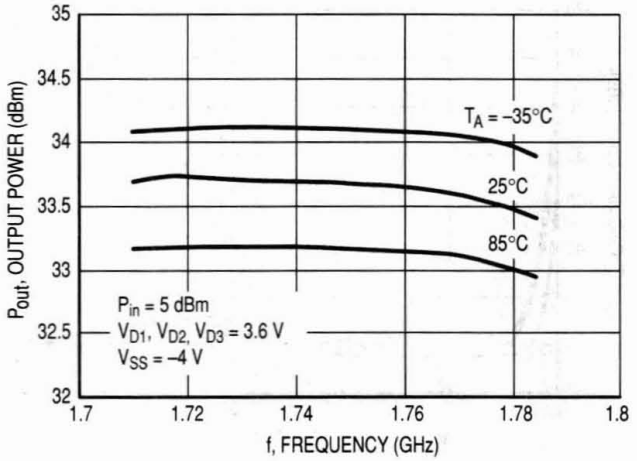


Figure 5. Output Power versus Frequency

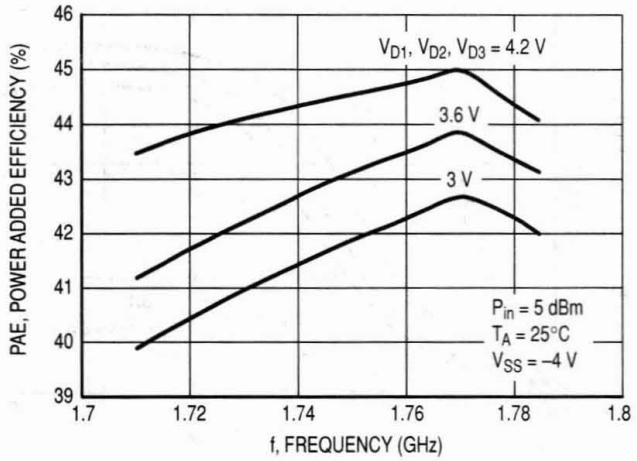


Figure 6. Power Added Efficiency versus Frequency

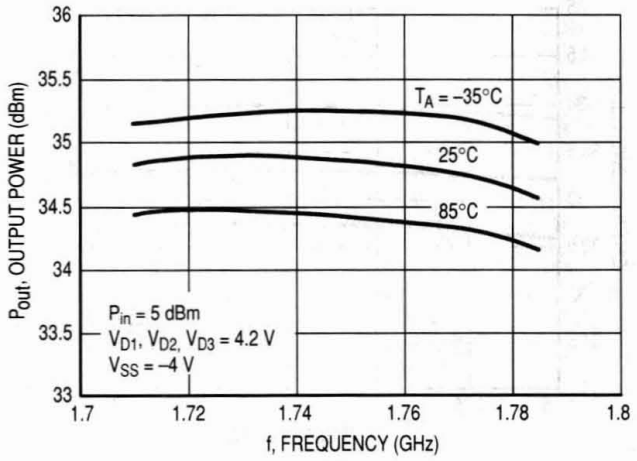


Figure 7. Output Power versus Frequency

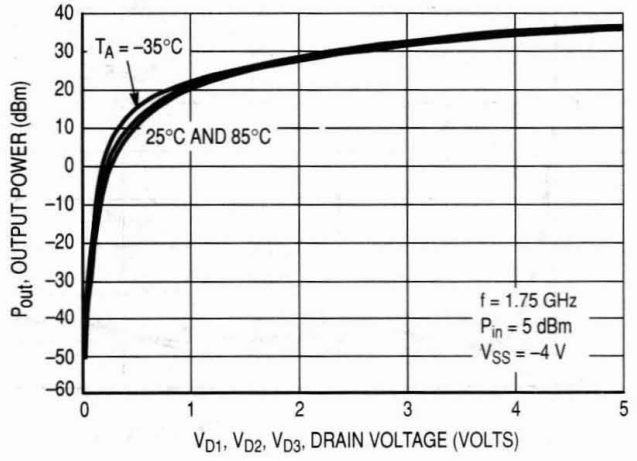


Figure 8. Output Power versus Drain Voltage

Typical Characteristics

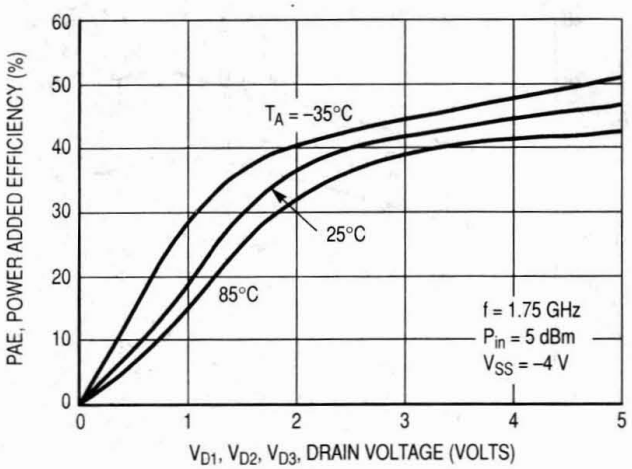


Figure 9. Power Added Efficiency versus Drain Voltage

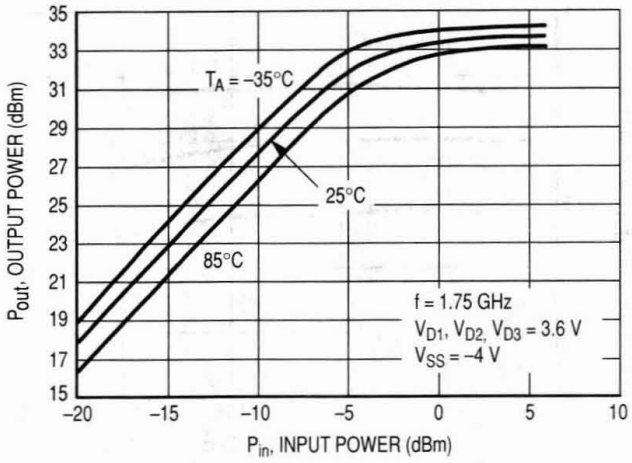


Figure 10. Output Power versus Input Power

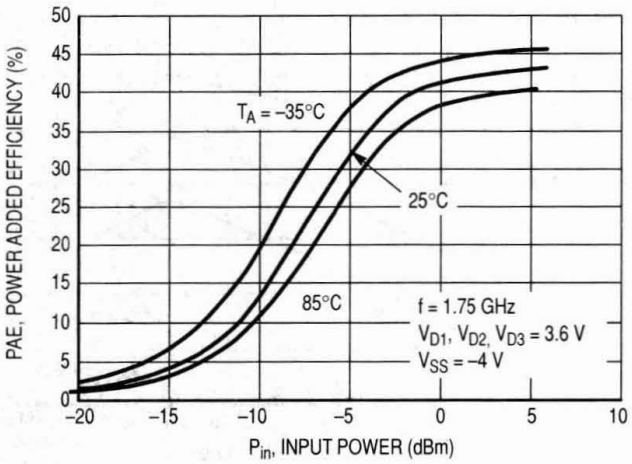


Figure 11. Power Added Efficiency versus Input Power

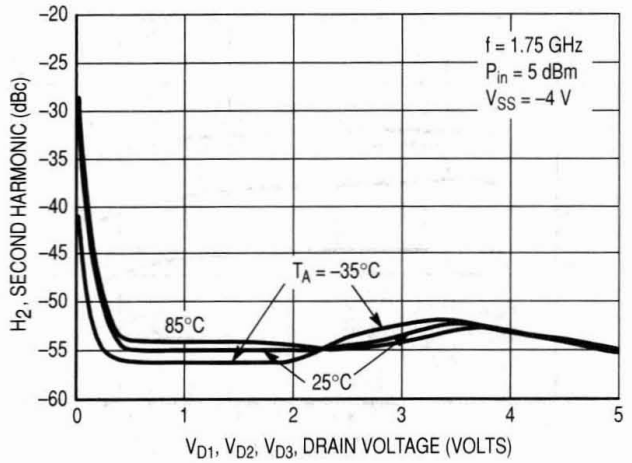


Figure 12. Second Harmonic versus Drain Voltage

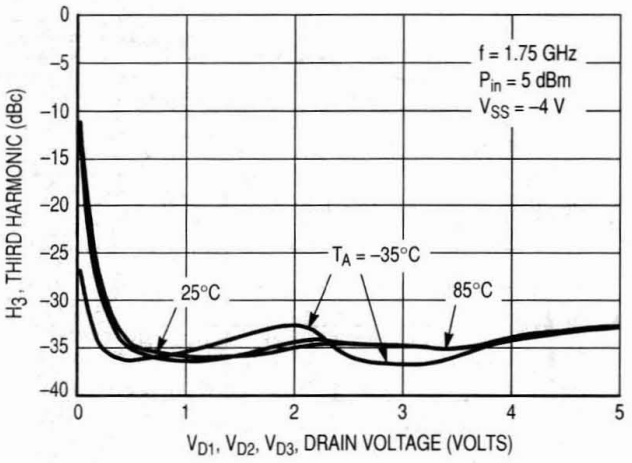


Figure 13. Third Harmonic versus Drain Voltage

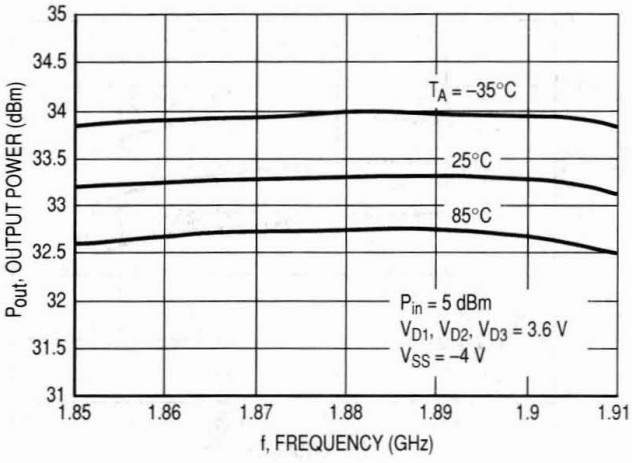


Figure 14. Output Power versus Frequency – PCS Band

Typical Characteristics

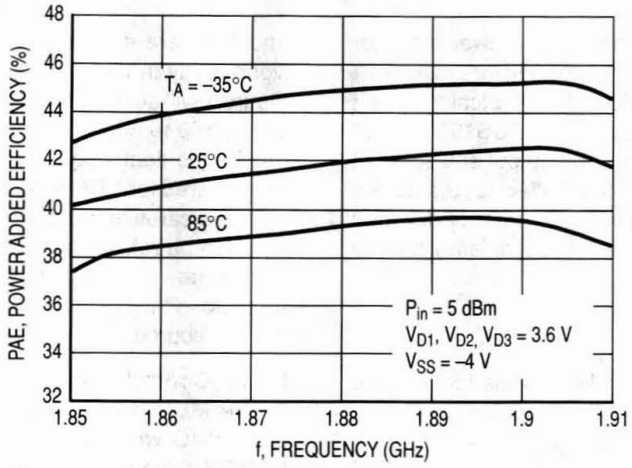


Figure 15. Power Added Efficiency versus Frequency – PCS Band

Table 1. Optimum Loads Derived from Circuit Characterization

f	Z_{in} OHMS		Z_{OL}^* OHMS	
MHz	R	jX	R	jX
1710	7.77	–34.15	4.89	9.50
1720	7.84	–34.37	4.87	9.34
1730	7.87	–34.67	4.86	9.18
1740	8.07	–34.79	4.78	8.94
1750	8.24	–35.05	4.77	8.70
1760	8.39	–35.22	4.73	8.51
1770	8.44	–35.56	4.70	8.32
1780	8.52	–35.79	4.67	8.12
1785	8.57	–35.82	4.65	7.95

Z_{in} represents the input impedance of the device.
Z_{OL}^* represents the conjugate of the optimum output load to present to the device.

Table 2. Optimum Loads Derived from Circuit Characterization – PCS Band

f	Z_{in} OHMS		Z_{OL}^* OHMS	
MHz	R	jX	R	jX
1850	3.97	–39.68	7.49	3.07
1860	3.94	–40.31	7.42	2.81
1870	4.09	–40.65	7.38	2.51
1880	4.04	–40.92	7.31	2.28
1890	4.18	–41.21	7.28	2.02
1900	4.27	–41.48	7.28	1.73
1910	4.26	–41.71	7.23	1.56

Z_{in} represents the input impedance of the device.
Z_{OL}^* represents the conjugate of the optimum output load to present to the device.

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1817 is a 3–stage integrated power amplifier designed for use in cellular phones, especially for those used in DCS1800 (PCN) 3.6 V operation. With matching circuit modifications, it is also applicable for use in DCS1900 (PCS) equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off–chip, the device can be tuned to operate anywhere within the 1500 to 2000 MHz frequency range. Typical performance at different battery voltages is:

- 33.5 dBm @ 3.6 V
- 32.0 dBm @ 3 V

This capability makes the MRFIC1817 suitable for portable cellular applications such as:

- 3 V and 3.6 V DCS1800 Class I and II
- 3 V and 3.6 V PCS tag5

RF Circuit Considerations

The MRFIC1817 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical DCS1800 Class I applications circuit. The input match is a shunt–L, series–C, high–pass structure and can be retuned as desired with the only limitation being the on–chip 6 pF blocking capacitor. For saturated applications such as DCS1800 and PCS1900, the input match should be optimized at the rated RF input power. Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} and V_{D2} supply lines. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin. Output matching is accomplished with a low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through high Q capacitors mounted along a 50 Ω microstrip transmission line. Values and positions are chosen to present a 2 W loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. All components used in this application are low–Q commercial chip capacitors, except for the output load line. Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes under worst case conditions. The bias supply line which supplies the output should include an RF choke of at least 18 nH, surface mount solenoid inductors or quarter wave microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

Biasing Considerations

Gate bias lines are tied together and connected to the V_{SS} voltage, allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of all stage in the same time while saving some board space. For applications where the amplifier is operated close to saturation, such as with TDMA amplifiers, the gate bias can be set with resistors. Variations in process and tempera–ture will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 20 to 40 mA for the first stage, 150 to 300 mA for the second stage, and 400 to 800 mA for the final stage. For linear modes of operation which are required for CDMA amplifiers, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1 mA is required in the divider network so a DAC can be used as the voltage source.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_{D2}. This provides a very linear and repeatable power control transfer function. This technique can be used open loop to achieve 40–45 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for DCS1800 control where 30 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control. The transmit waveform ramping function required for systems such as DCS1800 can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for DCS1800, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power. For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC1817 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 ms before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

The MRFIC1817 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as DCS1800 where saturated amplifier operation is used.

For more information about the power control using the MC33169, refer to application note AN1599, "Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC."

Evaluation Boards

Two versions of the MRFIC1817 evaluation board are available. Order MRFIC1817DCSTF for the 1.8 GHz version and order MRFIC1817PCSTF for the 1.9 GHz version. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

1800 MHz GaAs Integrated Power Amplifier

MRFIC1818

1700–1900 MHz MMIC
DCS1800/PCS1900
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

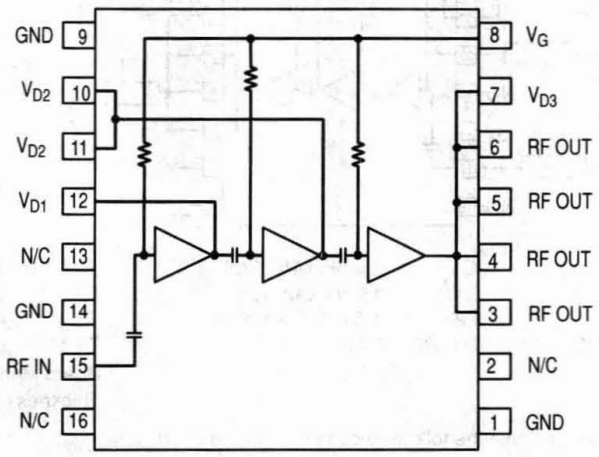
Designed specifically for application in Pan European digital 1.0 watt DCS1800 handheld radios, the MRFIC1818 is specified for 33 dBm output power with power gain over 30 dB from a 4.8 volt supply. With minor tuning changes, the MRFIC1818 can be used for PCS1900 as well as PCS CDMA. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal and electrical performance through a solderable backside contact while allowing the convenience and cost benefits of reflow soldering.

- Minimum Output Power Capabilities
  33 dBm @ 4.8 Volts
  32 dBm @ 4.0 Volts
- Specified 4.8 Volt Characteristics
  RF Input Power = 3.0 dBm
  RF Output Power = 33 dBm
  Minimum PAE = 35%
- Low Current required from Negative Supply – 2 mA max
- Guaranteed Stability and Ruggedness
- Order MRFIC1818R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1818

CASE 978–02
(PFP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Z_O = 50 Ω, unless otherwise noted)

Rating	Symbol	Value	Unit
DC Positive Supply Voltage	$V_{D1, 2, 3}$	7.5	Vdc
DC Negative Supply Voltage	V_{SS}	–5	Vdc
RF Input Power	P_{in}	10	dBm
RF Output Power	P_{out}	36	dBm
Operating Case Temperature Range	T_C	–35 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W



Pin Connections and Functional Block Diagram

REV 2

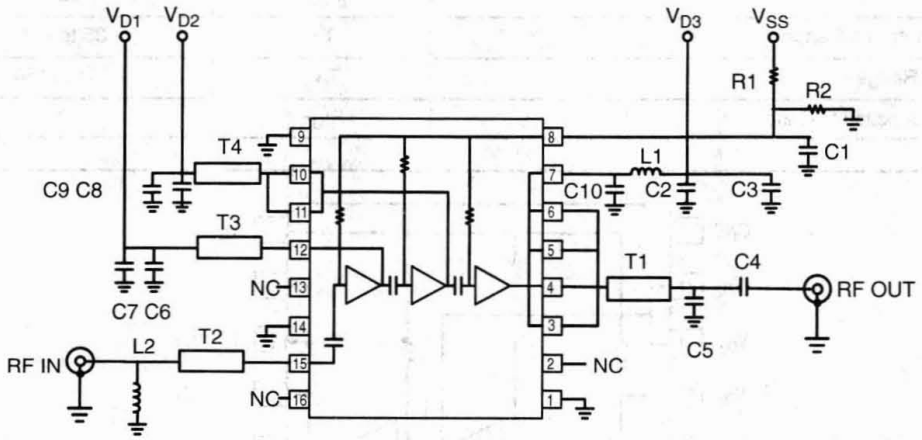
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{D1, 2, 3}$	2.7 to 6	Vdc
Gate Voltage	V_{SS}	–3.5 to –4.5	Vdc
RF Frequency Range	f_{RF}	1700 to 1900	MHz
RF Input Power	P_{RF}	0 to 6	dBm

ELECTRICAL CHARACTERISTICS ($V_{D1, 2, 3}$ = 4.8 V, V_{SS} = –4 V, P_{in} = 3 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	1710	—	1785	MHz
Output Power	33	34.5	—	dBm
Power Added Efficiency	35	42	—	%
Output Power (Tuned for PCS Band, 1850 to 1910 MHz)	—	34.5	—	dBm
Power Added Efficiency (Tuned for PCS Band, 1850 to 1910 MHz)	—	42	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output (2nd and 3rd)	—	–35	–30	dBc
Output Power at Low voltage (V_{D1}, V_{D2}, V_{D3}= 4.0 V)	32	33	—	dBm
Output Power, Isolation (V_{D1}, V_{D2}, V_{D3} = 0 V)	—	–40	–35	dBm
Noise Power (In 100 kHz, 1805 to 1880 MHz)	—	–85	–80	dBm
Stability – Spurious Output (P_{in} = 5 dBm, P_{out} = 0 to 33 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle) (1)	—	—	–60	dBc
Load Mismatch stress (P_{out} = 33 dBm, Load VSWR = 10:1 at any Phase Angle) (1)	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth	—	2	—	MHz
Negative Supply Current	—	0.7	2	mA

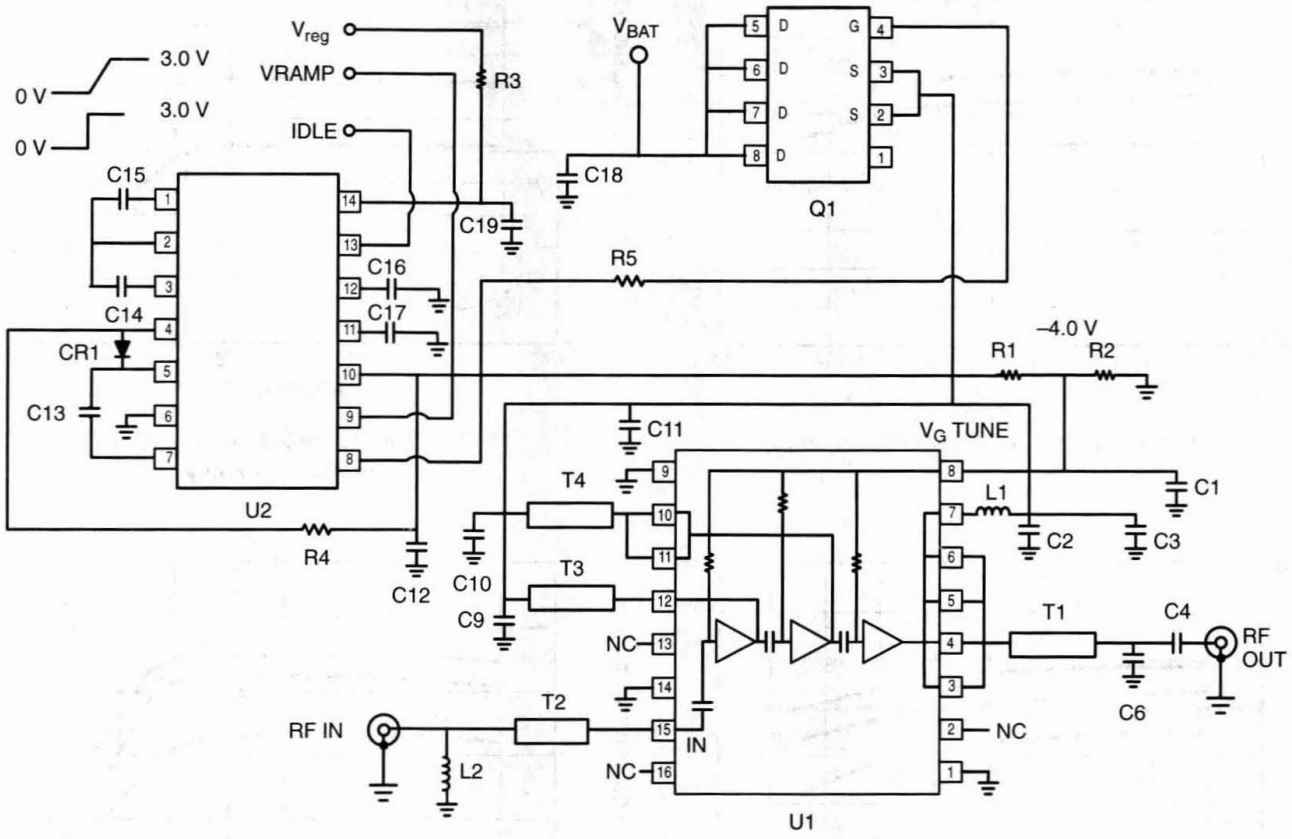
(1) Adjust $V_{D1, 2, 3}$ (0 to 4.8 V) for specified P_{out}; Duty Cycle = 12.5%, Period = 4.6 ms.



C1	6.8 nF	C5	3.9 pF, NPO/COG	T1	1.4 mm 25 Ω Microstrip Line
C2, C6, C8	22 pF, NPO/COG	L1	18 nH, Coilcraft	T2	5 mm 50 Ω Microstrip Line
C3, C7, C9	47 nF	L2	1.8 nH, Toko 2012	T3	4 mm 50 Ω Microstrip Line
C4	27 pF, NPO/COG	R1, R2 = 2.7 KΩ		T4	0.5 mm 50 Ω Microstrip Line
C10	0.5 pF			Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	

NOTE: For PCS/DCS1900 applications, the following components are used.
C5 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 1. Reference Circuit Configuration



C1	6.8 nF	C14, C15	1 μF	R3, R4	100 Ω
C2, C9, C10	22 pF, 0603 NPO/COG	C18	1 μF	R5	470 Ω
C3, C11	47 nF	CR1	MMBD701LT1	T1	2 mm 25 Ω Microstrip Line
C4	27 pF, 0603 NPO/COG	L1	18 nH, Coilcraft or 20 mm 50 Ω Microstrip Line	T2	5 mm 50 Ω Microstrip Line
C6	3.9 pF, 0603 NPO/COG	L2	1.8 nH, Toko 2012 or 5 mm 50 Ω Line	T3	8 mm 40 Ω Microstrip Line
C12	220 nF	Q1	MMSF4N01HD	T4	1 mm 40 Ω Microstrip Line
C13, C16, C17, C19	1 μF	R1, R2	2.7 kΩ	U1	MRFIC1818
				U2	MC33169 (–4 V Version)
				Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm	

NOTE: For PCS/DCS1900 applications, the following component values are changed.

C6 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 2. DCS1800 Applications Circuit Configuration

Typical Characteristics

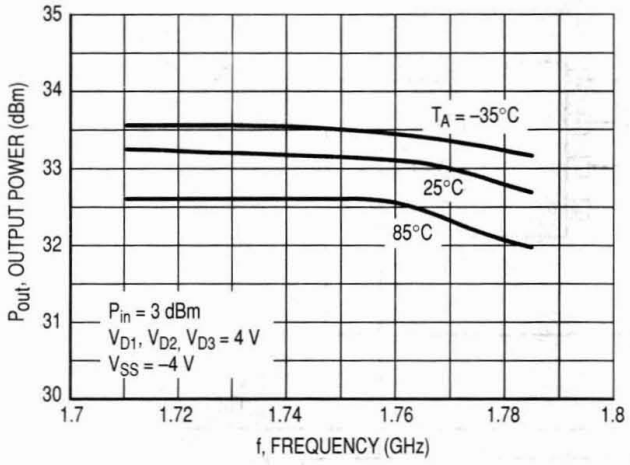


Figure 3. Output Power versus Frequency

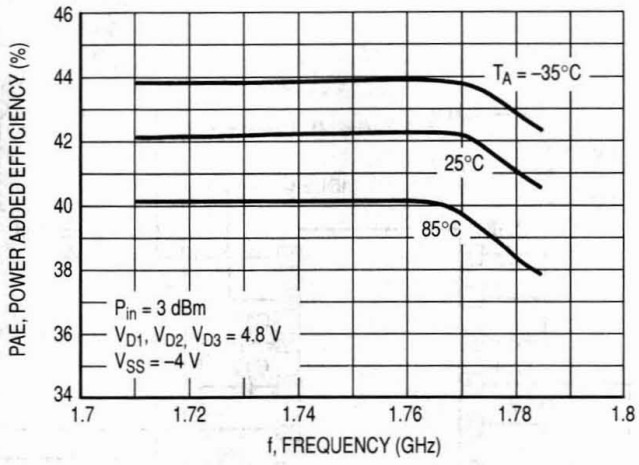


Figure 4. Power Added Efficiency versus Frequency

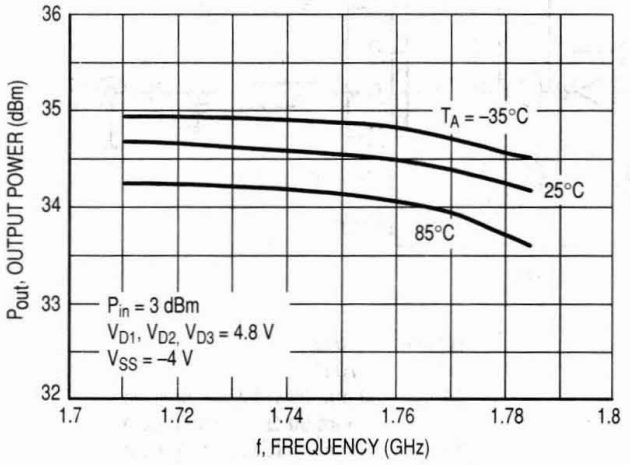


Figure 5. Output Power versus Frequency

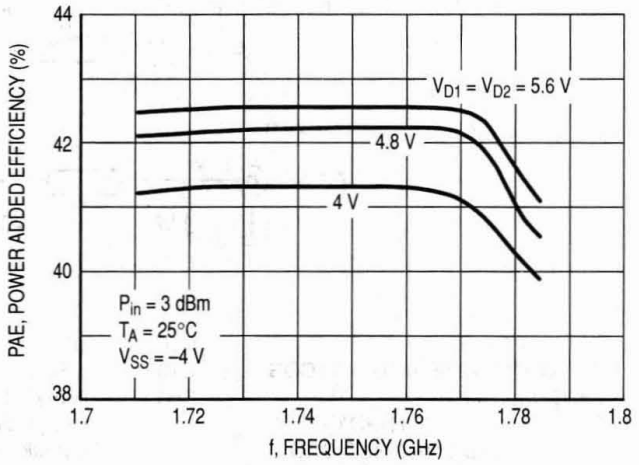


Figure 6. Power Added Efficiency versus Frequency

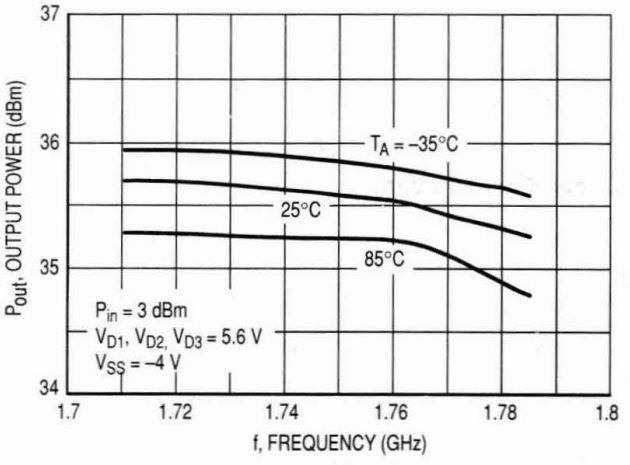


Figure 7. Output Power versus Frequency

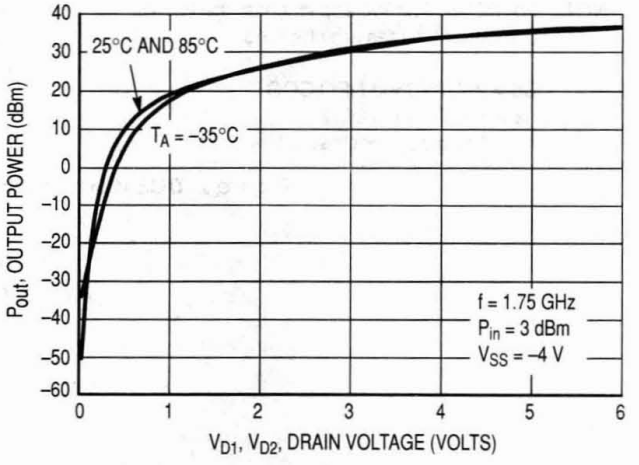


Figure 8. Output Power versus Drain Voltage

Typical Characteristics

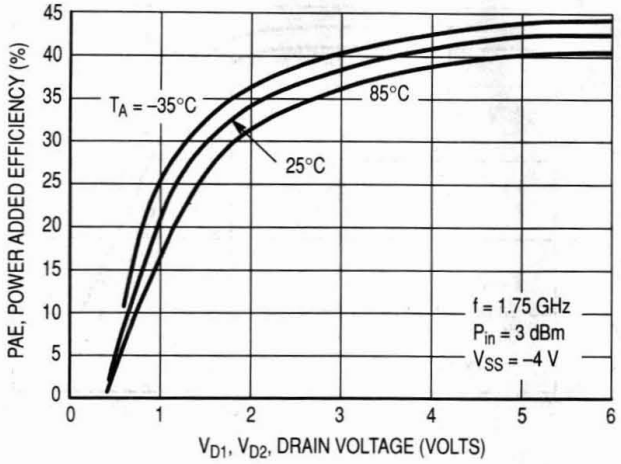


Figure 9. Power Added Efficiency versus Drain Voltage

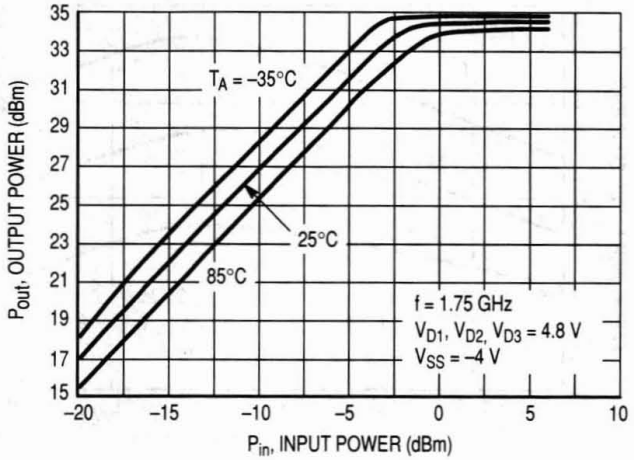


Figure 10. Output Power versus Input Power

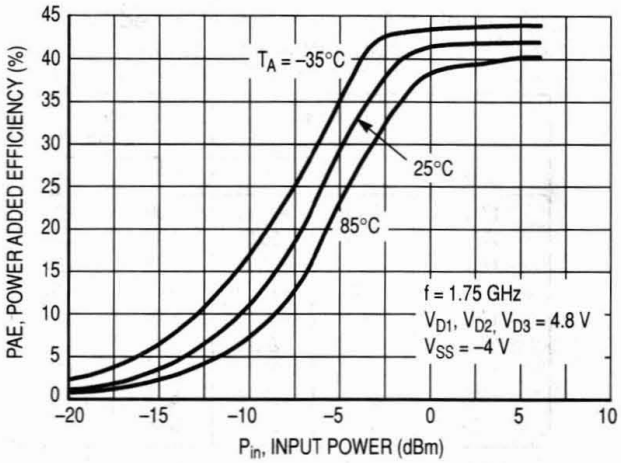


Figure 11. Power Added Efficiency versus Input Power

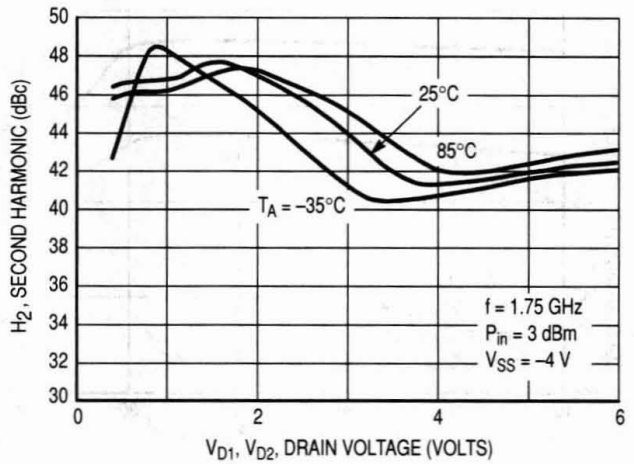


Figure 12. Second Harmonic versus Drain Voltage

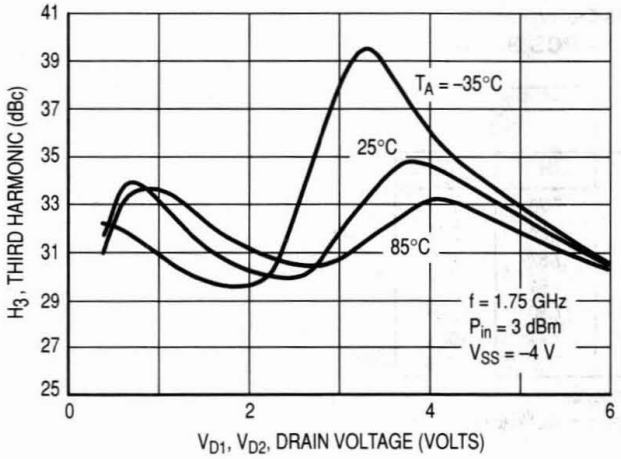


Figure 13. Third Harmonic versus Drain Voltage

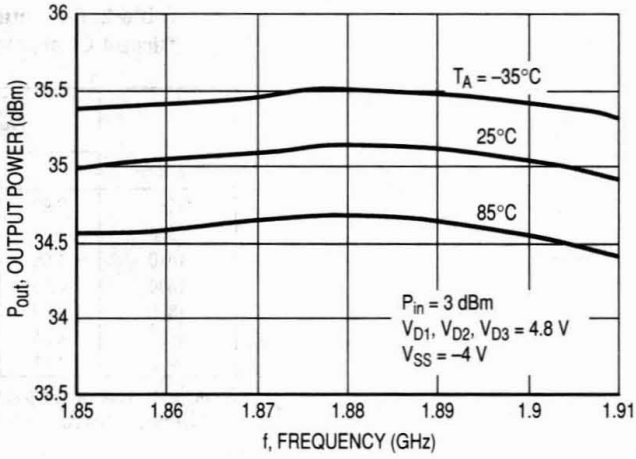


Figure 14. Output Power Versus Frequency – PCS Band

Typical Characteristics

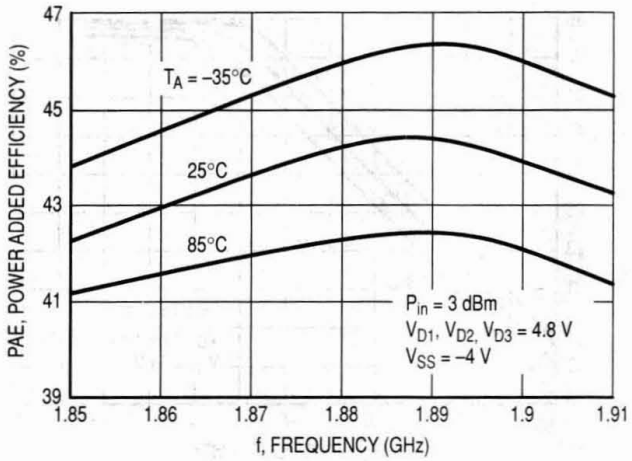


Figure 15. Power Added Efficiency versus Frequency – PCS Band

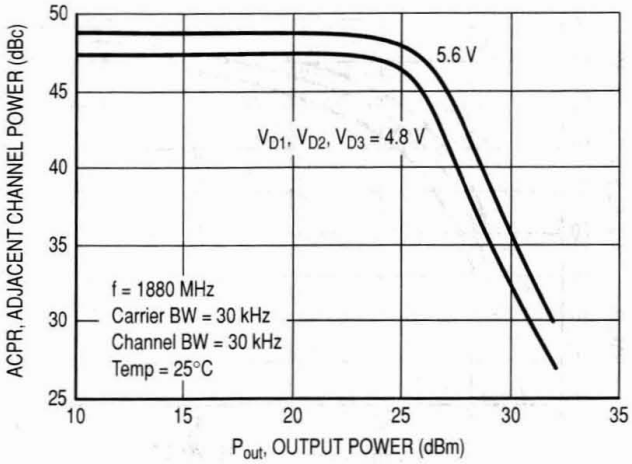


Figure 16. CDMA ACPR at 885 kHz Offset versus Output Power

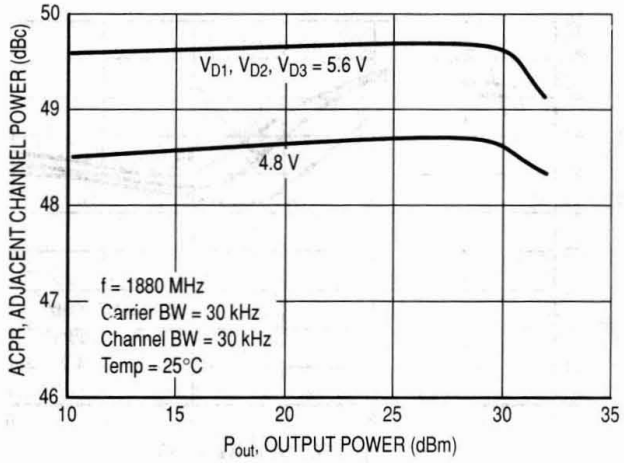


Figure 17. CDMA ACPR at 1980 kHz Offset versus Output Power

Table 1. Optimum Loads Derived from Circuit Characterization

f MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	R	jX	R	jX
1710	9.19	−30.10	6.00	3.80
1720	9.35	−29.60	5.96	3.71
1730	9.50	−29.30	5.88	3.60
1740	9.65	−29.10	5.80	3.46
1750	9.60	−29.00	5.75	3.33
1760	9.42	−28.79	5.67	3.20
1770	9.11	−28.60	5.60	3.07
1780	8.77	−28.30	5.51	2.93
1785	8.54	−28.15	5.45	2.79

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Table 2. Optimum Loads Derived from Circuit Characterization – PCS Board

f MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	R	jX	R	jX
1850	3.92	−43.30	7.70	0.39
1860	4.01	−43.56	7.64	0.23
1870	4.08	−43.78	7.57	0.15
1880	4.19	−44.00	7.51	0.07
1890	4.29	−44.29	7.50	−0.04
1900	4.31	−44.49	7.44	−0.06
1910	4.37	−44.81	7.35	−0.19

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1818 is a 3–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in DCS1800 (PCN) 4.8 V operation. With matching circuit modifications, it is also applicable for use in DCS1900 (PCS) equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 1500 to 2000 MHz frequency range. Typical performance at different battery voltages is:

- 36 dBm @ 6.0 V
- 34.5 dBm @ 4.8 V
- 32.0 dBm @ 3.6 V

This capability makes the MRFIC1818 suitable for portable cellular applications such as:

- 6V and 4.8 V DCS1800 Class I
- 6V and 4.8 V PCS tag5
- 3.6 V DCS1800 Class II

RF Circuit Considerations

The MRFIC1818 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical DCS1800 Class I applications circuit. The input match is a shunt–L, series–C, High–pass structure and can be retuned as desired with the only limitation being the on–chip 6 pF blocking capacitor. For saturated applications such as DCS1800 and DCS1900, the input match should be optimized at the rated RF input power. Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} and V_{D2} supply lines. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the in–ductance of the device's wirebonds and leadframe pin. Output matching is accomplished with a one–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50 Ω microstrip transmission line. Values and positions are chosen to present a 2.5 W loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. Low–Q commercial chip capacitors are used for the shunt capacitors, as shown in Figure 2. Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes under worst case conditions. The bias supply line which supplies the output should include an RF choke of at least 18 nH, surface mount solenoid inductors or quarter wave microstrip lines. Discrete inductors will usually give better efficiency and conserve board space. The DC blocking capacitor required at the output of the device is best mounted at the 50 Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Biasing Considerations

Gate bias lines are tied together and connected to the V_{SS} voltage, allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of all stage in the same time while saving some board space. For applications where the amplifier is operated close to saturation, such as TDMA amplifiers, the gate bias can be set with resistors. Variations in process and tempera–ture will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quies–cent currents of 20 to 40 mA for the first stage, 150 to 300 for the second stage and 400 to 800 mA for the final stage. For linear modes of operation which are required for CDMA amplifiers, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1 mA is required in the divider network so a DAC can be used as the voltage source.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_{D2}. This provides a very linear and repeatable power control transfer function. This technique can be used open loop to achieve 40–45 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for DCS1800 control where 30 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control. The transmit waveform ramping function required for systems such as DCS1800 can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for DCS1800, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power. For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC1818 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

The MRFIC1818 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as DCS1800 where saturated amplifier operation is used.

For more information about the power control using the MC33169, refer to application note AN1599, "Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC."

Evaluation Boards

Two versions of the MRFIC1818 evaluation board are available. Order MRFIC1818DCSTF for the 1.8 GHz version and order MRFIC1818PCSTF for the 1.9 GHz version. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

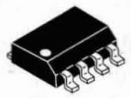
900 MHz Downconverter (LNA/Mixer)

MRFIC2001

900 MHz
DOWNCONVERTER
LNA/MIXER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

The MRFIC2001 is an integrated downconverter designed for receivers operating in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2001 include CT-1 and CT-2 cordless telephones, remote controls, video and audio short range links, low cost cellular radios, and ISM band receivers. A power down control is provided to minimize current drain with minimum recovery/turn-on time.

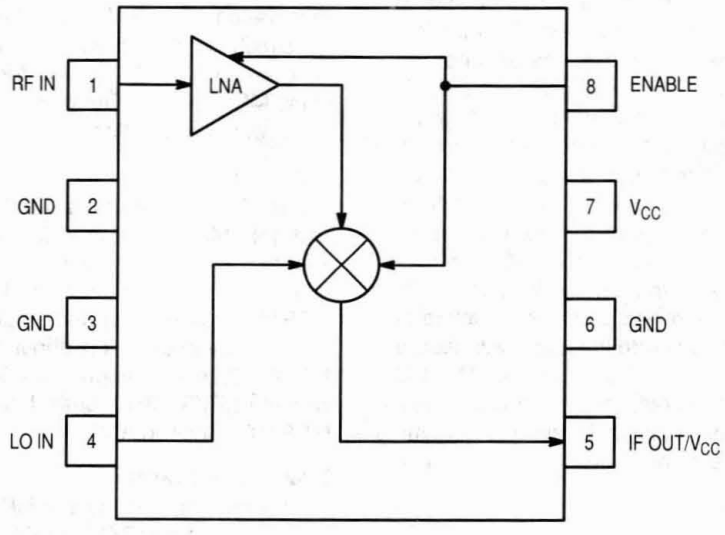
- Conversion Gain = 23 dB (Typ)
- Supply Current = 4.7 mA (Typ)
- Power Down Supply Current = 2.0 μA (Max)
- Low LO Drive = –10 dBm (Typ)
- LO Impedance Insensitive to Power Down
- No Image Filtering Required
- No Matching Required for RF IN Port
- All Ports are Single Ended
- Order MRFIC2001R2 for Tape and Reel.
  R2 suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2001



CASE 751-06
(SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.5	Vdc
Control Voltage	ENABLE	5.0	Vdc
Input Power, RF and LO Ports	P_{RF}, P_{LO}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C



Pin Connections and Functional Block Diagram

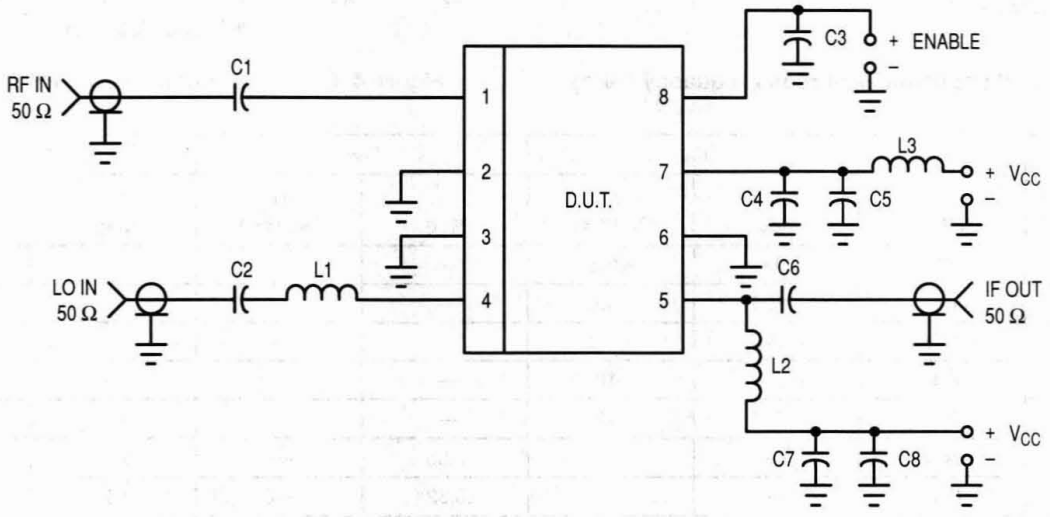
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	2.7 to 5.0	Vdc
Control Voltage Range	ENABLE	0 to 5.0	Vdc
RF Port Frequency Range	f_{RF}	500 to 1000	MHz
IF Port Frequency Range	f_{IF}	0 (dc) to 250	MHz

ELECTRICAL CHARACTERISTICS (V_{CC}, ENABLE = 3.0 V, T_A = 25°C, RF @ 900 MHz, LO @ 1.0 GHz, P_{LO} = –7.0 dBm, IF @ 100 MHz unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Supply Current: On-Mode	—	4.7	5.5	mA
Supply Current: Off-Mode (ENABLE < 1.0 Volts)	—	0.1	2.0	μA
ENABLE Response Time	—	1.0	—	μs
Conversion Gain	20	23	26	dB
Input Return Loss (RF IN Port)	—	13	—	dB
Single Sideband Noise Figure	—	5.5	—	dB
Input 3rd Order Intercept Point	– 26	– 22.5	—	dBm
Output Power at 1.0 dB Gain Compression	—	–10	—	dBm
LO – RF Isolation (1.0 GHz)	—	37	—	dB
LO – IF Isolation (1.0 GHz)	—	33	—	dB
RF – IF Isolation (900 MHz)	—	4.0	—	dB
RF – LO Isolation (900 MHz)	—	19	—	dB

NOTE:
1. All Electrical Characteristics measured in test circuit schematic shown in Figure 1 below:



C1, C2, C4, C7 — 100 pF Chip Capacitor
C3, C5, C8 — 1000 pF Chip Capacitor
C6 — 6.8 pF Chip Capacitor
L1 — 8.2 nH Chip Inductor
L2 — 270 nH Chip Inductor

L3 — 150 nH Chip Inductor
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Test Circuit Configuration

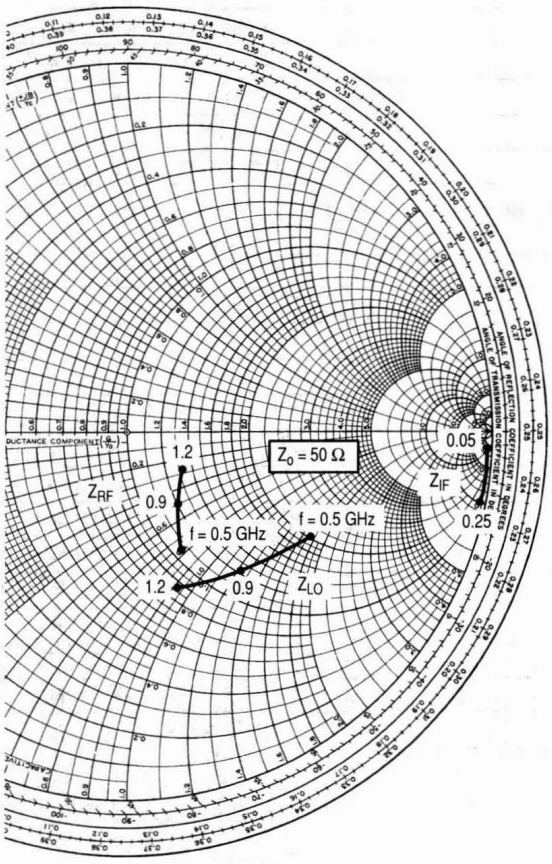


Figure 2. Port Impedances versus Frequency (GHz)

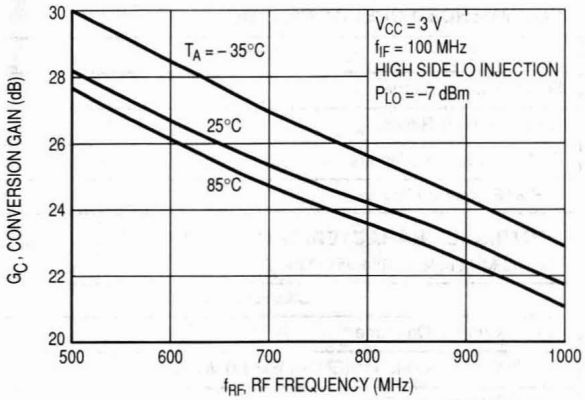


Figure 3. Conversion Gain versus RF Frequency

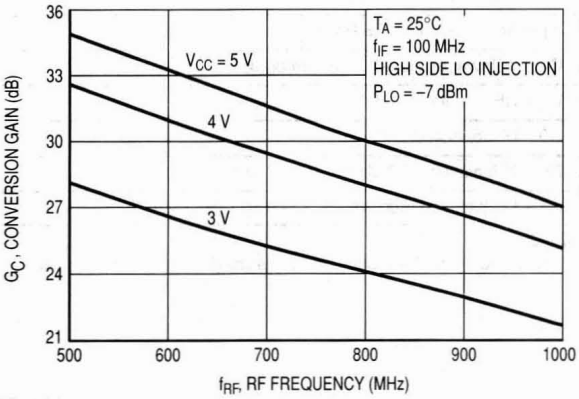


Figure 4. Conversion Gain versus RF Frequency

V_{CC} (Volts)	f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
		Mag	∠ϕ Degrees	Mag	∠ϕ Degrees	Mag	∠ϕ Degrees
3.0	50	0.998	− 2.5	—	—	—	—
	100	0.996	− 4.9	—	—	—	—
	150	0.993	− 7.2	—	—	—	—
	200	0.990	−10	—	—	—	—
	250	0.987	−12	—	—	—	—
	500	—	—	0.36	−70	0.58	− 31
	600	—	—	0.32	−70	0.55	− 36
	700	—	—	0.29	− 69	0.53	− 42
	800	—	—	0.26	− 68	0.51	− 48
	900	—	—	0.23	− 63	0.50	− 54
	1000	—	—	0.20	− 58	0.49	− 61
	1100	—	—	0.18	− 51	0.47	− 68
	1200	—	—	0.17	− 44	0.45	− 76

Table 1. Port Reflection Coefficients
(ENABLE = 3.0 V, Z_o = 50 Ω, T_A = 25°C)

TYPICAL CHARACTERISTICS

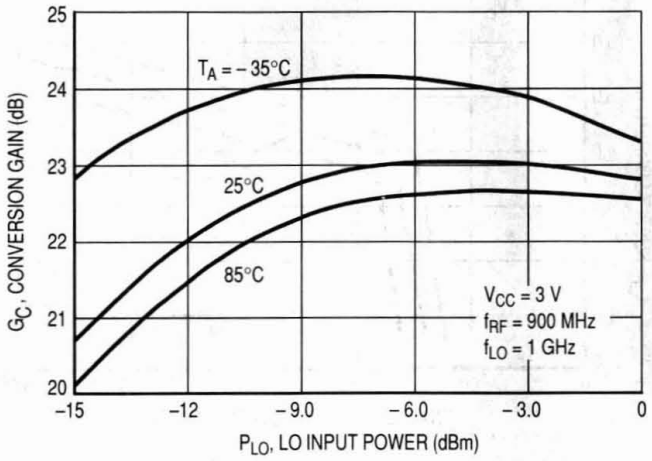


Figure 5. Conversion Gain versus LO Input Power

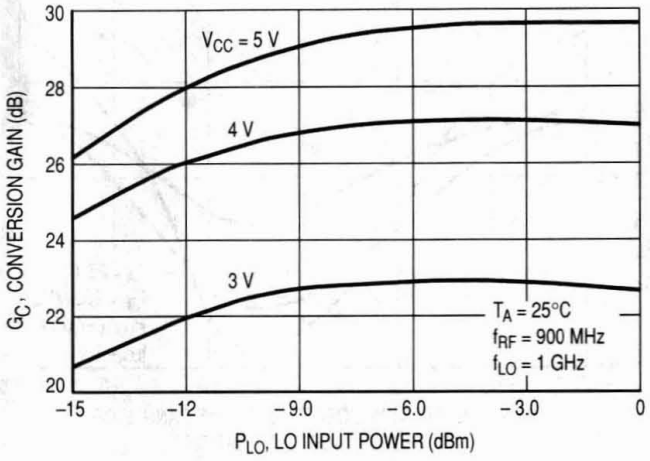


Figure 6. Conversion Gain versus LO Input Power

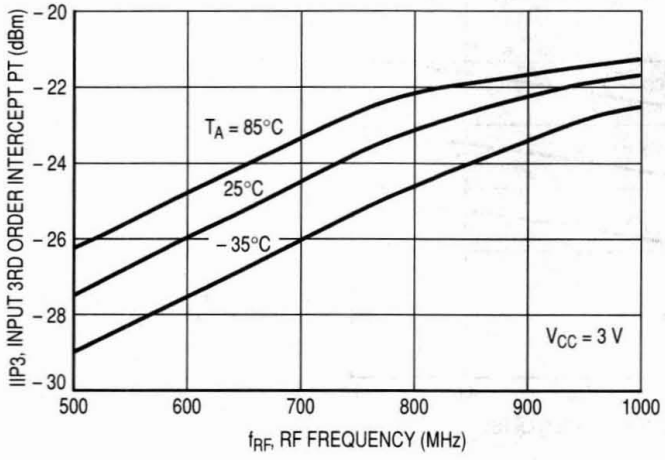


Figure 7. Input Third Order Intercept Point versus RF Frequency

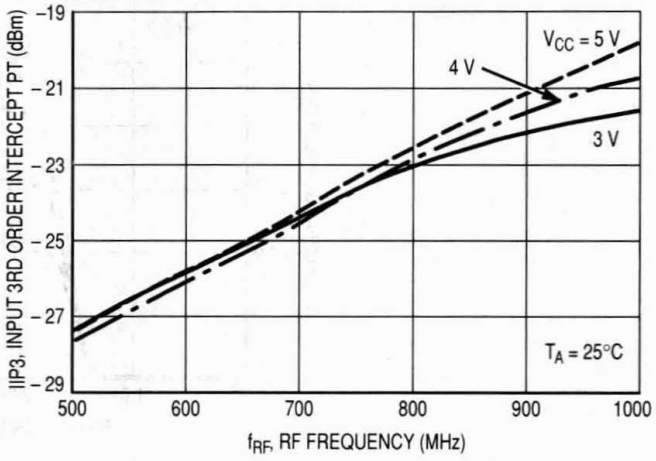


Figure 8. Input Third Order Intercept Point versus RF Frequency

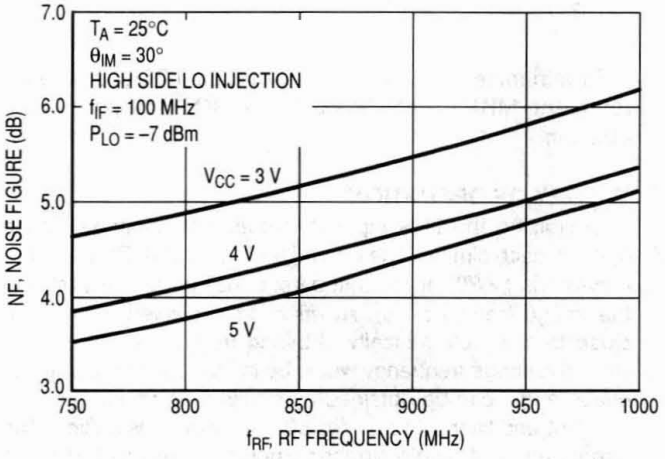


Figure 9. Noise Figure versus RF Frequency

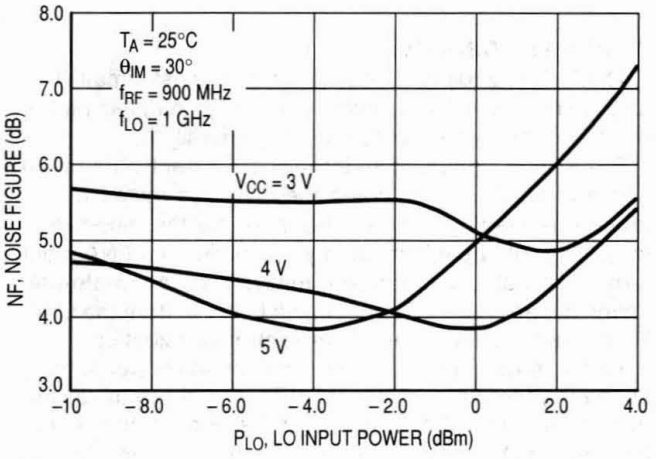


Figure 10. Noise Figure versus LO Input Power

TYPICAL CHARACTERISTICS

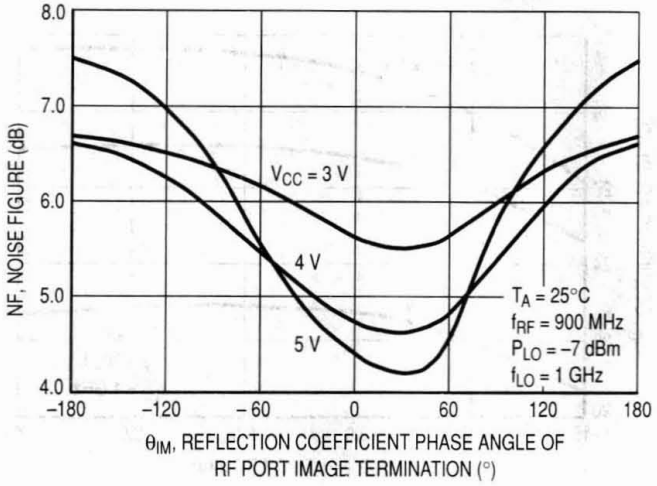


Figure 11. Noise Figure versus Reflection Coefficient Phase Angle of RF Port Image Termination

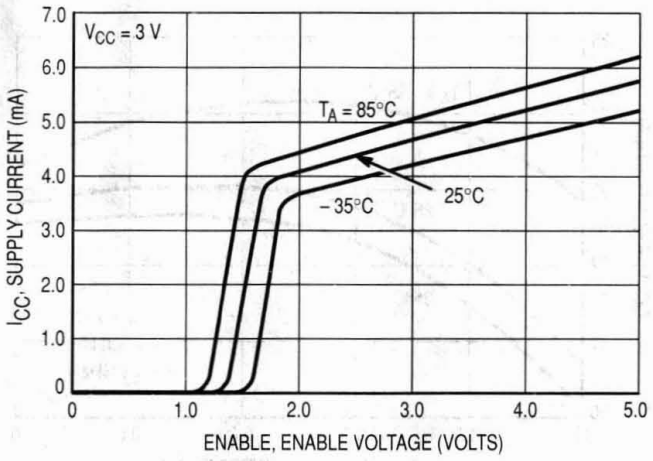


Figure 12. Supply Current versus Enable Voltage

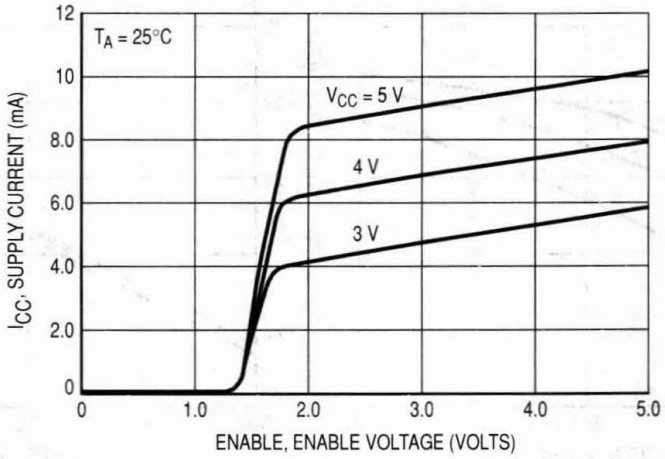


Figure 13. Supply Current versus Enable Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2001 was designed for low cost, small size, and ease of use. This is accomplished by minimizing the number of necessary external components.

The most significant external component eliminated was an image filter between the LNA and mixer. It was found the ensuing image noise entering the mixer from the LNA could be minimized by optimizing the LNA input termination at the image frequency. Also, a double-balanced mixer was used to reject the IF noise from the LNA. This results in excellent LO and spurious rejection.

To eliminate the need for external baluns or decoupling elements, the unused LO and RF ports of the mixer are decoupled internally. Only one of the IF outputs is used, eliminating the need for an external balun on the IF port as well. Also, the LNA input is matched to 50 ohms internally. External matching is required for the LO and IF ports.

To minimize current drain in various TDD/TDMA systems, the MRFIC2001 has a TTL/CMOS compatible enable pin.

THEORY OF OPERATION

Optimizing the LNA input termination to minimize image noise is quite simple. The optimum LNA input (RF IN pin) termination is $1\angle 30°$ at the image frequency (regardless of what the image frequency is). A reflection coefficient magnitude close to 1 is automatically obtained from a front-end filter, since the image frequency would be in the stop-band. The 30° phase angle can be obtained by rotating the phase angle of the front-end filter with a series 50 ohm transmission line. The dependance of single-sideband noise figure on the image phase angle is shown in Figure 11. As the plot indicates, there is a little over 1.0 dB of variation across all possible phase angles for a 3.0 V supply. Therefore, setting the phase angle is not critical. At higher supply voltages setting the phase angle is more critical (and more rewarding).

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8–15 nH depending on LO frequency) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since this will prevent the inductor from being close enough to the IC to provide a good match.

The IF port is an open collector resulting in a very high output impedance. For optimum linearity (IP3), the IF port should be loaded with a 1000 ohm load-line. Since the output requires a bias inductor and blocking capacitor, the IF filter impedance can be transformed to 1000 ohms with these two elements. If a low output VSWR is desired (to reduce IF filter ripple), a 2.0–4.0 K ohm resistor can be placed in parallel with the bias inductor. This will reduce the conversion gain by 1.0–2.0 dB.

The RF port is nearly 55 ohms resistive in series with a small amount of capacitive reactance, which results in a 12–13 dB return loss. If a higher return loss is desired, a 3.0–4.0 nH series inductor printed on the board as close to the IC as possible will improve it to over 20 dB. A DC block is also required.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the LO signal off the supply line.

Enabling/Disabling the MRFIC2001 can be done with its TTL/CMOS compatible Enable pin. The trip point is between 1.0 and 2.0 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

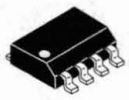
The MRFIC Line
900 MHz Transmit Mixer

MRFIC2002

900 MHz TX-MIXER SILICON MONOLITHIC INTEGRATED CIRCUIT

The MRFIC2002 is a double-balanced, active mixer designed for transmitters operating in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2002 include CT1 and CT2 cordless telephones, GSM, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters. A power down control is provided to minimize current drain with minimum recovery/turn-on time.

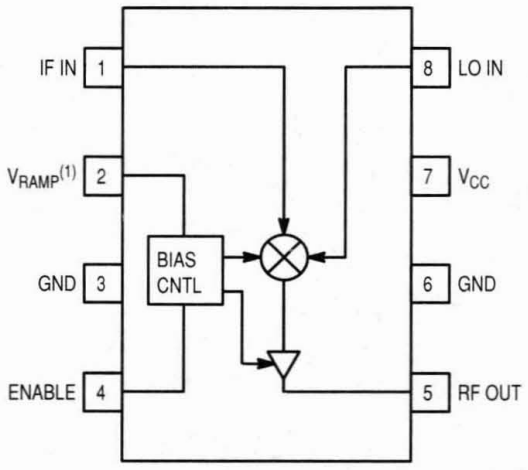
- Conversion Gain = 10 dB (Typ)
- Supply Current = 5.5 mA (Typ)
- Power Down Supply Current = 2.0 μA (Max)
- LO-RF Isolation = 25 dB (Typ)
- Low LO Drive Required = –10 dBm (Typ)
- LO Impedance Insensitive to Power Down
- No Matching Required for RF OUT Port
- All Ports are Single Ended
- Order MRFIC2002R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2002



CASE 751-06
(SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.5	Vdc
Control Voltages	ENABLE, V_{RAMP}	5.0	Vdc
Input Power, LO and IF Ports	P_{LO}, P_{IF}	+10	dBm
Operating Ambient Temperature	T_A	–35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C



(1) For CT2 applications, apply ramp voltage provided in MRFIC2004. For non-CT2, leave open circuited.

Pin Connections and Functional Block Diagram

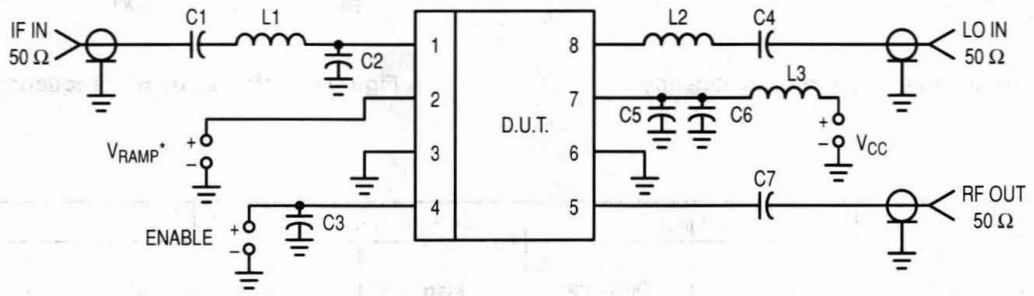
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	2.7 to 5.0	Vdc
Control Voltage Ranges	ENABLE, V_{RAMP}	0 to 5.0	Vdc
RF Port Frequency Range	f_{RF}	500 to 1000	MHz
IF Port Frequency Range	f_{IF}	0 (dc) to 250	MHz

ELECTRICAL CHARACTERISTICS (V_{CC}, Enable = 3.0 V and V_{Ramp}(1) Open Circuited, P_{LO} = −7.0 dBm, IF @ 100 MHz, LO @ 1.0 GHz, RF @ 900 MHz, T_A = 25°C unless otherwise noted)

Characteristic (2)	Min	Typ	Max	Unit
Supply Current: On-Mode Supply Current: Off-Mode (Enable < 1.0 V)	— —	5.5 0.1	7.0 2.0	mA μA
Enable Response Time	—	1.0	—	μs
Conversion Gain	8.0	10	12	dB
Single Sideband Noise Figure	—	10	—	dB
Output Power at 1.0 dB Gain Compression	—	–18	—	dBm
Output Power at Saturation	–16	–14	—	dBm
LO-RF Isolation (1.0 GHz)	—	25	—	dB
LO-IF Isolation (1.0 GHz)	—	65	—	dB
IF-RF Isolation (100 MHz)	—	18	—	dB
IF-LO Isolation (100 MHz)	—	50	—	dB

NOTES:
1. For CT2 applications, apply ramp voltage provided in MRFIC2004. For non-CT2, leave open circuited.
2. All Electrical Characteristics are measured in test circuit schematic as shown in Figure 1.



C1, C3, C6 — 1000 pF Chip Capacitor
C2 — 6.8 pF Chip Capacitor
C4 — 3.9 pF Chip Capacitor
C5 — 100 pF Chip Capacitor
C7 — 5.6 pF Chip Capacitor
L1 — 270 nH Chip Inductor
L2 — 10 nH Chip Inductor
L3 — 390 nH Chip Inductor
RF Connectors — SMA Type
Board Material — Glass/Epoxy ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Test Circuit Configuration

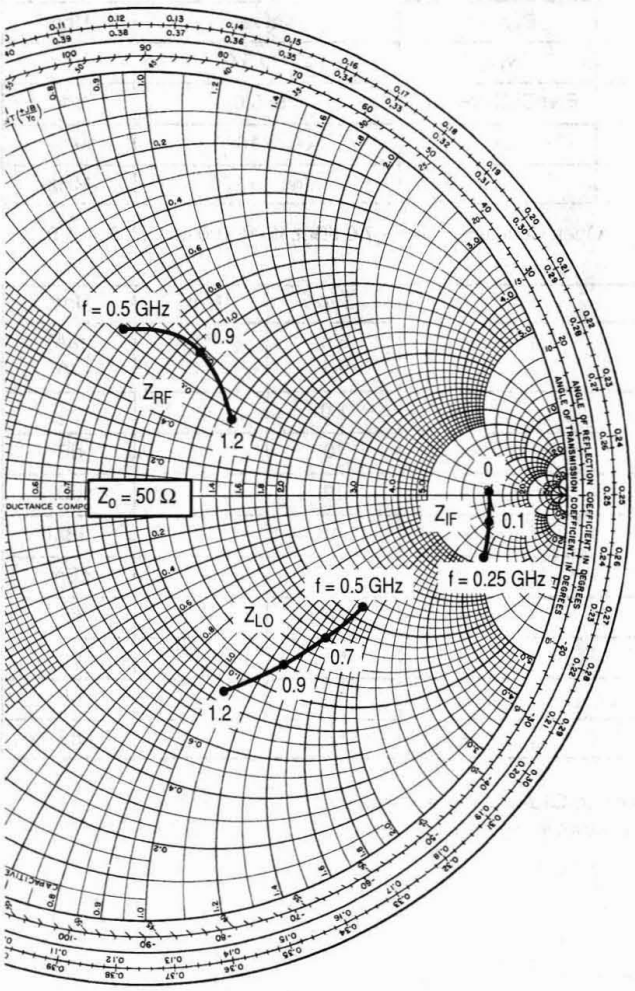


Figure 2. Port Impedances versus Frequency

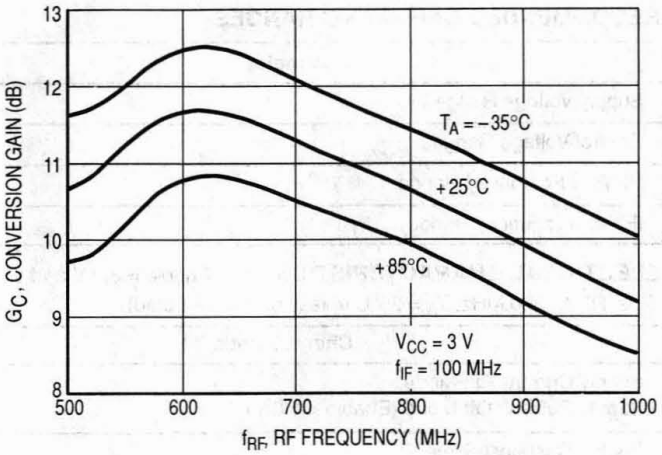


Figure 3. Gain versus RF Frequency

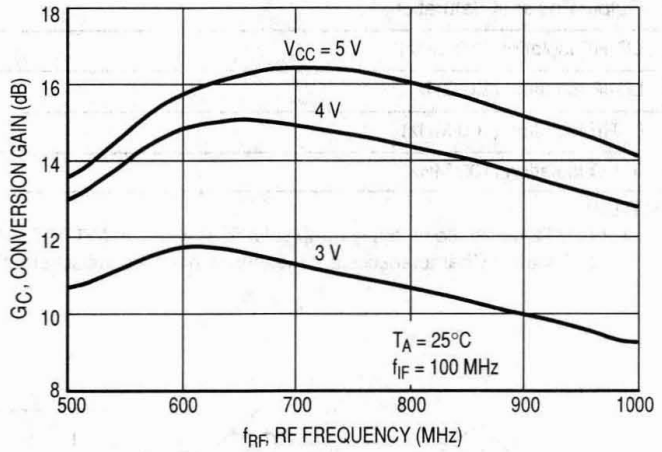


Figure 4. Gain versus RF Frequency

V_{CC} (Volts)	f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
		Mag	∠ϕ Degrees	Mag	∠ϕ Degrees	Mag	∠ϕ Degrees
3.0	50	0.83	−2.4	—	—	—	—
	100	0.82	−4.7	—	—	—	—
	150	0.82	−7.1	—	—	—	—
	200	0.81	−9.6	—	—	—	—
	250	0.81	−11.7	—	—	—	—
	500	—	—	0.42	100	0.57	−29
	600	—	—	0.41	94	0.55	−35
	700	—	—	0.40	88	0.54	−41
	800	—	—	0.39	80	0.52	−48
	900	—	—	0.36	71	0.51	−54
	1000	—	—	0.33	63	0.50	−60
	1100	—	—	0.31	55	0.49	−65
	1200	—	—	0.28	45	0.49	−70

Table 1. Deembedded Port Reflection Coefficients
(Enable = 3.0 V, Z_o = 50 Ω, T_A = 25°C)

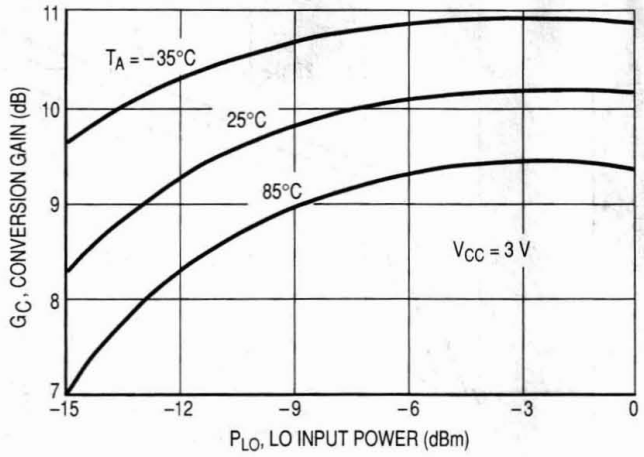


Figure 5. Gain versus LO Input Power

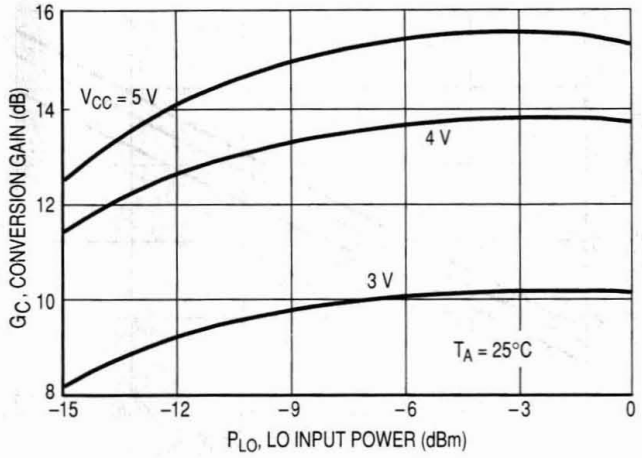


Figure 6. Gain versus LO Input Power

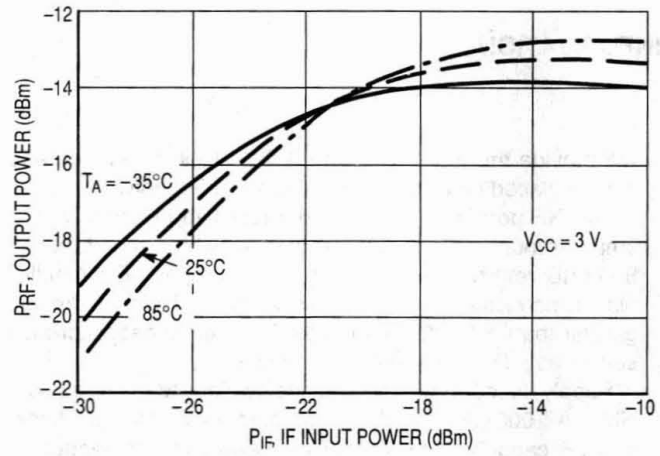


Figure 7. Output Power versus IF Input Power

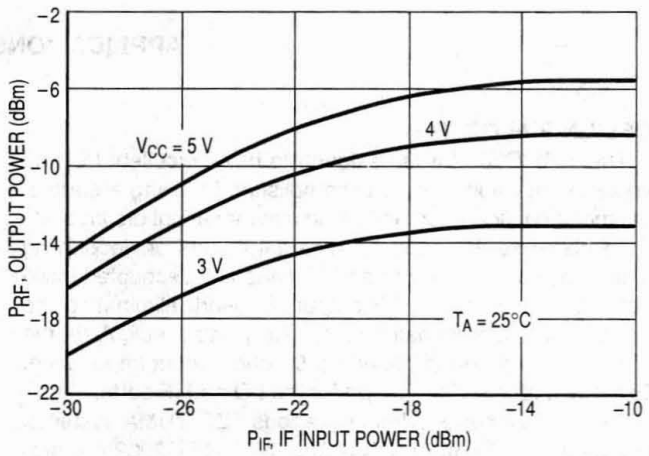


Figure 8. Output Power versus IF Input Power

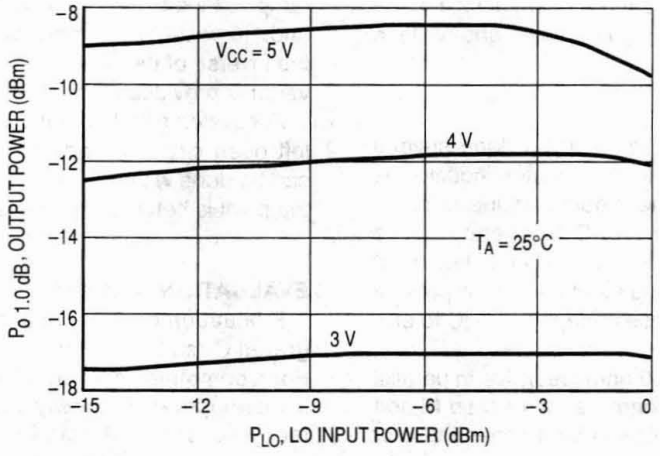


Figure 9. Output Power at 1.0 dB Gain Compression versus LO Input Power

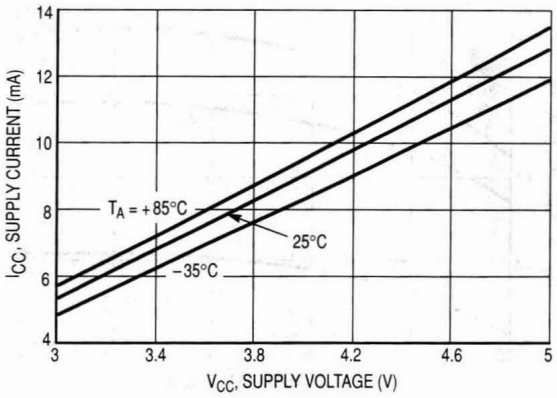


Figure 10. I_{CC} versus V_{CC}

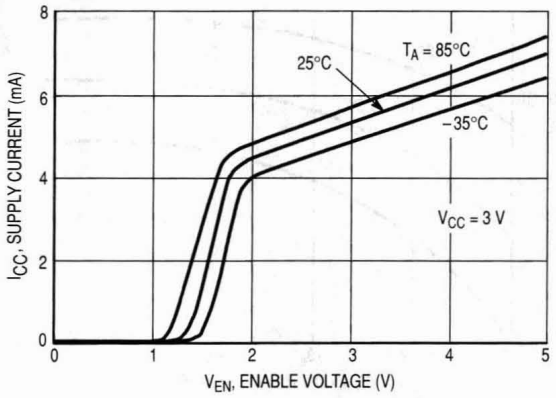


Figure 11. I_{CC} versus Enable Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2002 was designed to have excellent LO and spurious rejection. This is accomplished by using a double-balanced configuration and using a symmetrical die layout.

To eliminate the need for external baluns or decoupling elements, the unused LO and IF ports are decoupled internally. Only one of the RF outputs is used, eliminating the need for an external balun on the RF port as well. Also, the RF port is buffered to provide a 50 ohm output impedance. External matching is required for the LO and IF ports.

To minimize current drain in various TDD/TDMA systems, two methods of enabling/disabling the MRFIC2002 are provided: one that is TTL/CMOS compatible and one that is triggered from a ramp, such as the one provided in the MRFIC2004. The former method must be used if a ramp is not available. The latter method is more desirable since the MRFIC2002 can remain off during guard times and while in idle mode.

THEORY OF OPERATION

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8–15 nH depending on LO frequency) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since this will prevent the inductor from being placed close enough to the IC to provide a good match.

The IF port is approximately 500 ohms resistive in parallel with 1.3 pF of capacitance. If 50 ohms is the desired IF port impedance, a shunt capacitor followed by a series inductor will provide the transformation. A DC block is required and can be placed on either side of the matching network.

The RF port is nearly 50 ohms resistive in series with a small amount of inductive reactance, which results in an 8–11 dB return loss. However, a series 5.6 pF capacitor placed as close to the IC as possible will typically provide greater than a 15 dB return loss. The series capacitor also serves as a DC block which is required.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the RF and LO signals off the supply line.

For systems that use a ramp, like the one provided in the MRFIC2004, enabling/disabling can be done by applying the ramp voltage to the V_{RAMP} pin which trips the IC between 0.6 and 1.0 volts. The Enable pin must either be tied high or to the inverse of the receiver enable control line, $\overline{\text{RXEN}}$. An inverter is provided in the MRFIC2004 to invert RXEN.

For systems that do not use a ramp, the V_{RAMP} pin can be left open circuited and enabling/disabling the MRFIC2002 can be done with its TTL/CMOS compatible Enable pin. The trip point is between 1.0 and 2.0 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

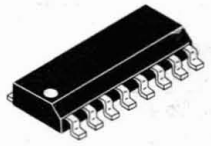
900 MHz Driver and Ramp

MRFIC2004

900 MHz DRIVER & RAMP SILICON MONOLITHIC INTEGRATED CIRCUIT

The MRFIC2004 is an integrated Driver and Ramp designed for transmitters operating in the 800 MHz to 1.0 GHz frequency range. The Ramp is an integrator which can be used for burst control for TDD/TDMA systems. The Driver uses a cascode configuration for high gain and reverse isolation. A power down control is provided to minimize current drain with minimum recovery/turn-on time. Also, an on-board inverter is included to provide complementary control for an antenna switch, such as the MRFIC2003. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2004 include CT1 and CT2 cordless telephones, GSM, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters.

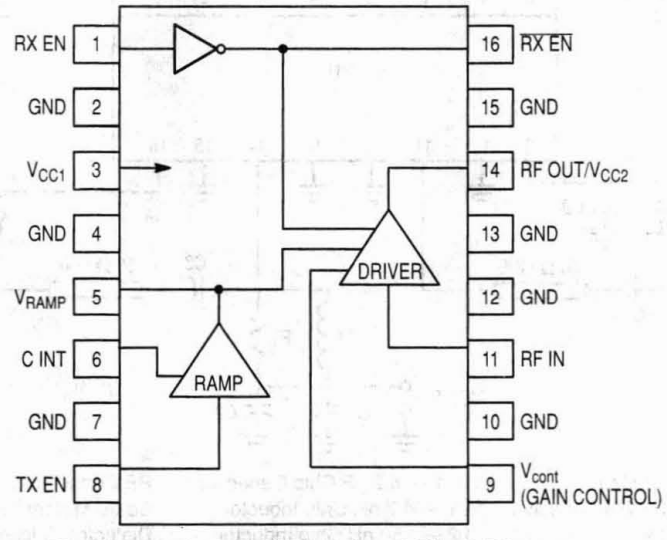
- Small Signal Gain = 21.5 dB (Typ)
- Small Signal Gain Control = 34 dB (Typ)
- $P_{o\ 1.0\ dB}$ = −1.0 dBm (Typ)
- On Board Ramp for Burst Control
- Power Down Supply Current = 0.7 mA (Typ)
- Low Operating Supply Voltage (2.7 to 4.0 Volts)
- Input/Output VSWR Insensitive to Gain Control
- Order MRFIC2004R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2004



CASE 751B-05
(SO-16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC1} V_{CC2}	4.5 6.0	Vdc
Control Voltages	RXEN, TXEN, V_{cont}	6.0	Vdc
Input Power, RF IN Port	P_{RF}	+10	dBm
Operating Ambient Temperature	T_A	−35 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C



Pin Connections and Functional Block Diagram

REV 2

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Ranges	V_{CC1}, V_{CC2}	2.7 to 4.0	Vdc
Control Voltage Ranges	TX EN, RX EN, V_{cont}	0 to V_{CC1}	Vdc
Frequency Range	f	800 to 1000	MHz

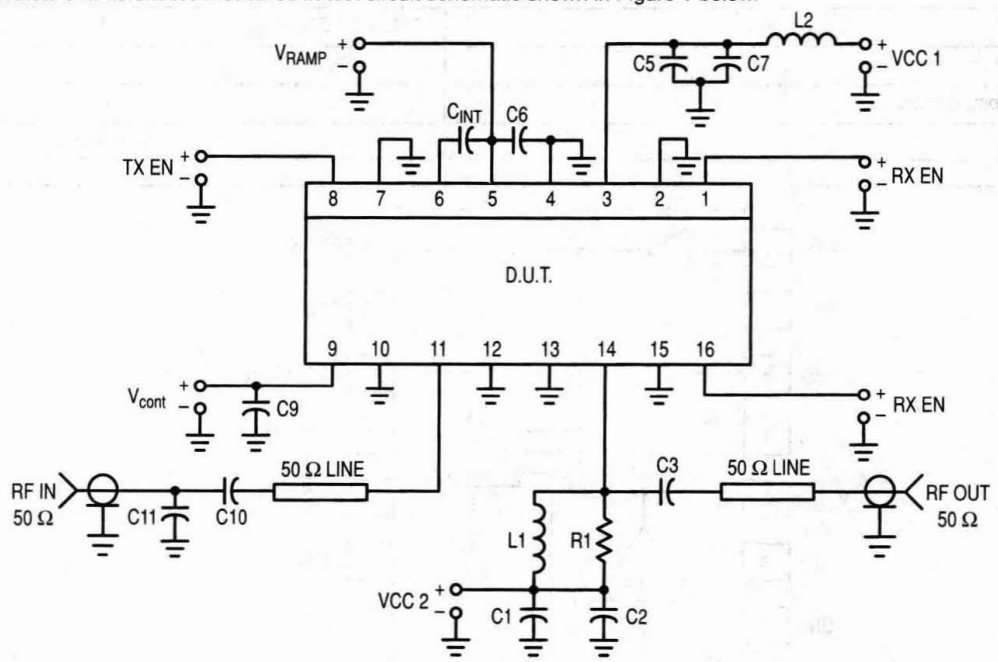
ELECTRICAL CHARACTERISTICS (V_{CC1}, V_{CC2} = 3.0 V, C_{INT} = 2.0 nF, T_A = 25°C, f = 900 MHz, V_{CONT} = 1.3 V)

Characteristics (1)	Min	Typ	Max	Unit
Supply Current, TX EN High, RX EN Low	—	11	13	mA
Supply Current, TX EN Low, RX EN High	—	0.7	1.5	mA
Driver Characteristics (1)				
Gain (Small Signal)	19	21.5	24	dB
Gain Control (Small Signal)	—	34	—	dB
Power Out @ 1.0 dB Gain Compression	−4.0	−1.0	—	dBm
Third Order Intercept Point (out)	—	+7.5	—	dBm
Reverse Isolation	—	32	—	dB
Ramp Characteristics (1)				
Ramp Up Delay Time	—	4.0	—	µs
Rise Time	—	18	—	
Total Time	—	22	—	
Ramp Down Delay Time	—	4.0	—	µs
Fall Time	—	18	—	
Total Time	—	22	—	

LOGIC LEVELS (V_{CC1} = 2.7 to 4.0 V, T_A = 25°C)

RX EN & TX EN Input Voltage	Min	Typ	Max	Unit
High	V_{CC1} − 0.8	—	—	V
Low	—	—	0.8	
$\overline{\text{RX EN}}$ Output Voltage				
High	V_{CC1} − 0.2	—	—	V
Low	—	—	0.2	

NOTE:
1. All electrical characteristics measured in test circuit schematic shown in Figure 1 below.



C1, C7, C9 — 1000 pF Chip Capacitor
C2, C5, C6, C10 — 100 pF Chip Capacitor
C3 — 1.6 pF Chip Capacitor
C_{INT} — 2000 pF Chip Capacitor
C11 — 6.2 pF Chip Capacitor
L1 — 4.7 nH Chip Inductor
L2 — 150 nH Chip Inductor
R1 — 330 Ω Chip Resistor
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Typical Biasing Configuration

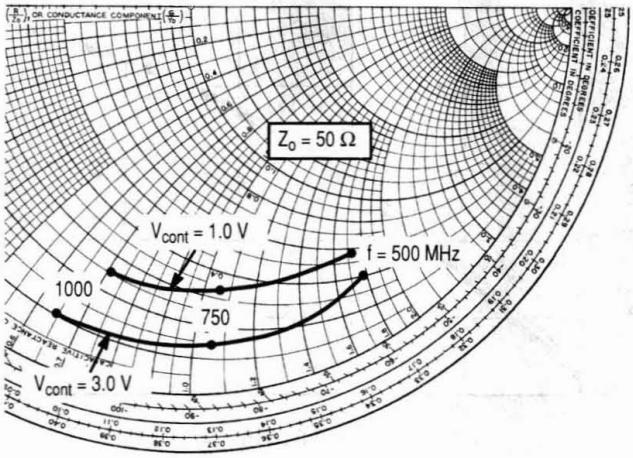


Figure 2. S_{11} versus Frequency versus V_{cont}

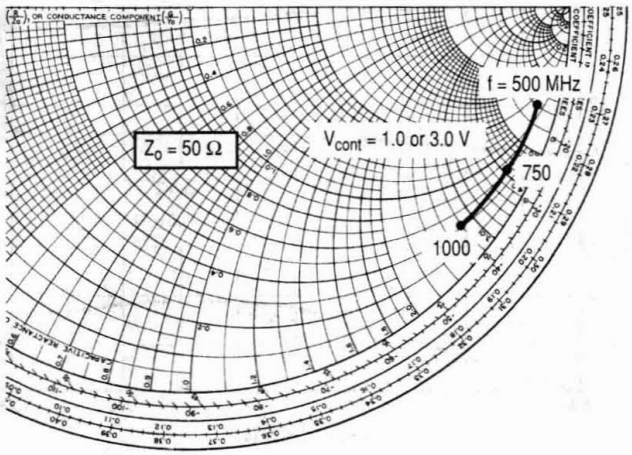


Figure 3. S_{22} versus Frequency

V_{cont}	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
		$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1.0	100	0.85	−11.3	10.48	171.5	0.0002	142.7	0.99	−2.9
	300	0.83	−32.8	10.33	156.3	0.0020	129.0	0.99	−7.3
	500	0.79	−56.9	10.15	140.5	0.0030	130.6	0.98	−15.9
	550	0.79	−62.5	10.04	135.9	0.0030	132.6	0.98	−17.9
	600	0.78	−68.5	9.85	130.2	0.0040	133.3	0.98	−20.0
	650	0.77	−74	9.47	126.9	0.0040	135.9	0.98	−22.3
	700	0.76	−79	9.23	123.6	0.0050	137.2	0.98	−24.7
	750	0.76	−84.4	9.02	119.4	0.0050	138.1	0.97	−27.0
	800	0.75	−89.6	8.69	113.8	0.0060	139.7	0.97	−29.3
	850	0.74	−94.5	8.33	110.8	0.0070	140.3	0.97	−31.4
	900	0.73	−99.1	8.13	108.9	0.0080	141.2	0.96	−33.2
	950	0.73	−102	7.98	105.4	0.0090	138.3	0.96	−36.3
	1000	0.72	−106.9	7.70	101.0	0.0100	133.7	0.95	−38.4
1.9	100	0.85	−11.3	0.53	−173.5	0.0002	104.3	0.99	−2.9
	300	0.86	−33.5	0.69	−169.7	0.0009	118.7	0.98	−8.7
	500	0.87	−59.3	0.89	−179.5	0.0010	134.3	0.98	−15.5
	550	0.87	−65.7	0.96	175.1	0.0020	136.3	0.98	−17.5
	600	0.88	−73.1	1.02	169.9	0.0020	138.9	0.97	−19.6
	650	0.88	−78.7	1.04	167.3	0.0020	142.6	0.97	−21.8
	700	0.88	−84.7	1.07	165.0	0.0030	147.8	0.97	−24.1
	750	0.89	−90.7	1.14	161.5	0.0030	153.4	0.96	−26.4
	800	0.89	−98.2	1.17	155.8	0.0040	161.0	0.96	−28.8
	850	0.88	−104.6	1.22	151.2	0.0050	161.8	0.96	−30.7
	900	0.87	−110.1	1.24	144.6	0.0060	162.7	0.95	32.8
	950	0.86	−114.6	1.26	139.9	0.0070	160.3	0.95	−35.1
	1000	0.85	−118.8	1.27	134.1	0.0080	158.2	0.94	−37.2
3.0	100	0.85	−10.9	0.003	−85.9	0.0001	115.0	0.99	−2.8
	300	0.86	−31.9	0.014	−78.8	0.0006	121.0	0.99	−8.5
	500	0.87	−56.9	0.032	−61.1	0.0010	128.0	0.98	−15.1
	550	0.88	−62.4	0.038	−65.8	0.0010	136.2	0.98	−17.0
	600	0.89	−69.4	0.048	−68.3	0.0010	140.0	0.98	−19.2
	650	0.90	−75.1	0.058	−75.1	0.0020	145.1	0.98	−21.3
	700	0.90	−81.3	0.069	−82.4	0.0020	150.8	0.97	−23.6
	750	0.91	−87.3	0.081	−89.4	0.0020	156.8	0.97	−25.8
	800	0.91	−93.8	0.092	−113.4	0.0030	160.3	0.97	−28.1
	850	0.92	−100.7	0.092	−121.8	0.0040	163.3	0.96	−30.1
	900	0.91	−106.8	0.089	−128.2	0.0050	163.3	0.96	−32.3
	950	0.90	−111.4	0.083	−137.1	0.0060	155.2	0.95	−34.5
	1000	0.89	−115.2	0.077	−151.9	0.0060	150.0	0.95	−36.6

Table 1. Small Signal Deembedded S Parameters

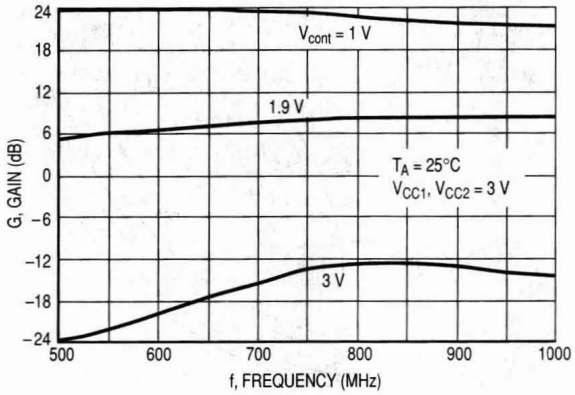


Figure 4. Small Signal Gain versus Frequency

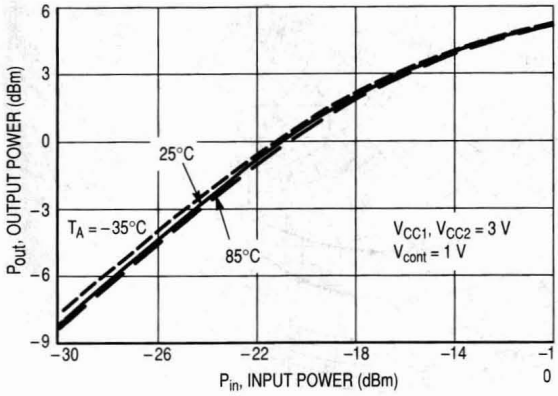


Figure 5. Output Power versus Input Power

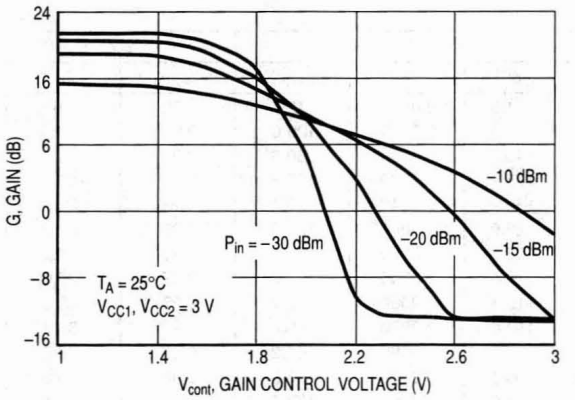


Figure 6. Driver Gain versus Gain Control Voltage

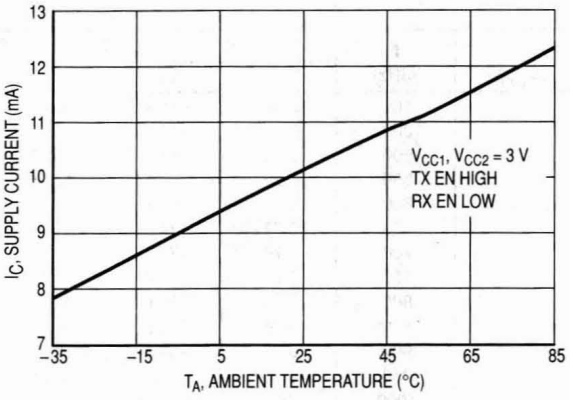


Figure 7. Supply Current versus Ambient Temperature

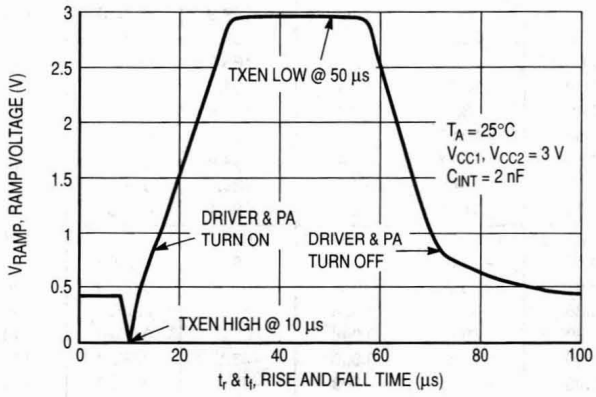


Figure 8. Ramp Voltage versus Rise & Fall Time

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2004 was designed as a support IC for a CT2 chip-set. The other chips making up the chip-set are the MRFIC2001 downconverter, the MRFIC2002 transmit mixer, the MRFIC2003 antenna switch and the MRFIC2006 PA. A complete CT2 front-end solution requires a ramp for burst control, an inverter for complementary antenna switch control and gain control (or an attenuator) for the transmitter low power mode. In order to keep the other chips in the chip-set relatively general purpose, yet provide the system designer with an easily controlled solution, these functions were combined with a driver amplifier into one IC, the MRFIC2004.

THEORY OF OPERATION

The driver is a cascode design that exits the IC open-collector. Impedance matching must be done externally. Since the output requires a bias inductor and DC blocking capacitor, the output can be matched with these two elements. To keep the driver unconditionally stable, it is recommended that a 300–400 ohm resistor be placed in parallel with the bias inductor as close to the IC as possible. Since the output impedance of the driver by itself is very high, the resistor sets the output impedance. The input can be matched with a series inductor followed by a shunt capacitor. Alternatively, a series transmission line followed by a shunt capacitor can be used. A DC block is also required on the input.

Gain control is provided to meet the CT2 low power mode requirement. The CT2 Common Air Interface specification requires the transmitter to be capable of dropping the output power by 16 ± 4.0 dB. Although the driver has 34 dB of small signal gain control, it can be reduced by adding a resistor in series with the gain control pin. The value of the resistor depends on the logic levels being used and the amount of gain compression after the driver. Also, the amount of gain control is a function of the driver input power level. The input power should be kept less than –10 dBm to allow for sufficient gain control to achieve the low power mode. The gain control can also be used for PA output power trimming. However, this is not an efficient method.

The ramp is an integrator which is used to slow down the driver and PA turn-on and turn-off times to reduce AM splatter. By applying a pulse waveform to the input, a linear ramp waveform is created at the output which is then applied to the current mirrors of the driver and PA. An external integrating capacitor is used so that the rise/fall time can be programmed externally. A minimum value of 2.0–2.4 nF is needed to meet the CT2 Common Air Interface splatter specification. For non-TDD/TDMA systems the ramp reverts to an enable/disable function.

The inverter is CMOS/TTL compatible and was included to provide complementary control for an antenna switch such as the MRFIC2003. By applying the receiver enable control line, RXEN, to the inverter the inverse $\overline{\text{RXEN}}$ will be created. RXEN and $\overline{\text{RXEN}}$ can then be used to control the MRFIC2003 antenna switch.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

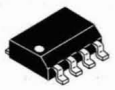
The MRFIC Line
900 MHz 2 Stage PA

MRFIC2006

The MRFIC2006 is an Integrated PA designed for linear operation in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2006 include CT-1 and CT-2 cordless telephones, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters.

- 50 Ω Input and Output Impedance
- Typical Gain = 23 dB @ 900 MHz
- Bias Current Externally Adjustable
- Bias Pin can be used to Ramp or Disable
- Class A or AB Linear Operation
- Unconditionally Stable
- SO-8 Leaded Plastic Package
- Order MRFIC2006R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2006

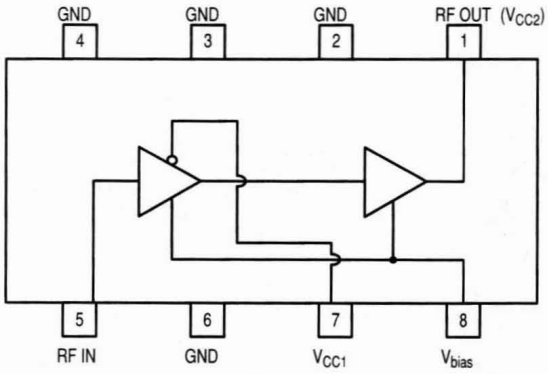
900 MHz 2 STAGE PA
SILICON MONOLITHIC
INTEGRATED CIRCUIT



CASE 751-06
(SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Z_o = 50 Ω unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC1}, V_{CC2}	5.0	Vdc
Bias Voltage	V_{bias}	6.0	Vdc
Total Supply Current	I_{CC1}, I_{CC2}	100	mA
RF Output Power (V_{CC2} < 4.0 V)	P_{out}	+21	dBm
RF Output Power (4.0 V < V_{CC2} ≤ 5.0 V)	P_{out}	53 – 8 V_{CC2}	dBm
RF Input Power	P_{in}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage and Junction Temperature	T_{stg}	– 65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	63	°C/W



Pin Connections and Functional Block Diagram

REV 3

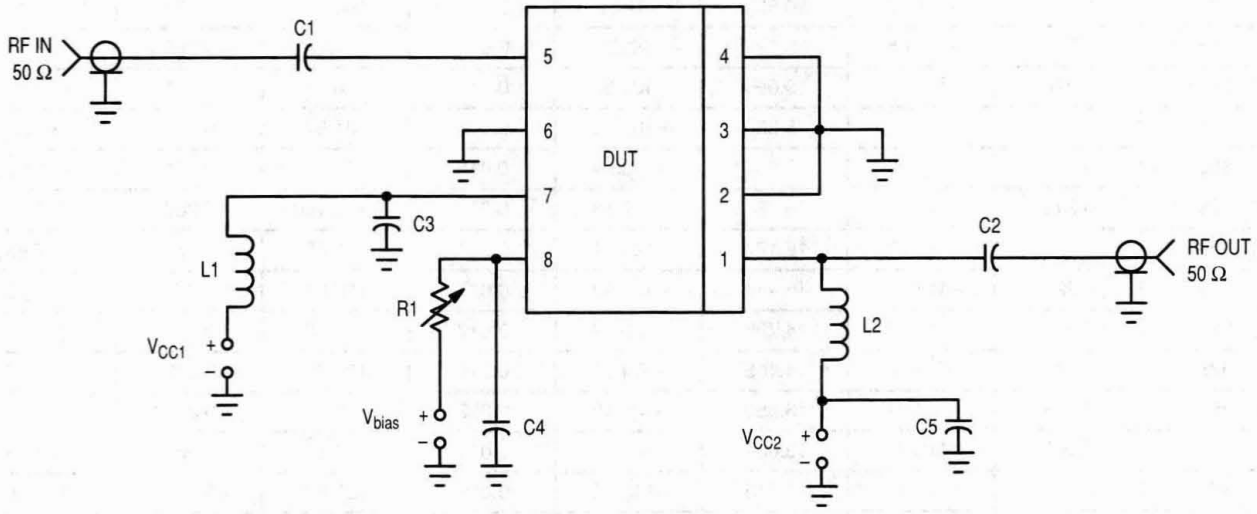
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Ranges	V_{CC1}, V_{CC2}	1.8 to 4.0	Vdc
Bias Voltage Range	V_{bias}	0 to 5.0	Vdc
RF Frequency Range	f	500 to 1000	MHz

ELECTRICAL CHARACTERISTICS (V_{CC1}, V_{CC2}, V_{bias} = 3.0 V, T_A = 25°C, f = 900 MHz, Z_o = 50 Ω unless otherwise noted)

Characteristics (1)	Min	Typ	Max	Unit
Supply Current — Total	—	46	55	mA
I_{CC1}	—	14	—	mA
I_{CC2}	—	29	—	mA
I Bias	—	3.0	—	mA
Small Signal Gain	19	23	26	dB
Input Return Loss, RF IN Port	—	15	—	dB
Output Return Loss, RF OUT Port	—	15	—	dB
Reverse Isolation	—	35	—	dB
Output Power at 1.0 dB Gain Compression	+12	+15.5	—	dBm
3rd Order Intercept Point (Out)	—	+ 25	—	dBm
5th Order Intercept Point (Out)	—	+ 21	—	dBm

NOTE:
1. All electrical characteristics measured in test circuit schematic shown in Figure 1 below.



C1, C2 — 100 pF Chip Capacitor
C3, C5 — 1.0 nF Chip Capacitor
C4 — 10 nF Chip Capacitor
L1 — 150 nH Chip Inductor
L2 — 10 nH Chip Inductor

R1 — Resistor Optional
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Typical Biasing Configuration

Table 1. Scattering Parameters for 900 MHz Two–Stage PA

(V_{CC1}, V_{CC2}, V_{BIAS} = 3 V, I = 49 mA, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.739	–16.67	3.785	51.56	0.003	–163.12	0.461	–89.23
100	0.702	–24.53	5.772	46.52	0.001	15.96	0.354	–117.30
150	0.671	–33.09	7.901	40.16	0.001	84.34	0.263	–144.77
200	0.649	–41.55	10.065	32.12	0.001	–165.89	0.208	–167.08
250	0.630	–49.79	12.287	23.06	0.002	–159.68	0.169	170.65
300	0.610	–58.60	14.576	12.25	0.002	171.75	0.136	145.40
350	0.592	–67.09	16.834	1.32	0.003	–160.23	0.113	113.52
400	0.567	–75.32	19.009	–10.72	0.005	–167.93	0.105	73.18
450	0.537	–83.69	20.901	–23.88	0.005	167.71	0.122	33.86
500	0.495	–91.79	22.237	–37.89	0.007	159.88	0.157	2.30
525	0.470	–95.35	22.626	–45.02	0.007	168.37	0.178	–10.93
550	0.448	–98.65	22.821	–52.22	0.010	162.65	0.196	–22.73
575	0.421	–101.69	22.834	–59.20	0.009	159.52	0.216	–32.62
600	0.397	–104.40	22.647	–66.13	0.010	155.15	0.233	–42.62
625	0.371	–106.50	22.299	–73.01	0.011	151.24	0.246	–50.98
650	0.349	–108.28	21.813	–79.43	0.011	148.14	0.258	–59.21
675	0.329	–109.85	21.204	–85.70	0.012	145.35	0.269	–66.61
700	0.310	–111.02	20.538	–91.62	0.012	140.66	0.273	–73.29
725	0.293	–111.65	19.824	–97.20	0.014	136.88	0.280	–79.97
750	0.278	–112.24	19.094	–102.54	0.014	136.98	0.281	–85.86
775	0.265	–112.60	18.334	–107.76	0.014	134.67	0.285	–91.50
800	0.252	–112.81	17.594	–112.54	0.016	133.71	0.284	–96.72
825	0.242	–113.50	16.880	–117.13	0.015	129.16	0.282	–102.24
850	0.233	–114.93	16.127	–122.44	0.017	131.80	0.281	–107.68
875	0.224	–115.32	15.438	–126.92	0.017	126.66	0.279	–112.88
900	0.216	–116.04	14.796	–130.89	0.017	127.06	0.275	–117.56
925	0.210	–116.66	14.165	–134.57	0.018	121.77	0.273	–120.85
950	0.203	–117.91	13.555	–138.19	0.019	122.40	0.269	–125.53
975	0.195	–118.87	13.009	–141.73	0.019	120.80	0.265	–129.73
1000	0.191	–120.47	12.515	–145.08	0.019	122.53	0.265	–132.68
1025	0.186	–122.39	12.004	–148.23	0.020	119.56	0.259	–137.22
1050	0.179	–124.03	11.517	–151.36	0.022	115.24	0.254	–140.85
1075	0.175	–126.22	11.063	–154.40	0.022	117.88	0.251	–144.69
1100	0.168	–128.77	10.634	–157.40	0.024	112.04	0.248	–148.25
1125	0.163	–131.41	10.228	–160.15	0.023	112.42	0.246	–151.75
1150	0.161	–133.93	9.841	–163.04	0.023	115.77	0.245	–155.28
1175	0.155	–136.68	9.479	–165.88	0.025	110.34	0.241	–158.69
1200	0.152	–140.85	9.125	–168.50	0.025	109.94	0.241	–161.95

TYPICAL CHARACTERISTICS

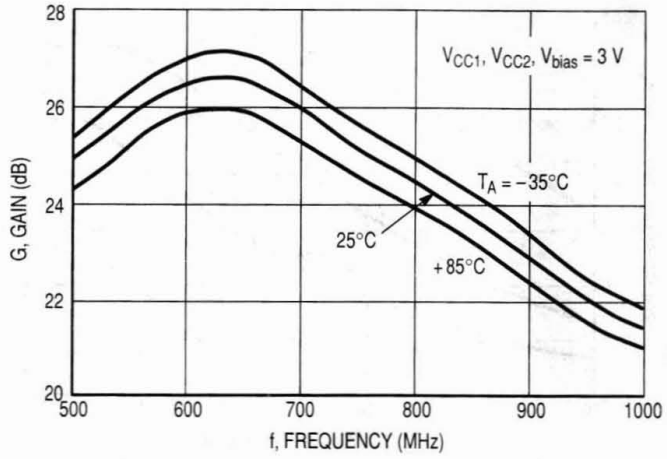


Figure 2. Gain versus Frequency

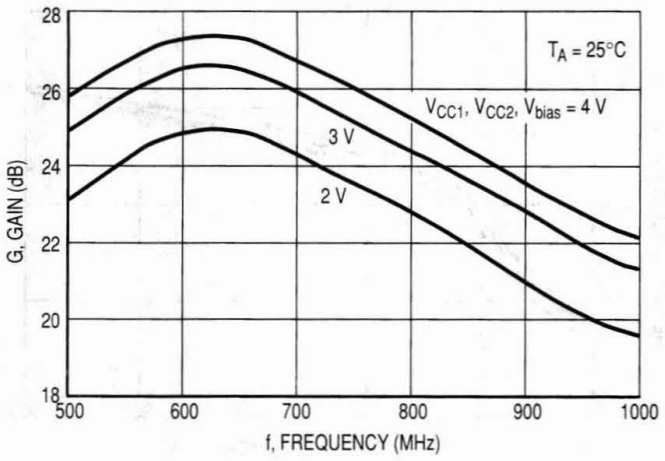


Figure 3. Gain versus Frequency

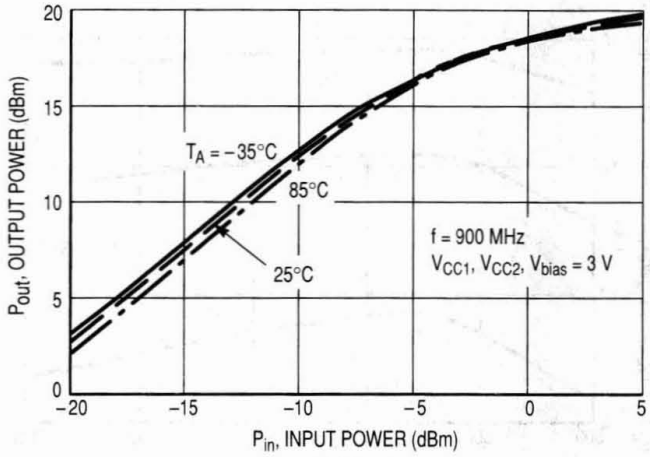


Figure 4. Output Power versus Input Power

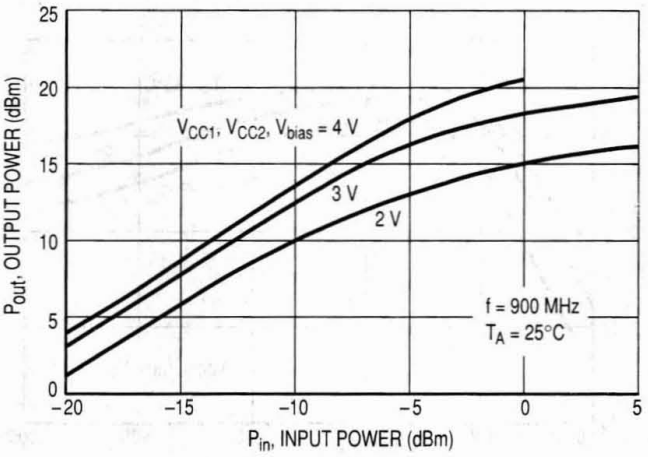


Figure 5. Output Power versus Input Power

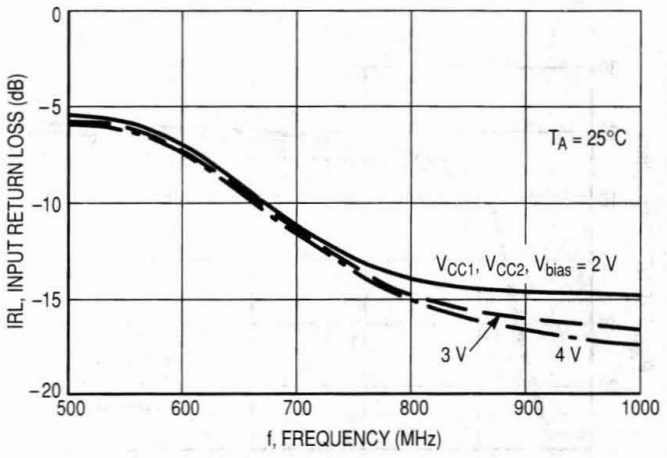


Figure 6. Input Return Loss versus Frequency

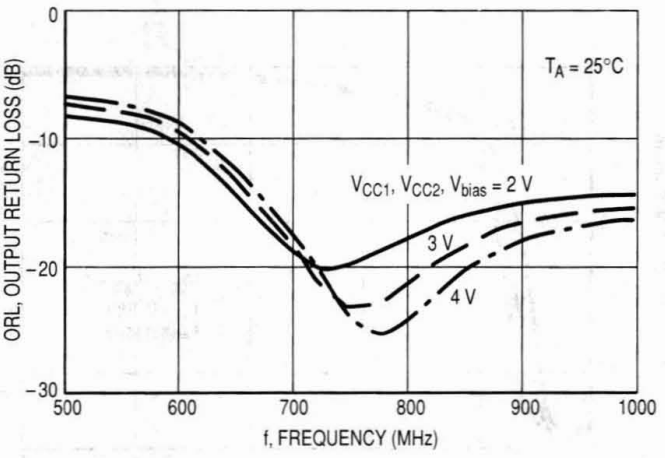


Figure 7. Output Return Loss versus Frequency

TYPICAL CHARACTERISTICS

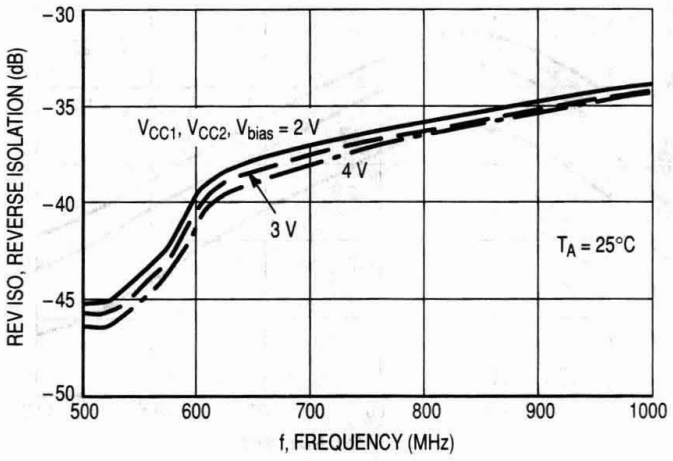


Figure 8. Reverse Isolation versus Frequency

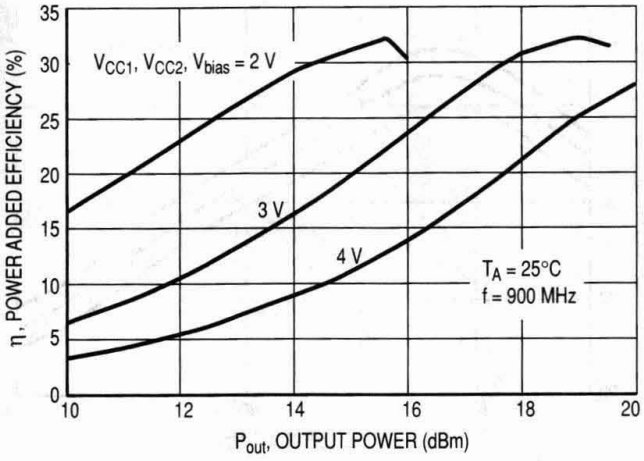


Figure 9. Power Added Efficiency versus Output Power

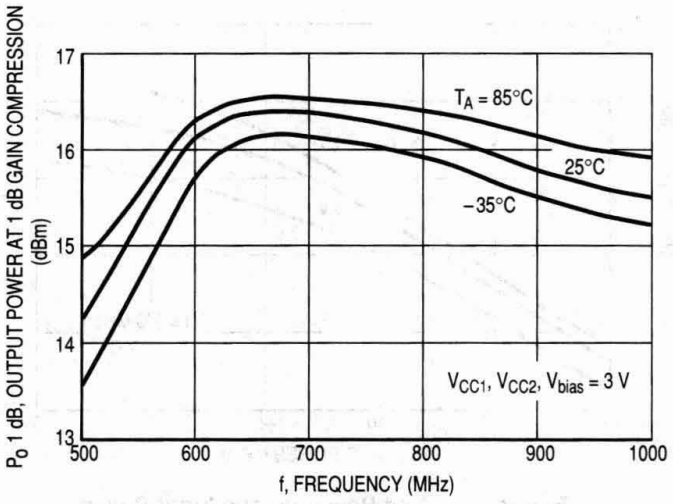


Figure 10. Output Power at 1 dB Gain Compression versus Frequency

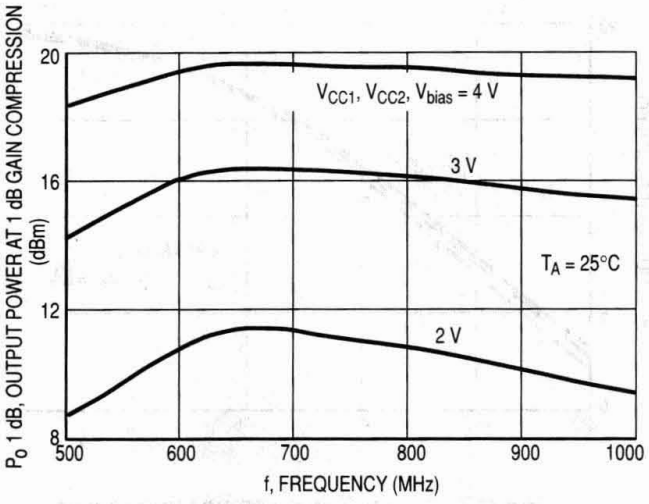


Figure 11. Output Power at 1 dB Gain Compression versus Frequency

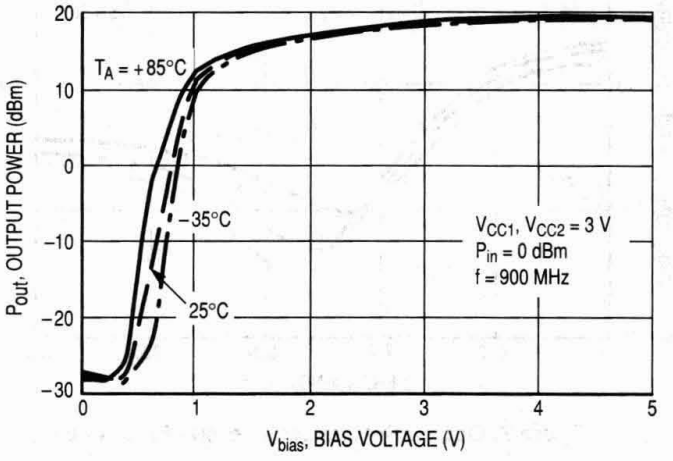


Figure 12. Output Power versus Bias Voltage

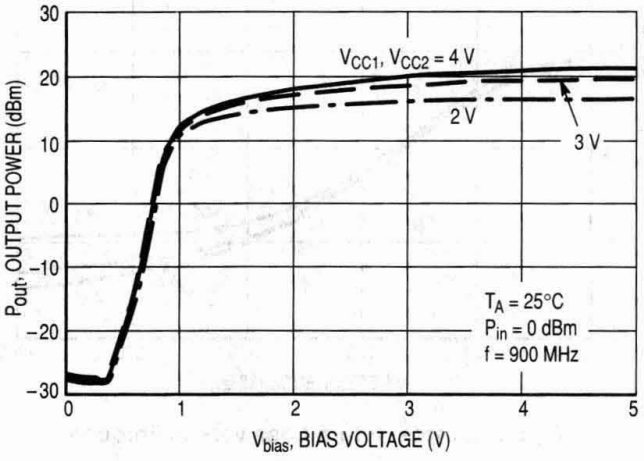


Figure 13. Output Power versus Bias Voltage

TYPICAL CHARACTERISTICS

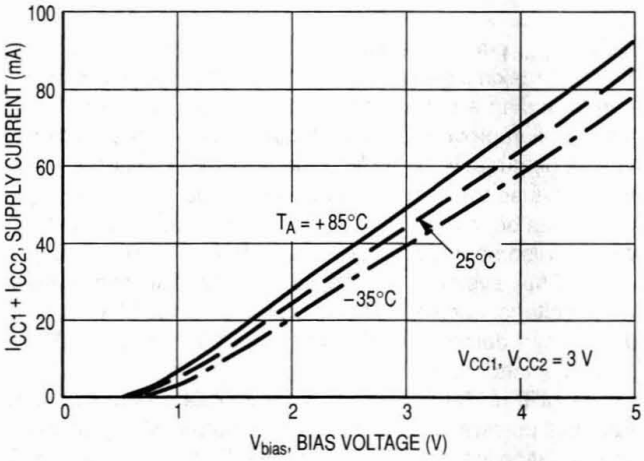


Figure 14. Supply Current versus Bias Voltage

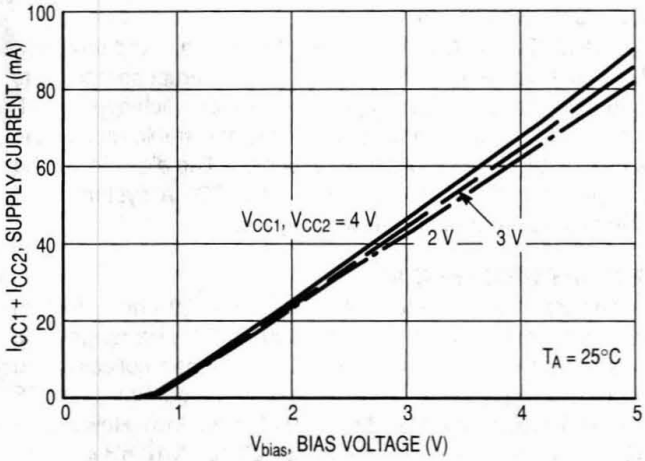


Figure 15. Supply Current versus Bias Voltage

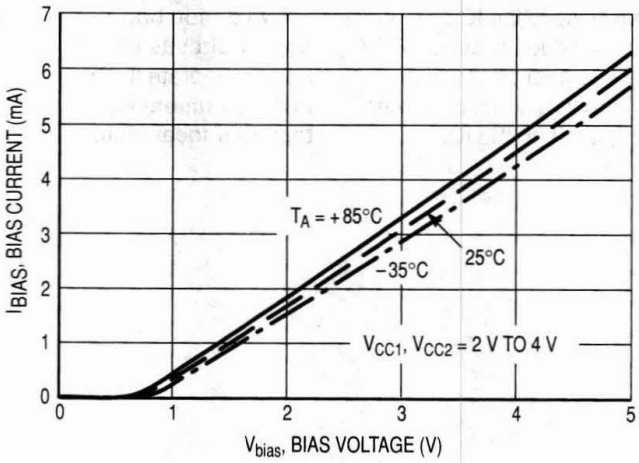


Figure 16. Bias Current versus Bias Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2006 was designed for low cost and flexibility. Low cost was achieved by minimizing external components and using an SOIC package. Flexibility was achieved by allowing the bias current to be externally adjustable resulting in a broad range of output power capability. The bias pin can be ramped to reduce AM splatter in TDD/TDMA systems and can be used to trim the RF output power.

THEORY OF OPERATION

The input port is internally matched to 50 ohms. Return loss is typically 15–16 dB in the 800–1000 MHz range. The output port is nearly 50 ohms but is an open collector and therefore requires an external bias inductor. Using an RF choke will result in a 11–12 dB output return loss. However, a 10 nH inductor will improve it to 15–20 dB. A 10 nH inductor is small enough in value to be printed on the board. DC blocks are required on the input and output. Values of 100 pF are recommended.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. A series RF choke is recommended to keep the RF signal off the supply line. A 10 nF decoupling capacitor is recommended on the V_{bias} line but does not need to be very close to the IC.

The V_{bias} pin can be used several ways. Tying it directly to V_{CC} will maximize the bias current which will maximize linearity. Adding a series resistor will reduce the bias current which will improve efficiency. Figure 9 shows the efficiency versus output power with V_{bias} tied to V_{CC}. The series resistor will cause these curves to shift to the left. The RF output power can be trimmed by using a variable resistor. The V_{bias} pin can also be used to power down the IC or, in the case of TDD/TDMA systems, to ramp the IC. By applying a linear ramp voltage, such as the one provided by the MRFIC2004, it has been demonstrated to meet the CT2 Common Air Interface splatter specifications.

The MRFIC2006 is internally temperature compensated. For input powers of −5.0 to 0 dBm the output power temperature variation is typically less than 0.2 dB from −35 to +85°C.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

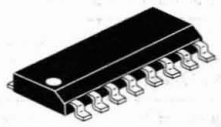
The MRFIC Line
900 MHz TX-Mixer/Exciter

MRFIC2101

900 MHz
TX-MIXER/EXCITER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

The MRFIC2101 is a high linearity transmit mixer and exciter designed primarily for Digital Cellular radio systems. The mixer is double-balanced for excellent LO and spurious rejection. An on-board LO buffer is provided to reduce LO power requirements and eliminate the need for an external LO balun. A power down control is provided to minimize current drain with minimum recovery/turn-on time. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device.

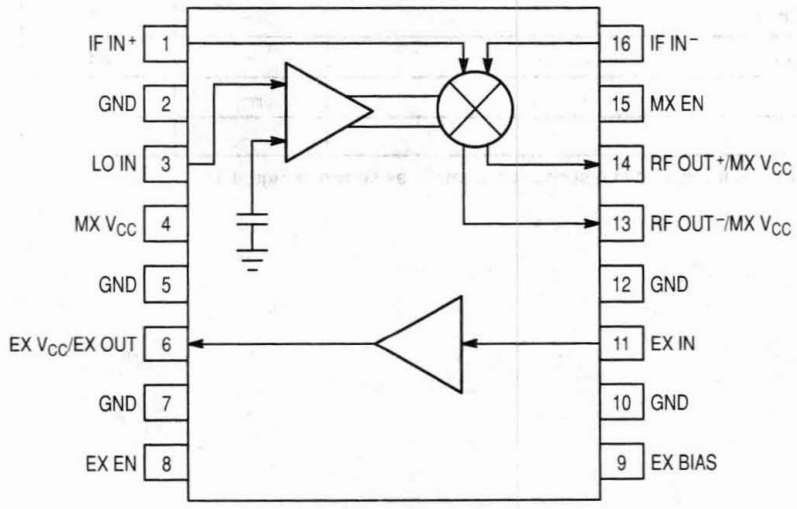
- High Linearity IP^3_0 = 23 dBm (Typ)
- Low LO Drive Required = –15 dBm (Typ)
- Externally Adjustable Exciter Bias Current
- Power Down Supply Current = 2.0 μA (Typ)
- SO-16 Narrow Body Plastic Package
- Order MRFIC2101R2 for Tape and Reel.
  R2 suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2101



CASE 751B-05
(SO-16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	EX V_{CC}, MX V_{CC}, EX BIAS	5	Vdc
Enable Voltages	MX EN, EX EN	6	Vdc
Input Power, LO and IF Ports	P_{LO}, P_{IF}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
RF Output Power (EX V_{CC} < 4 V)	P_{out}	18	dBm
RF Output Power (4 V< EX V_{CC} ≤ 5 V)	P_{out}	38 – 5 EX V_{CC}	dBm



Pin Connections and Functional Block Diagram

REV 3

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltages	EX V_{CC}, MX V_{CC}, EX BIAS	4.75	Vdc
Enable Voltages	MX EN, EX EN	0, 4.75	Vdc
RF Port Frequency Range	RF	800 to 1000	MHz
IF Port Frequency Range	IF	0 to 250	MHz

LOGIC LEVELS (T_A = 25°C)

Input Voltage (MX EN, EX EN)	Min	Max	Unit
High	MX V_{CC} –0.8, EX V_{CC} –0.8	—	Volts
Low	—	0.8	Volts

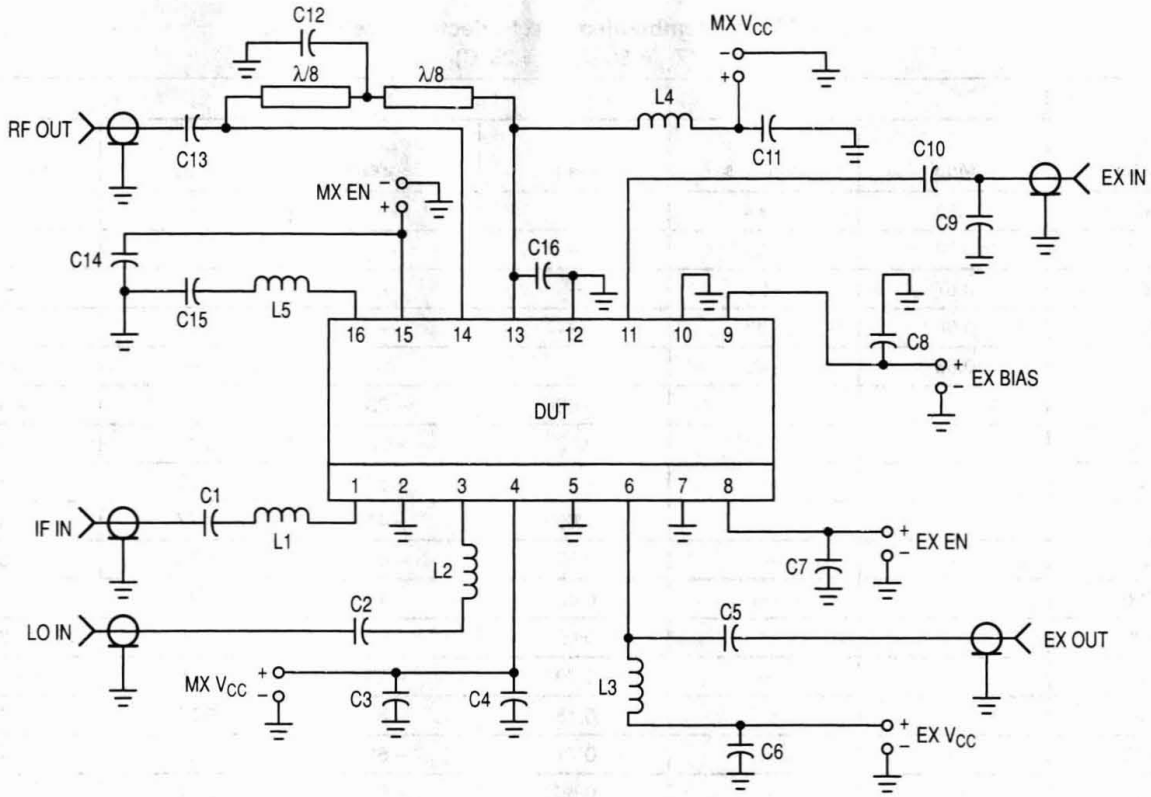
MIXER ELECTRICAL CHARACTERISTICS (MX V_{CC}, MX EN = 4.75 V, T_A = 25°C, RF @ 900 MHz, LO @ 800 MHz, IF @ 100 MHz, P_{LO} = –15 dBm unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Conversion Gain (Small Signal)	24	26.5	29	dB
Output Power at 1 dB Gain Compression	2.5	4.5	—	dBm
Output Third Order Intercept Point (– 5 dBm out/tone)	—	14	—	dBm
Output Fifth Order Intercept Point (– 5 dBm out/tone)	—	11	—	dBm
LO Leakage	—	– 30	—	dBm
Supply Current (Enabled)	—	45	54	mA
Supply Current (Disabled)	—	1	—	µA
Noise Figure (Single Sideband)	—	5	—	dB

EXCITER ELECTRICAL CHARACTERISTICS (EX V_{CC}, EX EN, EX BIAS = 4.75 V, T_A = 25°C, RF @ 900 MHz unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Gain (Small Signal)	14	16	18	dB
Output Power at 1 dB Gain Compression	16	18	—	dBm
Output Third Order Intercept Point (+ 3 dBm out/tone)	—	30	—	dBm
Output Fifth Order Intercept Point (+ 3 dBm out/tone)	—	22	—	dBm
LO Leakage (P_{LO} = –15 dBm into Mixer)	—	– 30	—	dBm
Supply Current (Enabled)	—	38	46	mA
Supply Current (Disabled)	—	1	—	µA
Noise Figure	—	5	—	dB

(1) All electrical characteristics are measured in test circuit schematic as shown in Figure 1.



C1, C2, C3,	1000 pF, Chip Capacitor	L1, L5	82 nH, Chip Inductor
C4	100 pF, Chip Capacitor	L2	15 nH, Chip Inductor
C5, C6, C7	1000 pF, Chip Capacitor	L3	8.2 nH, Chip Inductor
C8, C10, C11	1000 pF, Chip Capacitor	L4	12 nH, Chip Inductor
C9, C12	5.6 pF, Chip Capacitor	RF Connectors	SMA Type
C13, C16	2.7 pF, Chip Capacitor	Board Material	0.031″ Thick FR4, 0.5 oz. Copper, ε_r = 4.45, Coplanar Waveguide
C14, C15	1000 pF, Chip Capacitor		

Figure 1. Test Circuit Configuration

Table 1. Mixer Deembedded Port Reflection Coefficients
(Z_O = 50 Ω, T_A = 25°C)

f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
	Mag	∠ϕ Degrees	Mag	∠ϕ Degrees	Mag	∠ϕ Degrees
50	0.68	– 9.4	—	—	—	—
100	0.68	– 18	—	—	—	—
150	0.67	– 26	—	—	—	—
200	0.66	– 33	—	—	—	—
250	0.65	– 40	—	—	—	—
500	—	—	0.93	– 28	0.79	– 30
600	—	—	0.92	– 33	0.79	– 32
700	—	—	0.91	– 37	0.79	– 33
800	—	—	0.89	– 41	0.77	– 34
900	—	—	0.87	– 45	0.75	– 34
1000	—	—	0.85	– 48	0.73	– 35
1100	—	—	0.82	– 50	0.69	– 36
1200	—	—	0.79	– 53	0.65	– 37
1300	—	—	0.75	– 56	0.61	– 41
1400	—	—	0.71	– 61	0.56	– 47
1500	—	—	0.66	– 66	0.52	– 55

Table 2. Exciter Small Signal Deembedded S Parameters
(Z_O = 50 Ω, T_A = 25°C)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\lvert S_{11}\rvert$	∠ϕ	$\lvert S_{21}\rvert$	∠ϕ	$\lvert S_{12}\rvert$	∠ϕ	$\lvert S_{22}\rvert$	∠ϕ
100	0.51	–121	35.51	131	0.02	50	0.65	–67
200	0.62	–149	22.61	109	0.03	42	0.49	–103
300	0.65	–162	16.05	96	0.03	41	0.43	–122
400	0.65	–170	12.16	87	0.04	41	0.40	–134
500	0.63	–177	9.75	81	0.04	42	0.38	–141
600	0.61	176	8.18	75	0.05	41	0.37	–146
700	0.59	169	7.06	70	0.05	40	0.36	–149
800	0.58	161	6.18	65	0.06	38	0.35	–153
900	0.58	154	5.44	60	0.07	33	0.35	–156
1000	0.59	145	4.91	55	0.07	30	0.35	–163
1100	0.61	139	4.39	51	0.08	27	0.35	–170
1200	0.65	134	3.94	47	0.08	22	0.35	–177
1300	0.67	131	3.56	43	0.08	20	0.37	174
1400	0.69	129	3.22	39	0.09	16	0.40	166
1500	0.71	127	2.92	36	0.09	13	0.43	160

TYPICAL CHARACTERISTICS

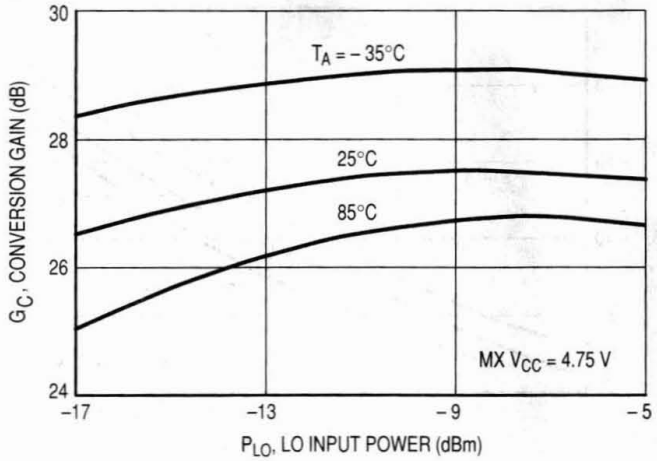


Figure 2. Mixer Gain versus LO Input Power

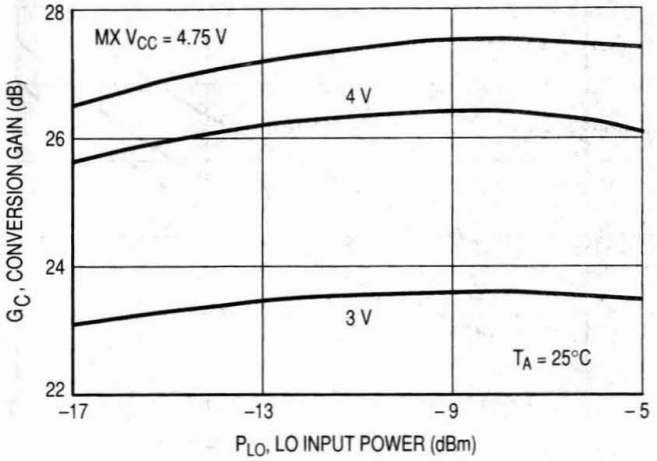


Figure 3. Mixer Gain versus LO Input Power

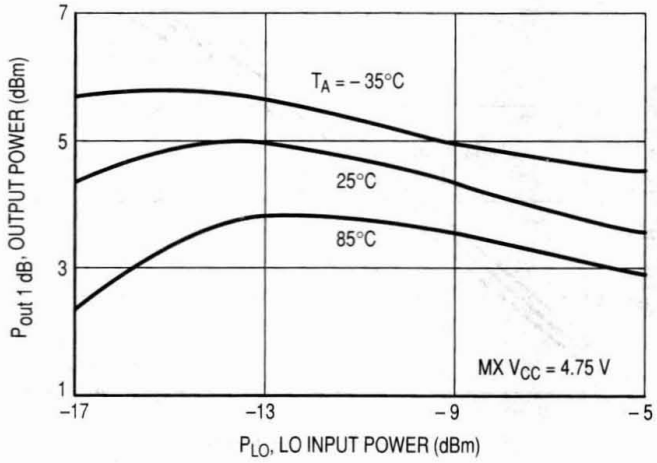


Figure 4. Mixer Output Power at 1 dB Gain Compression versus LO Input Power

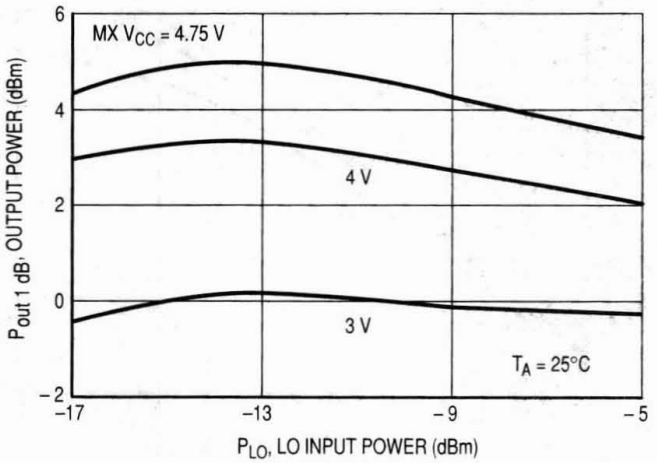


Figure 5. Mixer Output Power at 1 dB Gain Compression versus LO Input Power

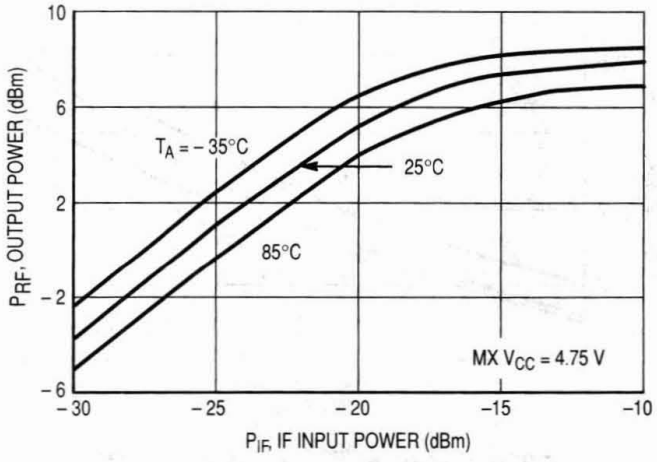


Figure 6. Mixer Output Power versus IF Input Power

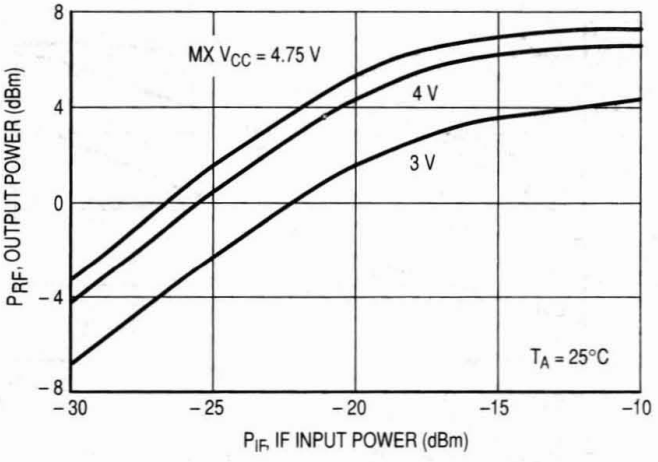


Figure 7. Mixer Output Power versus IF Input Power

TYPICAL CHARACTERISTICS

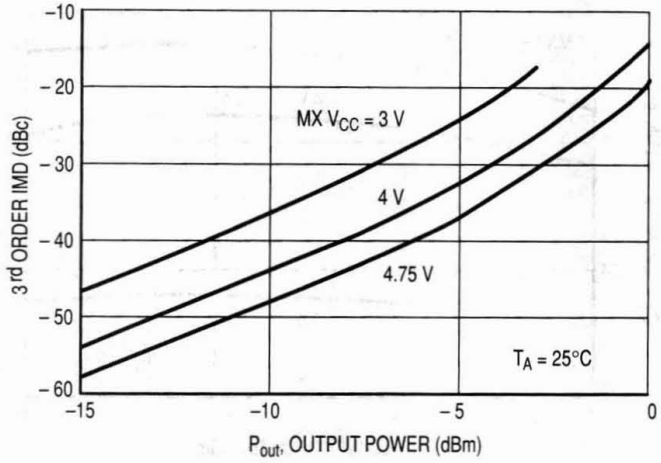


Figure 8. Mixer 3rd Order Intermodulation Distortion versus Output Power

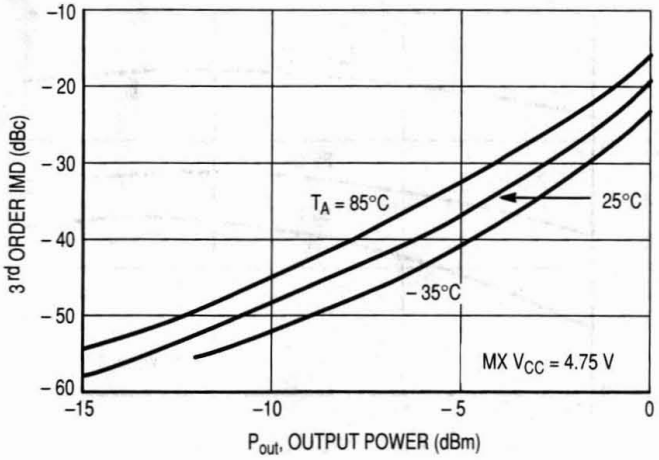


Figure 9. Mixer 3rd Order Intermodulation Distortion versus Output Power

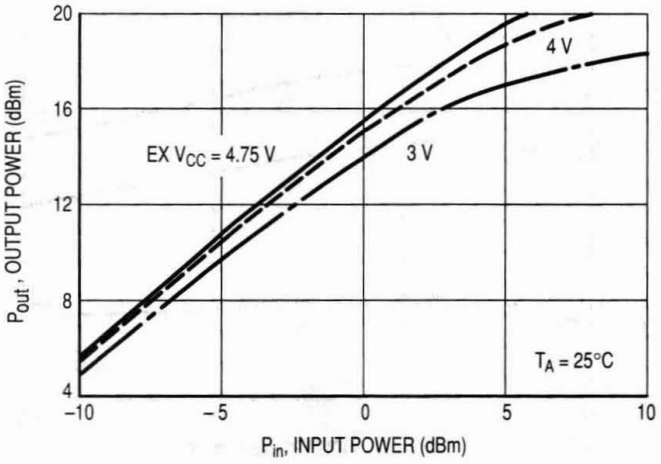


Figure 10. Exciter Output Power versus Input Power

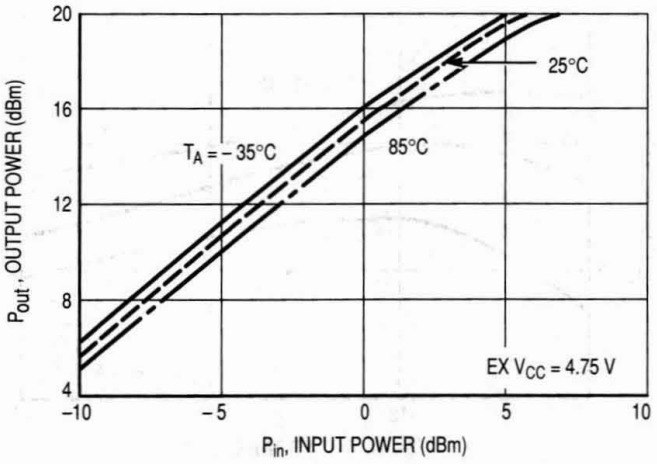


Figure 11. Exciter Output Power versus Input Power

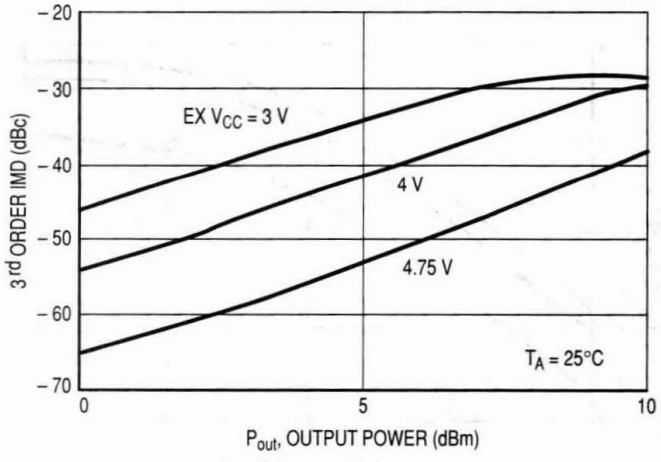


Figure 12. Exciter 3rd Order Intermodulation Distortion versus Output Power

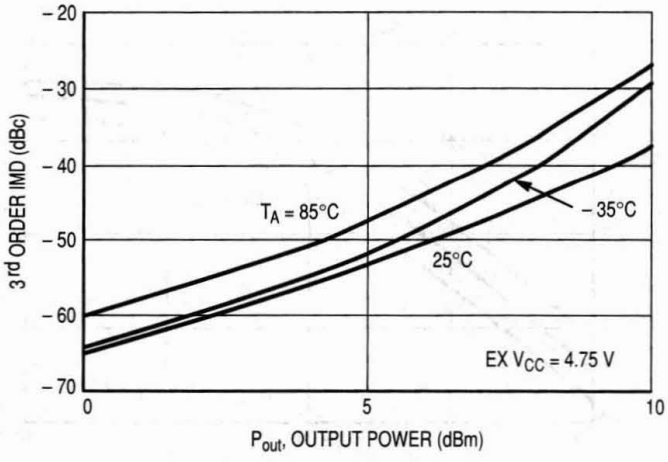


Figure 13. Exciter 3rd Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

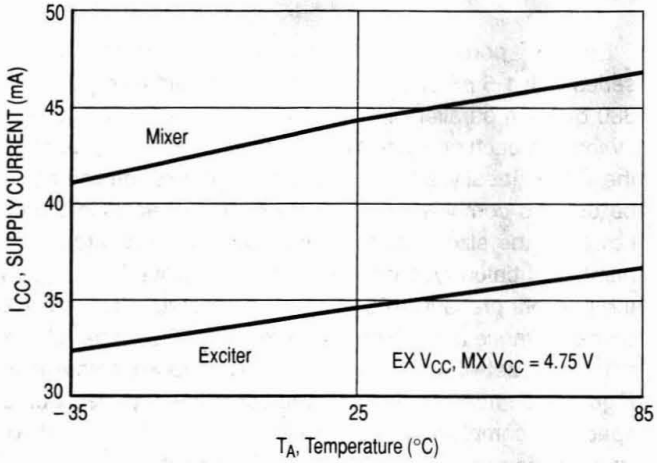


Figure 14. I_{CC} versus Temperature

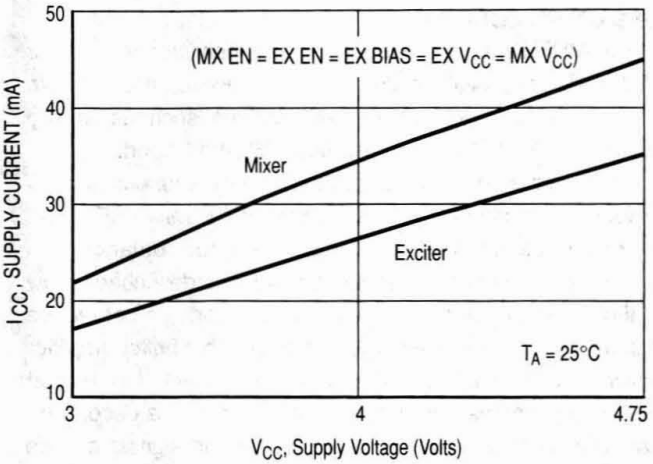


Figure 15. I_{CC} versus V_{CC}

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2101 was designed as a linear upconverter for U.S. and Japan digital cellular radios. However, it is versatile enough to be used in other applications such as analog cellular, GSM, CDMA and the 900 MHz ISM band.

The mixer is double-balanced to minimize spurious and LO emission. An external balun is required on the mixer RF output to maximize linearity and maintain good balance. An inexpensive and easy to implement balun is described below in the theory of operation. The IF and LO ports do not require baluns. The LO split is achieved on-chip with a buffer amplifier which also reduces the LO power requirement. The IF port can be driven differentially or single-ended with a decoupling capacitor on the unused IF input. Baseband signals can be applied directly to the IF inputs and the device becomes a complete low–power transmitter.

To maximize efficiency in various systems, the exciter bias current is externally adjustable. The bias current can also be ramped to reduce spectral splatter.

To minimize current drain in TDD/TDMA systems, the MRFIC2101 has separate TTL/CMOS compatible enable pins for the mixer and the exciter.

THEORY OF OPERATION

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8 – 15 nH depending on LO frequency and distance from the IC) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since the added electrical length will cause a poor match.

The IF ports are approximately 250 ohms resistive in parallel with 5.0 pF of capacitance. Matching directly into this impedance is not recommended. Series 82 nH chip inductors should first be placed as close to both IF ports as possible. This presents a high impedance to the IF ports at the LO frequency which substantially reduces the LO leakage out of the RF port. The resulting impedance then may be matched to the desired characteristic impedance. DC blocking capacitors are also required.

Both RF ports are approximately 25 ohms resistive in series with 1.5 pF of capacitance (or the parallel equivalent, 380 ohms in parallel with 1.9 pF). Best linearity is achieved by loading each port with 100 ohms resistive and resonating the 1.9 pF. Ideally, a half wavelength transmission line could be used to combine the two differential RF ports into one; however, the size of such a line would be very large. Any number of balun type network can be employed so long as the network presents 100 ohms to each port, resonates 1.9 pF capacitance at each port, and exhibits 180 degree phase difference between the two ports. The network shown in Figure 1 combines very well without a lot of added board space or complexity. Essentially, a quarter wavelength of transmission line (~1.5 inches of 50 ohms stripline in FR4) is used with additional phase shift coming from capacitors C12, C13 and C16. This network will operate anywhere from 800–1000 MHz by adjusting bias inductor L4 and C16 only.

The exciter input requires external matching and a DC block. It is best matched to 50 ohms using a short 50 ohms transmission line followed by a 5–10 pF shunt capacitor. The exciter output is approximately 50 ohms resistive in parallel with 4 pF of capacitance in the 800–1000 MHz range. It is best matched to 50 ohms using a 6–10 nH bias inductor placed as close to the IC as possible. The exciter is conditionally stable. Placing a 100-300 ohm resistor in parallel with the bias inductor, when driving large VSWR loads, may be needed to keep the exciter stable.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the LO signal off the supply line.

Enabling/Disabling the MRFIC2101 can be done with the separate TTL/CMOS compatible enable pins for the mixer and exciter. The trip point is between 1 and 2 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

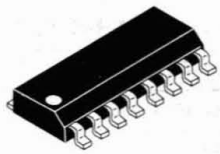
2.4 GHz GaAs Downconverter

MRFIC2401

2.4 GHz DOWNCONVERTER GaAs MONOLITHIC INTEGRATED CIRCUIT

The MRFIC2401 is a GaAs low–noise amplifier and downmixer in a low–cost 16 lead plastic package designed for use in the 2.4 to 2.5 GHz Industrial–Scientific–Medical (ISM) band. The design is optimized for efficiency at 5.0 Volt operation at 2.45 GHz but is usable from 2.0 to 3.0 GHz in applications such as telemetry and Multichannel Multipoint Distribution System (MMDS) wireless cable TV systems. Performance is suitable for frequency hopping or direct sequence spread spectrum as well as single–frequency applications. LNA output and mixer input are available to allow image filtering.

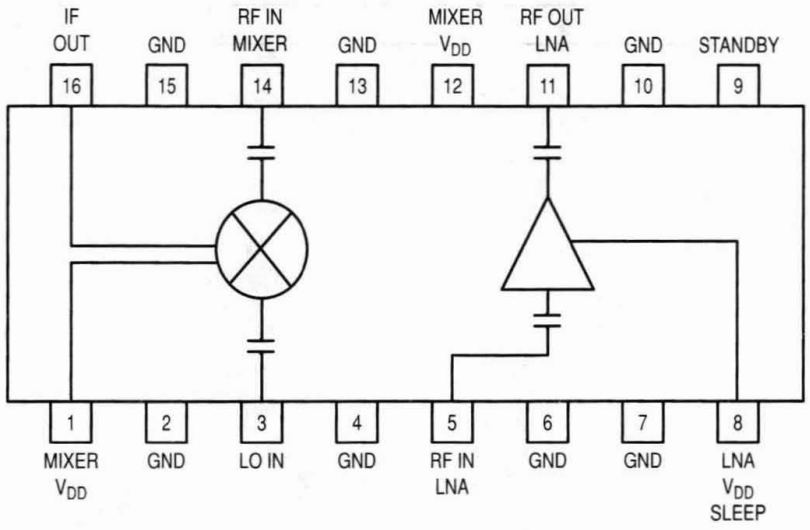
- Single Supply Voltage = 5.0 Volts
- High Conversion Gain = 21 dB Typical Less Image Filter
- Low Supply Current = 9.5 mA Typical
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC2401R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2401



CASE 751B-05
(SO-16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Input Power, RF IN Ports	P_{RF}	+5.0	dBm
Input Power, LO IN Port	P_{LO}	+5.0	dBm
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C
Bias Control Voltage	STANDBY	6.0	Vdc



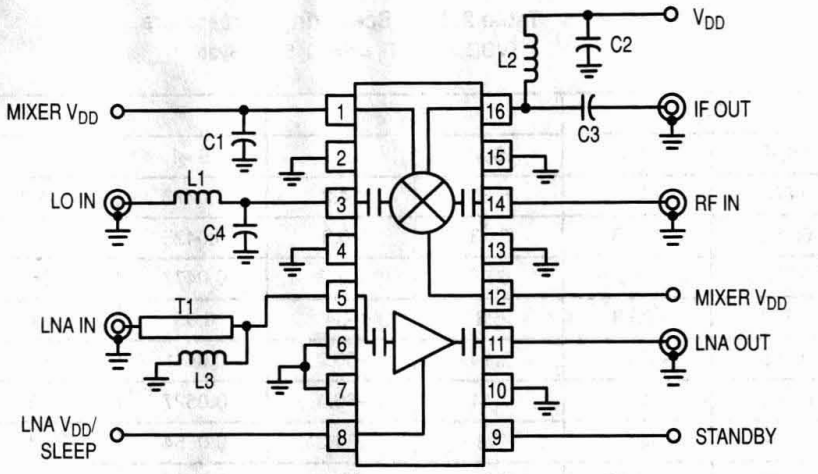
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.75 to 5.25	Vdc
IF Frequency Range	f_{IF}	100 to 350	MHz
LO Drive Power Level	P_{LO}	–10 to 0	dBm
LO Frequency Range	f_{LO}	2050 to 2400	MHz
RF Frequency Range	f_{RF}	2400 to 2500	MHz
STANDBY Mode ON	STANDBY	V_{DD}	Vdc
STANDBY Mode OFF	STANDBY	0	Vdc
SLEEP Mode OFF	SLEEP	V_{DD}	Vdc
SLEEP Mode ON	SLEEP	0	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 Vdc, T_A = 25°C, RF = 2.45 GHz, LO = 2.125 GHz @ –5.0 dBm, STANDBY = 0 Vdc)

Characteristic	Min	Typ	Max	Unit
Conversion Gain – Downconverter (Less Image Filter Loss)	19	21	–	dB
Gain – LNA	–	17	–	dB
Conversion Gain – Mixer	–	4.0	–	dB
Noise Figure – LNA	–	1.9	–	dB
Noise Figure – Mixer	–	11	–	dB
Return Loss – Mixer Input, LO Input, LNA Output	–	10	–	dB
Input Third Order Intercept – Downconverter (Less Image Filter Loss)	–	–18	–	dBm
Input Third Order Intercept – LNA	–	–13	–	dBm
Input Third Order Intercept – Mixer	–	0	–	dBm
Reverse Isolation – Downconverter (Less Image Filter Loss)	–	30	–	dB
Isolation – LO to RF, LO to IF	–	20	–	dB
Supply Current – Downconverter	–	9.5	11	mA
SLEEP Mode Supply Current – Downconverter (No LO, STANDBY= 5 Vdc, V_{DD}/SLEEP = 5 Vdc)	–	600	–	μA
Turn On, Turn Off Time – LNA	–	1.0	–	μs



325 MHz IF:
C1, C2 – 100 pF
C3 – 5.6 pF
C4 – 0.5 pF
L1 – 4.7 nH
L2 – 8.2nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92 MILS

240 MHz IF:
C1, C2 – 100 pF
C3 – 5.6 pF
C4 – 0.5 pF
L1 – 8.2 nH
L2 – 18 nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92mils

Board Material – FR4

110 MHz IF:
C1 – 100 pF
C2 – 1000 pF
C3 – 8.2 pF
C4 – 0.3 pF
L1 – 8.2 nH
L2 – 82 nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92 mils

Figure 1. Applications Circuit Configuration

f	LO Z_{in}	
Frequency (GHz)	**R**	**jX**
2.0	39.7	23.9
2.1	35.7	22.1
2.2	32.1	19.8
2.3	29.1	17.1
2.4	26.5	14.0
2.5	24.4	10.7

Table 1. Selected Port Impedances (from Conjugate Match)

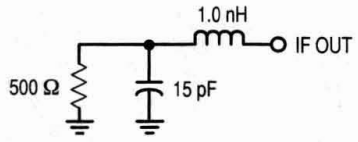


Figure 2. Equivalent IF Output Circuit

Table 2. LNA Scattering Parameters
(VDD = 5 V, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
2000	0.823	–50.8	5.35	14.3	0.0373	164.2	0.609	–64.1
2050	0.783	–62.9	6.13	–0.3	0.0425	154.3	0.558	–78.7
2100	0.752	–76.8	6.56	–18.3	0.0477	138	0.497	–94.3
2150	0.713	–89.8	6.8	–34	0.05	121	0.425	–110.7
2200	0.656	–104.2	7.14	–50.2	0.0511	106.4	0.343	–129.6
2250	0.583	–119	7.44	–66.4	0.0527	91.8	0.25	–152.3
2300	0.509	–134.1	7.8	–84.2	0.0554	78.1	0.155	176.2
2350	0.425	–148.2	7.86	–102.6	0.0579	59.89	0.088	120.7
2400	0.34	–163.6	7.84	–119.4	0.0552	42.31	0.111	43.8
2450	0.261	–177.8	7.78	–138.1	0.0528	28.27	0.191	2.2
2500	0.175	173.4	7.43	–154.6	0.0514	13.37	0.269	–21.9
2550	0.103	170.4	7.15	–170.6	0.0484	–0.842	0.338	–41.8
2600	0.056	–160.5	6.72	173	0.0455	–15.4	0.393	–59.4
2650	0.067	–130.7	6.47	159.1	0.0422	–28.11	0.436	–76.2
2700	0.102	–117.8	6.25	142.3	0.039	–41.5	0.472	–92.2
2750	0.132	–119.5	5.53	127.1	0.0353	–53.47	0.496	–107.5
2800	0.166	–125.2	5.26	117.5	0.0329	–63.28	0.513	–121.3
2850	0.19	–134.8	5.15	102.4	0.0309	–75.04	0.533	–135
2900	0.219	–144.8	4.71	87.6	0.0283	–87.86	0.547	–148.8
2950	0.235	–155.9	4.43	76.1	0.025	–95.83	0.559	–162.4
3000	0.262	–165.9	4.08	62.3	0.0235	–108.4	0.57	–175.7

TYPICAL CHARACTERISTICS

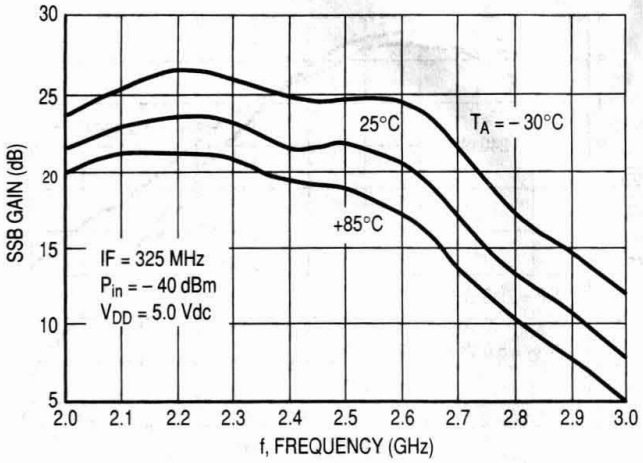


Figure 3. Downconverter Gain versus Frequency

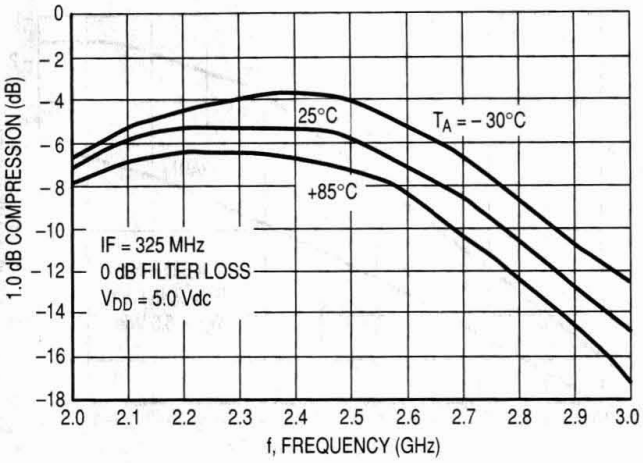


Figure 4. Downconverter 1.0 dB Compression versus Frequency

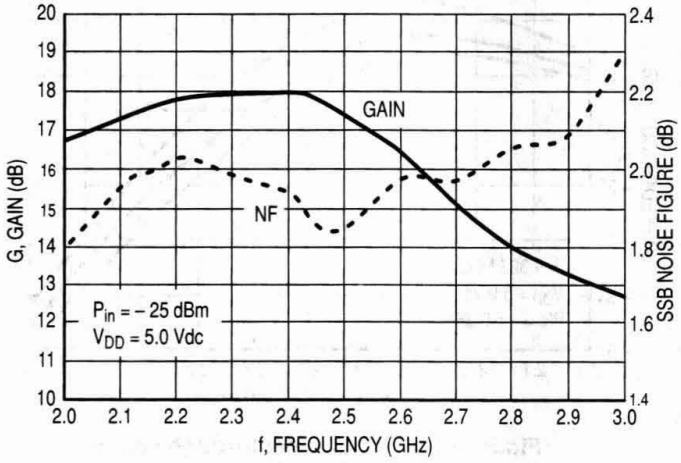


Figure 5. LNA Gain and Noise Figure versus Frequency

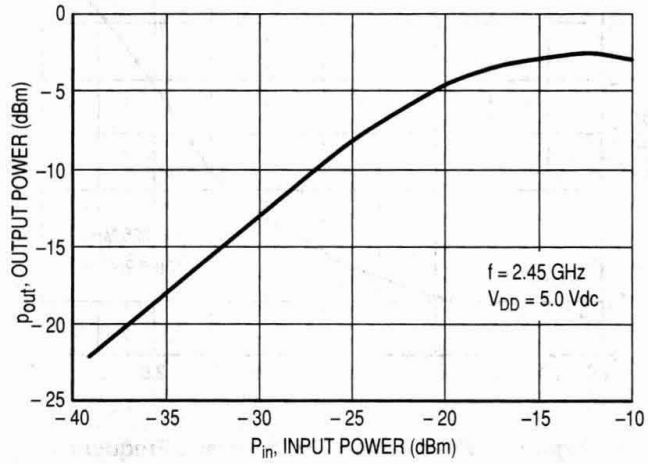


Figure 6. LNA Output Power versus Input Power

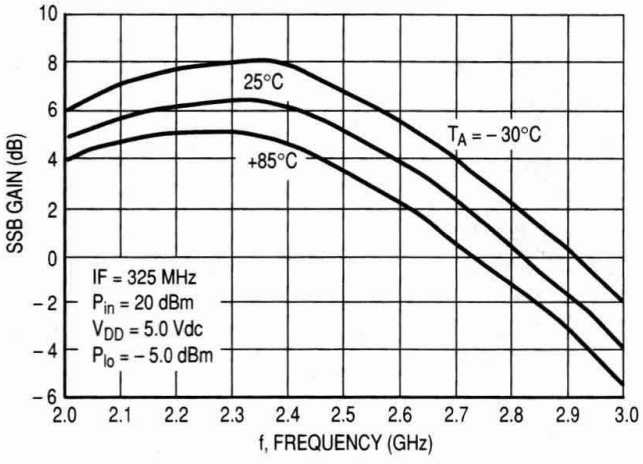


Figure 7. Mixer Conversion Gain versus Frequency

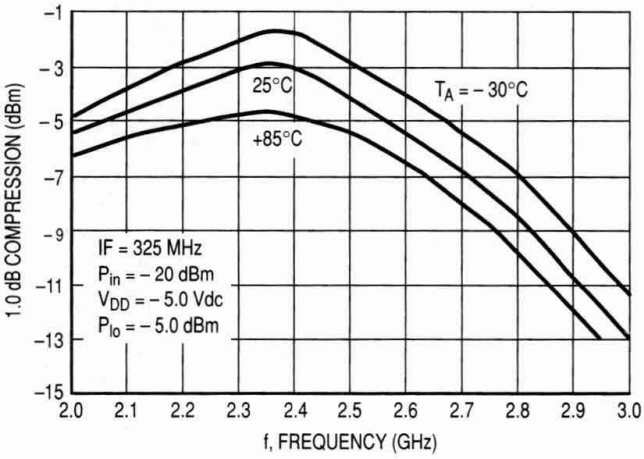


Figure 8. Mixer 1.0 dB Compression versus Frequency

TYPICAL CHARACTERISTICS

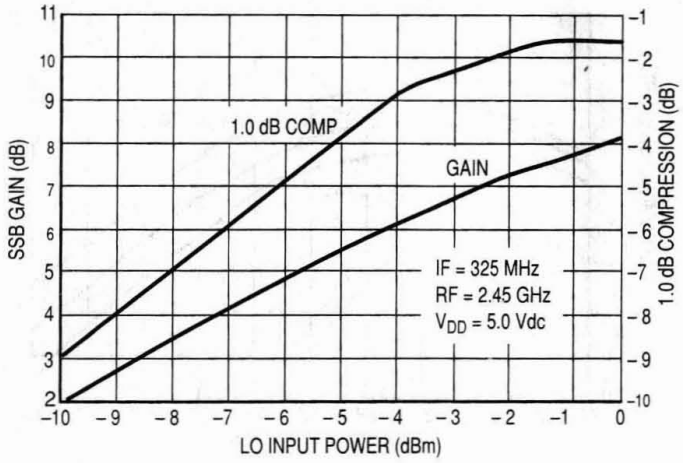


Figure 9. Mixer 1.0 dB Compression and Gain versus LO Power

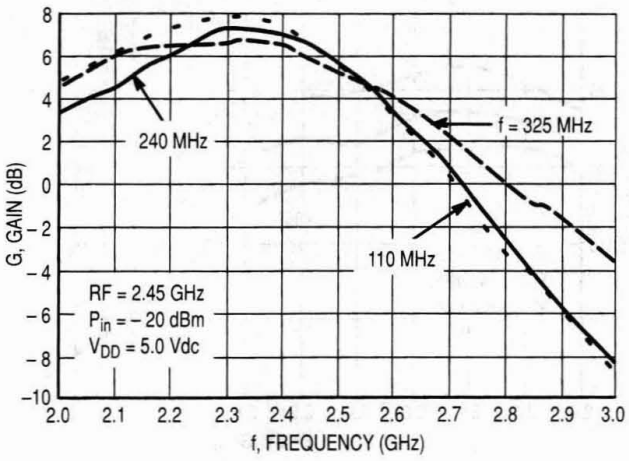


Figure 10. Mixer Gain versus Frequency

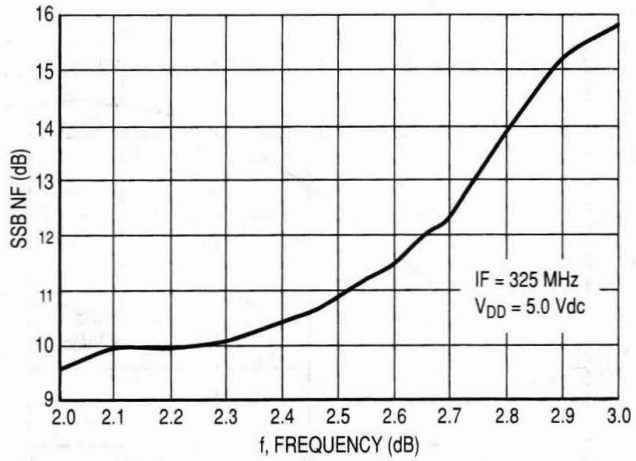


Figure 11. Mixer Noise Figure versus Frequency

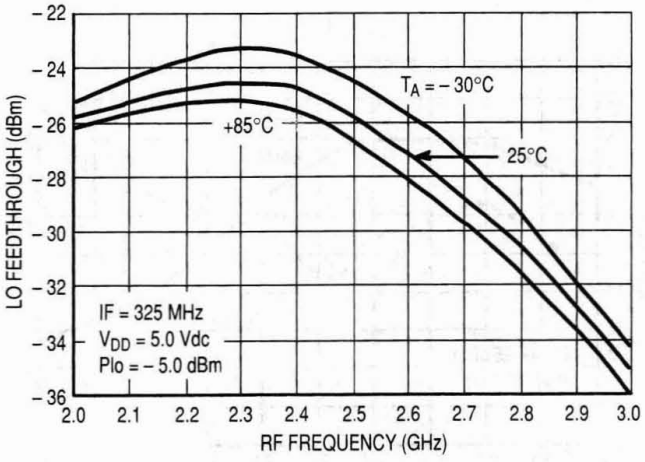


Figure 12. Mixer LO Feedthrough versus RF Frequency

DESIGN AND APPLICATIONS INFORMATION

The MRFIC2401 consists of a two–stage GaAs MESFET low noise amplifier and a single ended MESFET mixer. The LNA design conserves bias current through stacking of the two FETs, thus reusing the current. The mixer consists of a common gate stage driving a common source stage with the IF output being the drain of the common source stage shunted with 15 pF. The LNA output and mixer input have been separated to allow the addition of an external image filter. Such a filter, usually ceramic, is useful in improving the mixer noise figure and third order intercept performance. It also provides LO rejection to reduce the amount of LO power which may leak to the antenna. Alternatively, image trapping can be implemented at the LNA input or output with discrete or distributed components.

The design has been optimized for best performance from 2.4 to 2.5 GHz, but the device is usable with reduced performance from 2.0 to 3.0 GHz as shown in the performance curves. These curves were generated using the circuit shown in Figure 1 and performance above 2.5 GHz can be enhanced by rematching the LO input port. Matching circuit details are shown for IFs of 110 MHz, 240 MHz, and 325 MHz matched to 50 Ω and LO frequencies consistent with an RF frequency of 2.45 GHz. Customized IF matching can be accomplished by using the Equivalent IF Output circuit model shown in Figure 2. The best gain/noise figure tradeoff match is shown in the LNA input impedance column of Table 1. The LO input impedance is shown in the same table. These numbers are derived from conjugate match measurements of the applications circuit. The LNA output and mixer input are matched to 50 Ω.

As with all RF circuitry, layout is important. Controlled impedance lines should be used at all RF ports. RF bypassing of power supply connections as close to the part as possible, while not always shown in the applications circuit, are recommended. Additional power supply "stiffening" and digital transient bypassing should be accomplished with electrolytic or tantalum capacitors.

The device can be placed in a reduced current "standby" mode by applying 5.0 Vdc to the STANDBY pin and removing the LO drive. Further current reduction "sleep" mode, is enabled by applying 0 Vdc to V_{DD}/SLEEP. This sleep mode can also be used to disable the LNA under high signal level conditions and give higher input intercept point if V_{DD} is still applied to the mixer.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

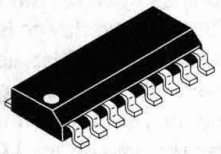
2.4 GHz GaAs Power Amplifier

MRFIC2403

2.4 GHz
POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

The MRFIC2403 is a two–stage class B GaAs power amplifier in a low–cost 16 lead plastic package designed for use in the 2.4 to 2.5 GHz Industrial–Scientific–Medical (ISM) band. The design is optimized for efficiency at 5.0 Volt operation at 2.5 GHz but is usable from 2.0 to 3.0 GHz in applications such as telemetry and Multichannel Multipoint Distribution System (MMDS) wireless cable TV systems. Performance is suitable for frequency hopping or direct sequence spread spectrum as well as single–frequency applications. Power control circuitry allows 20 dB dynamic range for setting the output power.

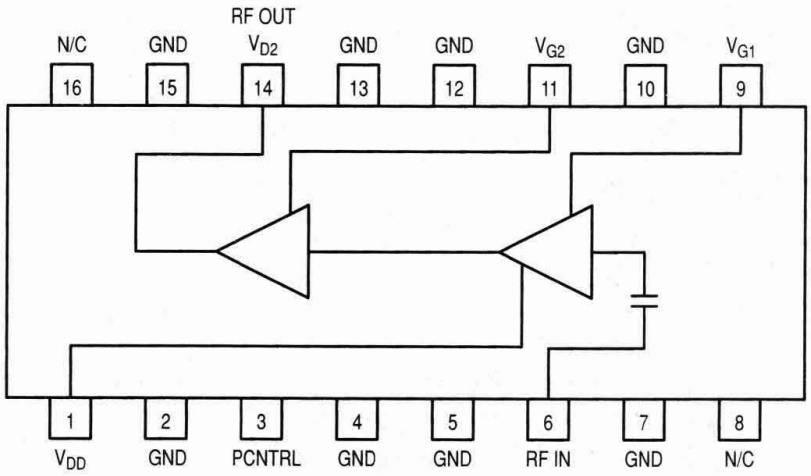
- High Output Power = +23.5 dBm Typical
- High Gain = 23 dB Typical
- Excellent Efficiency = 55% Typical
- Power Control = 20 dB Range
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC2403R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2403



CASE 751B-05
(SO–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Power Control Voltage	V_{CONTRL}	6.0	Vdc
Gate Bias Voltage	V_{G1}, V_{G2}	–4.0	Vdc
RF Input Power	RF IN	+10	dBm
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



Pin Connections and Functional Block Diagram

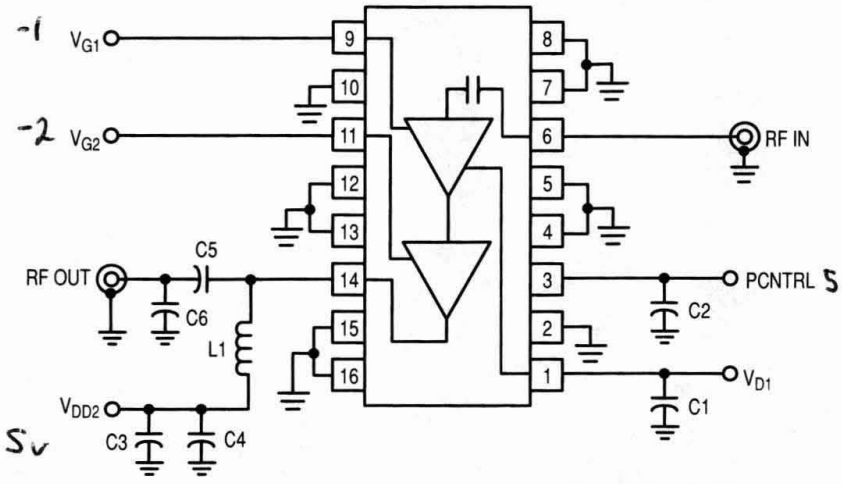
REV 1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.75 to 5.25	Vdc
Gate Bias Voltage, Input Stage	V_{G1}	–1.0	Vdc
Gate Bias Voltage, Output Stage	V_{G2}	–2.0	Vdc
Quiescent Drain Current, Stage One	I_{DQ1}	12	mA
Quiescent Drain Current, Stage Two	I_{DQ2}	10	mA
Operating Frequency Range	f_{OP}	2200 to 2700	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 Vdc, T_A = 25°C, RF = 2.45 GHz @ +4.0 dBm, V_{G1} = –1.0 Vdc, V_{G2} = –2.0 Vdc, PCNTRL = 5.0 Vdc)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{in} = –6.0 dBm)	–	23	–	dB
Power Output (P_{in} = +4.0 dBm)	23	23.5	–	dBm
Power Output, Saturation	–	23.5	–	dBm
Power Output, 1.0 dB Compression	–	19	–	dBm
2nd Harmonic Output	–	–20	–	dBc
3rd Harmonic Output	–	–30	–	dBc
Third Order Intermodulation Products (P_{in} = +4.0 dBm PEP)	–	–15	–	dBc
Reverse Isolation	–	32	–	dB
Power Control Range, PCNTRL	–	20	–	dB
Reverse Isolation	–	30	–	dB
Supply Current	–	95	140	mA
SLEEP Mode Supply Current (VG1 = VG2 = –3.0 Vdc, PCNTRL = 0 Vdc)	–	150	–	μA



C1, C2, C3 – 0.01 μF
C4 – 5.1 pF
C5 – 15 pF
C6 – 1.0 pF
L1 – 6.8 nH
Board Material – 30 MIL FR4
Connectors – SMA type

12 dB att from 100mW input

Figure 1. Applications Circuit Configuration

Table 1. Class A Scattering Parameters

(VDD = 5 V, I_{DQ1} = 24 mA, I_{DQ2} = 96 mA, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
2000	0.377	–157.00	27.625	57.40	0.004	–74.70	0.740	–102.10
2050	0.218	–171.70	28.938	36.80	0.006	–101.60	0.763	–115.30
2100	0.075	–178.80	29.088	17.20	0.007	–130.70	0.724	–126.80
2150	0.049	–96.10	27.904	–0.20	0.007	–163.20	0.663	–135.80
2200	0.104	–56.60	26.930	–14.90	0.008	–169.60	0.601	–141.80
2250	0.130	–60.60	24.246	–27.80	0.009	173.50	0.550	–146.30
2300	0.125	–65.40	24.286	–39.40	0.010	165.00	0.504	–149.10
2350	0.106	–67.60	22.287	–49.60	0.010	157.70	0.471	–151.60
2400	0.083	–56.10	21.867	–59.80	0.009	140.70	0.444	–153.80
2450	0.064	–27.00	21.837	–68.90	0.011	141.40	0.422	–155.90
2500	0.072	26.20	20.113	–78.00	0.012	139.80	0.401	–158.60
2550	0.110	44.60	19.828	–86.40	0.009	140.00	0.385	–161.20
2600	0.160	44.50	18.941	–94.30	0.007	124.50	0.364	–164.50
2650	0.194	40.60	18.001	–101.90	0.012	128.30	0.350	–167.70
2700	0.237	36.60	17.268	–109.20	0.011	102.30	0.335	–171.40
2750	0.269	31.30	16.379	–116.30	0.010	110.90	0.317	–174.50
2800	0.304	25.50	15.826	–123.40	0.009	105.80	0.311	–178.60
2850	0.325	19.80	15.125	–130.40	0.010	103.60	0.292	177.50
2900	0.345	14.50	14.611	–137.50	0.008	99.70	0.279	172.80
2950	0.356	9.40	14.048	–143.60	0.009	92.80	0.271	168.90
3000	0.370	2.40	13.663	–150.40	0.011	88.20	0.259	163.80

Table 2. Class B Scattering Parameters

(VDD = 5 V, I_{DQ1} = 12 mA, I_{DQ2} = 10 mA, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
2000	0.634	–149.00	12.40	88.00	0.007	–59.00	0.893	–81.00
2050	0.554	–170.00	14.76	72.00	0.013	–81.00	0.966	–89.00
2100	0.456	163.00	17.00	53.00	0.015	–95.00	0.990	–100.00
2150	0.362	129.00	18.09	32.00	0.017	–117.00	0.955	–110.00
2200	0.310	91.00	18.81	12.00	0.020	–138.00	0.870	–119.00
2250	0.298	58.00	17.37	–5.00	0.021	–156.00	0.771	–125.00
2300	0.298	30.00	17.22	–21.00	0.021	–169.00	0.681	–128.00
2350	0.289	11.00	15.89	–34.00	0.020	179.00	0.612	–130.00
2400	0.275	0.00	14.74	–45.00	0.020	168.00	0.562	–130.00
2450	0.248	–8.00	15.35	–56.00	0.021	155.00	0.528	–131.00
2500	0.216	–10.00	13.62	–66.00	0.019	147.00	0.498	–131.00
2550	0.199	–8.00	13.46	–75.00	0.021	143.00	0.473	–132.00
2600	0.187	–2.00	12.95	–83.00	0.020	134.00	0.447	–132.00
2650	0.185	4.00	12.32	–91.00	0.020	129.00	0.426	–134.00
2700	0.202	10.00	11.78	–99.00	0.021	123.00	0.405	–135.00
2750	0.218	13.00	11.25	–107.00	0.021	115.00	0.384	–136.00
2800	0.244	14.00	10.83	–114.00	0.018	106.00	0.373	–137.00
2850	0.268	13.00	10.34	–121.00	0.019	98.00	0.353	–139.00
2900	0.285	10.00	10.05	–129.00	0.019	99.00	0.332	–140.00
2950	0.301	7.00	9.61	–135.00	0.018	102.00	0.316	–143.00
3000	0.317	3.00	9.46	–142.00	0.018	90.00	0.302	–145.00

TYPICAL CHARACTERISTICS

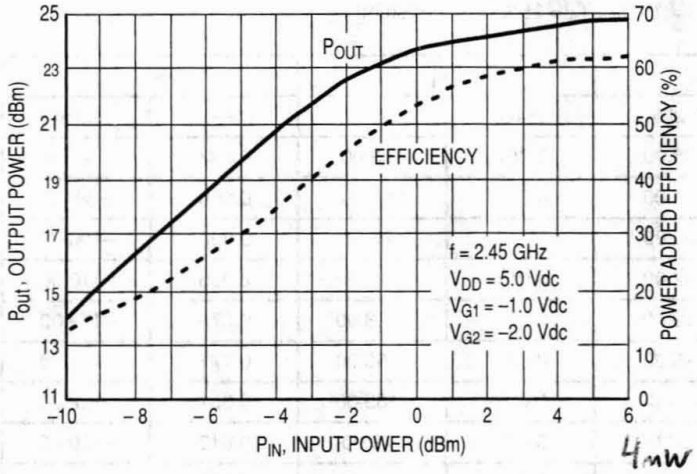


Figure 2. Output Power and Efficiency versus Input Power

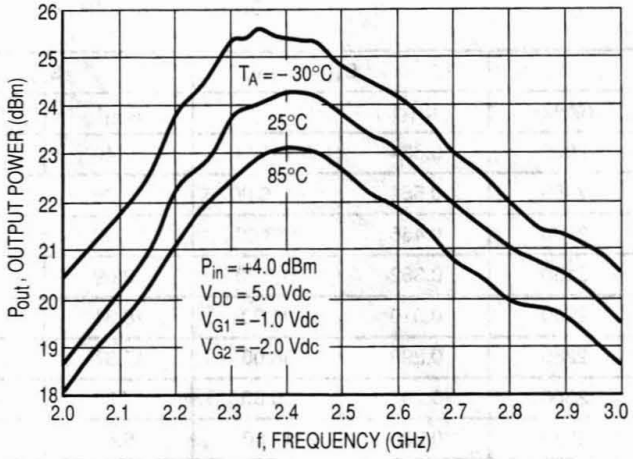


Figure 3. Output Power versus Frequency

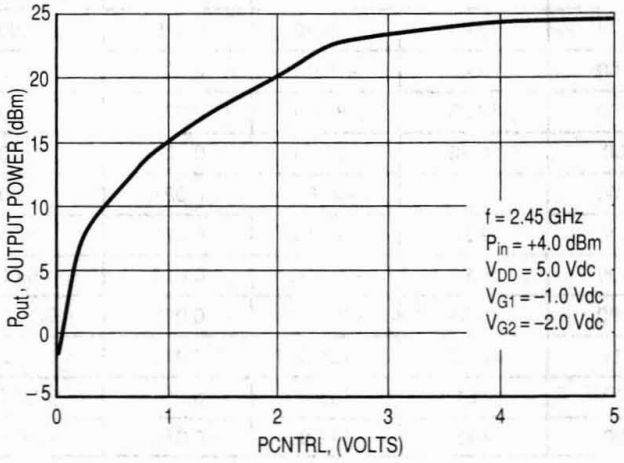


Figure 4. Output Power versus PCNTRL Voltage

DESIGN AND APPLICATIONS INFORMATION

The MRFIC2403 is a two–stage power amplifier designed using Motorola's MAFET planar, refractory gate MESFET IC process. The RF MESFETs are power, depletion mode devices and, therefore, require negative bias on the MESFET gates. For class B operation, –1.0 Vdc is applied to V_{G1} and –2.0 Vdc is applied to V_{G2}. Class A biasing will yield slightly higher gain and 1.0 dB compression point and can be accomplished by adjusting the bias on VG1 for I_{DQ1} = 24 mA and V_{G2} for I_{DQ2} = 96 mA. Where negative voltages are not already available, Motorola's MC33128 Power Management IC can produce –2.5 Vdc from a single positive supply.

The device is capable of better than +23 dBm saturated output power in the 2.4 to 2.5 GHz ISM band with the output matching circuit shown in Figure 1. The device can be operated at other frequencies in the 2.0 GHz to 3.0 GHz range with this circuit but performance can be improved with tuning for the specific frequency of use. Input matching is provided on chip. This circuit provides the best gain, saturated output power and efficiency tradeoff. Saturated operation has the advantage of best efficiency with less variation in performance over frequency and temperature. Operation in saturation is acceptable for constant envelope modulation schemes such as 2 and 4 level FM as specified for frequency hopping (FHSS) radios in the proposed IEEE 802.11 PHY layer specification. For direct sequence (DSSS) IEEE 802.11 operation, where differential binary phase shift keying (DBPSK) and differential quadrature phase shift keying (DQPSK) are specified, the amplifier will have to be "backed off" from saturation by 5.0 dB or more to avoid spectral regrowth. Care must be taken in the layout of the circuit and controlled impedance lines must be used at the RF pins. Capacitive bypassing as shown in the Applications Circuit must be implemented as close to the chip as possible to avoid amplifier instability. Additionally, the supply voltage should be supported by sufficient "stiffening" capacitance, typically electrolytic or tantalum bypass capacitors, to eliminate noise from digital circuits.

Output power control is accomplished by varying the voltage on the PCNTRL pin. 0 Vdc gives minimum output and reduces the current drawn by the amplifier to the quiescent value. The amplifier can be put into "sleep" mode by decreasing the voltage on the gate bias pins to –3.0 Vdc and the current drain is reduced to a few hundred microamps.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

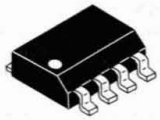
2.4 GHz GaAs Exciter Amplifier

MRFIC2404

2.4 GHz
EXCITER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

The MRFIC2404 is a single–stage class A GaAs amplifier in a low–cost 8 lead plastic package designed to drive the MRFIC2403 power amplifier for use in the 2.4 to 2.5 GHz Industrial–Scientific–Medical (ISM) band. The design is optimized for 5.0 Volt operation at 2.45 GHz but is usable from 2.0 to 3.0 GHz in applications such as telemetry and Multichannel Multipoint Distribution System (MMDS) wireless cable TV systems. Performance is suitable for frequency hopping or direct sequence spread spectrum as well as single–frequency applications.

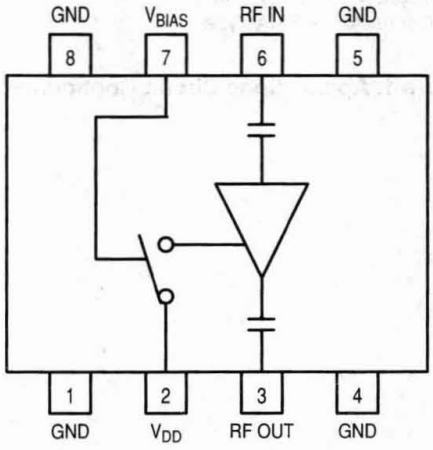
- High Output Capability = +5.0 dBm Typical
- High Gain = 17 dB Typical
- Low Current Drain = 9.0 mA Typical
- Single Supply Voltage = 5.0 Volts
- Good Noise Figure = 4.3 dB Typical
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC2404R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2404



CASE 751-06
(SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	12	Vdc
RF Input Power	RF IN	+10	dBm
Bias Enable Voltage	V_{bias}	6.0	Vdc
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



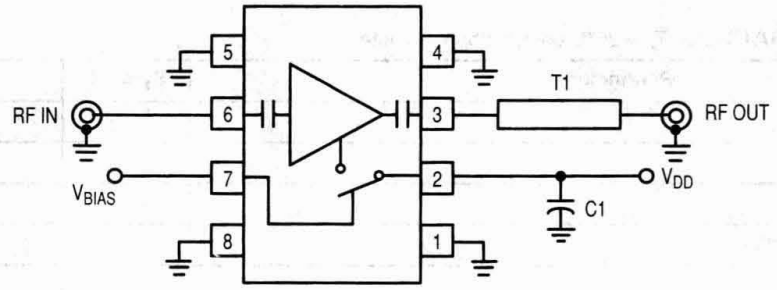
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.75 to 5.25	Vdc
Bias Enable Voltage – ON	V_{bias}	0	Vdc
Bias Enable Voltage – OFF	V_{bias}	5.0	Vdc
Operating Frequency Range	f_{OP}	2000 to 3000	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 Vdc, T_A= 25°C, RF = 2.45 GHz, V_{bias} = 0 Vdc)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain	16	17	–	dB
Power Output, 1.0 dB Compression	–	+5.0	–	dBm
Power Output (P_{in} = –11 dBm)	4.0	5.0	–	dBm
Third Order Intercept Point	–	+15	–	dBm
Noise Figure	–	4.3	–	dB
Reverse Isolation	–	25	–	dB
Turn On Time	–	1.0	–	µs
Supply Current	–	9.0	12	mA
SLEEP Mode Supply Current (V_{bias} = 5.0 Vdc)	–	800	–	µA



C1 – 15 pF
T1 – 100 Ω Line, 185 MILs (3.3 nH)
Board Material – 30 MIL FR4
Connectors – SMA Type

Figure 1. Applications Circuit Configuration

Table 1. Scattering Parameters
(VDD = 5 V, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
2000	0.232	–92.34	6.290	165.97	0.024	–51.08	0.483	–123.13
2050	0.174	–90.78	7.049	147.75	0.029	–66.26	0.383	–125.77
2100	0.122	–76.88	7.563	127.95	0.032	–78.38	0.281	–124.34
2150	0.102	–48.38	7.803	109.02	0.035	–97.84	0.191	–109.23
2200	0.128	–19.45	8.046	91.04	0.037	–105.62	0.159	–80.33
2250	0.185	–6.60	8.144	72.36	0.039	–123.88	0.196	–53.35
2300	0.244	–5.52	7.977	55.31	0.038	–135.36	0.273	–42.38
2350	0.300	–8.04	7.979	39.91	0.043	–144.83	0.350	–41.15
2400	0.343	–12.42	8.147	23.40	0.044	–160.94	0.423	–43.39
2450	0.379	–17.11	8.020	5.27	0.045	–173.09	0.477	–47.05
2500	0.403	–21.90	7.550	–10.93	0.041	173.83	0.522	–50.67
2550	0.424	–26.32	7.245	–25.36	0.043	165.85	0.556	–54.67
2600	0.436	–30.95	6.911	–39.88	0.042	154.14	0.582	–58.35
2650	0.443	–34.94	6.631	–52.32	0.041	145.35	0.600	–62.23
2700	0.447	–39.48	6.566	–65.57	0.044	135.12	0.610	–65.41
2750	0.445	–43.12	6.338	–79.97	0.043	123.72	0.622	–68.57
2800	0.446	–46.68	6.009	–93.15	0.042	114.52	0.624	–72.06
2850	0.441	–50.42	5.733	–105.10	0.043	107.18	0.620	–74.86
2900	0.439	–53.14	5.565	–116.69	0.041	98.95	0.617	–77.74
2950	0.437	–57.27	5.393	–129.54	0.042	90.72	0.608	–80.01
3000	0.409	–61.28	4.938	–142.70	0.043	81.68	0.611	–81.12

Typical Characteristics

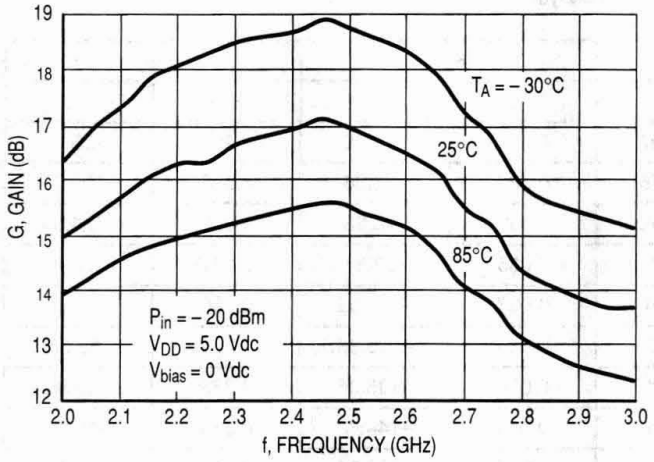


Figure 2. Gain versus Frequency

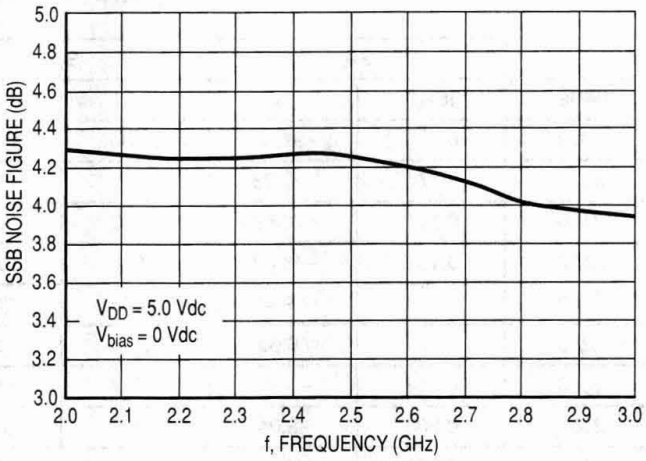


Figure 3. Noise Figure versus Frequency

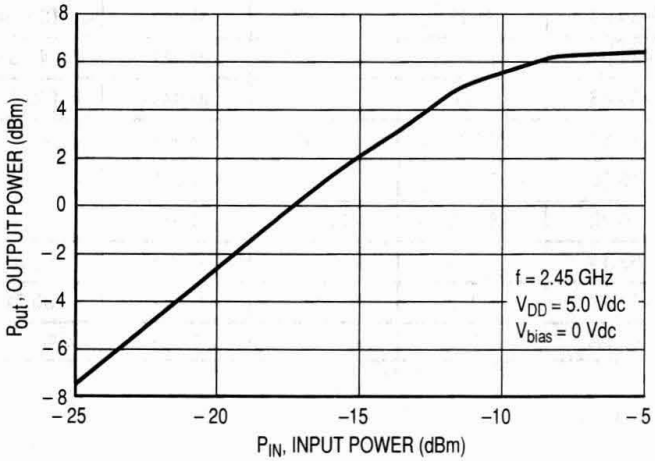


Figure 4. Output Power versus Input Power

DESIGN AND APPLICATIONS INFORMATION

The MRFIC2404 is a single–stage GaAs amplifier designed for exciter applications such as driving the MRFIC2403 power amplifier. The 4.3 dB noise figure, 17 dB gain and +5.0 dBm power output at 1.0 dB gain compression make the MRFIC2404 suitable for high–performance receiver IF application, Multichannel Multipoint Distribution System (MMDS) applications, telemetry and other applications in the 2.0 to 3.0 GHz range.

The characterization curves show typical performance in the 2.0 to 3.0 GHz range in the circuit shown in Figure 1. This circuit was also used to derive the device impedance shown in Table 1. The amplifier input is matched to 50 Ω while the output requires about 3.3 nH series inductance for best match at 2.45 GHz. The V_{DD} supply line should be bypassed as close to the chip as possible to avoid low frequency oscillations. Power supply "stiffening" and digital transient bypassing in the form of electrolytic of tantalum capacitors should be added.

The device can be put into a reduced current "sleep" mode by 5.0 Vdc to the V_{bias} pin.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

Advance Information

The MRFIC Line

2.4 GHz Upmixer

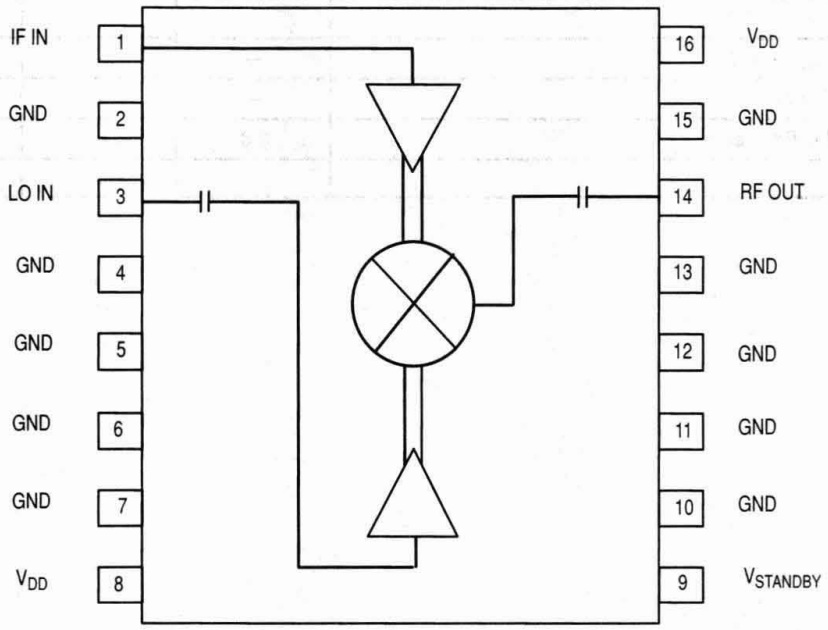
MRFIC2406

2.4 GHz
INTEGRATED UPMIXER
GaAs MONOLITHIC
INTEGRATED CIRCUIT

Designed primarily for use in Industrial, Scientific, Medical (ISM) frequency band applications, the MRFIC2406 is an active GaAs upmixer in a low–cost SOIC 16–lead, surface mount package. The integrated circuit has internal active Baluns and requires minimal off-chip matching. In STANDBY mode, the device draws less than 0.6 mA for low battery drain.

- Usable Frequency Range = 2 to 3 GHz
- Single Voltage Supply = 3 to 5 Volts
- Low Current Drain = 15 mA Max Supply Current
- IF to RF Conversion Gain = 6 dB Typical
- STANDBY Mode for Low Current Consumption
- No External Baluns Required
- Simple Off-Chip Matching for Maximum Flexibility
- Order MRFIC2406R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2406

CASE 751B–05
(SO–16)



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

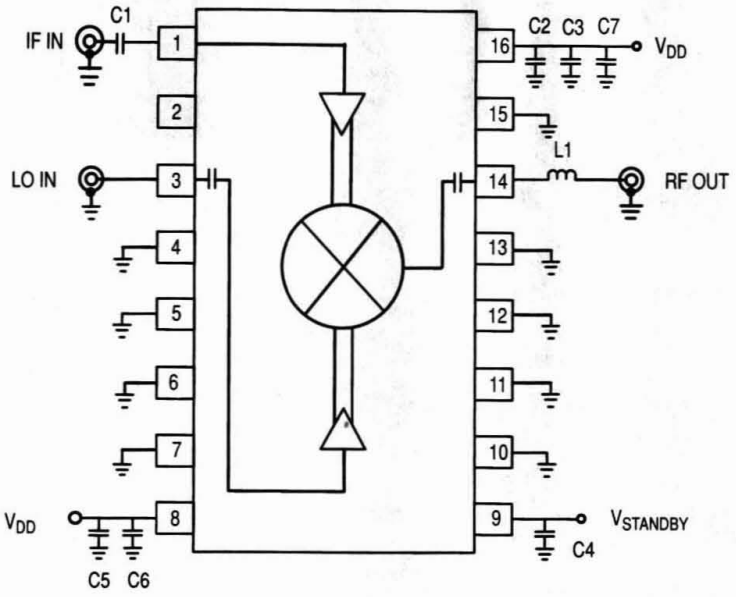
Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	7	Vdc
Standby Voltage	$V_{STANDBY}$	7	Vdc
IF Input Power	IF IN	+10	dBm
LO Input Power	LO IN	+10	dBm
Storage Temperature Range	T_{stg}	– 65 to +125	°C
Ambient Operating Temperature	T_A	– 35 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	2.4 to 2.5	GHz
IF Frequency	f_{IF}	100 to 370	MHz
LO Frequency	f_{LO}	2.03 to 2.4	GHz
Supply Voltage	V_{DD}	3 to 5	Vdc
Standby Voltage	$V_{STANDBY}$	0 to 3	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, f_{RF} = 2.45 GHz, f_{IF} = 237 MHz, IF IN = –15 dBm, f_{LO} = 2.213 GHz, LO IN = –5 dBm, $V_{STANDBY}$ = 0 V, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
IF to RF Conversion Gain	4	6	—	dB
LO to RF Isolation	10	12	—	dB
Return Loss, All Ports, (Matching as shown in Figure 1)	–10	–12	—	dB
Spurious Output @ 2.4–2.5 GHz	—	—	–55	dBc
Output 1dB Gain Compression	—	–10	—	dBm
ON State Current, ($V_{STANDBY}$ = 0 V)		—	15	mA
OFF State Current, ($V_{STANDBY}$ = 3 V)	—	—	0.6	mA
$V_{STANDBY}$ Voltage (ON State)	—	—	0.1	V
$V_{STANDBY}$ Voltage (STANDBY State)	2.8	—	—	V
On/Off Switching Time	—	1	—	µsec



C1	240 pF
C2	1000 pF
C3, C4, C5, C8	15 pF
C6	100 pF
C7	10,000 pF
L1	2.2 nH

Figure 1. Applications Circuit Configuration

Chapter Three
RF/IF Integrated Circuits

Section One **3.1–0**
RF/IF Integrated Circuits – Selector Guide

Section Two **3.2–0**
RF/IF Integrated Circuits – Data Sheets

Section One
Selector Guide

Motorola RF/IF Integrated Circuits

Radio communication has greatly expanded its scope in the past several years. Once dominated by public safety radio, the 30 to 1000 MHz spectrum is now packed with personal and low cost business radio systems. The vast majority of this equipment uses FM or FSK modulation and is targeted at short range applications. From mobile phones and VHF marine radios to garage door openers and radio controlled toys, these new systems have become a part of our lifestyle. Motorola has focused on this technology, adding a wide array of new products including complete receivers processed in our exclusive 3.0 GHz MOSAIC® 1.5 process. New surface mount packages for high density assembly are available for all of these products, as well as a growing family of supporting application notes.

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Motorola RF/IF Monolithic Integrated Circuits

Table 1. RF Front End ICs

Receiver												
	Low Noise Amplifier				Mixer							
Device	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	Input P1dB (dBm)	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	P1dB (dBm)	Voltage Cont Osc	V_{CC} (V)	I_{CC} (mA)	Suffix/ Package
MC13142	17	1.8	–5.0	–15	±3.0	12	–3 to +21	3.0	Yes	2.7 to 6.5	13	D/751B
MC13143	–	–	–	–	±3.0	12	–3 to +21	3.0	–	1.8 to 6.5	1.0	D/751
MC13144	13 to 19	1.4	–1.0	–7.0	–	–	–	–	–	1.8 to 6.5	2 to 9	D/751
MC13145	14	1.8	–5.0	–8.0	0	13	9.0	–1.0	Yes	2.7 to 6.5	30	FTA/932
Transmitter												
	Low Power Amplifier				Mixer							
Device	PA Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	Output P1dB (dBm)	P_{IFOut} (dB)	Noise Figure (dB)	IIP3 (dBm)	P1dB (dBm)	Voltage Cont Osc	V_{CC} (V)	I_{CC} (mA)	Suffix/ Package
MC13146	15	–	–	8.0	15	–	10	–	Yes	2.7 to 6.5	25	FTA/977

NOTES: All devices operate over a wide range of RF input and IF frequencies, from dc to 2.0 GHz.
Typical performance shown at 900 MHz.

Table 2. Wideband (FM/FSK) IFs

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC13055	3–12 V	25 mA	20 µV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF, includes data shaper	P/648, D/751B
MC13155	3–6 V	7.0 mA	100 µV	250 MHz	–		10 Mb	Video Speed FM IF	D/751B

Table 3. Wideband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3356	3–9 V	25 mA	30 µV	200 MHz	10.7 MHz	✓	✓	500 kb	Includes front end mixer/L.O.	P/738, DW/751D
MC13156	2–6 V	5.0 mA	2.0 µV	500 MHz	21.4 MHz	–			CT–2 FM/Demodulator	DW/751E, FB/873
MC13158	2–6 V	6.0 mA						>1.2 Mb	FM IF/Demodulator with split IF for DECT	FTB/873
MC13159	2.7–5 V	5.5 mA		600 MHz				500 kb	FM IF for PHS	DTB/948F

Table 4. Narrowband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3357	4–8 V	5.0 mA	5.0 μV	45 MHz	455 kHz	✓	–	>4.8 kb	Ceramic Quad Detector/Resonator	P/648, D/751B
MC3359	4–9 V	7.0 mA	2.0 μV						Scan output option	P/707, DW/751D
MC3371	2–8 V	6.0 mA		60 MHz			✓	>4.8 kb	RSSI	P/648, D/751B, DTB/948F
MC3372									RSSI, Ceramic Quad Detector/Resonator	
MC13150	3–6 V	1.8 mA	1.0 μV	500 MHz			✓ 110 dB	>9.6 kb	Coilless Detector with Adjustable Bandwidth	FTB/873, FTA/977

Table 5. Narrowband Dual Conversion Receivers – FM/FSK – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF1	IF2 (Limiter In)	Mute	RSSI	Data Rate	Notes	Suffix/ Package
MC3362	2–7 V	3.0 mA	0.7 μV	180 MHz	10.7 MHz	455 kHz	–	✓	> 4.8 kb	Includes buffered VCO output	P/724, DW/751E
MC3363		4.0 mA	0.4 μV				✓			Includes RF amp/mute	DW/751F
MC13135			1.0 μV				–			Voltage buffered RSSI, LC Quad Detector	DW/751E, P/724
MC13136										Voltage Buffered RSSI, Ceramic Quad Detector	DW/751E

Table 6. Universal Cordless Phone Subsystem ICs

Device	V_{CC}	I_{CC}	Dual Conversion Receiver	Universal Dual PLL	Compander and Audio Interface	Voice Scrambler	Low Battery Detect	Programmable R_x, T_x Trim Gain and LBD Voltage Reference	Suffix/ Package
MC13109	2.0–5.5 V	Active Mode 6.7 mA Inactive Mode 40 μA	✓	✓	✓	–	1	–	FB/848B, FTA/932
MC13110	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 μA	✓	✓	✓	✓	2	✓	FB/848B
MC13111	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 μA	✓	✓	✓	–	2	✓	FB/848B

Table 7. Transmitters – AM/FM/FSK

Device	V_{CC}	I_{CC}	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Package
MC2833	3–8 V	10 mA	–30 dBm to +10 dBm	150 MHz	50 kHz	FM transmitter. Includes two frequency multiplier/amplifier transistors	P/648, D/751B
MC13175	2–5 V	40 mA	8.0 dBm	500 MHz	5.0 MHz	AM/FM transmitter. Single frequency PLL $f_{out} = 8 \times f_{ref}$, includes power down function	D/751B
MC13176				1.0 GHz		$f_{out} = 32 \times f_{ref}$, includes power down function	

Table 8. Balanced Modulator/Demodulator

Device	V_{CC}	I_{CC}	Function	Suffix/ Package
MC1496	3–5 V	10 mA	General purpose balanced modulator/demodulator for AM, SSB, FM detection with Carrier Balance >50 dB	P/646, D/751A

Table 9. Infrared Transceiver

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Max IF Freq	Carr Det	RSSI	Data Rate	Notes	Suffix/ Package
MC13173	3–5 V	6.5 mA	5.0 µV	10.7 MHz	✓	✓	200 kb	Includes Single Frequency PLL for T_x Carrier and R_x L_O	FTB/873

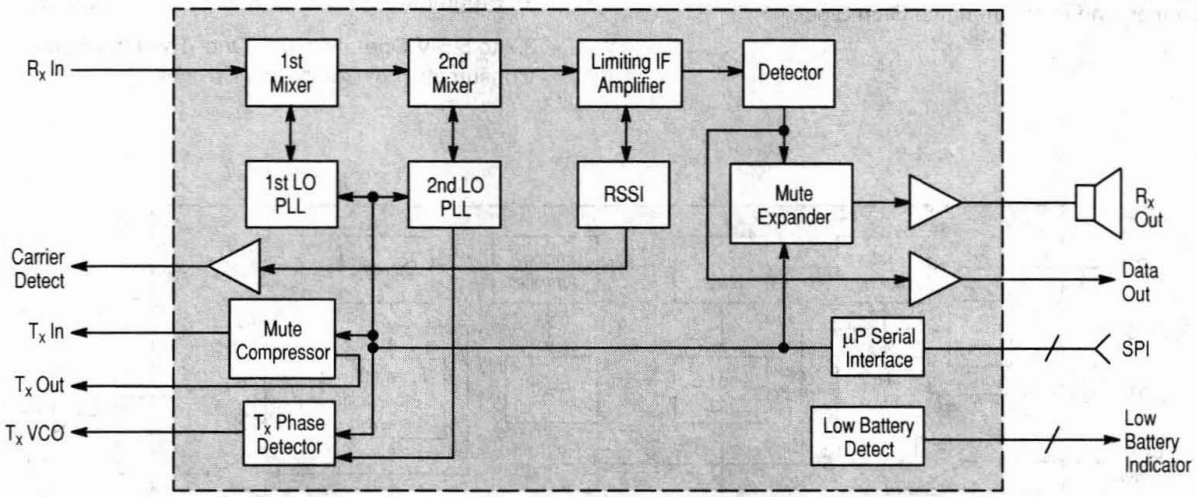
Universal Cordless Telephone Subsystem IC

MC13109FB, FTA

T_A = −20° to +85°C, Case 848B, 932

The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



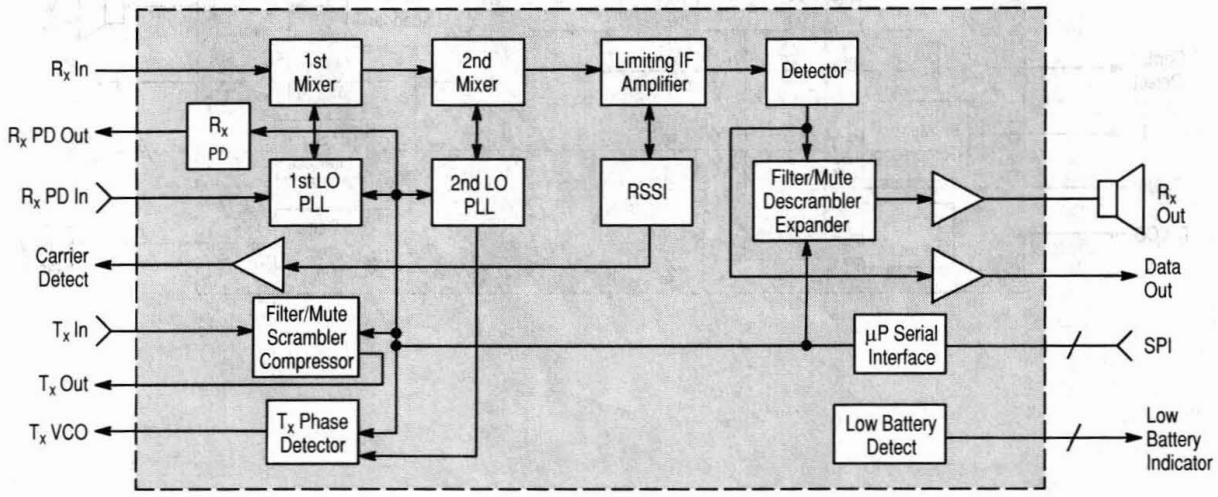
Universal Cordless Telephone Subsystem IC with Scrambler

MC13110FB

T_A = –40° to +85°C, Case 848B

The MC13110 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with New External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Frequency Inversion Scrambler/Descrambler
  - Can Be Enabled/Disabled Via MPU Interface
  - Programmable Carrier Modulation Frequency
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices

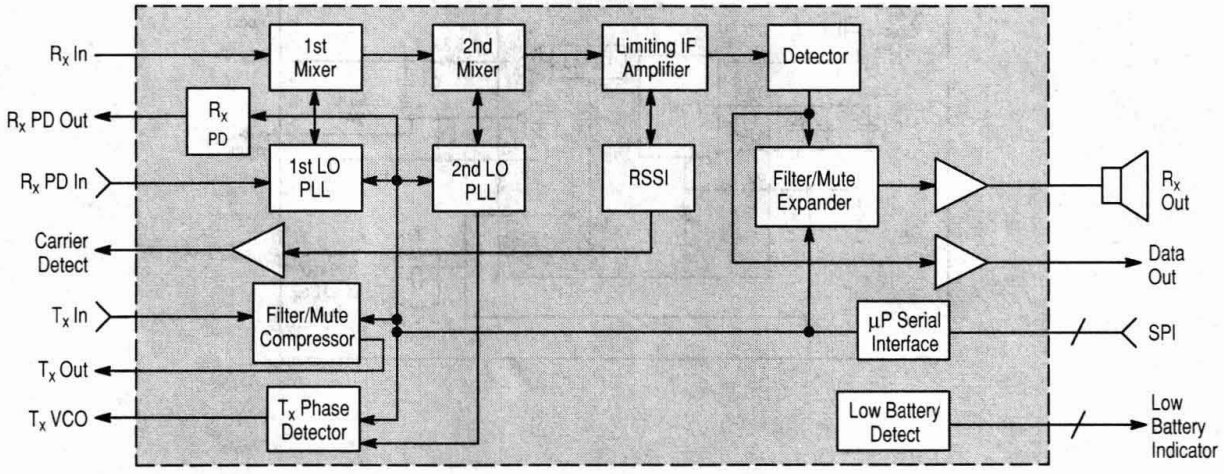


MC13111FB

T_A = –40° to +85°C, Case 848B, 932

The MC13111 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, external adjustments, and lowers overall costs. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Programmable Corner Frequency Selection
- MC13111 is Pin–for–Pin Compatible with MC13110
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices
- AN1575: Refer to this Application Note for a List of the "Worldwide Cordless Telephone Frequencies" (List can also be found in Chapter 8 Addendum of DL128 Data Book)



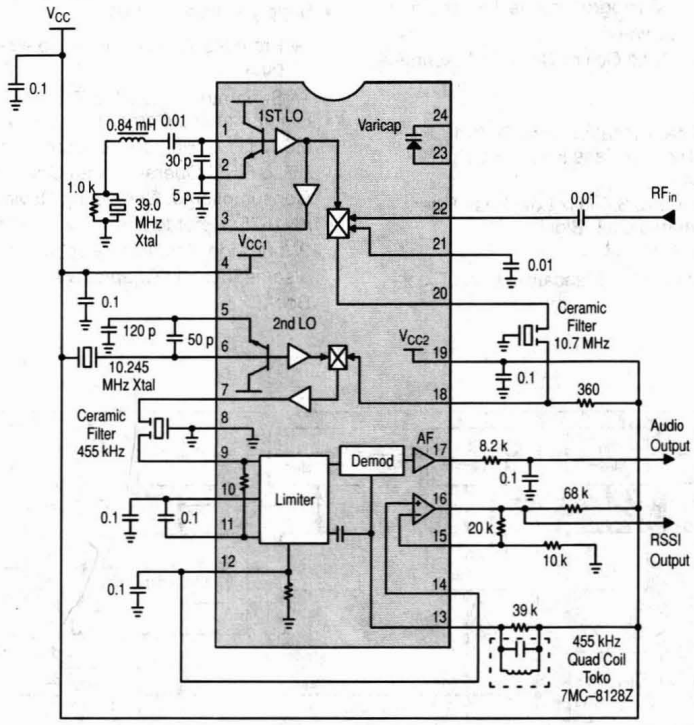
Narrowband FM Receiver

MC13135P,DW, MC13136DW

T_A = –40° to +85°C, Case 724, 751E

The MC13135 is a full dual conversion receiver with oscillators, mixers, Limiting IF Amplifier, Quadrature Discriminator, and RSSI circuitry. It is designed for use in security systems, cordless phones, and VHF mobile and portable radios. Its wide operating supply voltage range and low current make it ideal for battery applications. The Received Signal Strength Indicator (RSSI) has 65 dB of dynamic range with a voltage output, and an operational amplifier is included for a dc buffered output. Also, an improved mixer third order intercept enables the MC13135 to accommodate larger input signal levels.

- Complete Dual Conversion Circuitry
- Low Voltage: 2.0 to 6.0 Vdc
- RSSI with Op Amp: 65 dB Range
- Low Drain Current: 3.5 mA Typical
- Improved First and Second Mixer 3rd Order Intercept
- Detector Output Impedance: 25 Ω Typically



Low Power DC – 1.8 GHz LNA, Mixer and VCO

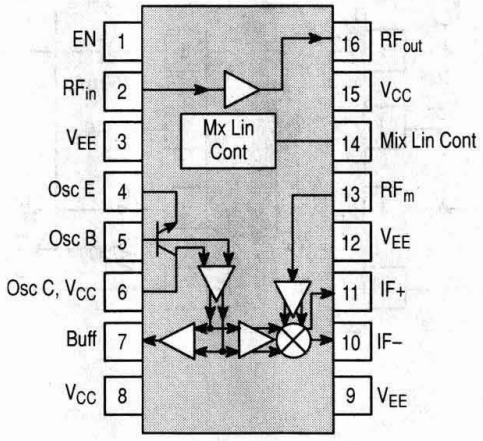
MC13142D

T_A = –40° to +85°C, Case 751B

The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7 – 6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm
- Linearity Adjustment Increases IP_{3in} Up to 20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output

SO–16



Ultra Low Power DC – 2.4 GHz Linear Mixer

MC13143,D

T_A = –40° to +85°C, Case 751

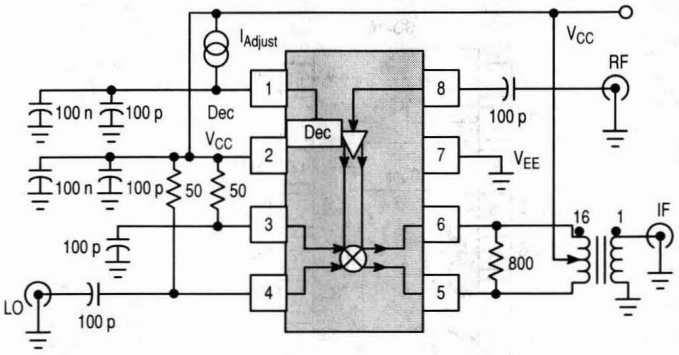
The MC13143 is a high compression linear mixer with single–ended RF input, differential IF output and differential LO inputs which consumes as little as 1.8 mW. A new circuit topology is used to achieve a high third order intermodulation intercept point, high linearity and high 1.0 dB output compression point while maintaining a linear 50 Ω input impedance. It is designed for Up or Down conversion anywhere from dc to 2.4 GHz.

Ultra Low Power: 1.0 mA @ V_{CC} = 1.8 – 6.5 V

- Wide Input Bandwidth: DC–2.4 GHz
- Wide Output Bandwidth: DC–2.4 GHz
- Wide LO Bandwidth: DC–2.4 GHz
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm

Linearity Adjustment of up to IP_{3in} = 20 dBm

- 50 Ω Mixer Input
- Single–Ended Mixer Input
- Double Balanced Mixer Operation
- Differential Open Collector Mixer Output



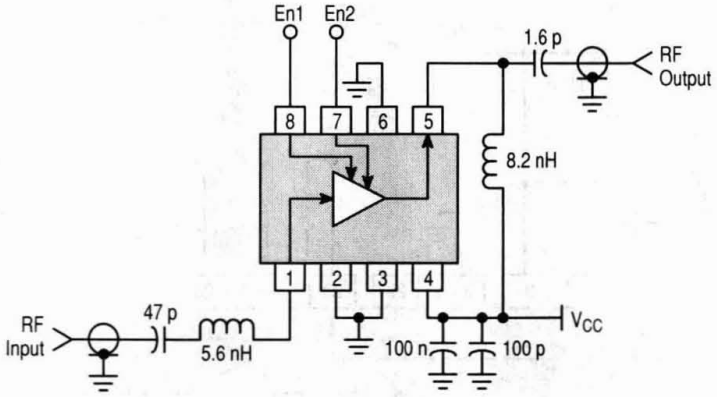
VHF – 2.0 GHz Low Noise Amplifier with Programmable Bias

MC13144,D

T_A = –40° to +85°C, Case 751

The MC13144 is designed in the Motorola High Frequency Bipolar MOSIAC V™ wafer process to provide excellent performance in analog and digital communication systems. It includes a cascoded LNA usable up to 2.0 GHz and at 1.8 Vdc, with 2 bit digital programming of the LNA bias. Targeted applications are in the UHF Family Radio Services, UHF and 800 MHz Special Mobile Radio, 800 MHz Cellular and GSM, PCS, DECT and PHS at 1.8 to 2.0 GHz and Cordless Telephones in the 902 to 928 MHz band covered by FCC Title 47; Part 15. The MC13144 offers the following features:

- 17 dB Gain at 900 MHz
- 1.4 dB Noise Figure at 900 MHz
- 1.0 dB Compression Point of –7.0 dBm; Input Third Order Intercept Point of –5.0 dBm
- Low Operating Supply Voltage (1.8 to 6.0 Vdc)
- Programmable Bias with Enable 1 and Enable 2
- Enable 1 and Enable 2 Programmed High for Optimal Noise Figure and Gain Associated with NF
- Can Override Enable and Externally Program In Up to 15 mA



Narrowband FM Coilless Detector IF Subsystem

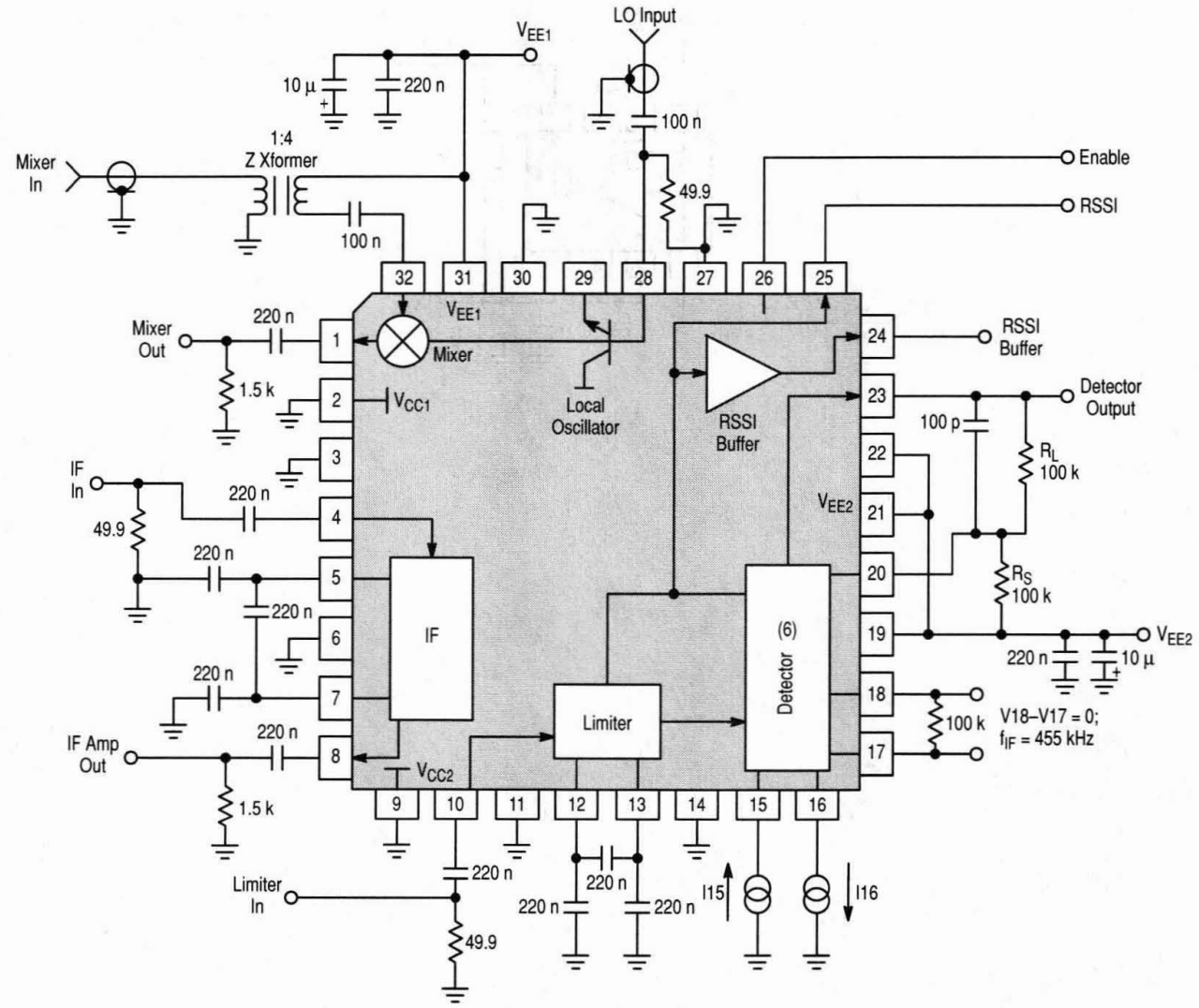
MC13150FTA, FTB

T_A = –40° to +85°C, Case 977, 873

The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 μV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF System

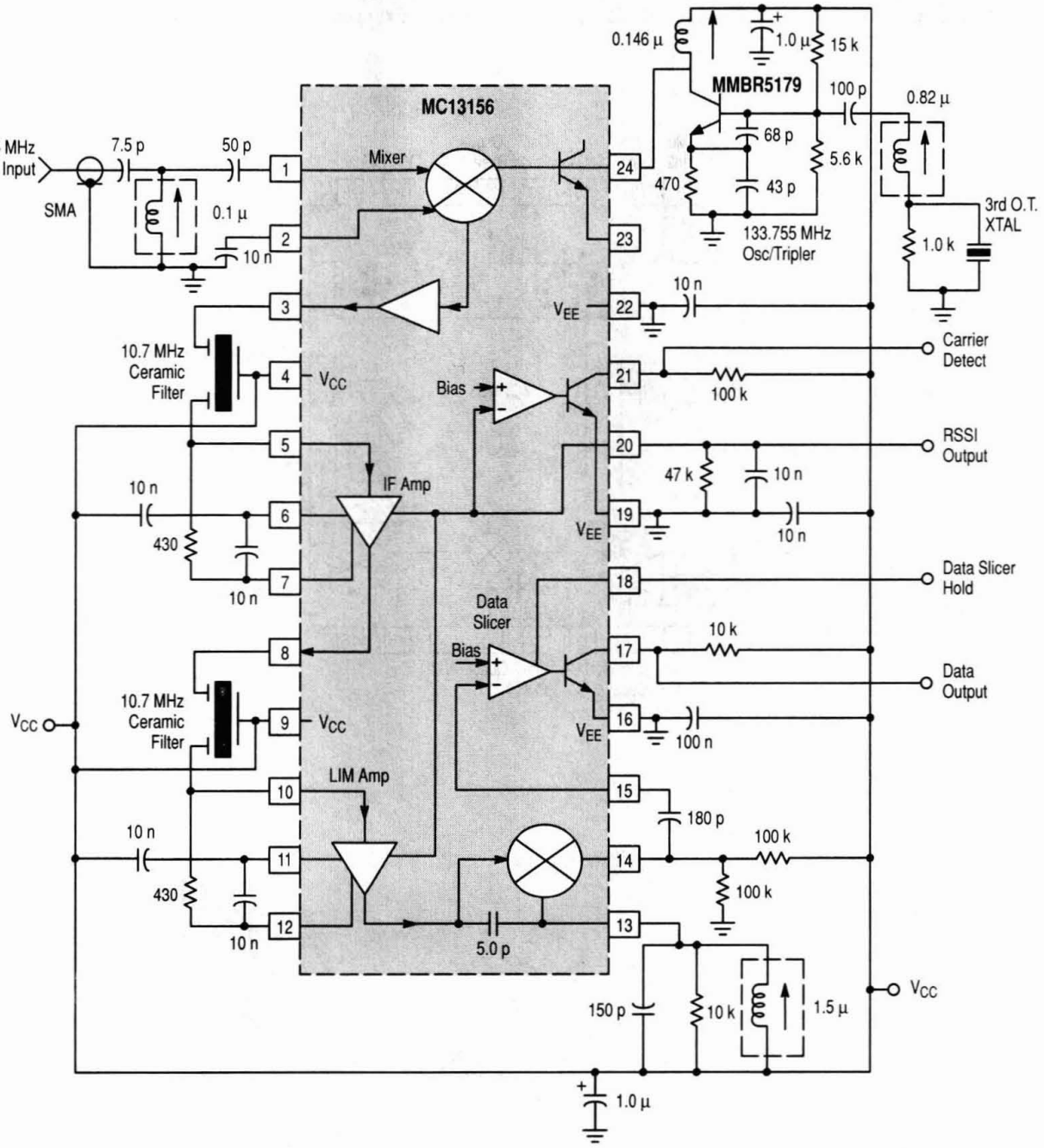
MC13156DW, FB

T_A = –40° to +85°C, Case 751E, 873

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13156 has an onboard Colpitts VCO for PLL controlled multichannel operation. The mixer is useful to beyond 200 MHz and may be used in a differential, balanced, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity of 6.0 μV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 300 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF Subsystem

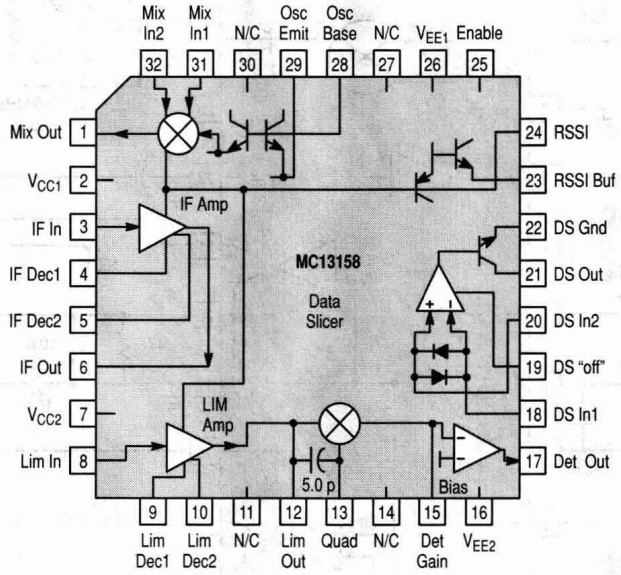
MC13158FTB

T_A = –40° to +85°C, Case 873

The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output "off" to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count



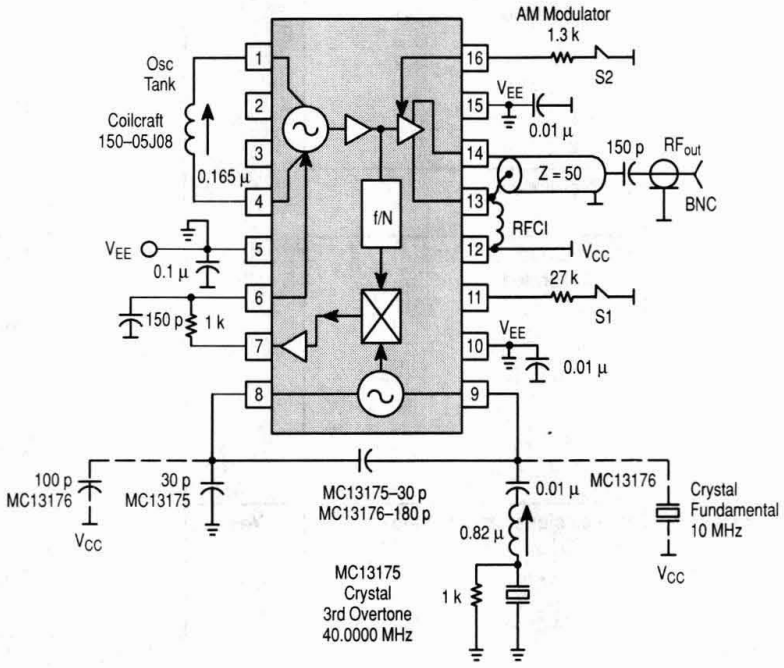
UHF, FM/AM Transmitter

MC13175/176D

T_A = 0° to +70°C, Case 751B

The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems operating in the 260 to 470 MHz band covered by FCC Title 47; Part 15. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷8 (MC13175) or ÷32 (MC13176) prescaler, and phase detector forming a versatile PLL system. Another application is as a local oscillator in a UHF or 900 MHz receiver. MC13175/176 offer the following features:

- UHF Current Controlled Oscillator
- Use Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Low Number of External Parts Required
- Low Operating Supply Voltage (1.8–5 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output "On"/"Off"
- MC13175 – f_o = 8 × f_{ref}
- MC13176 – f_o = 32 × f_{ref}



Phase–Locked Loop Components

Motorola offers a choice of phase–locked loop components ranging from complete functional frequency synthesizers for dedicated applications to a wide selection of general purpose PLL circuit elements. Technologies include CMOS for lowest power consumption and bipolar for high speed operation. Typical applications include TV, CATV, radios, scanners, WLANs, cordless telephones plus home and personal computers.

Table 1. PLL Frequency Synthesizers

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
4 @ 5 V	4.5 to 12	6 @ 5 V	Single–ended 3–state	No	Parallel	MC145106	P/707, DW/751D
15 @ 5 V	3 to 9	–	Two single–ended 3–state		Serial	MC145149*	P/738, DW/751D
		7.5 @ 5 V	Analog			MC145159–1	P/738, DW/751D
20 @ 5 V	3 to 9	7.5 @ 5 V	Single–ended 3–state, double–ended		4–Bit	MC145145–2	P/707, DW/751D
						MC145146–2	P/738, DW/751D
					Parallel	MC145151–2	P/710, DW/751F
			Double–ended			MC145152–2	P/710, DW/751F
			Single–ended 3–state, double–ended		Serial	MC145155–2	P/707, DW/751D
						MC145156–2	P/707, DW/751D
						MC145157–2	P/648, DW/751G
						MC145158–2	P/648, DW/751G
60 @ 3 V	2.5 to 5.5	3 @ 3 V	Two single–ended 3–state	Yes		MC145162*	P/648, D/751B
60 @ 2 V	1.8 to 3.6	1.5 @ 1.8 V				MC145165*	P/648, D/751B
60 @ 3 V	2.5 to 5.5	3 @ 3 V			Parallel	MC145166*	P/648, DW/751G
					Serial	MC145167*	P/648, DW/751G
					Parallel	MC145168*	
					Serial	MC145169*	
85 @ 3 V	2.5 to 5.5	3 @ 3 V				MC145162–1*	P/648, D/751B
40/130 @ 5 V	4.5 to 5.5	9 @ 5 V	Single–ended 3–state, Current source/sink			MC145173	DW/751E
100 @ 3 V 185 @ 5 V	2.5 to 5.5	2 @ 3 V 6 @ 5 V		No		MC145170–1	P/648, D/751B, DT/948C

* Dual PLL

PLL Frequency Synthesizers (continued)

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
1100	4.5 to 5.5	7 @ 5 V	Current source/sink, double–ended	Yes	Serial	MC145190	F/751J, DT/948D
						MC145191	F/751J, DT/948D
1100	2.7 to 5	6 @ 2.7 V				MC145192	F/751J, DT/948D
1100	2.7 to 5.5	12	Two current source/sink, double–ended			MC145220*	F/803C, DT/948D
1200, 400	1.8 to 3.6	5	Loop 1 = Current source/sink Loop 2 = Three–state			MC145225*	FTA/873C
2000	4.5 to 5.5	12 @ 5 V	Current source/sink, double–ended			MC145200	F/751J, DT/948D
2000	4.5 to 5.5	12 @ 5 V				MC145201	F/751J, DT/948D
2000	2.7 to 5.5	4 @ 3 V				MC145202	F/751J, DT/948D
2600, 400	1.8 to 3.6	7	Loop 1 = Current source/sink Loop 2 = Three–state			MC145230*	FTA/873C

* Dual PLL

NOTE: Evaluation kits available for the MC145190, MC145191, MC145192, MC145200, MC145201, MC145202, and MC145220. Order part number MC145_ _ _EVK.

Table 2. Phase–Locked Loop Functions

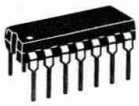
Device	Function	Pins	DIP	SM
MC12002	Analog Mixer	14	P	–
MC12009	480 MHz ÷5/6 Dual Modulus Prescaler	16	P	–
MC12011	550 MHz ÷8/9 Dual Modulus Prescaler	16	P	–
MC12013	550 MHz ÷10/11 Dual Modulus Prescaler	16	P	–
MC12015	225 MHz ÷32/33 Dual Modulus Prescaler	8	P	D
MC12016	225 MHz ÷40/41 Dual Modulus Prescaler	8	P	D
MC12017	225 MHz ÷64/65 Dual Modulus Prescaler	8	P	D
MC12018	520 MHz ÷128/129 Dual Modulus Prescaler	8	P	D
MC12019	225 MHz ÷20/21 Dual Modulus Prescaler	8	P	D
MC12022LVA	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022LVB	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12023	225 MHz ÷64 Prescaler	8	P	D
MC12026A	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12026B	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12028A	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12028B	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12033A	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D
MC12033B	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D

Phase–Locked Loop Components (continued)

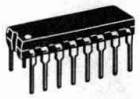
Phase–Locked Loop Functions (continued)

Device	Function	Pins	DIP	SM
MC12034A	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12034B	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12038A	1.1 GHz ÷64/65, ÷127/128, ÷255/256 Low Power Dual Modulus Prescaler	8	P	D
MC12040	Phase-Frequency Detector	14,20	P	–
MC12052A	1.1 GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	8	–	D, SD
MC12053A	1.1 GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler With Stand-By Mode	8	–	D, SD
MC12054A	2.0 GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	8	–	D, SD
MC12058	1.1 GHz ÷126/128. ÷254/256 Low Power Dual Modulus Prescaler	8	–	D, SD
MC12061	Crystal Oscillator	16	P	–
MC12066	1.3 GHz ÷64/256 Prescaler	8	–	D
MC12079	2.8 GHz ÷64/128/256 Prescaler	8	P	D
MC12080	1.1 GHz ÷10/20/40/80 Prescaler	8	P	D
MC12089	2.8 GHz ÷64/128 Prescaler	8	P	D
MC12093	1.1 GHz ÷2/4/8 Low Power Prescaler With Stand-By Mode	8	–	D, SD
MC12095	2.5 GHz ÷2/4 Low Power Prescaler With Stand-By Mode	8	–	D, SD
MC12098	2.5 GHz ÷8192 Prescaler	8	–	D, SD
MCH/K12140	Phase-Frequency Detector	8	–	D
MC12147	Low Power Voltage Controlled Oscillator Buffer	8	–	D, SD
MC12148	Low Power Voltage Controlled Oscillator	8	–	D, SD, P
MC12149	Ultra Low Power Voltage Controlled Oscillator	8	–	D, SD
MC12179	500–2800 MHz Single Channel Frequency Synthesizer	8	–	D
MC12181	125–1000 MHz Frequency Synthesizer	16	–	D

RF/IF Integrated Circuits Packages



CASE 646
P SUFFIX



CASE 648
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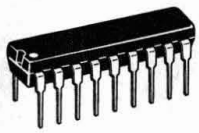
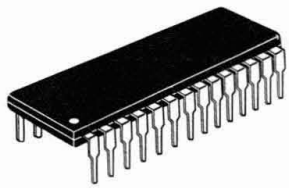
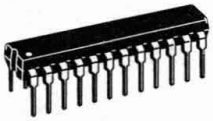


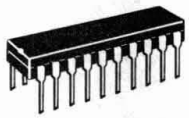
CASE 707
P SUFFIX



CASE 710
P SUFFIX



CASE 724
P SUFFIX



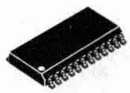
CASE 738
P SUFFIX

CASE 751
D SUFFIX

CASE 751A
D SUFFIX

CASE 751B
D SUFFIX

CASE 751D
DW, FP SUFFIX



CASE 751E
DW SUFFIX

CASE 751F
DW SUFFIX

CASE 751G
DW SUFFIX

CASE 751J
F SUFFIX

CASE 803C
F SUFFIX

CASE 848B
FB SUFFIX

CASE 873
FB, FTB SUFFIX

CASE 873C
FTA SUFFIX

CASE 932
FTA SUFFIX

CASE 948C
DT SUFFIX

CASE 948D
DT SUFFIX

CASE 948F
DTB SUFFIX

CASE 976
FTB SUFFIX

CASE 977
FTA SUFFIX

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MOTOROLA

MC1350

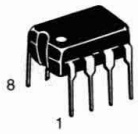
Monolithic IF Amplifier

The MC1350 is an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over an operating temperature range of 0° to +75°C.

- Power Gain: 50 dB Typ at 45 MHZ
  50 dB Typ at 58 MHZ
- AGC Range: 60 dB Min, DC to 45 MHz
- Nearly Constant Input & Output Admittance over the Entire AGC Range
- Y_{21} Constant (–3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance: < < 1.0 µmho Typ
- 12 V Operation, Single–Polarity Power Supply

IF AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

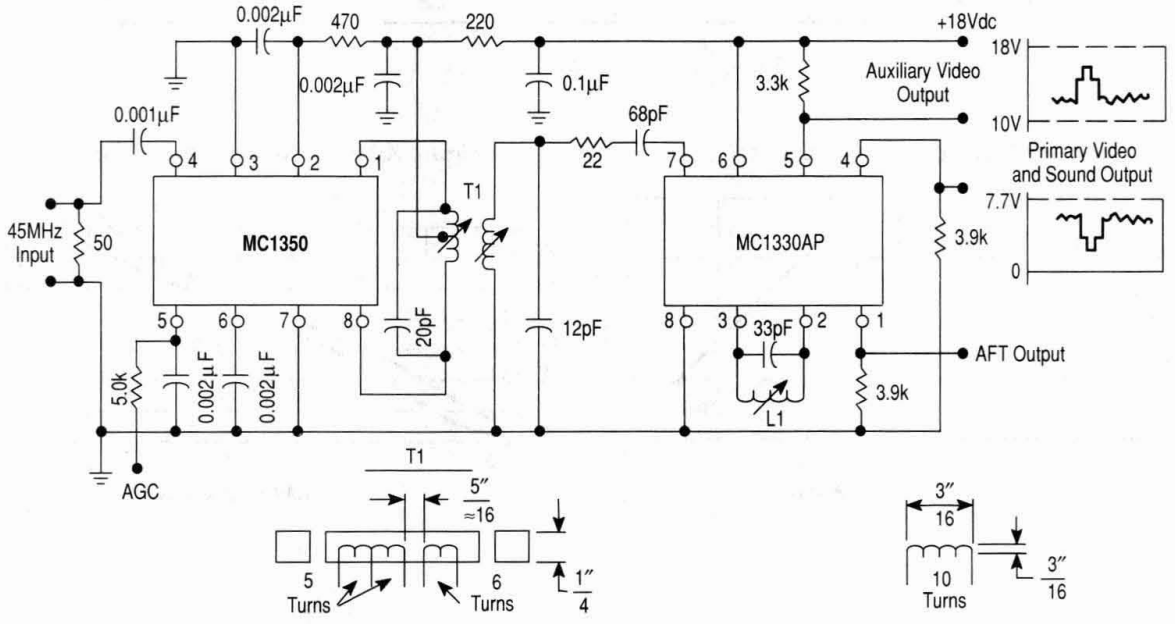
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1350P	T_A = 0° to +75°C	Plastic DIP
MC1350D		SO–8

Figure 1. Typical MC1350 Video IF Amplifier and MC1330 Low–Level Video Detector Circuit



All windings #30 AWG tinned nylon acetate wire tuned with Carbonyl E or J slugs.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor)	A_p				dB
f = 58 MHz, BW = 4.5 MHz See Figure 6(a)		–	48	–	
f = 45 MHz, BW = 4.5 MHz See Figure 6(a), (b)		46	50	–	
f = 10.7 MHz, BW = 350 kHz See Figure 7		–	58	–	
f = 455 kHz, BW = 20 kHz		–	62	–	
Maximum Differential Voltage Swing	V_O				V_{pp}
0 dB AGC		–	20	–	
–30 dB AGC		–	8.0	–	
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V^+ = +12 Vdc, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single–Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmho
Input Admittance Variations with AGC (0 dB to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	µmho
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	µmho
Output Admittance Variations with AGC (0 dB to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	µmho
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12} \rvert$	< < 1.0	< < 1.0	< < 1.0	< < 1.0	µmho
Forward Transfer Admittance						
Magnitude	$\lvert y_{21} \rvert$	160	160	200	180	mmho
Angle (0 dB AGC)	$< y_{21}$	–5.0	–20	–80	–105	Degrees
Angle (–30 dB AGC)	$< y_{21}$	–3.0	–18	–69	–90	Degrees
Single–Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_O	1.2	1.2	1.3	1.6	pF

Figure 2. Typical Gain Reduction

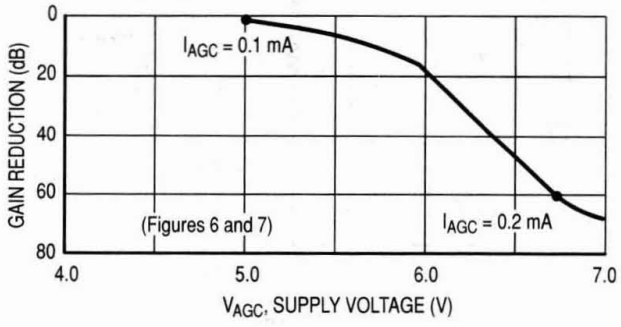
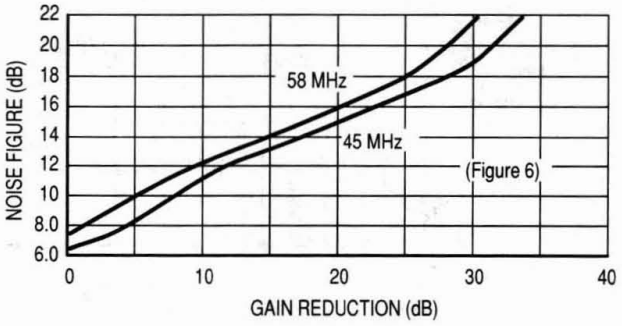


Figure 3. Noise Figure versus Gain Reduction



GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single–ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center–tapped tuning coil to Pins 1 and 8. The 12 V supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15 V supply ($V^{+\ +}$) is used, because the base voltage on the output amplifier varies with AGC bias.

Figure 4. Circuit Schematic

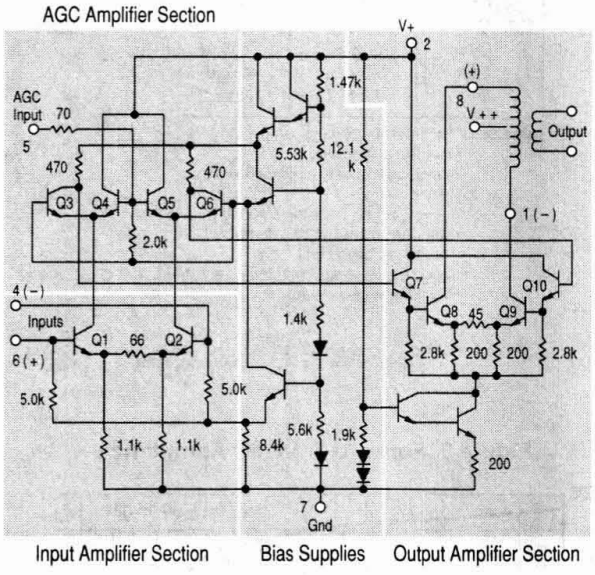


Figure 5. Frequency Response Curve (45 MHz and 58 MHz)

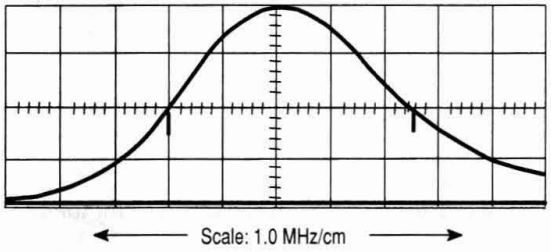
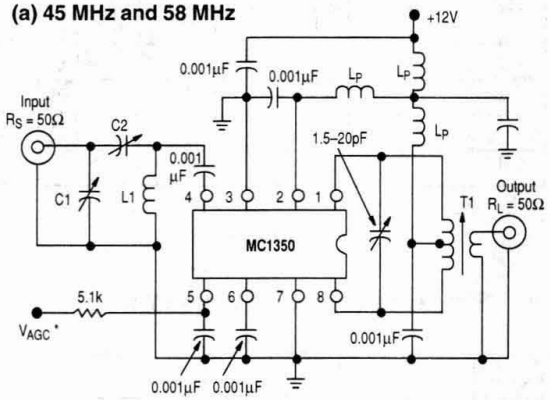
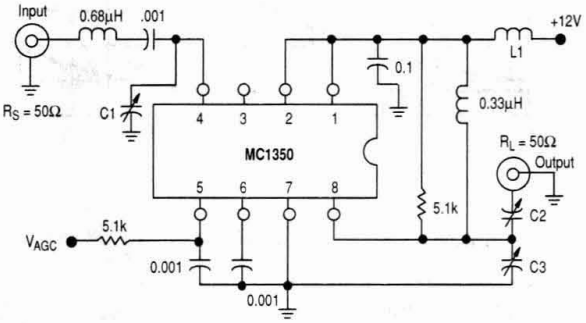


Figure 6. Power Gain, AGC and Noise Figure Test Circuits

(a) 45 MHz and 58 MHz



(b) Alternate 45 MHz



*Connect to ground for maximum power gain test.
All power supply chokes (Lp), are self–resonant at input frequency. $L_P \geq 20\ k\Omega$.
See Figure 5 for Frequency Response Curve.

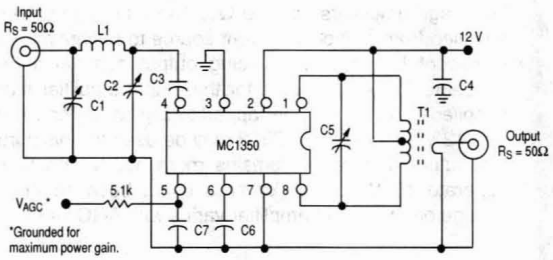
L1 @ 45 MHz = 7 1/4 Turns on a 1/4″ coil form
@ 58 MHz = 6 Turns on a 1/4″ coil form

T1 Primary Winding = 18 Turns on a 1/4″ coil form, center–tapped, #25 AWG
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Carbonyl E or J

L1	Ferrite Core 14 Turns 28 S.W.G.
C1	5–25 pF
C2	5–25 pF
C3	5–25 pF

	45 MHz		58 MHz	
L1	0.4 µH	Q ≥ 100	0.3 µH	Q ≥ 100
T1	1.3 µH to 3.4 µH	Q ≥ 100 @ 2.0 µH	1.2 µH to 3.8 µH	Q ≥ 100 @ 2.0 µH
C1	50 pF to160 pF		8.0 pF to 60 pF	
C2	8.0 pF to 60 pF		3.0 pF to 35 pF	

Figure 7. Power Gain and AGC Test Circuit (455 kHz and 10.7 MHz)



Component	Frequency	
	455 kHz	10.7 MHz
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 µF	0.001 µF
C4	0.05 µF	0.05 µF
C5	0.001 µF	36 pF
C8	0.05 µF	0.05 µF
C7	0.05 µF	0.05 µF
L1	–	4.6 µF
T1	Note 1	Note 2

NOTES: 1. Primary: 120 µH (center–tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13
2. Primary: 6.0 µH
Primary winding = 24 turns #36 AWG
(close–wound on 1/4″ dia. form)
Core = Carbonyl E or J
Secondary winding = 1–1/2 turns #36 AWG, 1/4″ dia.
(wound over center–tap)

Figure 8. Single–Ended Input Admittance

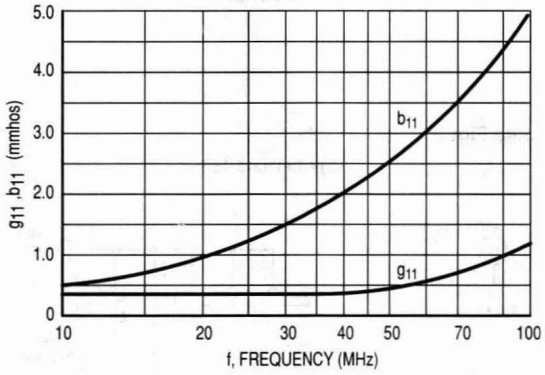


Figure 9. Forward Transfer Admittance

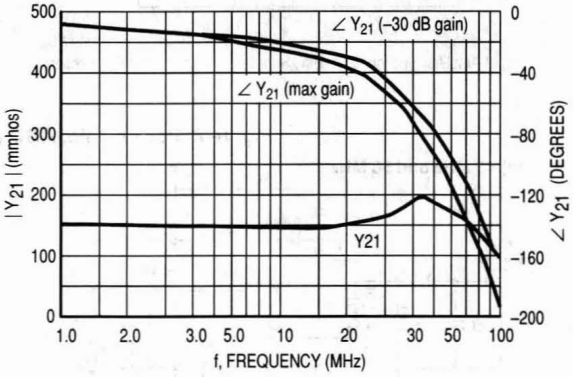


Figure 10. Differential Output Admittance

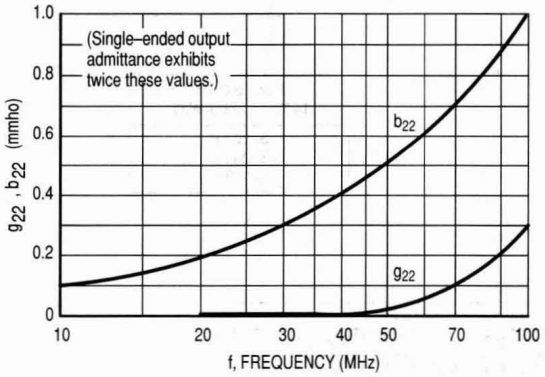
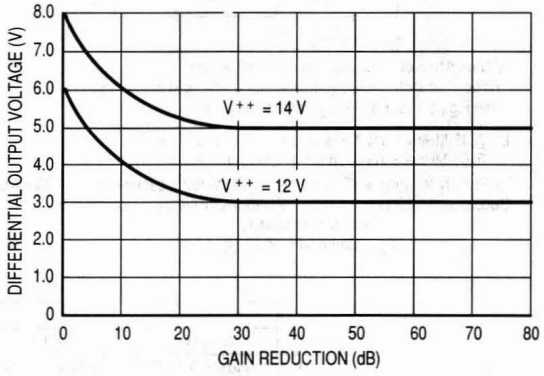


Figure 11. Differential Output Voltage



MOTOROLA

MC1490

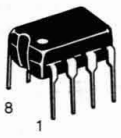
RF/IF/Audio Amplifier

The MC1490 is an integrated circuit featuring wide–range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, –40° to +85°C.

- High Power Gain: 50 dB Typ at 10 MHz
  45 dB Typ at 60 MHz
  35 dB Typ at 100 MHz
- Wide Range AGC: 60 dB Min, DC to 60 MHz
- 6.0 V to 15 V Operation, Single Polarity Supply
- See MC1350D for Surface Mount

WIDEBAND AMPLIFIER WITH AGC

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

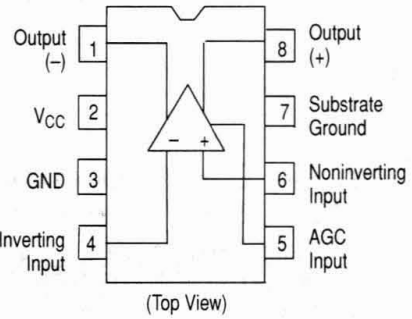
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
AGC Supply	V_{AGC}	V_{CC}	Vdc
Input Differential Voltage	V_{ID}	5.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

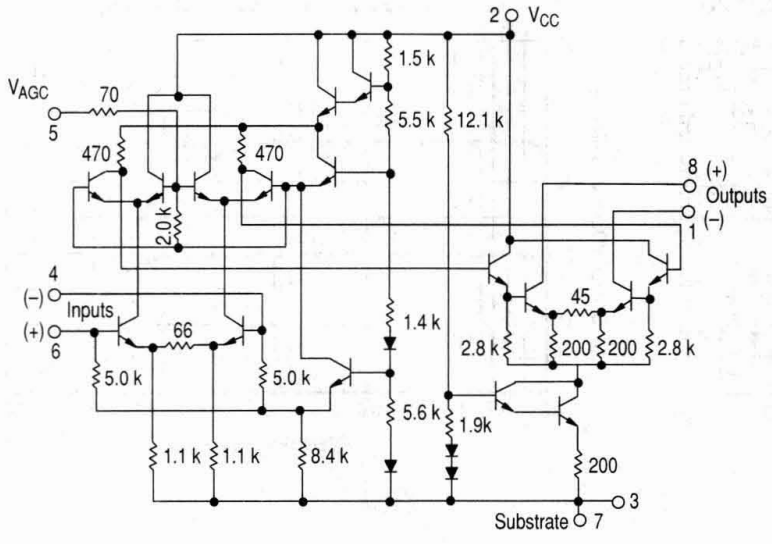
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1490P	T_A = –40° to +85°C	Plastic

PIN CONNECTIONS



Representative Schematic Diagram



Pins 3 and 7 should both be connected to circuit ground.

SCATTERING PARAMETERS
(V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	$\|S_{11}\|$ $\theta 11$	0.95 –7.3	0.93 –16	– deg
Output Reflection Coefficient	$\|S_{22}\|$ $\theta 22$	0.99 –3.0	0.98 –5.5	– deg
Forward Transmission Coefficient	$\|S_{21}\|$ $\theta 21$	16.8 128	14.7 64.3	– deg
Reverse Transmission Coefficient	S_{12} $\theta 12$	0.00048 84.9	0.00092 79.2	– deg

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = 25°C)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current Drain	–	I_{CC}	–	–	17	mA
AGC Range (AGC) 5.0 V Min to 7.0 V Max	19	M_{AGC}	–60	–	–	dB
Output Stage Current (Sum of Pins 1 and 8)	–	I_O	4.0	–	7.5	mA
Single–Ended Power Gain R_S = R_L = 50 Ω	19	G_P	40	–	–	dB
Noise Figure R_S = 50 Ohms	19	NF	–	6.0	–	dB
Power Dissipation	–	P_D	–	168	204	mW

Figure 1. Unneutralized Power Gain versus Frequency (Tuned Amplifier, See Figure 19)

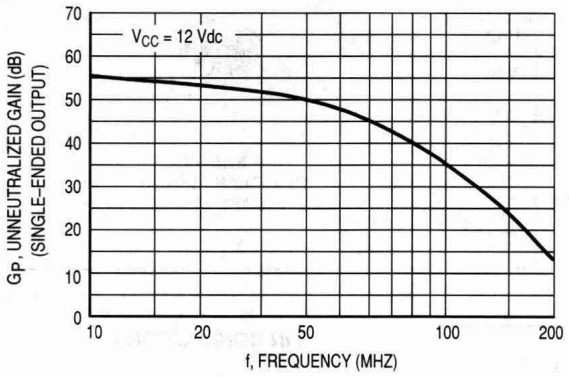


Figure 2. Voltage Gain versus Frequency (Video Amplifier, See Figure 20)

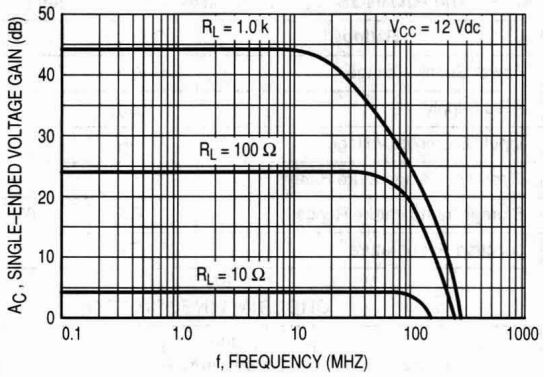


Figure 3. Dynamic Range: Output Voltage versus Input Voltage (Video Amplifier, See Figure 20)

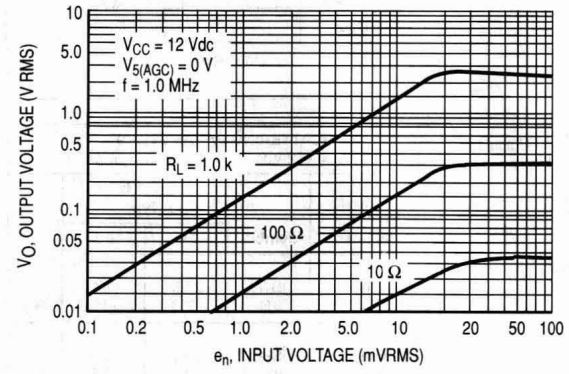


Figure 4. Voltage Gain versus Frequency (Video Amplifier, See Figure 20)

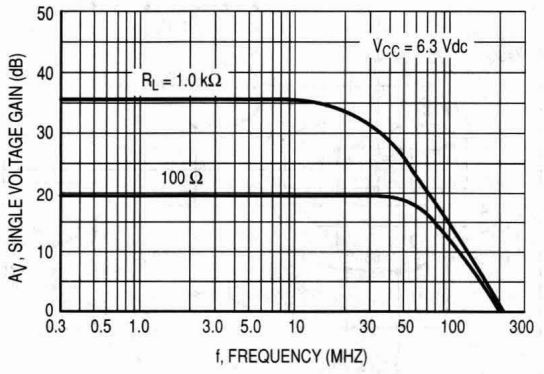


Figure 5. Voltage Gain and Supply Current versus Supply Voltage (Video Amplifier, See Figure 20)

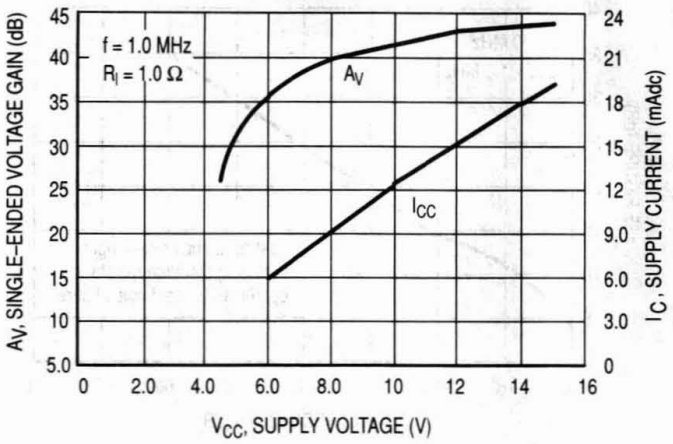


Figure 6. Typical Gain Reduction versus AGC Voltage

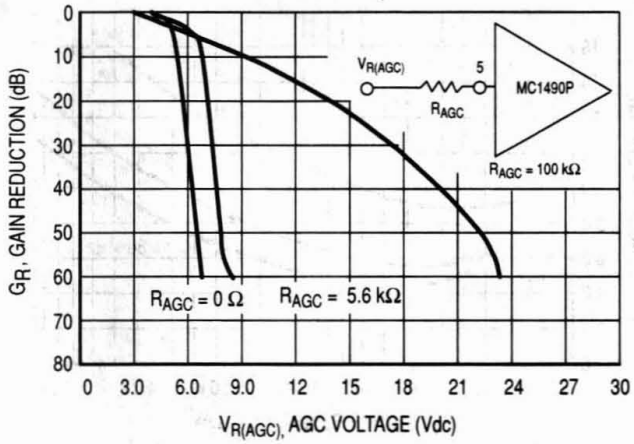


Figure 7. Typical Gain Reduction versus AGC Current

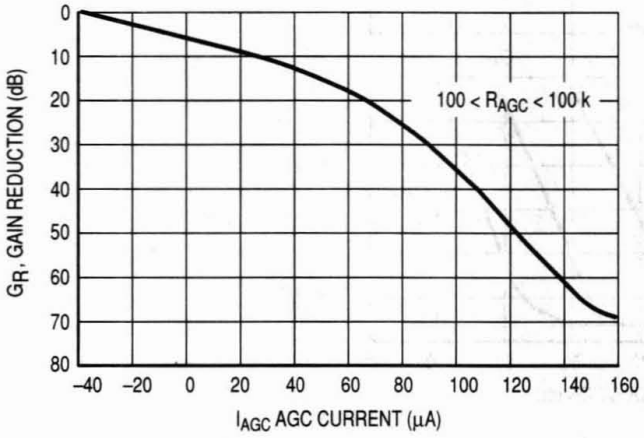


Figure 8. Fixed Tuned Power Gain Reduction versus Temperature (See Test Circuit, Figure 19)

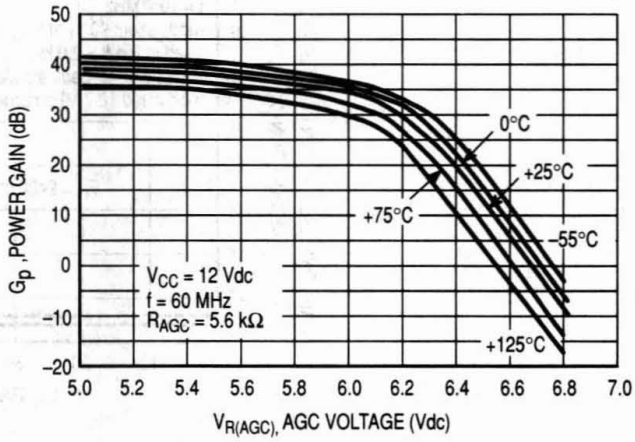


Figure 9. Power Gain versus Supply Voltage (See Test Circuit, Figure 19)

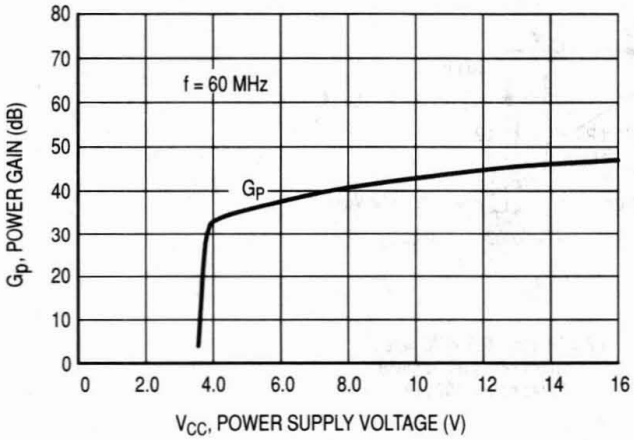


Figure 10. Noise Figure versus Frequency

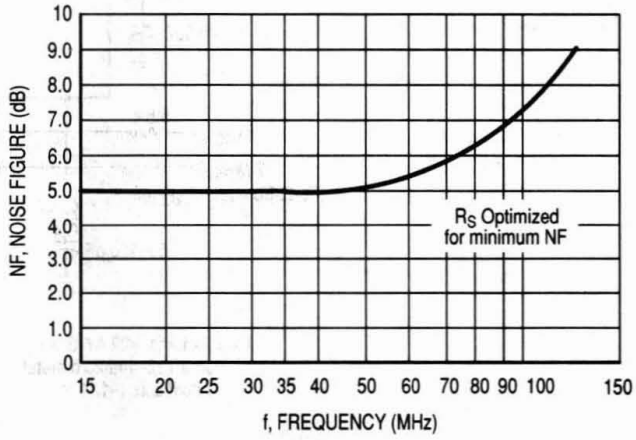


Figure 11. Noise Figure versus Source Resistance

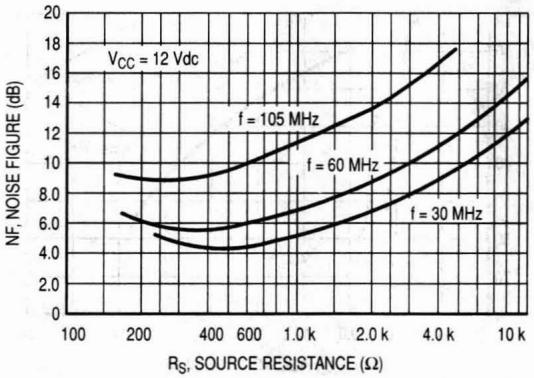


Figure 12. Noise Figure versus AGC Gain Reduction

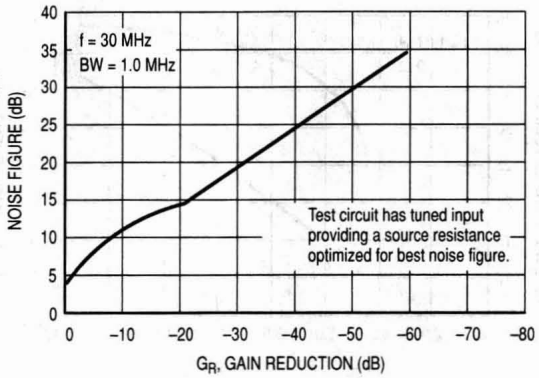


Figure 13. Harmonic Distortion versus AGC Gain Reduction for AM Carrier (For Test Circuit, See Figure 14)

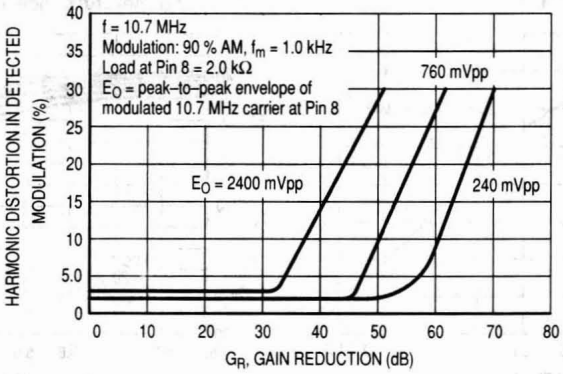
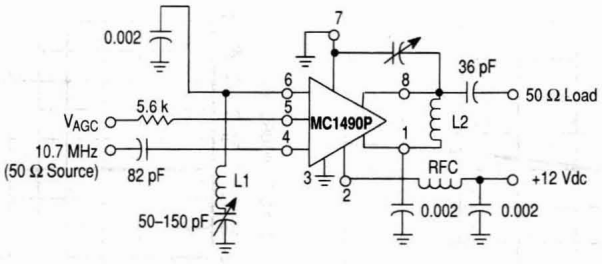


Figure 14. 10.7 MHz Amplifier Gain ≃ 55 dB, BW ≃ 100 kHz



L1 = 24 turns, #22 AWG wire on a T12–44 micro metal Toroid core (–124 pF)

L2 = 20 turns, #22 AWG wire on a T12–44 micro metal Toroid core (–100 pF)

Figure 15. S_{11} and S_{22}, Input and Output Reflection Coefficient

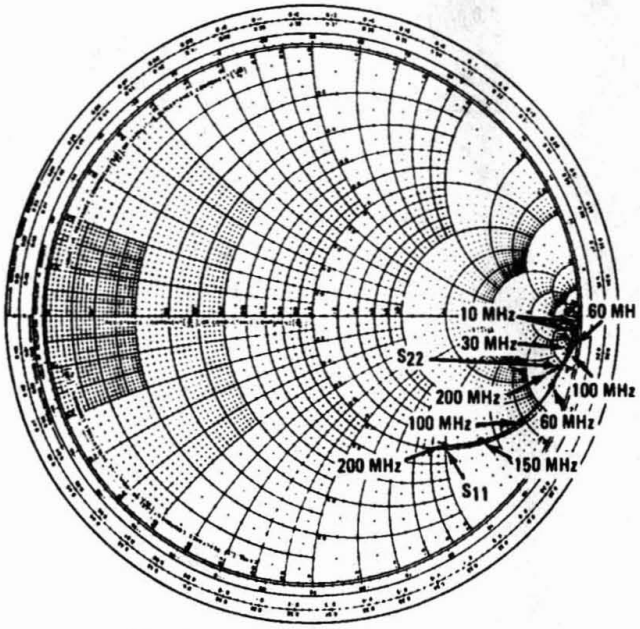


Figure 16. S_{11} and S_{22}, Input and Output Reflection Coefficient

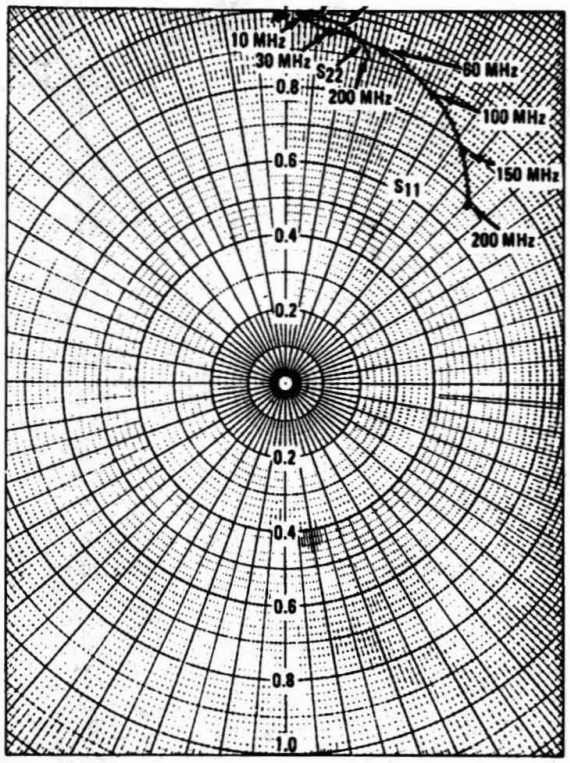


Figure 17. S_{21}, Forward Transmission Coefficient (Gain)

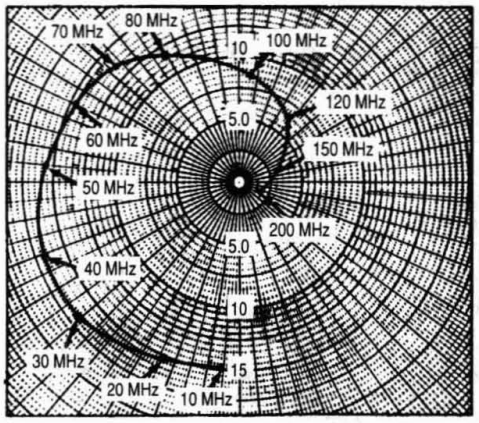


Figure 18. S_{12}, Reverse Transmission Coefficient (Feedback)

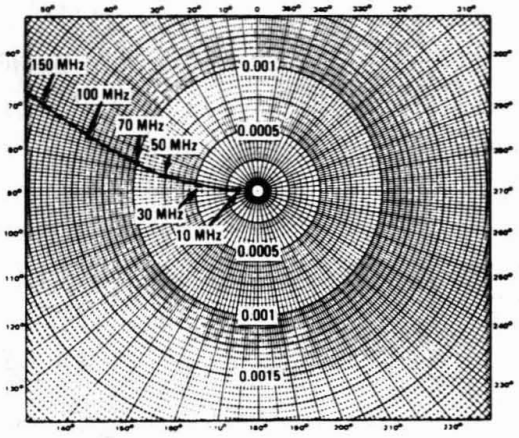
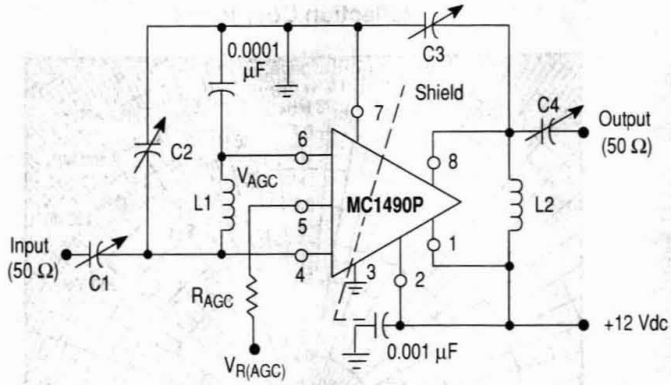


Figure 19. 60 MHz Power Gain Test Circuit



L1 = 7 turns, #20 AWG wire, 5/16″ Dia., 5/8″ long
L2 = 6 turns, #14 AWG wire, 9/16″ Dia., 3/4″ long
C1,C2,C3 = (1–30) pF
C4 = (1–10) pF

Figure 20. Video Amplifier

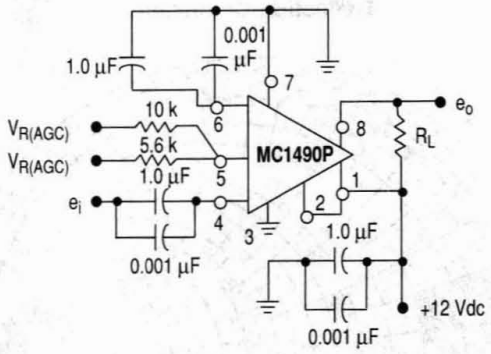
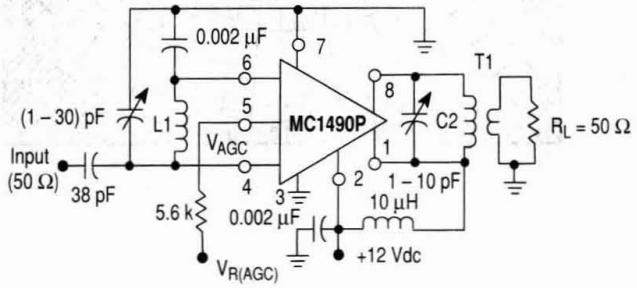
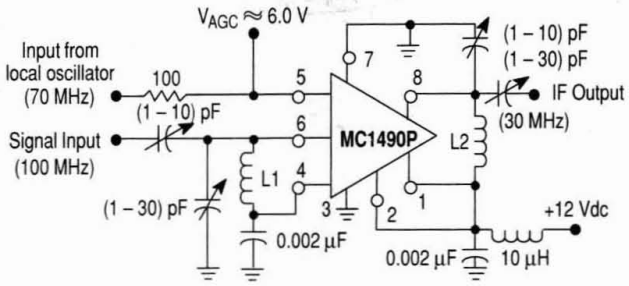


Figure 21. 30 MHz Amplifier (Power Gain = 50 dB, BW ≈ 1.0 MHz)



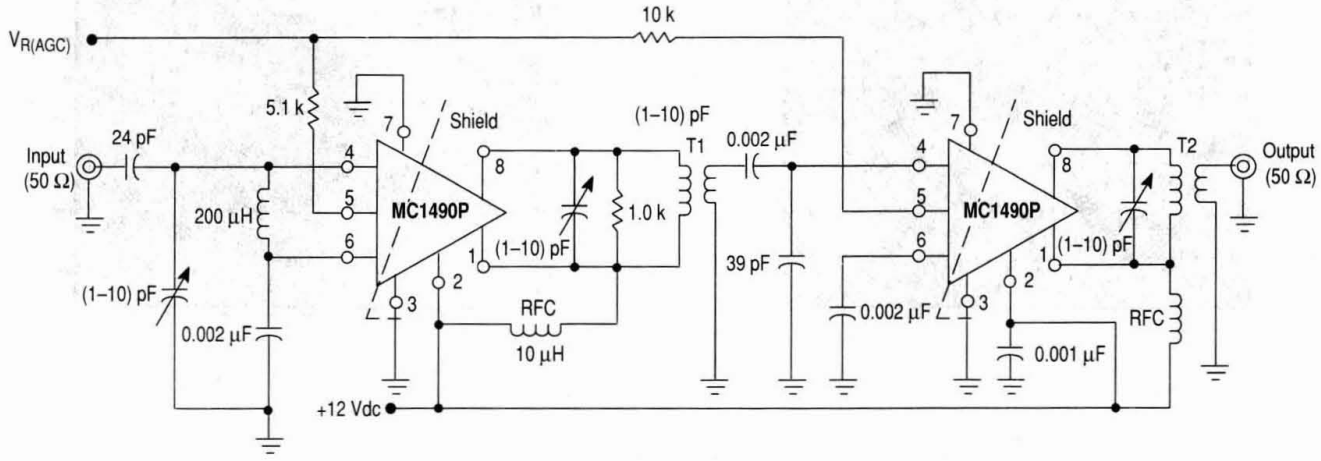
L1 = 12 turns, #22 AWG wire on a Toroid core, (T37–6 micro metal or equiv).
T1: Primary = 17 turns, #20 AWG wire on a Toroid core, (T44–6).
Secondary = 2 turns, #20 AWG wire.

Figure 22. 100 MHz Mixer



L1 = 5 turns, #16 AWG wire, 1/4″, ID Dia., 5/8″ long
L2 = 16 turns, #20 AWG wire on a Toroid core, (T44–6).

Figure 23. Two–Stage 60 MHz IF Amplifier (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 4 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 2 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP transistor operating common–emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \simeq 7.0$ V. The resulting output is filtered by C_x, R_x.

R_x controls the charging time constant or attack time. C_x is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter–follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_x small and R2 large. (A Darlington emitter–follower may be needed if extremely slow decay times are required.)

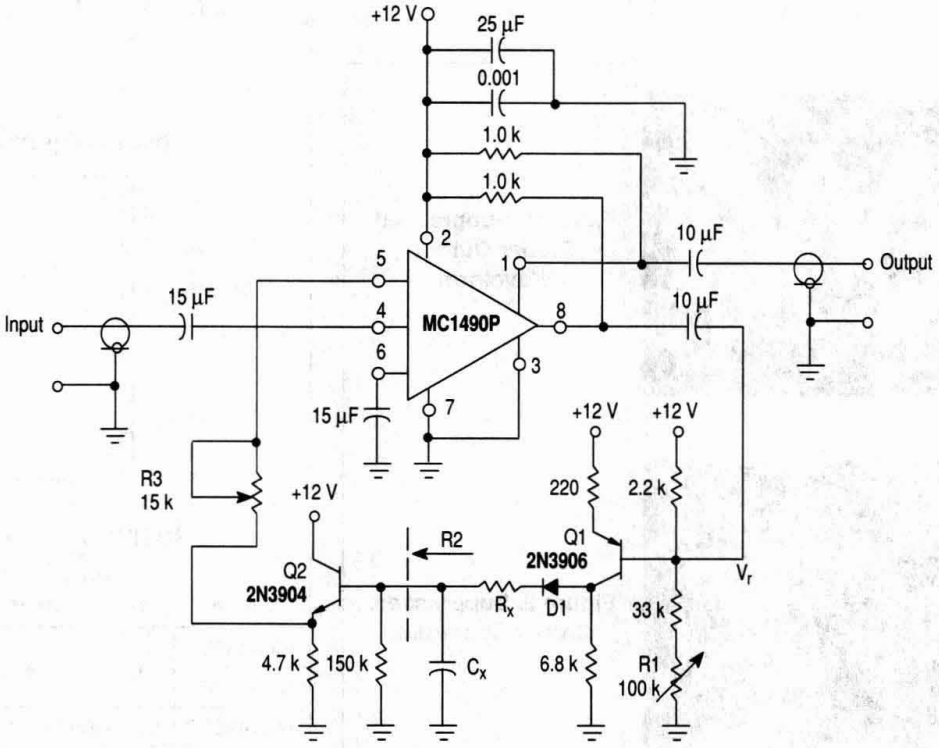
The emitter–follower Q2 drives the AGC Pin 5 of the MC1490P and reduces the gain. R3 controls the slope of signal compression.

Table 1. Distortion versus Frequency

Frequency	Distortion		Distortion	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
	Notes 1 and 2		Notes 3 and 4	

Notes: (1) Decay = 300 ms, Attack = 20 ms
(2) C_x = 7.5 µF, R_x = 0 (Short)
(3) Decay = 20 ms, Attack = 3.0 ms
(4) C_x = 0.68 µF, R_x = 1.5 kΩ

Figure 24. Speech Compressor



MOTOROLA

MC1496, B

Balanced Modulators/ Demodulators

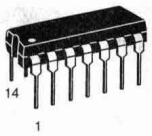
These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN531 for additional design information.

- Excellent Carrier Suppression –65 dB typ @ 0.5 MHz
  –50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection –85 dB typical

This device contains 8 active transistors.

BALANCED MODULATORS/DEMODULATORS

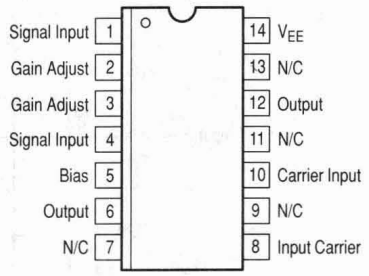
SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1496D	T_A = 0°C to +70°C	SO–14
MC1496P		Plastic DIP
MC1496BP	T_A = –40°C to +125°C	Plastic DIP

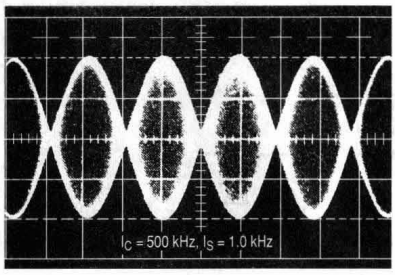


Figure 1. Suppressed Carrier Output Waveform

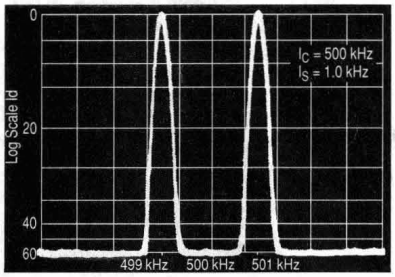


Figure 2. Suppressed Carrier Spectrum

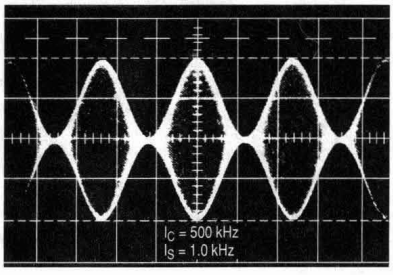
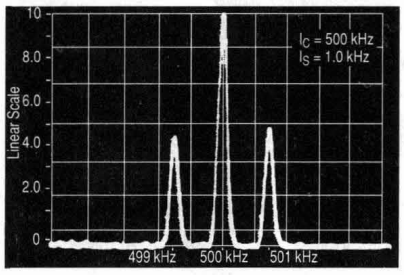


Figure 3. Amplitude Modulation Output Waveform

Figure 4. Amplitude–Modulation Spectrum



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V6 – V8, V10 – V1, V12 – V8, V12 – V10, V8 – V4, V8 – V1, V10 – V4, V6 – V10, V2 – V5, V3 – V5)	ΔV	30	Vdc
Differential Input Signal	V8 – V10 V4 – V1	+5.0 ±(5+I5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction–to–Air Plastic Dual In–Line Package	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{EE} = –8.0 Vdc, I5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = T_{low} to T_{high}, all input and output characteristics are single–ended, unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	Min	Typ	Max	Unit
Carrier Feedthrough	5	1	V_{CFT}				μVrms
V_C = 60 mVrms sine wave and f_C = 1.0 kHz				–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	
V_C = 300 mVpp square wave:							mVrms
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	200	
Carrier Suppression	5	2	V_{CS}				dB
f_S = 10 kHz, 300 mVrms							
f_C = 500 kHz, 60 mVrms sine wave				40	65	–	
f_C = 10 MHz, 60 mVrms sine wave				–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 Ω)	8	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mVrms sine wave				–	300	–	
f_S = 1.0 kHz, 300 mVrms sine wave							
Signal Input Port, V_S = 300 mVrms sine wave				–	80	–	
$\|V_C\|$ = 0.5 Vdc							
Signal Gain (V_S = 100 mVrms, f = 1.0 kHz; $\|V_C\|$= 0.5 Vdc)	10	3	A_{VS}	2.5	3.5	–	V/V
Single–Ended Input Impedance, Signal Port, f = 5.0 MHz	6	–					
Parallel Input Resistance			r_{ip}	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	pF
Single–Ended Output Impedance, f = 10 MHz	6	–					
Parallel Output Resistance			r_{op}	–	40	–	kΩ
Parallel Output Capacitance			c_{oo}	–	5.0	–	pF
Input Bias Current	7	–					μA
$I_{bS} = \frac{I1 + I4}{2}$; $I_{bC} = \frac{I8 + I10}{2}$			I_{bS} I_{bC}	– –	12 12	30 30	
Input Offset Current	7	–					μA
I_{ioS} = I1–I4; I_{ioC} = I8–I10			$\|I_{ioS}\|$ $\|I_{ioC}\|$	– –	0.7 0.7	7.0 7.0	
Average Temperature Coefficient of Input Offset Current (T_A = –55°C to +125°C)	7	–	$\|TC_{Iio}\|$	–	2.0	–	nA/°C
Output Offset Current (I6–I9)	7	–	$\|I_{oo}\|$	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = –55°C to +125°C)	7	–	$\|TC_{Ioo}\|$	–	90	–	nA/°C
Common–Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	Vpp
Common–Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$= 0.5 Vdc	9	–	ACM	–	–85	–	dB
Common–Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_{out}	–	8.0	–	Vpp
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	Vpp
Power Supply Current I6 +I12	7	6	I_{CC}	–	2.0	4.0	mAdc
I14			I_{EE}	–	3.0	5.0	
DC Power Dissipation	7	5	P_D	–	33	–	mW

GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal–input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input–signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single–ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \quad \text{where } r_e = \frac{26\ mV}{I5(mA)}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I5.

$$V_S \leq I5\ R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1.0 V peak.

Common Mode Swing

The common–mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage–current products at each port, i.e. assuming V12 = V6, I5 = I6 = I12 and ignoring base current, $P_D = 2\ I5\ (V6 - V14) + I5)\ V5 - V14$ where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

$$I5 = I6 = I12,$$
$$I_B << I_C \text{ for all transistors}$$

then :

$$R5 = \frac{V - -\phi}{I5} - 500\ \Omega$$

where: R5 is the resistor between Pin 5 and ground
ϕ = 0.75 at T_A = +25°C

The MC1496 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common–Mode Quiescent Output Voltage

$$V6 = V12 = V+ - I5\ R_L$$

Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector–base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\ Vdc \geq [(V6, V12) - (V8, V10)] \geq 2\ Vdc$$
$$30\ Vdc \geq [(V8, V10) - (V1, V4)] \geq 2.7\ Vdc$$
$$30\ Vdc \geq [(V1, V4) - (V5)] \geq 2.7\ Vdc$$

The foregoing conditions are based on the following approximations:

$$V6 = V12,\ V8 = V10,\ V1 = V4$$

Bias currents flowing into Pins 1, 4, 8 and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21C = \frac{i_o\ (\text{each sideband})}{v_s\ (\text{signal})} \Bigg|\ V_o = 0$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21S = \frac{i_o\ (\text{signal})}{v_s\ (\text{signal})} \Bigg|\ V_C = 0.5\ Vdc,\ V_o = 0$$

Coupling and Bypass Capacitors

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

Output Signal

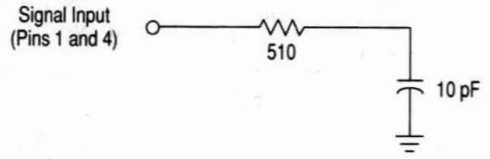
The output signal is taken from Pins 6 and 12 either balanced or single–ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single–ended output connection.

Negative Supply

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source–tuned circuits that cause the oscillation.



An alternate method for low–frequency applications is to insert a 1.0 kΩ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

Figure 5. Carrier Rejection and Suppression

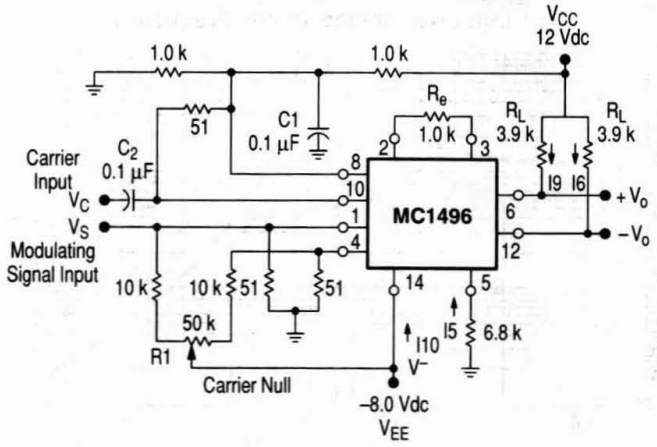
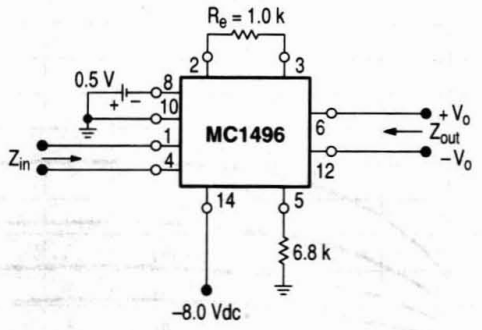


Figure 6. Input–Output Impedance



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

Figure 7. Bias and Offset Currents

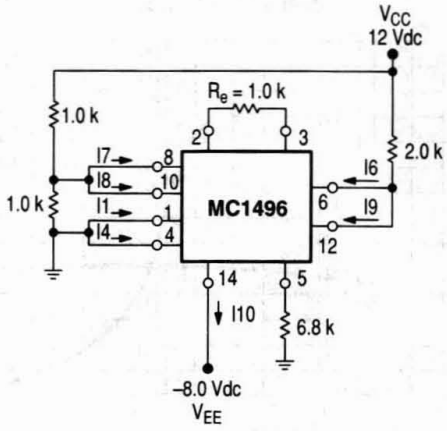


Figure 8. Transconductance Bandwidth

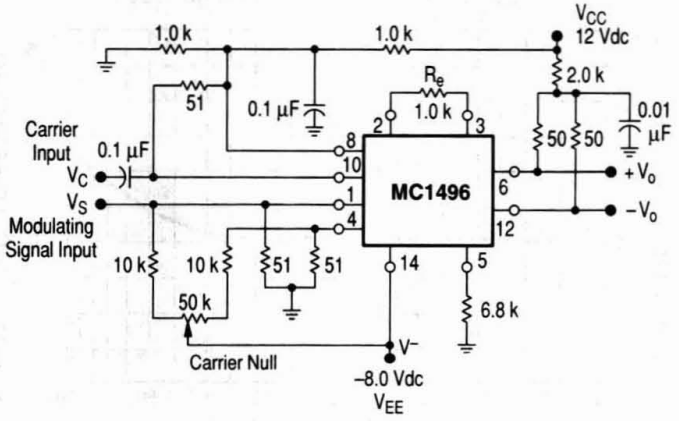


Figure 9. Common Mode Gain

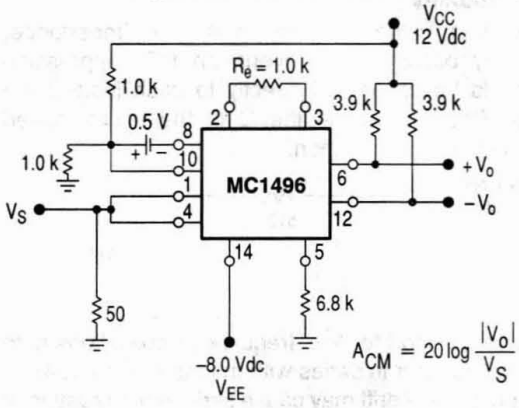
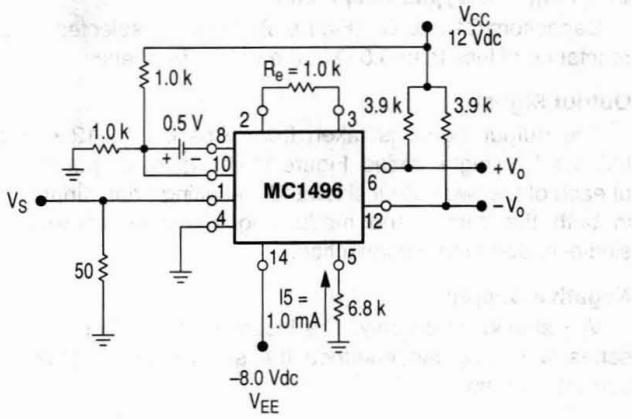


Figure 10. Signal Gain and Output Swing



TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

Figure 11. Sideband Output versus Carrier Levels

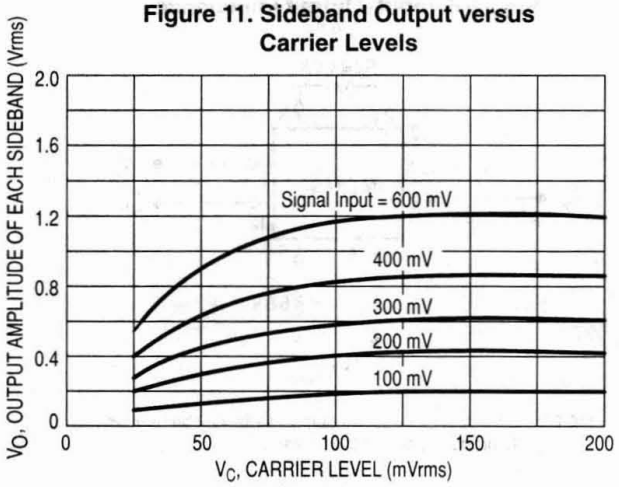


Figure 12. Signal–Port Parallel–Equivalent Input Resistance versus Frequency

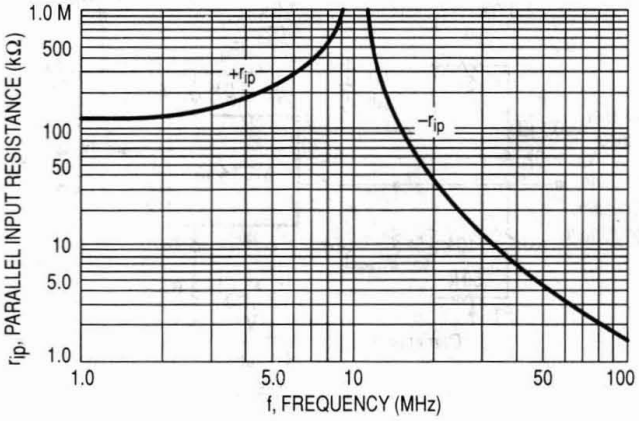


Figure 13. Signal–Port Parallel–Equivalent Input Capacitance versus Frequency

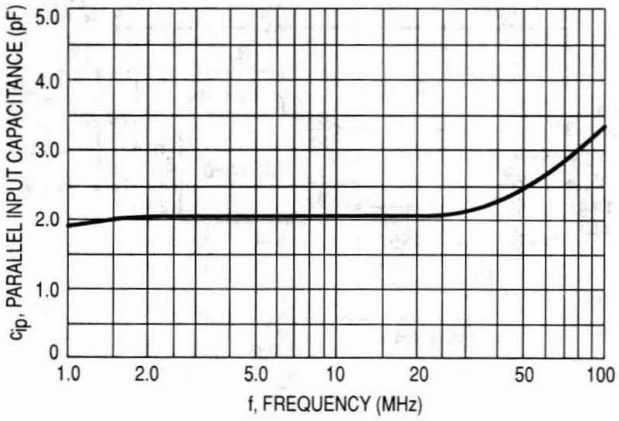
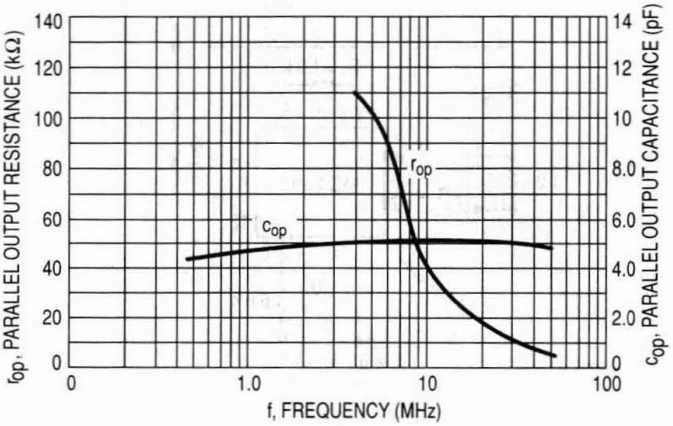


Figure 14. Single–Ended Output Impedance versus Frequency



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

Figure 15. Sideband and Signal Port Transadmittances versus Frequency

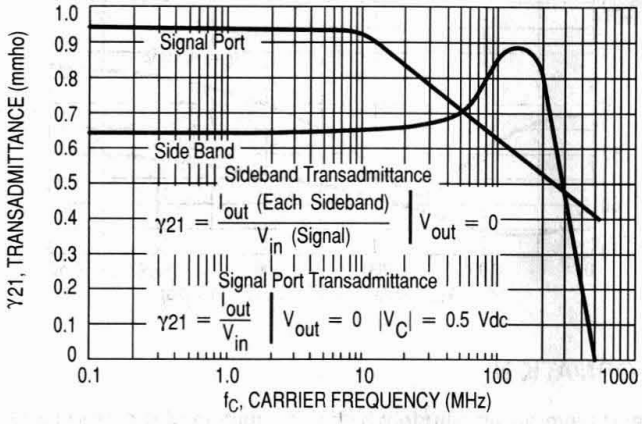


Figure 16. Carrier Suppression versus Temperature

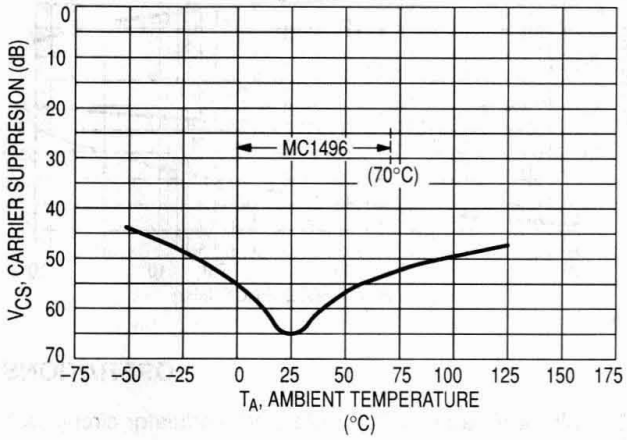


Figure 17. Signal–Port Frequency Response

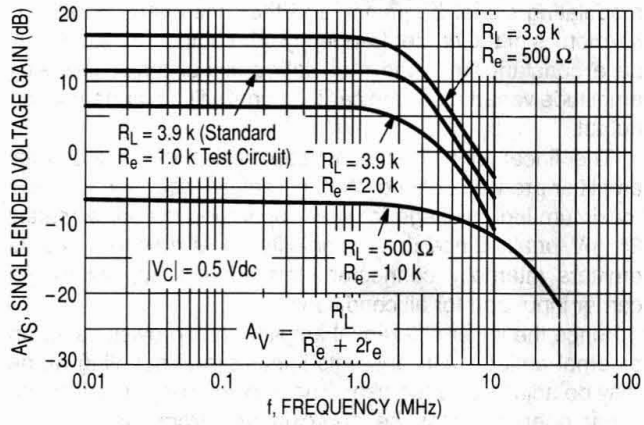


Figure 18. Carrier Suppression versus Frequency

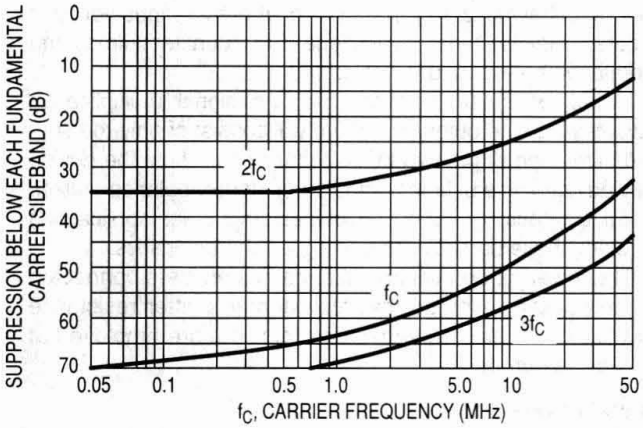


Figure 19. Carrier Feedthrough versus Frequency

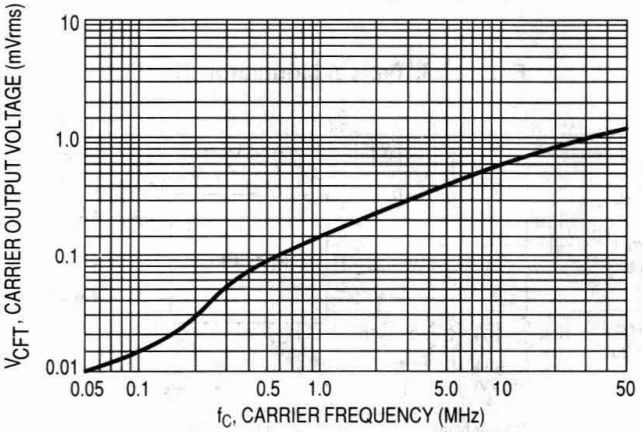


Figure 20. Sideband Harmonic Suppression versus Input Signal Level

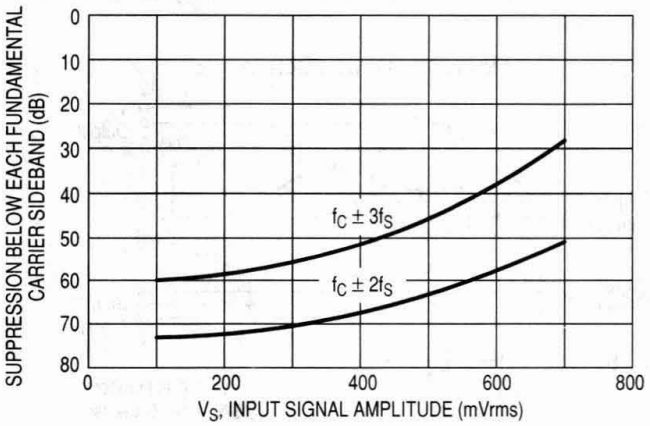


Figure 21. Suppression of Carrier Harmonic Sidebands versus Carrier Frequency

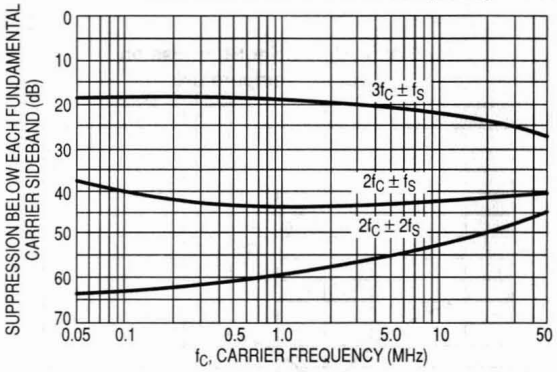
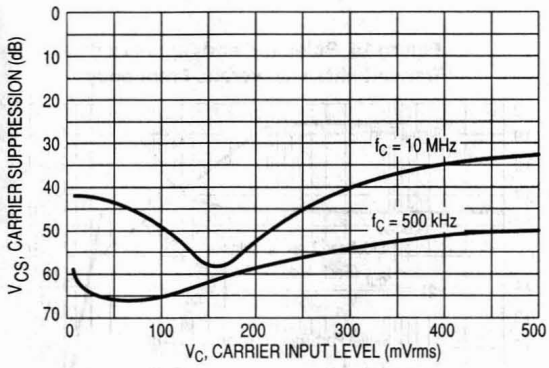


Figure 22. Carrier Suppression versus Carrier Input Level



OPERATIONS INFORMATION

The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross–coupled so that full–wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low–level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high–level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I5)\ (R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

Figure 23. Circuit Schematic

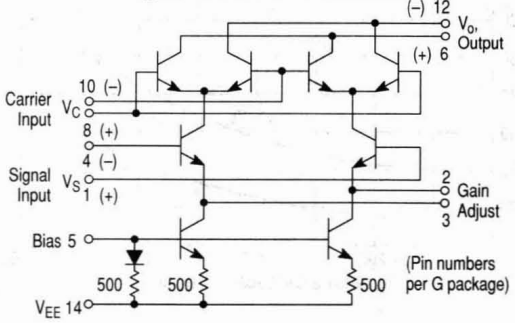


Figure 24. Typical Modulator Circuit

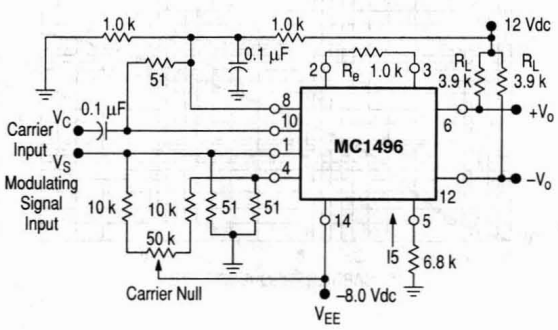


Figure 25. Voltage Gain and Output Frequencies

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low–level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High–level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low–level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High–level ac	$\frac{0.637\ R_L}{R_E + 2r_e}$	$f_C \pm f_M, 3f_C \pm f_M, 5f_C \pm f_M, \ldots$

NOTES: 1. Low–level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single–ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between Pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at 25°C;

$$re \approx \frac{26\ mV}{I_5\ (mA)}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ mV \text{ at room temperature}$$

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low–level modulating signal input and the following carrier input conditions:

1) Low–level dc
2) High–level dc
3) Low–level ac
4) High–level ac

These gains are summarized in Figure 25, along with the frequency components contained in the output signal.

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on Pins 8 and 10 should be increased to 1.0 μF. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential

amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

Doubly Balanced Mixer

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms.

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1496 will function as a phase detector. High–level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

Figure 26. Balanced Modulator (12 Vdc Single Supply)

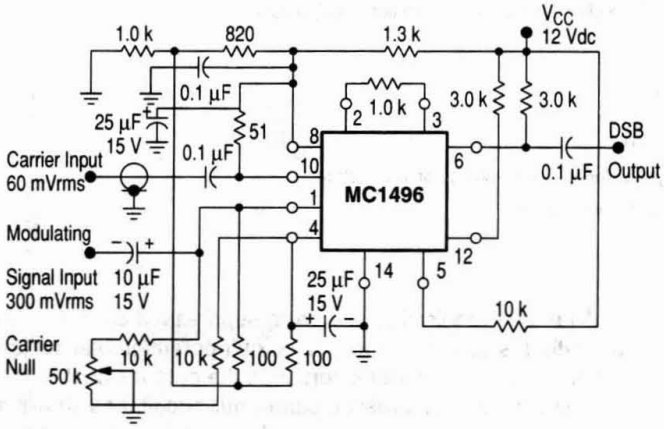


Figure 27. Balanced Modulator–Demodulator

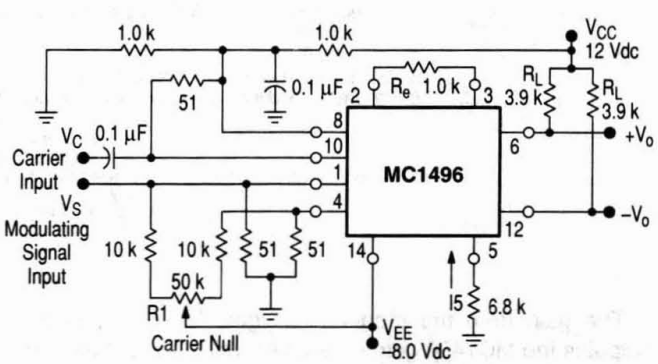


Figure 28. AM Modulator Circuit

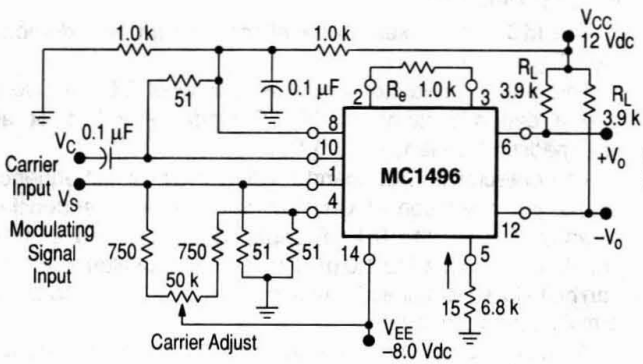


Figure 29. Product Detector (12 Vdc Single Supply)

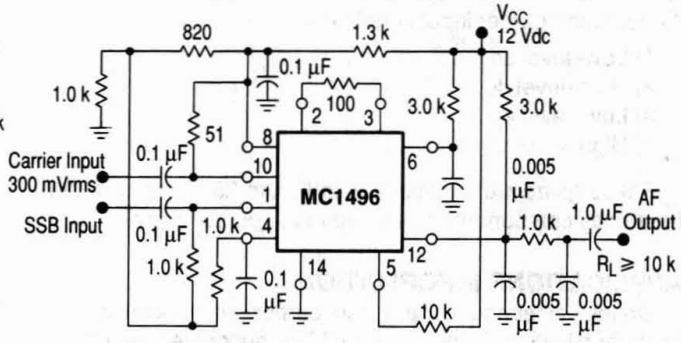
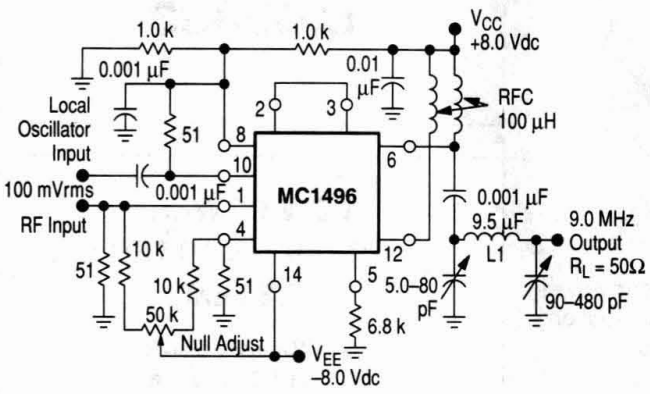


Figure 30. Doubly Balanced Mixer (Broadband Inputs, 9.0 MHz Tuned Output)



L1 = 44 Turns AWG No. 28 Enameled Wire, Wound on Micrometals Type 44–6 Toroid Core.

Figure 31. Low–Frequency Doubler

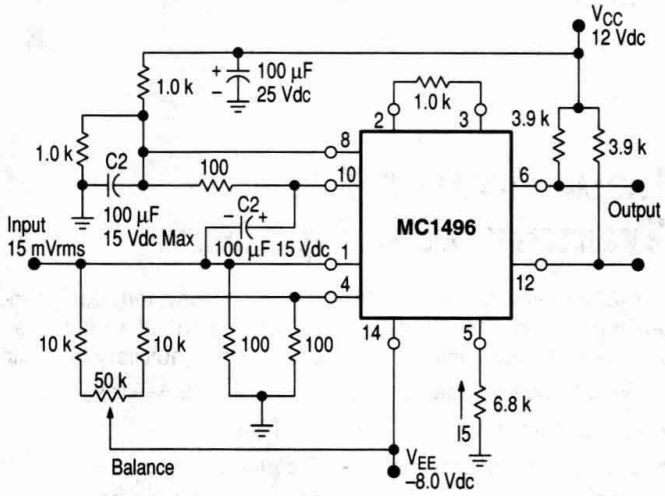
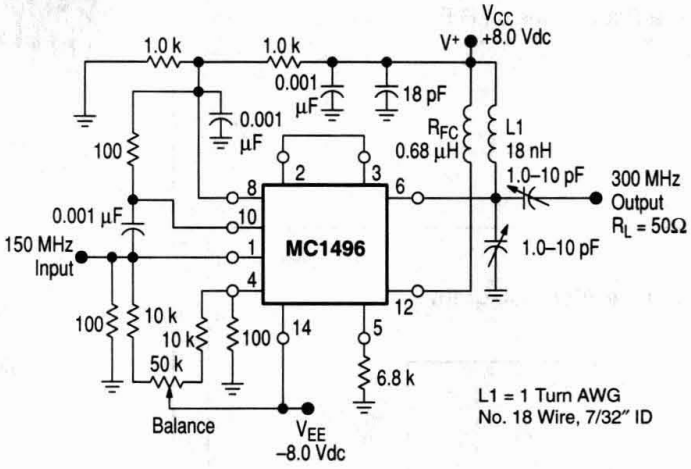
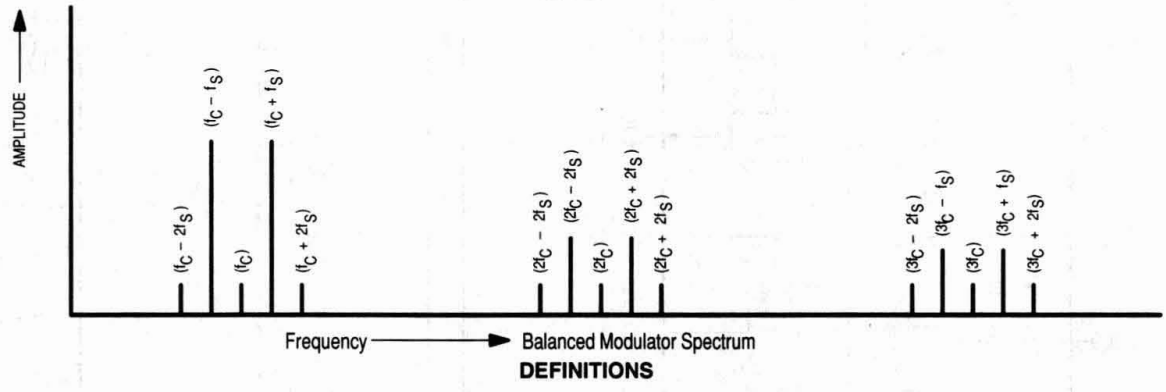


Figure 32. 150 to 300 MHz Doubler



L1 = 1 Turn AWG No. 18 Wire, 7/32″ ID



DEFINITIONS

f_C	Carrier Fundamental	$f_C \pm nf_S$	Fundamental Carrier Sideband Harmonics
f_S	Modulating Signal	nf_C	Carrier Harmonics
$f_C \pm f_S$	Fundamental Carrier Sidebands	$nf_C \pm nf_S$	Carrier Harmonic Sidebands

MOTOROLA

MC2833

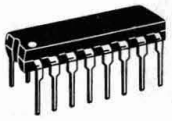
Low Power FM Transmitter System

MC2833 is a one–chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current (I_{CC} = 2.9 mA Typ)
- Low Number of External Parts Required
- – 30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On–Chip Transistor Amplifiers
- Users Must Comply with Local Regulations on R.F. Transmission (FCC, DOT, P.T.T., etc)

LOW POWER FM TRANSMITTER SYSTEM

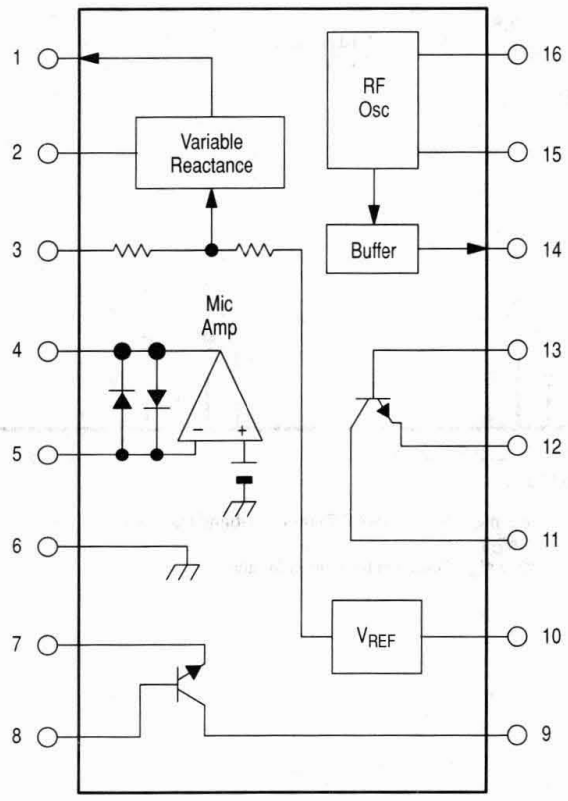
SEMICONDUCTOR TECHNICAL DATA



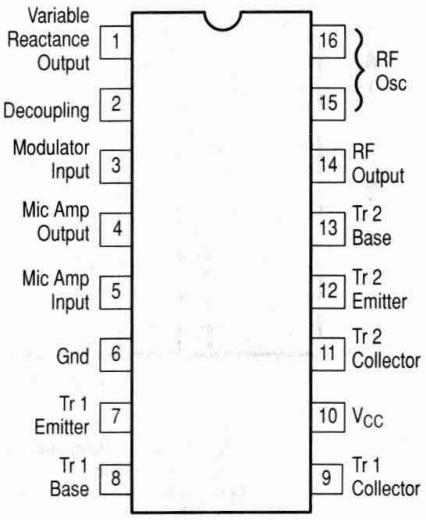
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC2833D	T_A = – 30 to +75°C	SO–16
MC2833P		Plastic DIP

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature	T_A	– 30 to + 75	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA
FM MODULATOR						
Output RF Voltage (f_o = 16.6 MHz)	V_{out} RF	14	60	90	130	mVrms
Output DC Voltage (No input signal)	Vdc	14	2.2	2.5	2.8	V
Modulation Sensitivity (f_o = 16.6 MHz) (V_{in} = 0.8 V to 1.2 V)	SEN	3 14	7.0 –	10 –	15 –	Hz/mVdc
Maximum Deviation (f_o = 16.6 MHz) (V_{in} = 0 V to 2.0 V)	Fdev	3 14	3.0 –	5.0 –	10 –	kHz
MIC AMPLIFIER						
Closed Loop Voltage Gain (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	A_v	4 5	27 –	30 –	33 –	dB
Output DC Voltage (No input signal)	V_{out} dc	4	1.1	1.4	1.7	V
Output Swing Voltage (V_{in} = 30 mVrms) (f_{in} = 1.0 kHz)	V_{out} p–p	4	0.8	1.2	1.6	Vp–p
Total Harmonic Distortion (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	THD	4	–	0.15	2.0	%

AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage (I_C = 5.0 μA)	$V_{(BR)CBO}$	15	45	–	V
Collector Emitter Breakdown Voltage (I_C = 200 μA)	$V_{(BR)CEO}$	10	15	–	V
Collector Substrate Breakdown Voltage (I_C = 50 μA)	$V_{(BR)CSO}$	–	70	–	V
Emitter Base Breakdown Voltage (I_E = 50 μA)	$V_{(BR)EBO}$	–	6.2	–	V
Collector Base Cut Off Current (V_{CB} = 10 V) (I_E = 0)	I_{CBO}	–	–	200	nA
DC Current Gain (I_C = 3.0 mA) (V_{CE} = 3.0 V)	h_{FE}	40	150	–	–

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (V_{CE} = 3.0 V) (I_C = 3.0 mA)	f_T	–	500	–	MHz
Collector Base Capacitance (V_{CE} = 3.0 V) (I_C = 0)	C_{CB}	–	2.0	–	pF
Collector Substrate Capacitance (V_{CS} = 3.0 V) (I_C = 0)	C_{CS}	–	3.3	–	pF

Figure 1. Test Circuit

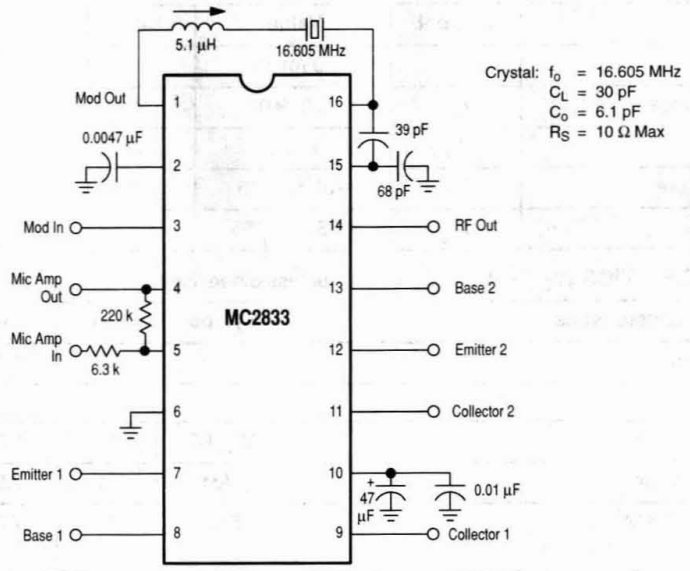
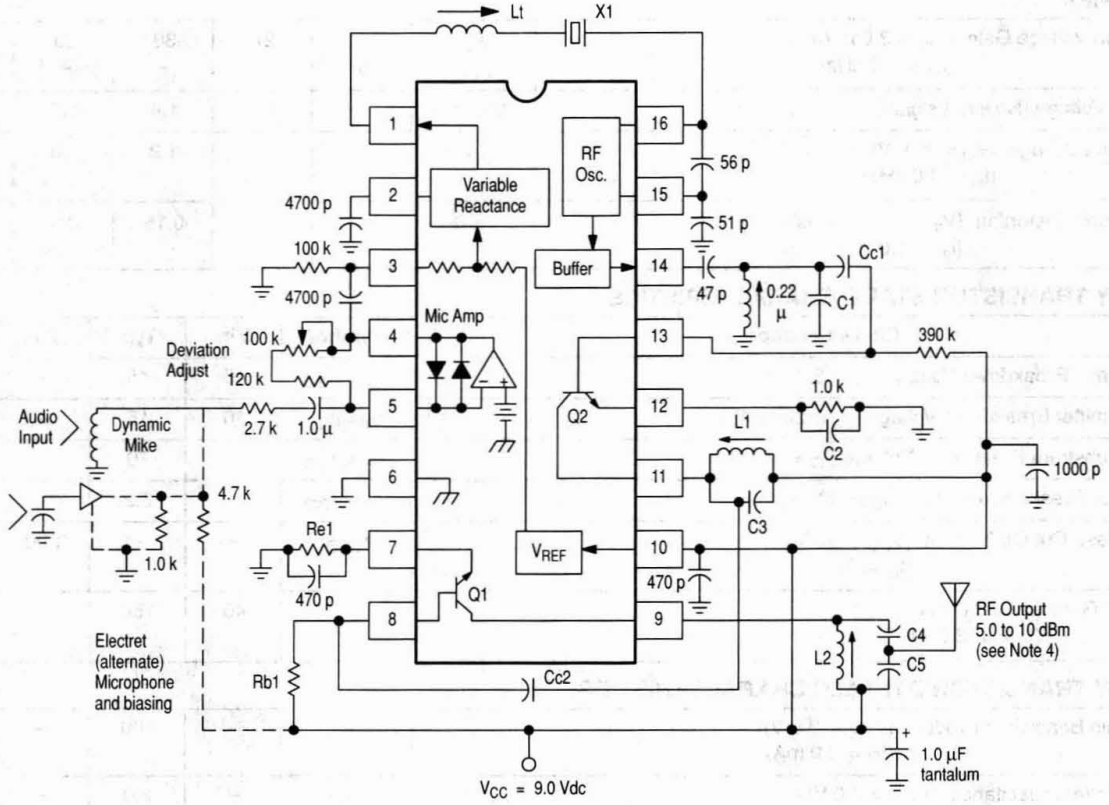


Figure 2. Single Chip VHF Narrowband FM Transmitter



NOTES:

1. Components versus output frequency:

Output RF	X1 (MHz)	Lt (µH)	L1 (µH)	L2 (µH)	Re1	Rb1	Cc1	Cc2	C1	C2	C3	C4	C5
49.7 MHz	16.5667	3.3–4.7	0.22	0.22	330	390 k	33 p	33 p	33 p	470 p	33 p	47 p	220 p
76 MHz	12.6000	5.1	0.22	0.22	150	300 k	68 p	10 p	68 p	470 p	12 p	20 p	120 p
144.6 MHz	12.05	5.6	0.15	0.10	150	220 k	47 p	10 p	68 p	1000 p	18 p	12 p	33 p

2. Crystal X1 is fundamental mode, calibrated for parallel resonance with a 32 pF load. The final output frequency is generated by frequency multiplication within the MC2833 IC. The RF output buffer (Pin 14) and Q2 transistor are used as a frequency tripler and doubler, respectively, in the 76 and 144.6 MHz transmitters. The Q1 output transistor is a linear amplifier in the 49.7 MHz and 76 MHz transmitters, and a frequency doubler in the 144.6 MHz transmitter.
3. All coils used are 7 mm shielded inductors, CoilCraft series M1175A, M1282A–M1289A, M1312A or equivalent.
4. Power output is ≈ + 10 dBm for 49.7 MHz and 76 MHz transmitters, and ≈ + 5.0 dBm for the 144.6 MHz transmitter at V_{CC} = 8.0 V. Power output drops with lower V_{CC}.
5. All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.
6. Other frequency combinations may be set–up by simple scaling of the 3 examples shown.

Figure 3. Buffer/Multiplier (x3, Pin 14)
(16 MHz Fundamental)

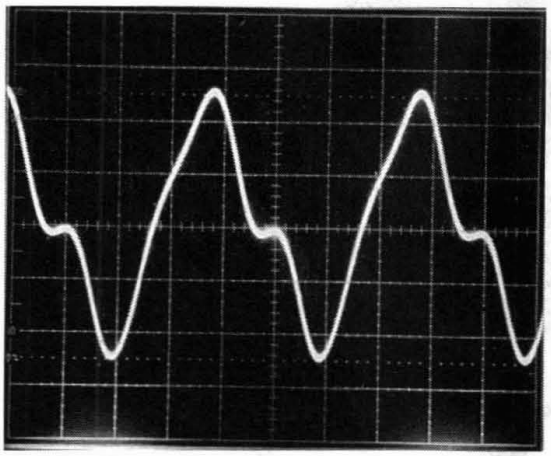


Figure 4. Input to Doubler (Pin 13)
(49.7 MHz x 3 Component)

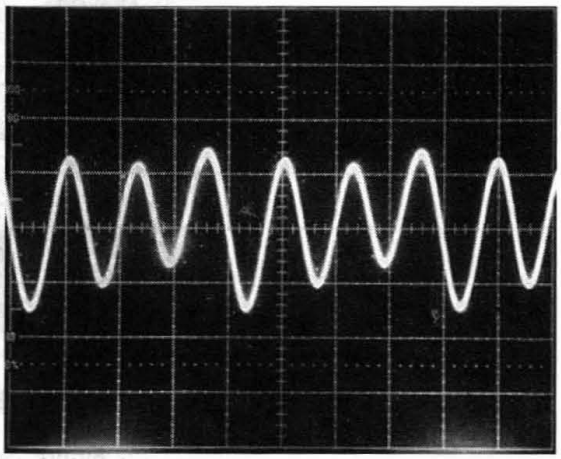


Figure 5. Doubler Output 76 MHz (Pin 11)

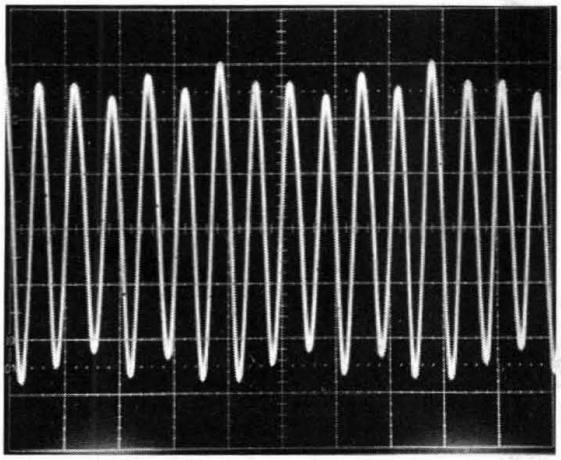


Figure 6. Spectrum

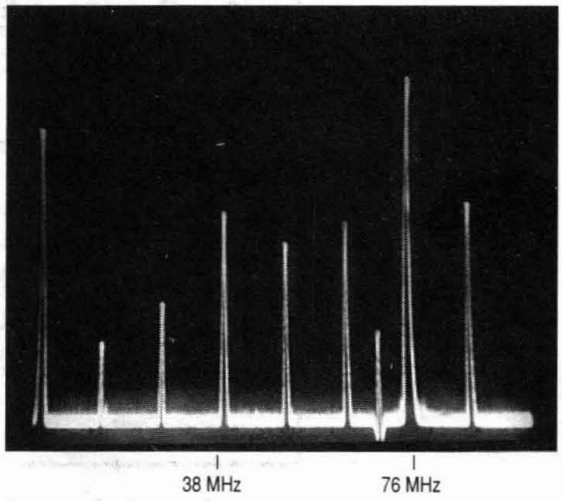


Figure 7. Output Spectrum (49.7 MHz)

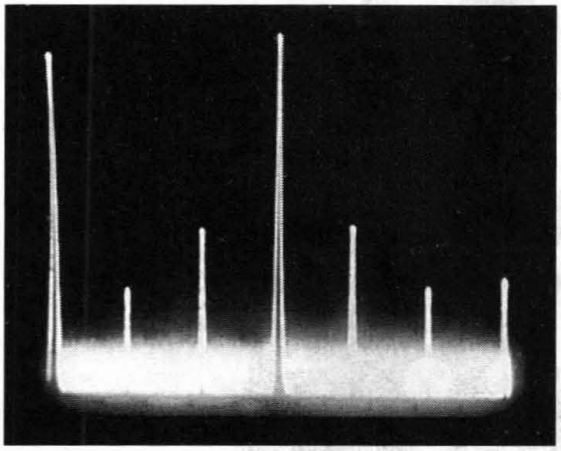


Figure 8. Modulation Spectrum
(1.0 kHz Showing Carrier Null)

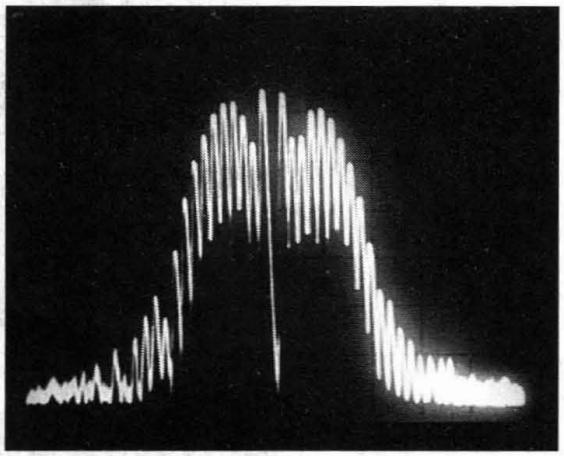


Figure 9. 144.6 MHz/x12 Multiplier

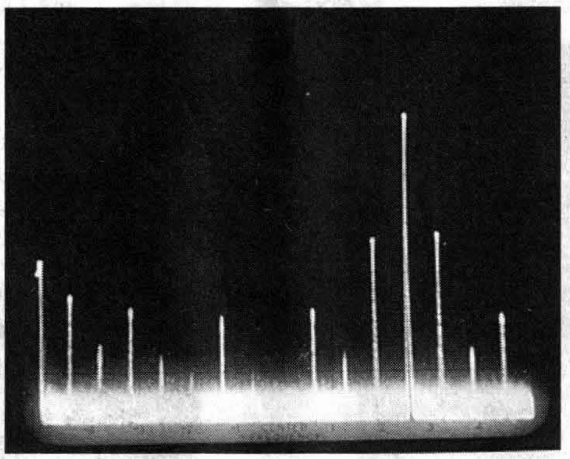


Figure 10. Circuit Side View

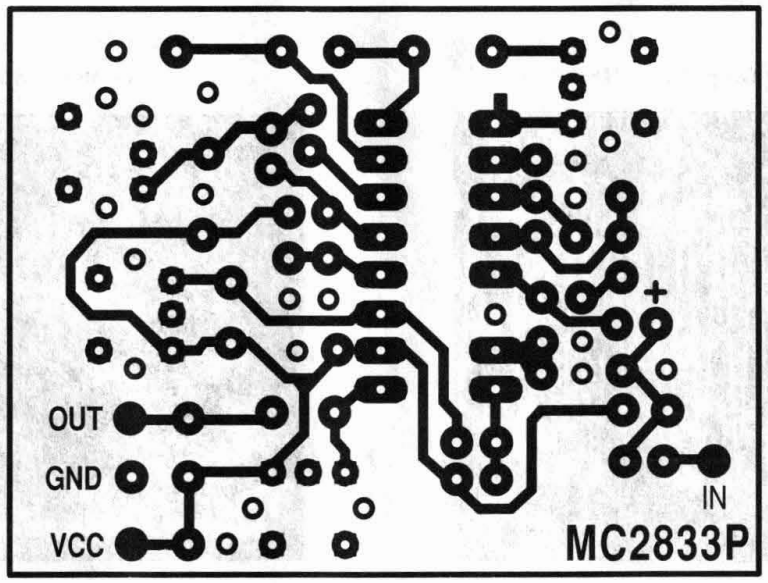


Figure 11. Ground Plane on Component Side

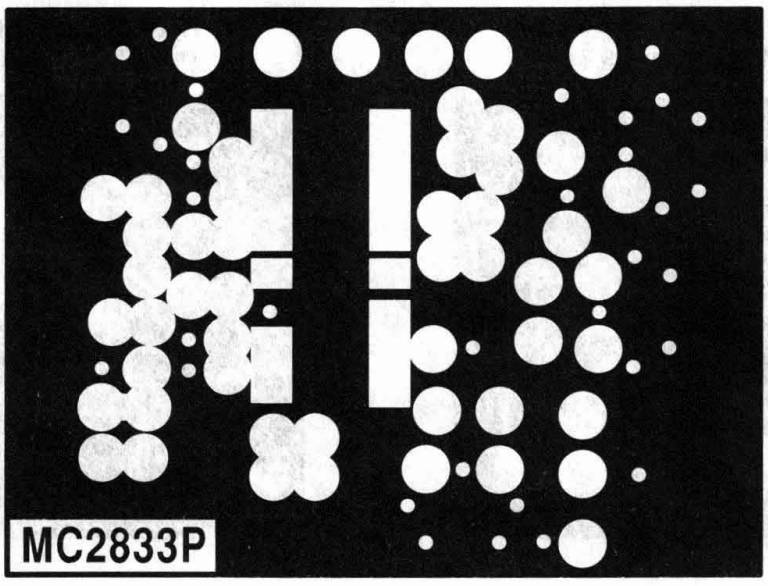
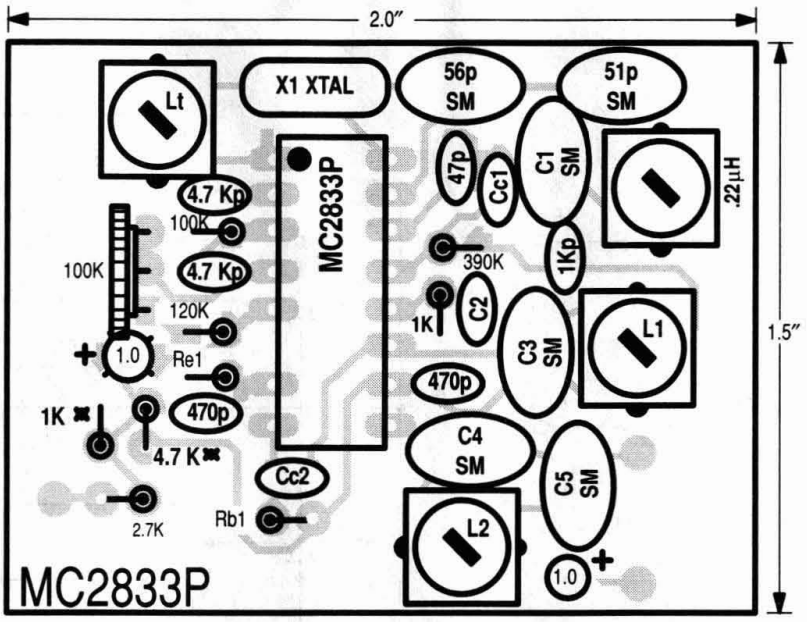
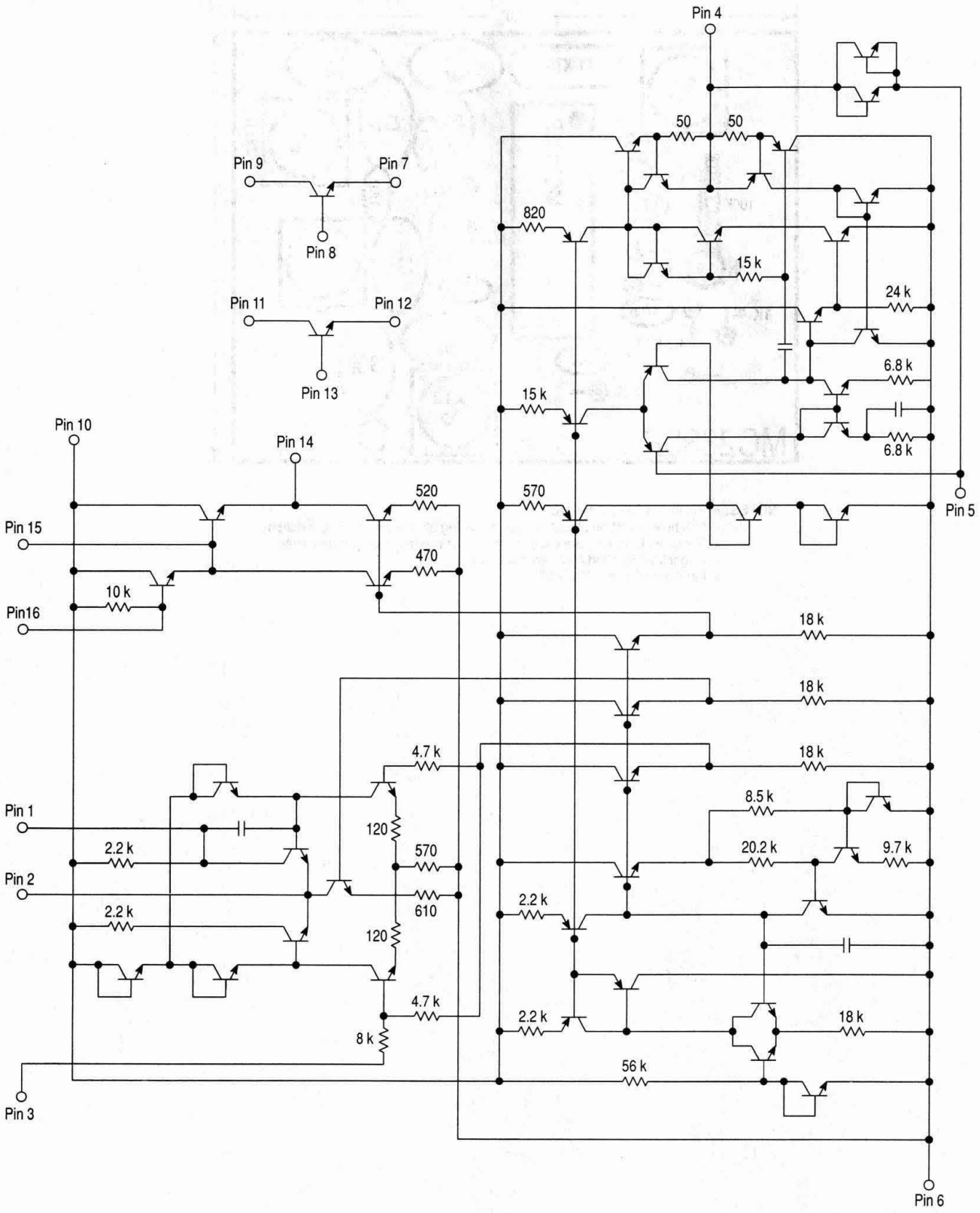


Figure 12. Component View



NOTES:
- Positive artwork provided.
- Drill holes must be plated to ensure making all ground (V_{EE}) connections!
- Resistors labelled * are used for biasing of electret microphone if used.
- Capacitors labelled "SM" are silver mica.
- Final board size 1.5″ × 2.0″.

Figure 13. Circuit Schematic



MOTOROLA

MC3356

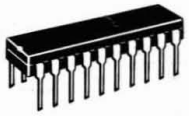
Wideband FSK Receiver

The MC3356 includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communciations equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: – 3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly Versatile, Full Function Device, yet Few External Parts are Required
- Down Converter Can be Used Independently — Similar to NE602

WIDEBAND FSK RECEIVER

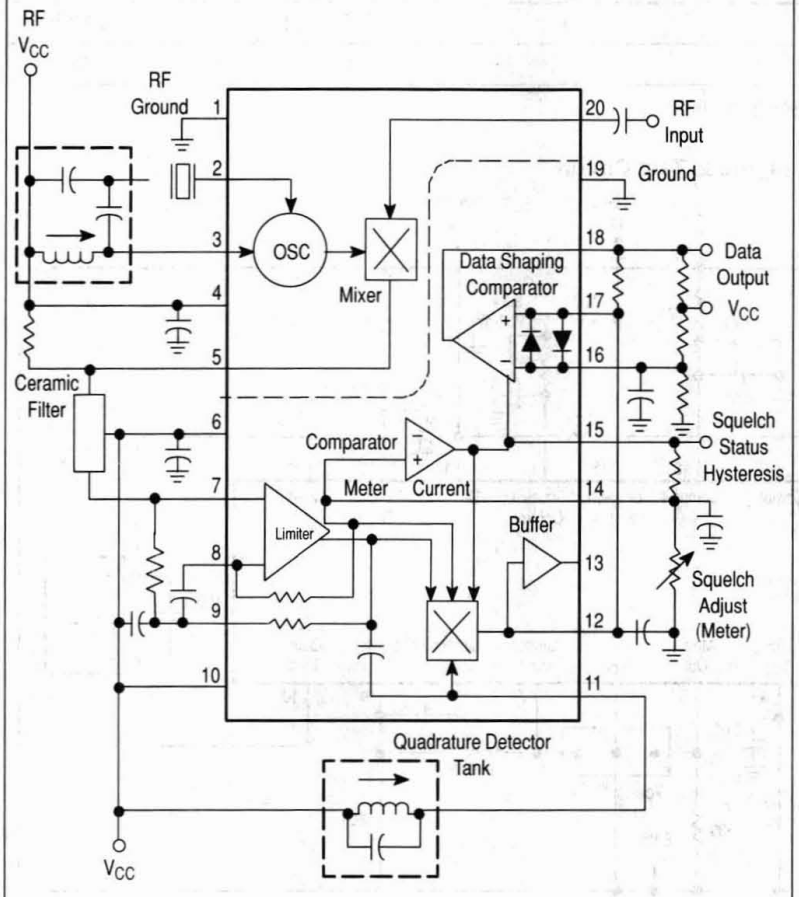
SEMICONDUCTOR TECHNICAL DATA



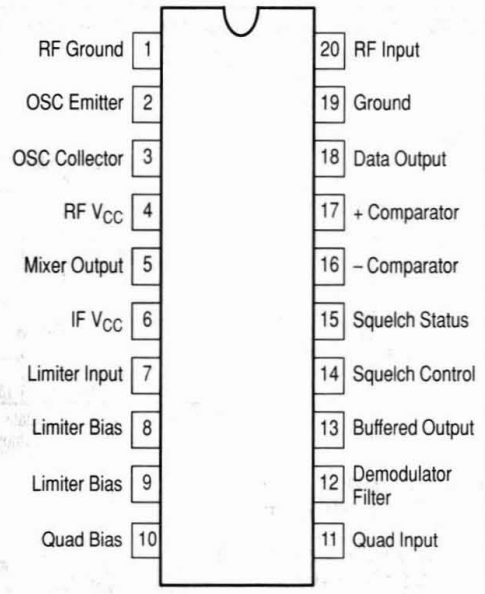
P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3356DW	T_A = – 40 to +85°C	SO–20L
MC3356P		Plastic DIP

MAXIMUM RATINGS

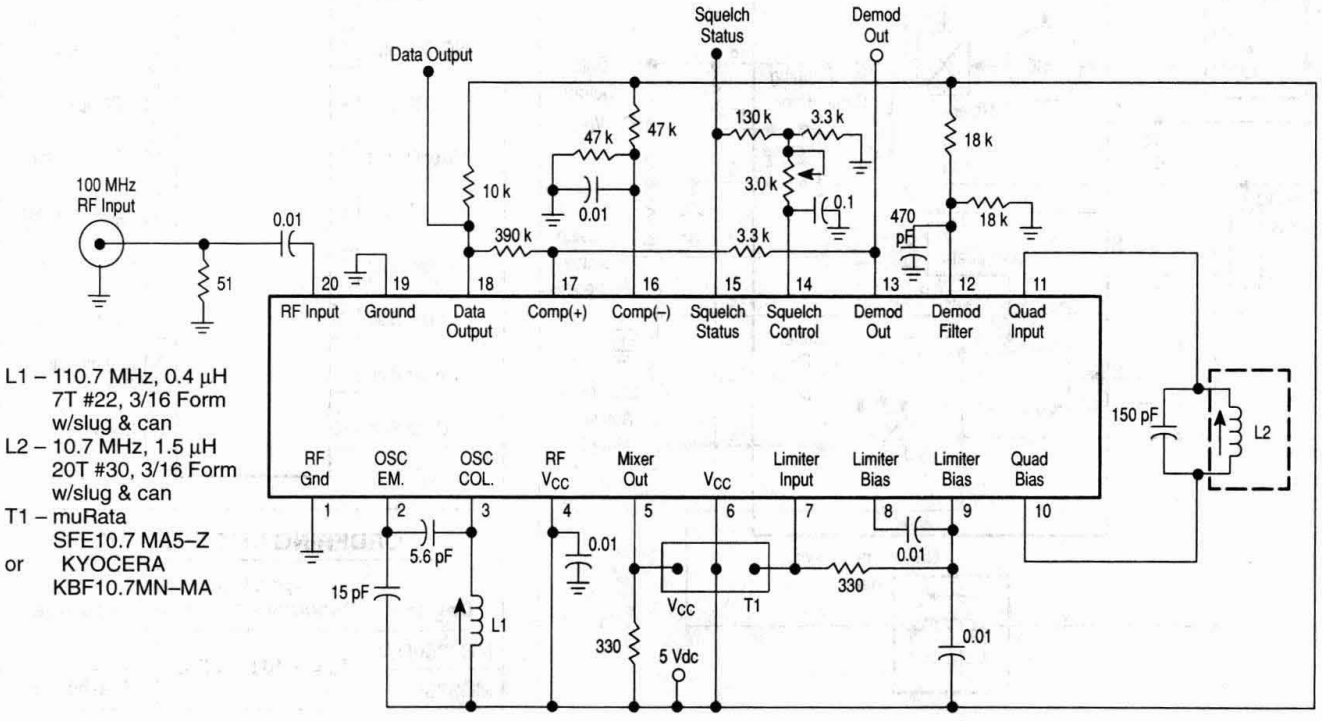
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating RF Supply Voltage Range (Pin 4)	RF V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 2, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	–	20	25	mAdc
Input for – 3 dB limiting	–	30	–	μVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	–	60	–	μVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	–	–	
Mixer Input Resistance, 100 MHz	–	260	–	Ω
Mixer Input Capacitance, 100 MHz	–	5.0	–	pF
Mixer/Oscillator Frequency Range (Note 1)	–	0.2 to 150	–	MHz
IF/Quadrature Detector Frequency Range (Note 1)	–	0.2 to 50	–	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	–	50	–	dB
Demodulator Output, Pin 13	–	0.5	–	Vrms
Meter Drive	–	7.0	–	μA/dB
Squelch Threshold	–	0.8	–	Vdc

NOTE: 1. Not taken in Test Circuit of Figure 2; new component values required.

Figure 2. Test Circuit



L1 – 110.7 MHz, 0.4 μH
7T #22, 3/16 Form
w/slug & can
L2 – 10.7 MHz, 1.5 μH
20T #30, 3/16 Form
w/slug & can
T1 – muRata
SFE10.7 MA5–Z
or KYOCERA
KBF10.7MN–MA

Figure 3. Output Components of Signal, Noise, and Distortion

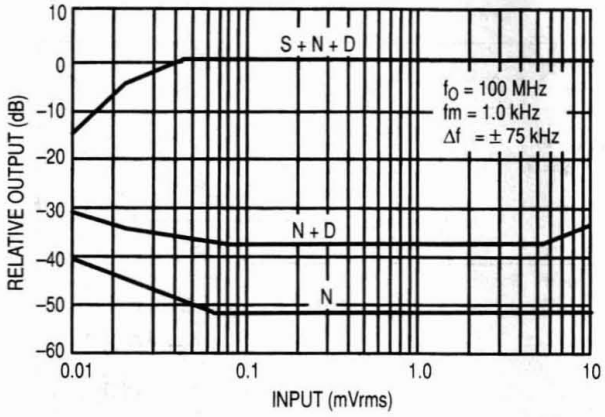
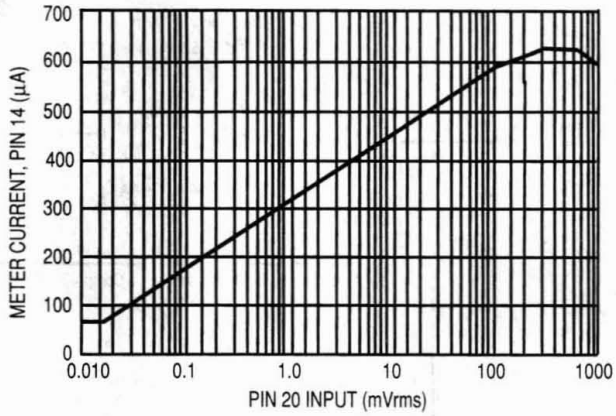


Figure 4. Meter Current versus Signal Input



GENERAL DESCRIPTION

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L–C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but non–linearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The –3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

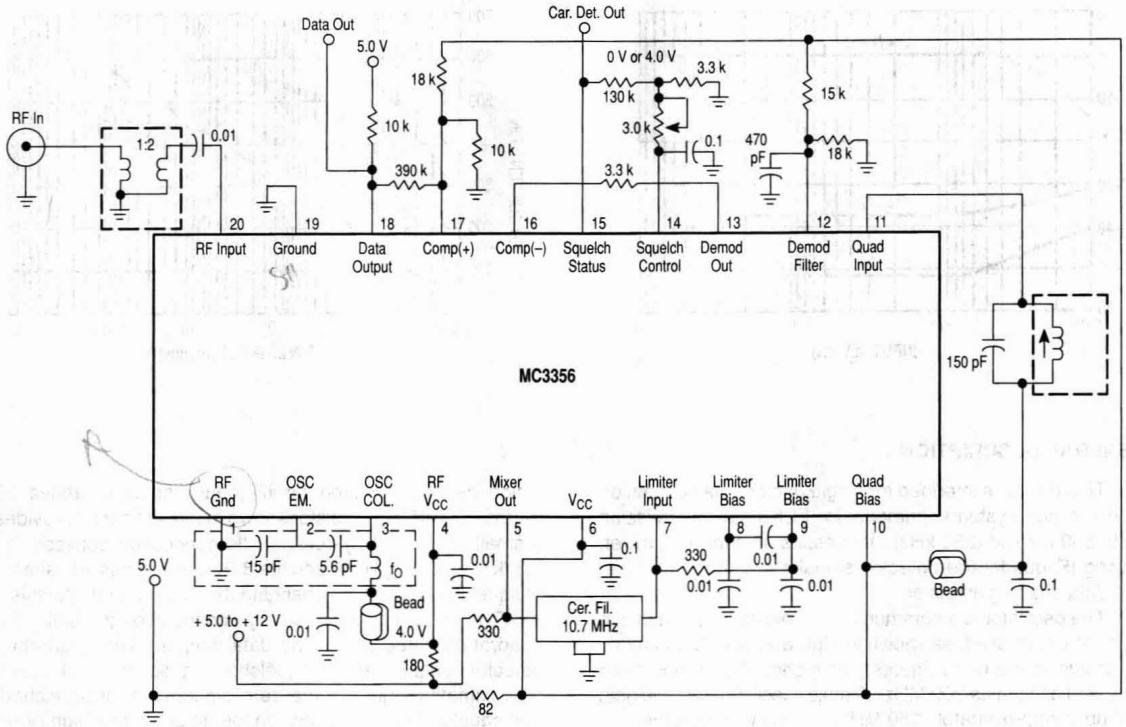
The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low (input to (+) input of Data Shaper as shown in Figures 1 and 2).

APPLICATION NOTES

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

Figure 5. Application with Fixed Bias on Data Shaper



APPLICATION NOTES (continued)

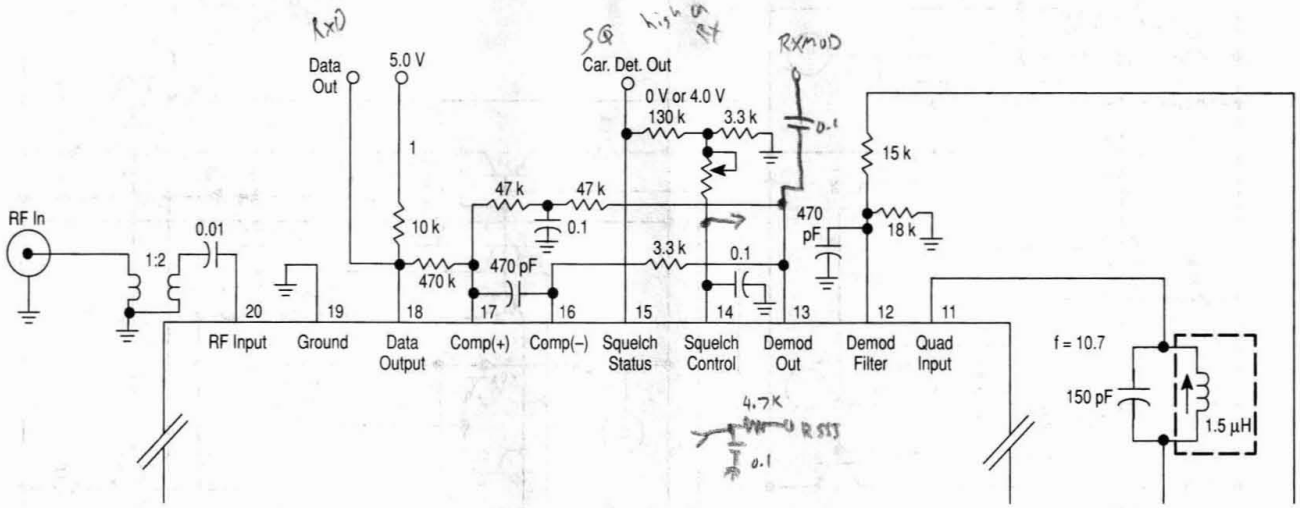
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has a separate V_{CC} and ground for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of Figures 1 and 2 have RF, Oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 5, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a **separate** path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 2 shows a successful implementation on a common 5.0 V supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 2 has a 3 dB limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in Figures 5 and 6. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at 5.0 V, the mixer/oscillator optimum performance is at 8.0 V to 12 V. A minimum of 8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

Figure 6. Application with Self–Adjusting Bias on Data Shaper

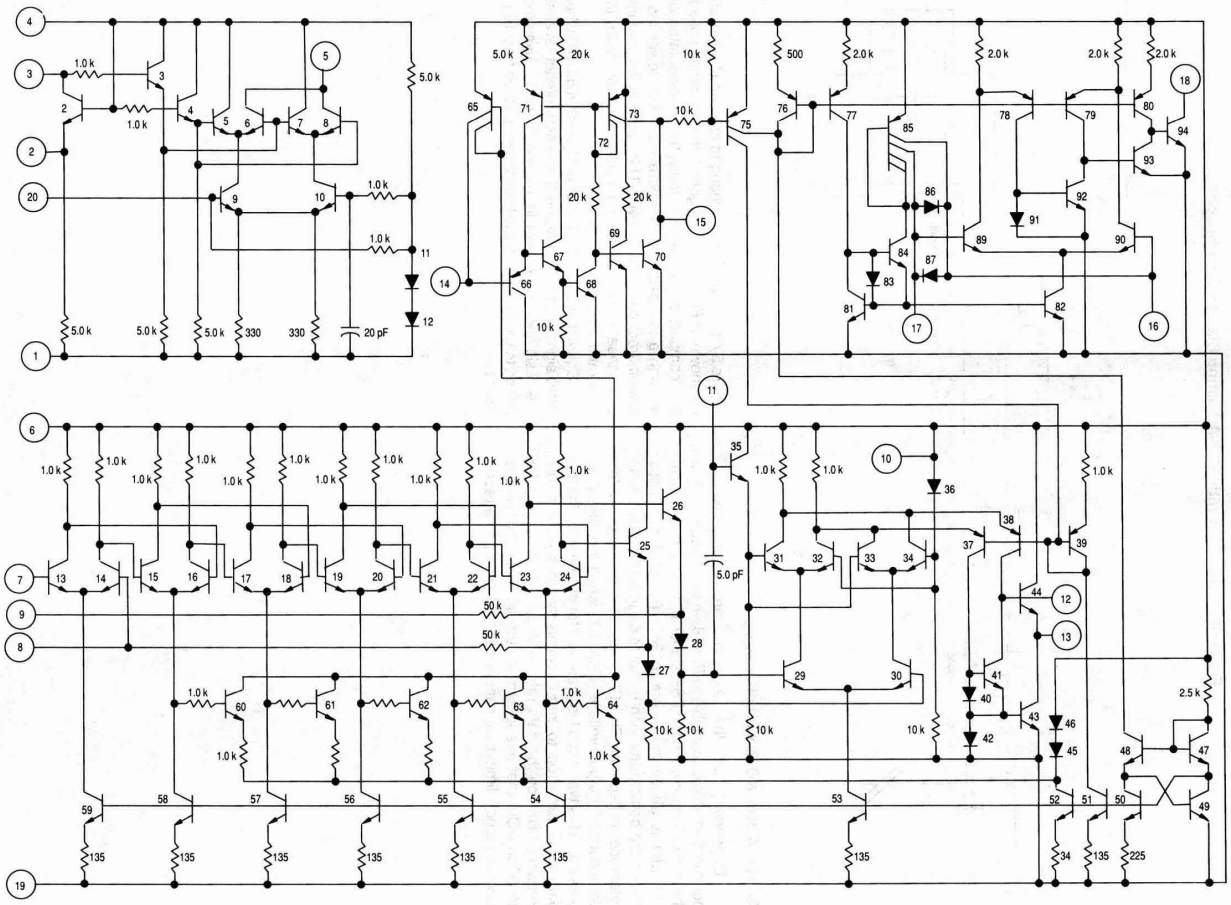


APPLICATION NOTES (continued)

Depending on the external circuit, inverted or noninverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a "one" when the local oscillator is above the incoming RF. Figure 5 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 5 circuit can then be changed to a circuit configuration as shown in Figure 6. In Figure 6 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

Figure 7. Internal Schematic



MOTOROLA

Low Power Narrowband FM IF

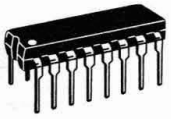
. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typical) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (– 3.0 dB) = 5.0 μV (Typical)
- Low Number of External Parts Required
- Recommend MC3372 for Replacement/Upgrade

MC3357

LOW POWER FM IF

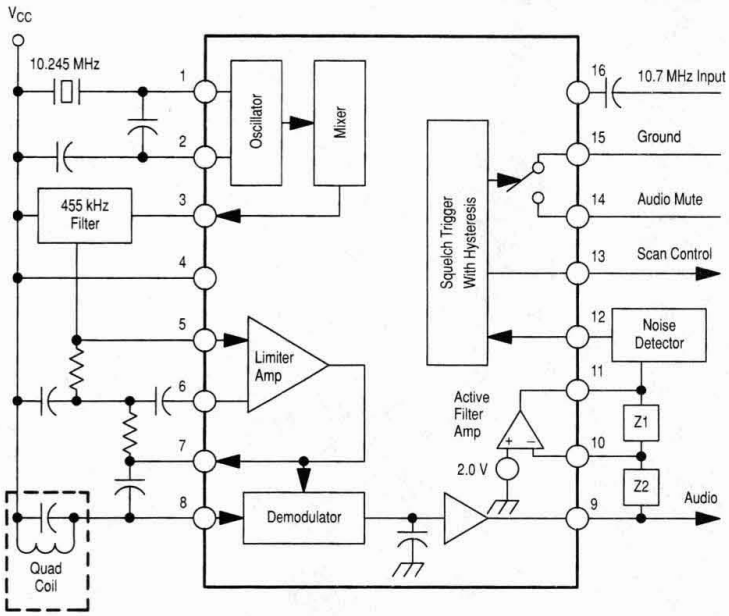
SEMICONDUCTOR TECHNICAL DATA



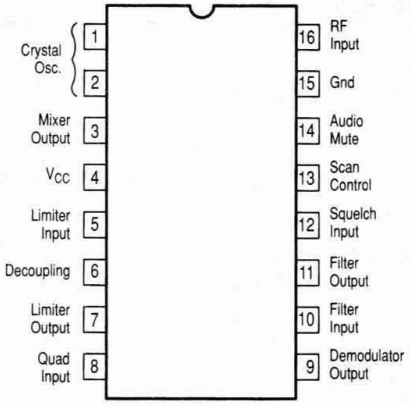
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3357D	T_A = – 30 to +70°C	SO–16
MC3357P		Plastic DIP

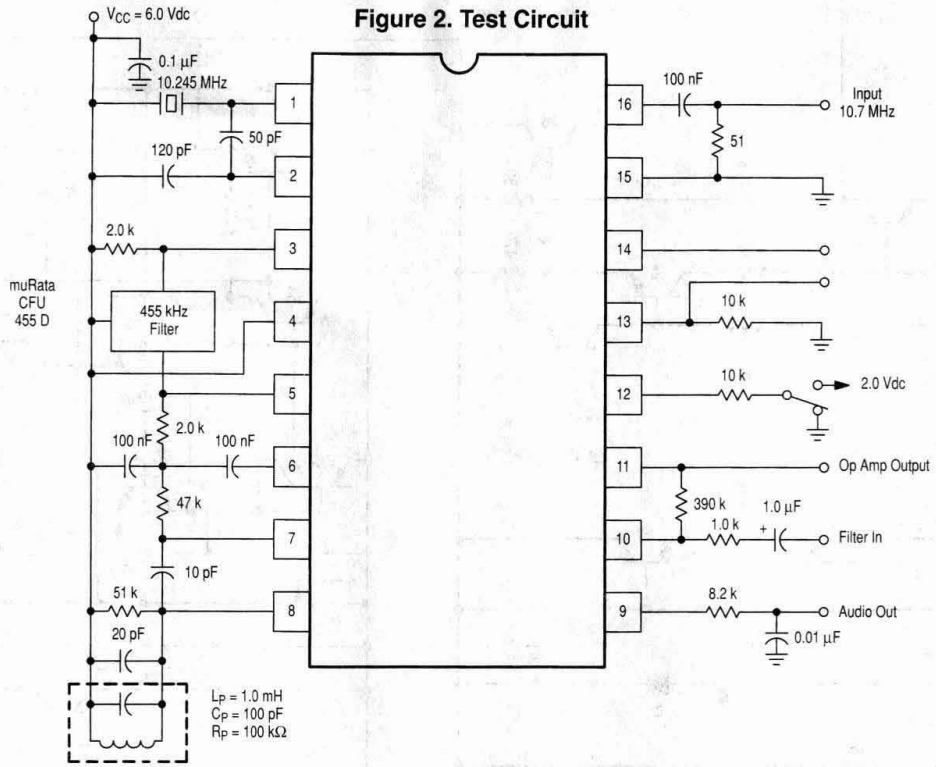
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp–p
Input Voltage (V_{CC} ≥ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	–0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 30 to + 70	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current Squelch Off Squelch On	4	– –	2.0 3.0	– 5.0	mA
Input Limiting Voltage (– 3 dB Limiting)	16	–	5.0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

Figure 2. Test Circuit



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer–oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of a noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally–biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly–balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B +, below which it can swing 0.5 V.

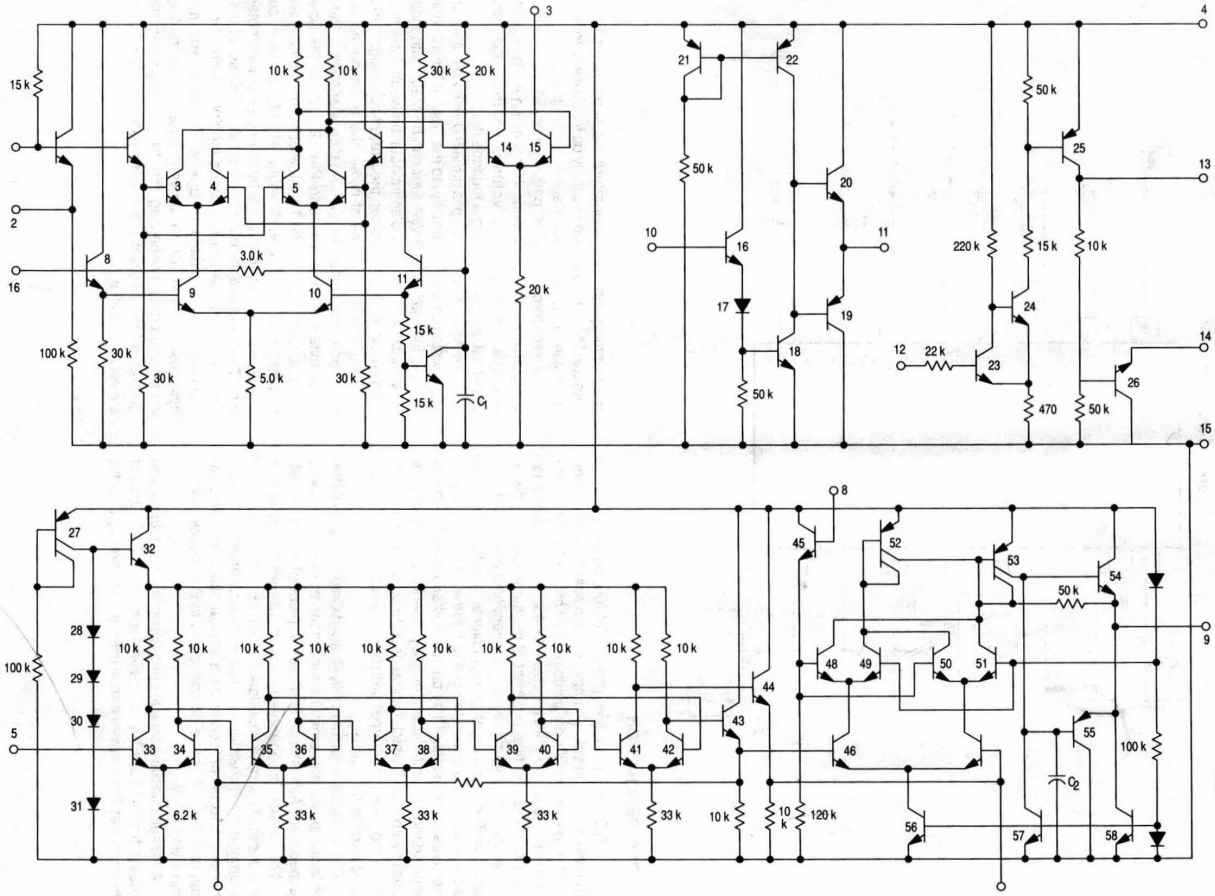
After suitable bandpass filtering (ceramic or LC), the signal goes to the input of a five–stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered, giving an impedance of around 400 Ω at Pin 9. The signal still requires de–emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 µA and Pin 14 is internally short–circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high–impedance ground–reference point in the audio path between Pin 9 and the audio amplifier.

Figure 3. Circuit Schematic



MOTOROLA

MC3359

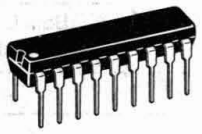
Low Power Narrowband FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts. For low cost applications requiring V_{CC} below 6.0 V, the MC3361BP,BD are recommended. For applications requiring a fixed, tuned, ceramic quadrature resonator, use the MC3357. For applications requiring dual conversion and RSSI, refer to these devices; MC3335, MC3362 and MC3363.

- Low Drain Current: 3.6 mA (Typical) @ V_{CC} = 6.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage – – 3.0 dB = 2.0 μV (Typical)
- Low Number of External Parts Required
- For Low Voltage and RSSI, use the MC3371

HIGH GAIN LOW POWER FM IF

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3359DW	T_A = –30 to +70°C	SO–20L
MC3359P		Plastic DIP

Figure 1. Simplified Application in a Scanner Receiver

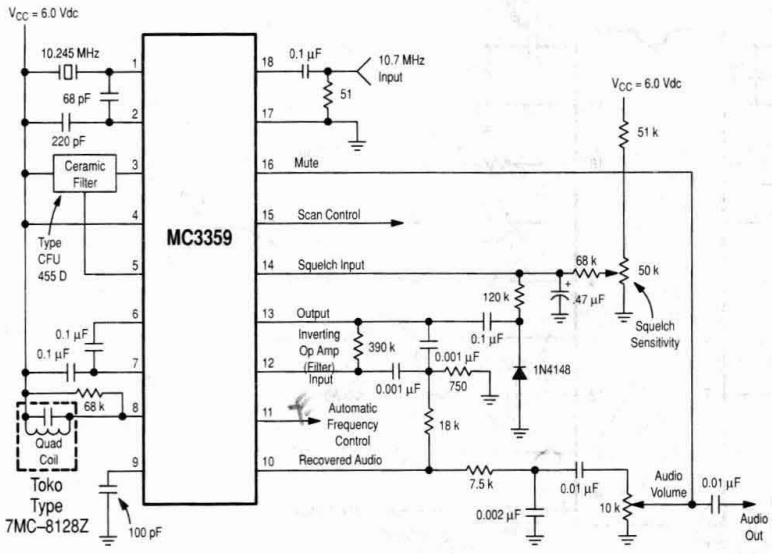
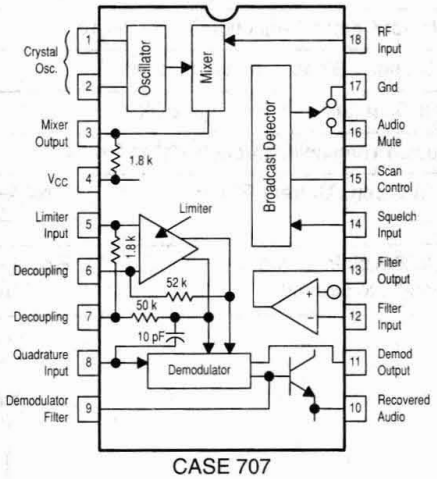
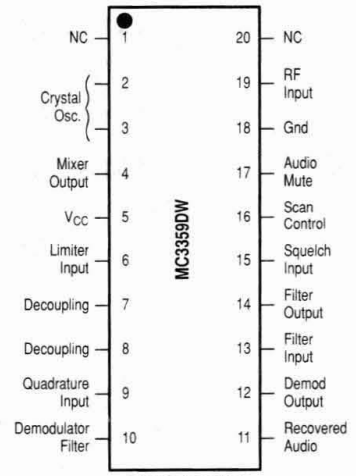


Figure 2. Pin Connections and Functional Block Diagram



CASE 707



CASE 751D

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	6 to 9	Vdc
Input Voltage (V_{CC} ≥ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	– 0.7 to 12	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 30 to + 70	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (Pins 4 and 8)	Squelch Off Squelch On	– –	3.6 5.4	6.0 7.0	mA
Input for 20 dB Quieting		–	8.0	–	µVrms
Input for – 3.0 dB Limiting		–	2.0	–	µVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		–	6	–	
Mixer Third Order Intercept, 50 Ω Input		–	– 1.0	–	dBm
Mixer Input Resistance		–	3.6	–	kΩ
Mixer Input Capacitance		–	2.2	–	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	–	mVrms
Detector Center Frequency Slope, Pin 10		–	0.3	–	V/kHz
AFC Center Slope, Pin 11, Unloaded		–	12	–	V/kHz
Filter Gain (test circuit of Figure 3)		40	51	–	dB
Squelch Threshold, Through 10K to Pin 14		–	0.62	–	Vdc
Scan Control Current, Pin 15	Pin 14 – High – Low	– 2.0	0.01 2.4	1.0 –	µA mA
Mute Switch Impedance Pin 16 to Ground	Pin 14 – High – Low	–	5.0 1.5	10 –	Ω MΩ

Figure 3. Test Circuit

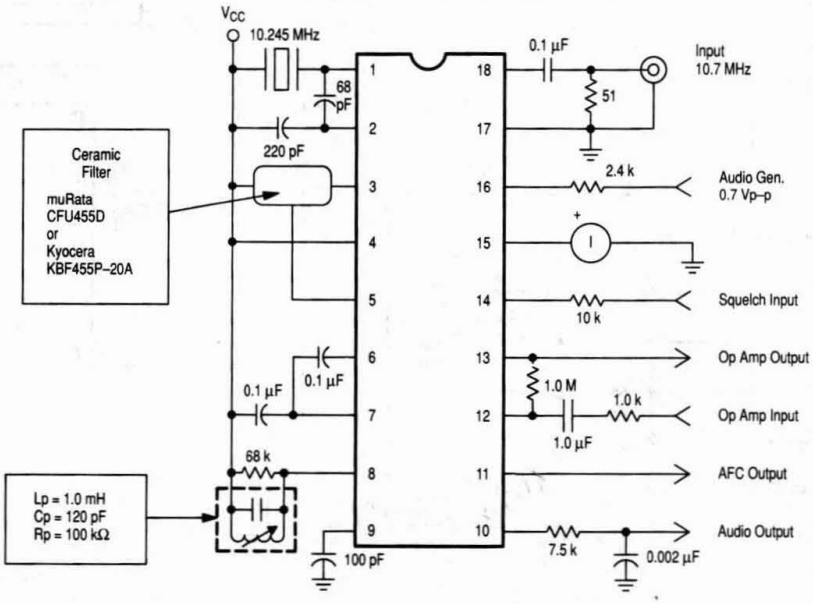


Figure 4. Mixer Voltage Gain

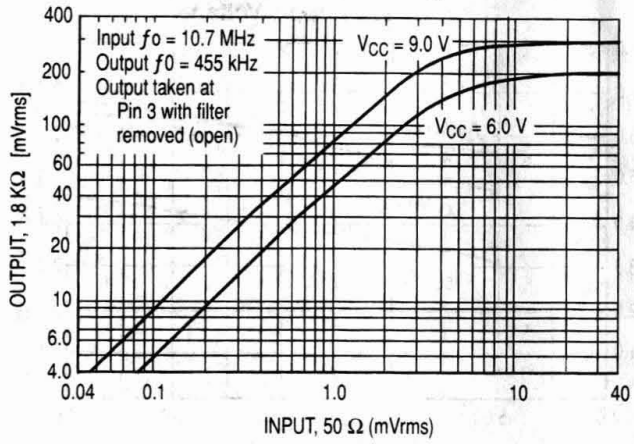


Figure 5. Limiting IF Frequency Response

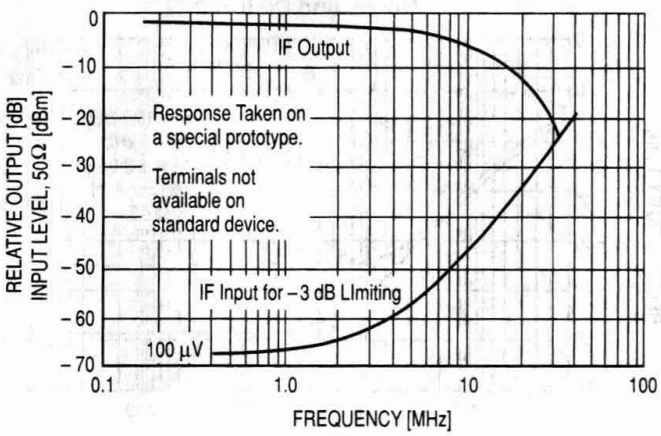


Figure 6. Mixer Third Order Intermodulation Performance

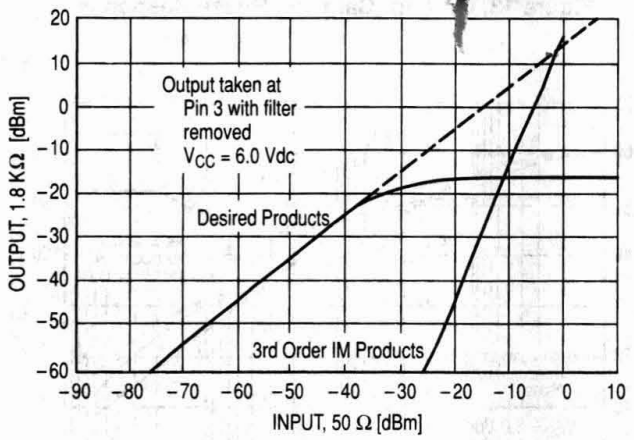


Figure 7. Detector and AFC Responses

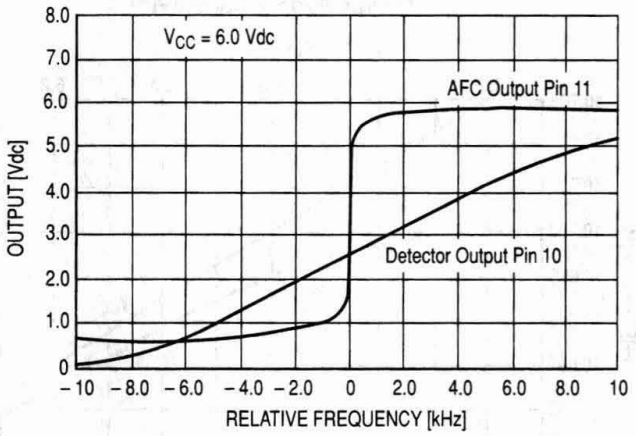


Figure 8. Relative Mixer Gain

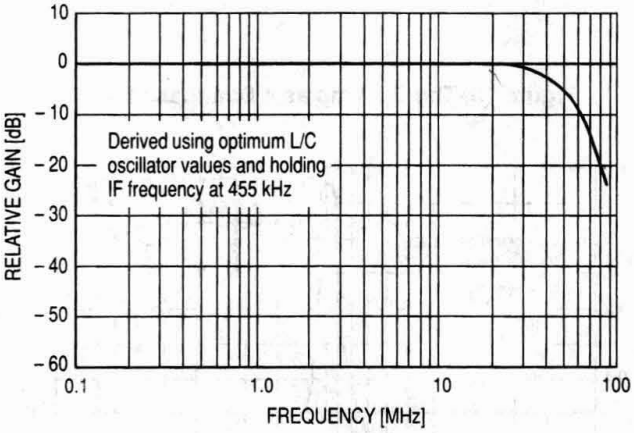


Figure 9. Overall Gain, Noise, and AM Rejection

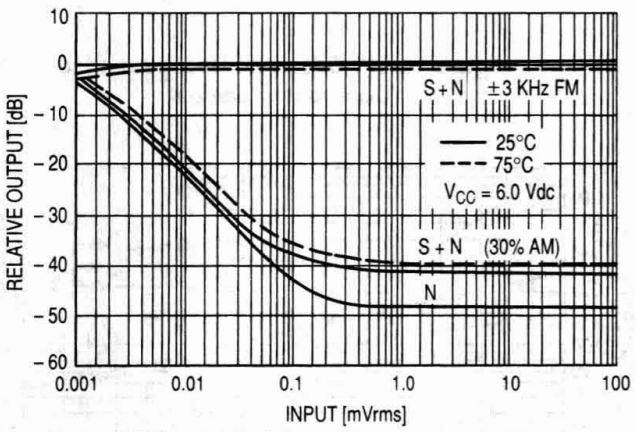


Figure 10. Output Components of Signal, Noise, and Distortion

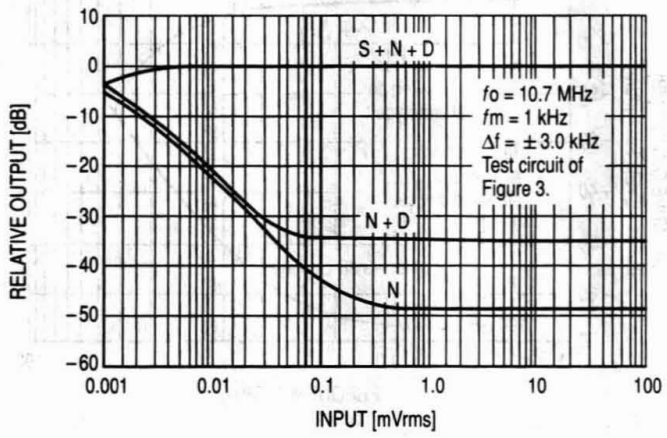


Figure 11. Audio Output and Total Current Drain versus Supply Voltage

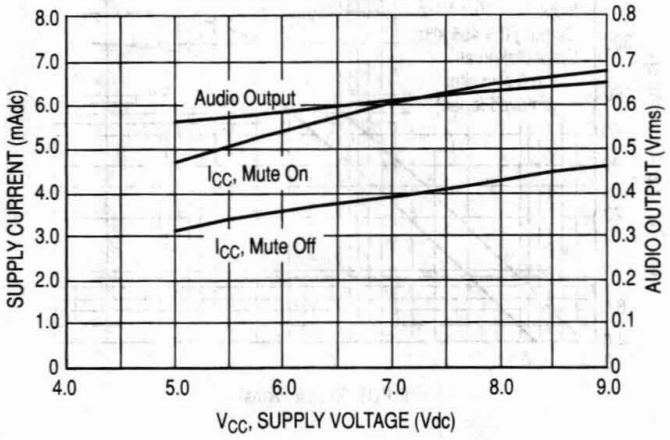


Figure 12. L/C Oscillator, Temperature and Power Supply Sensitivity

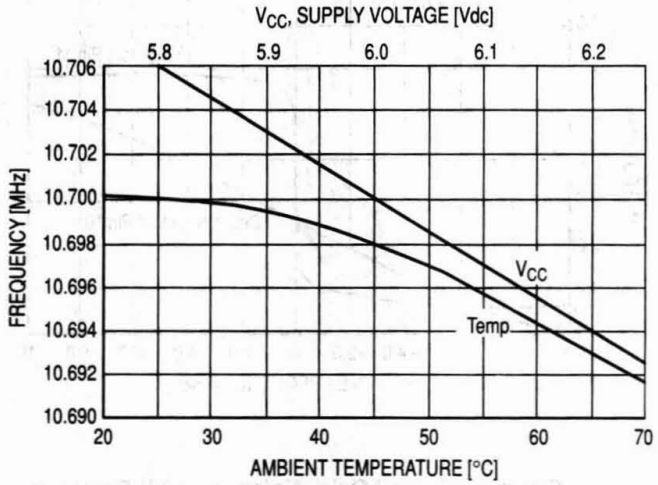


Figure 13. Op Amp Gain and Phase Response

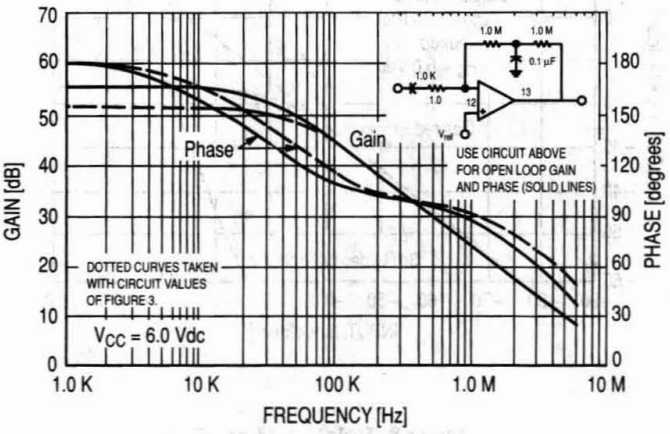

GAIN [dB]
PHASE [degrees]
FREQUENCY [Hz]
Phase
Gain
USE CIRCUIT ABOVE FOR OPEN LOOP GAIN AND PHASE (SOLID LINES)
DOTTED CURVES TAKEN WITH CIRCUIT VALUES OF FIGURE 3.
VCC = 6.0 Vdc

Figure 14. L/C Oscillator Recommended Component Values

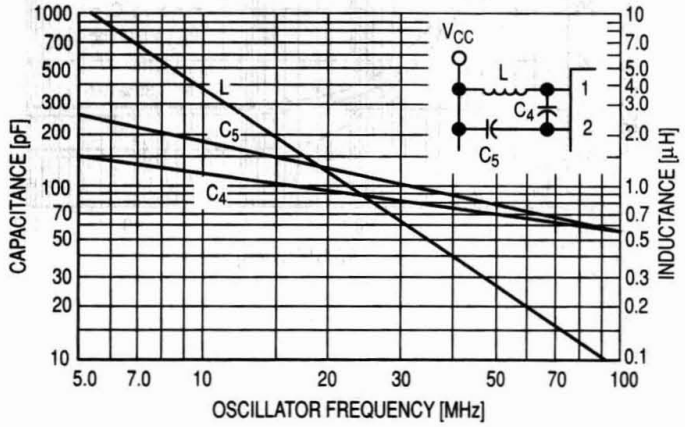


Figure 15. The Op Amp as a Bandpass Filter

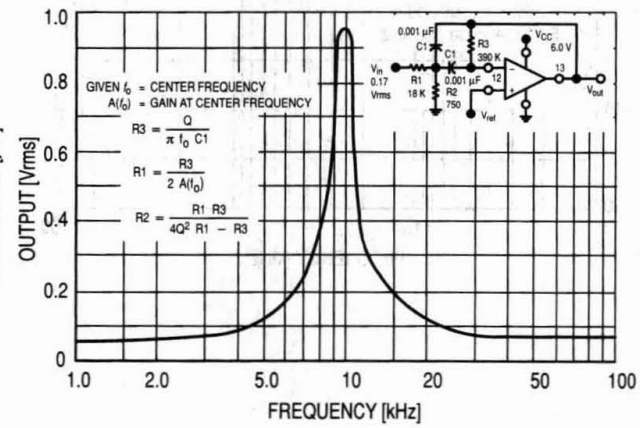
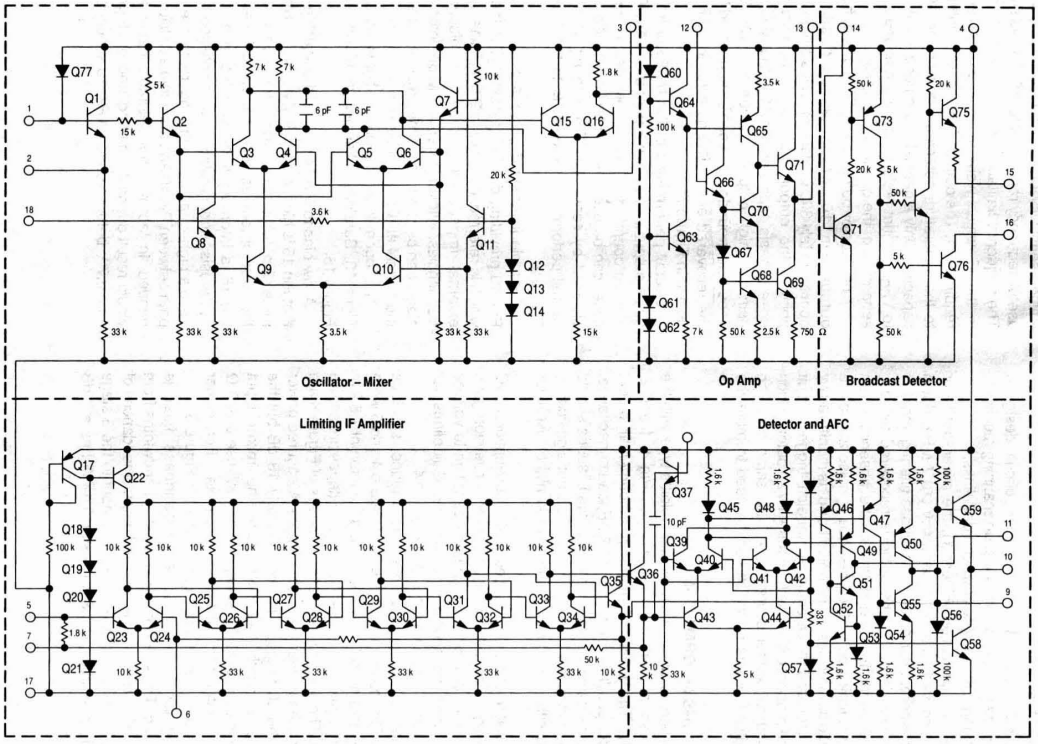


Figure 16. Representative Schematic Diagram



CIRCUIT DESCRIPTION

The MC3359 is a low–power FM IF circuit designed primarily for use in voice–communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer–oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch–trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATIONS INFORMATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1 and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ±2 kHz to ±15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC}. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximately 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de–emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode, the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch–trigger circuit so that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open–circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high–impedance ground–reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.

MOTOROLA

MC3361C

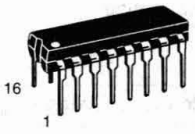
Low Power Narrowband FM IF

The MC3361C includes an Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control and Mute Switch. This device is designed for use in FM dual conversion communications equipment.

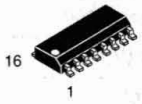
- Operates from 2.0 to 8.0 V Supply
- Low Drain Current 2.8 mA Typical @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage – – 3.0 dB = 2.6 μV Typical
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz
- Full ESD Protection

LOW POWER NARROWBAND FM IF

SEMICONDUCTOR TECHNICAL DATA

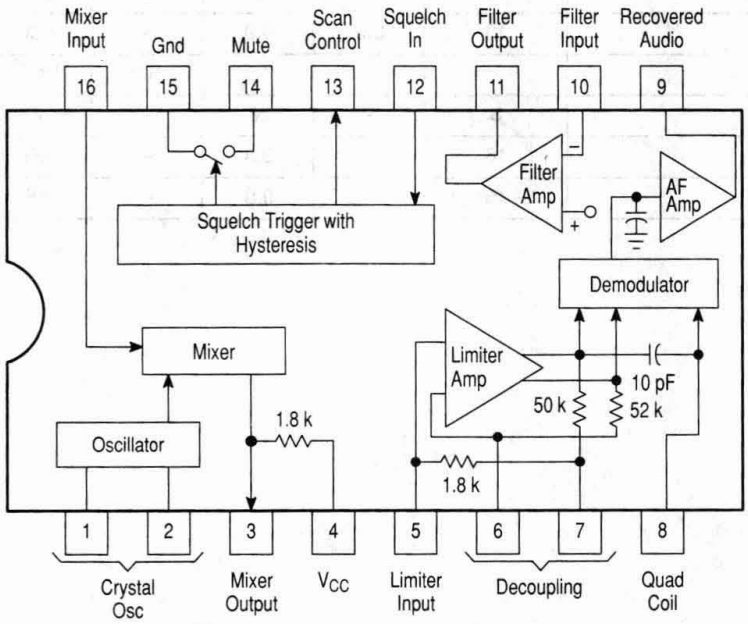


P SUFFIX
PLASTIC PACKAGE
CASE 648



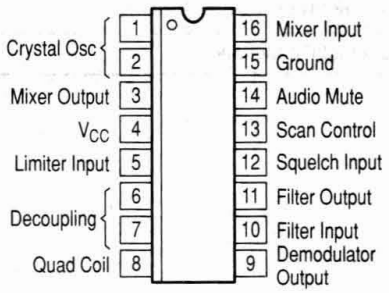
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Representative Block Diagram



This device contains 92 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3361CD	T_A = – 30 to +70°C	SO–16
MC3361CP		Plastic DIP

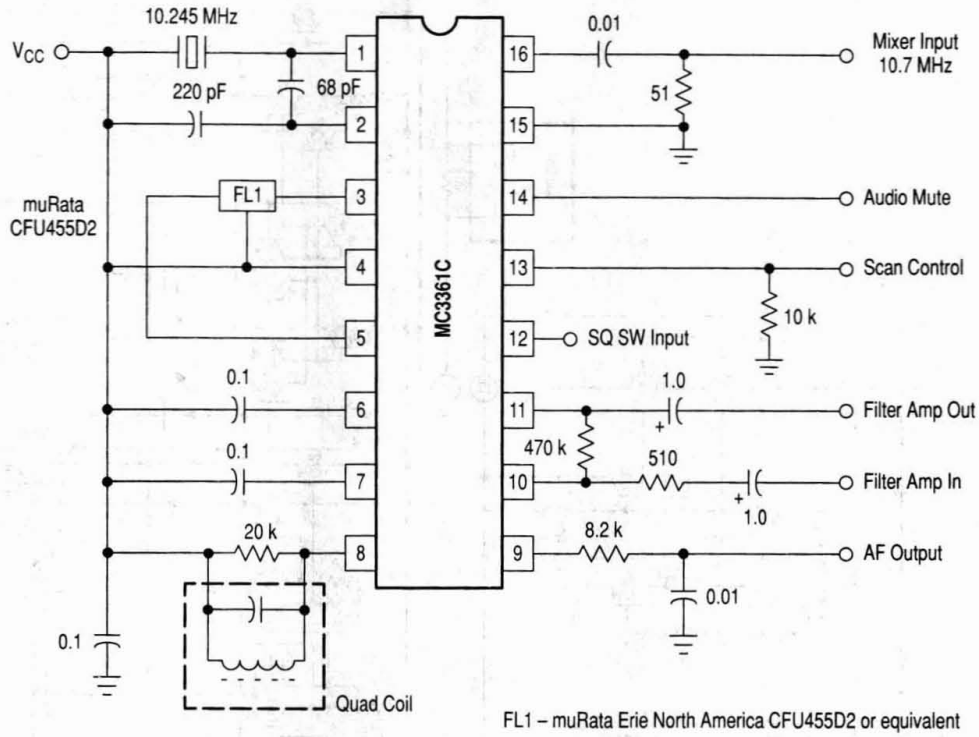
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	–	1.0	Vp–p
Input Voltage (V_{CC} ≥ 4.0 V)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	–0.5 to +5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	–30 to +70	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (No Signal)	4				mA
Squelch "Off"		2.0	2.8	3.5	
Squelch "On"		3.7	5.2	6.3	
Recovered Audio Output Voltage (V_{in} = 10 mVrms)	9	130	170	210	mVrms
Input Limiting Voltage (–3.0 dB Limiting)	16	–	2.6	6.0	μV
Total Harmonic Distortion	9	–	0.86	–	%
Recovered Output Voltage (No Input Signal)	9	60	190	350	mVrms
Drop Voltage AF Gain Loss	9	– 3.0	– 0.6	–	dB
Detector Output Impedance	–	–	450	–	Ω
Filter Gain (10 kHz) (V_{in} = 0.3 mVrms)	–	40	50	–	dB
Filter Output Voltage	11	0.5	0.7	0.9	Vdc
Mute Function Low	14	–	30	50	Ω
Mute Function High	14	1.0	11	–	MΩ
Scan Function Low (Mute "Off") (V_{12} = 1.0 Vdc)	13	–	0	0.4	Vdc
Scan Function High (Mute "On") (V_{12} = Gnd)	13	3.0	3.9	–	Vdc
Trigger Hysteresis	–	–	45	100	mV
Mixer Conversion Gain	3	–	28	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	9.0	–	pF

Figure 1. Test Circuit



FL1 – muRata Erie North America CFU455D2 or equivalent

Quadrature Coil – Toko America Type 7MC–8128Z or equivalent

C – µF, unless noted

Figure 2. Audio Output, Distortion versus Supply Voltage

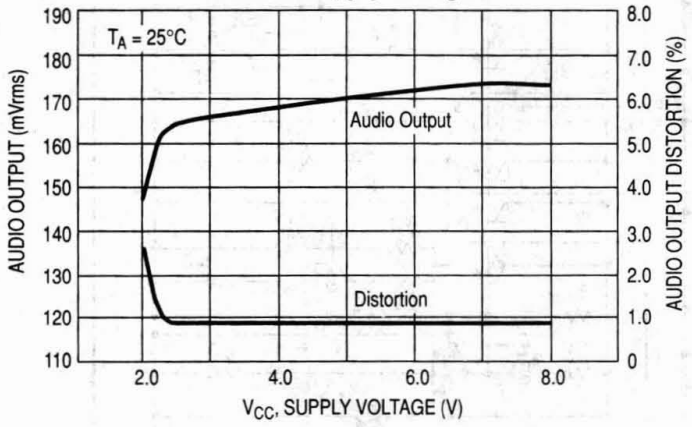
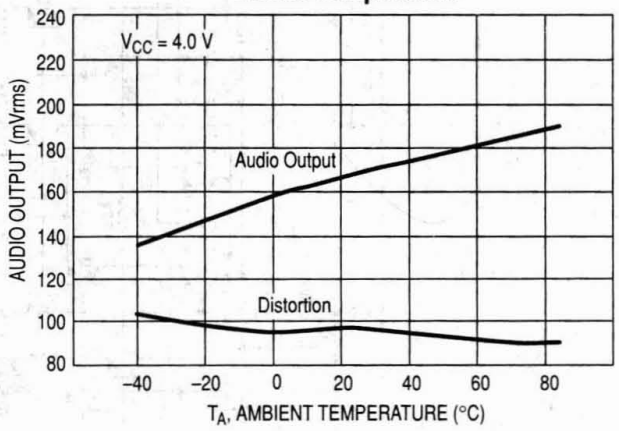


Figure 3. Audio Output, Distortion versus Temperature



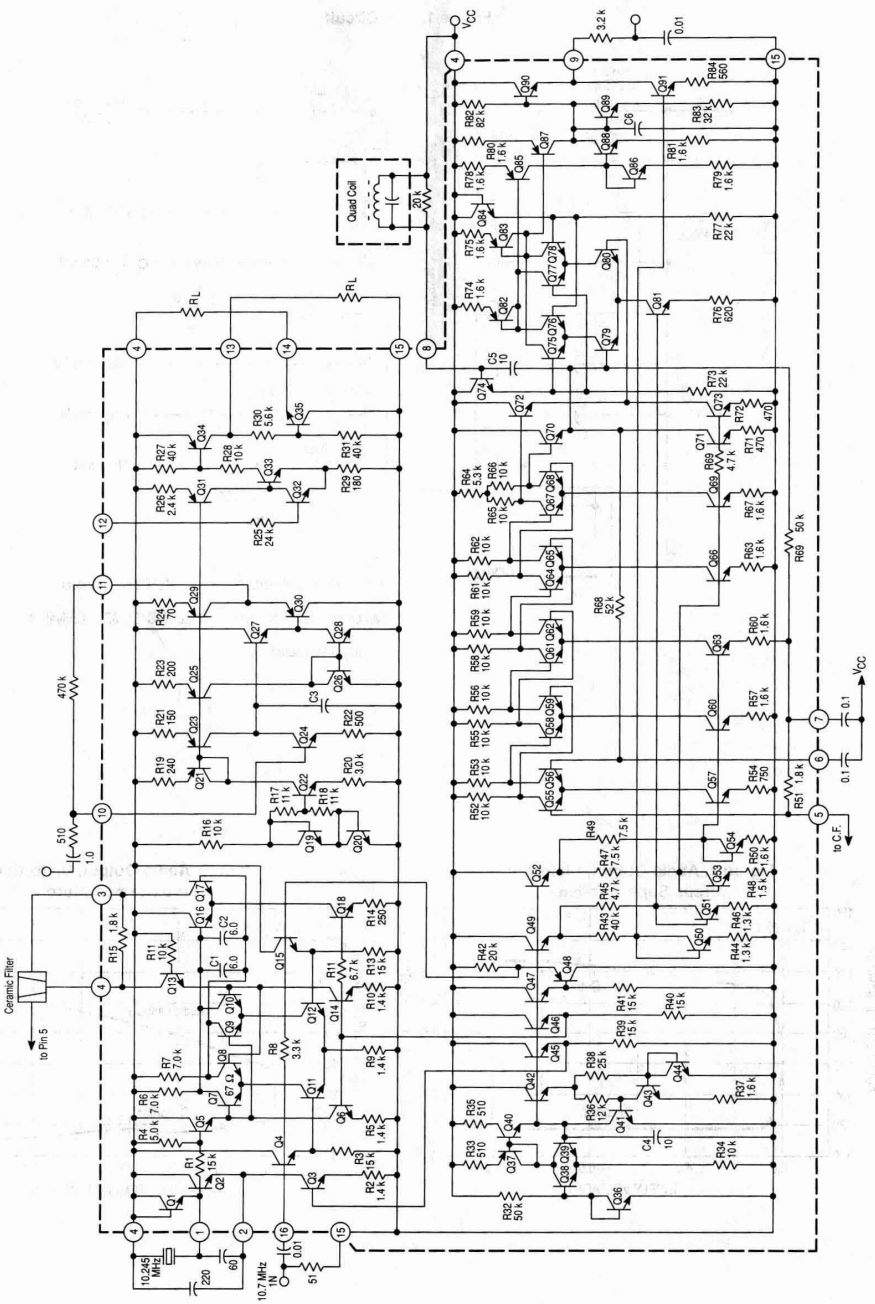


Figure 4. Low Voltage Low Power Narrowband FM IF

Figure 5. Input Limiting Voltage

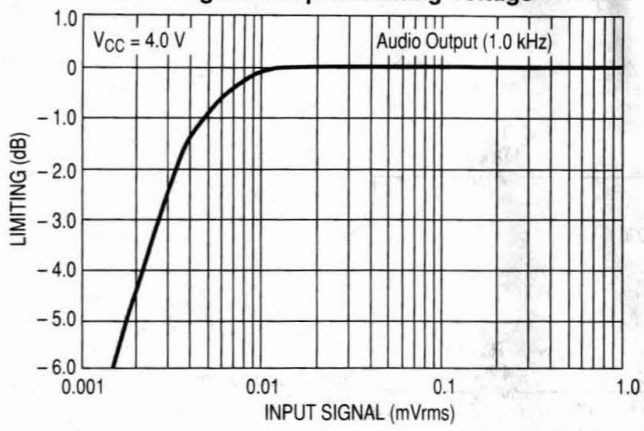


Figure 6. Overall Gain, Noise and AM Rejection

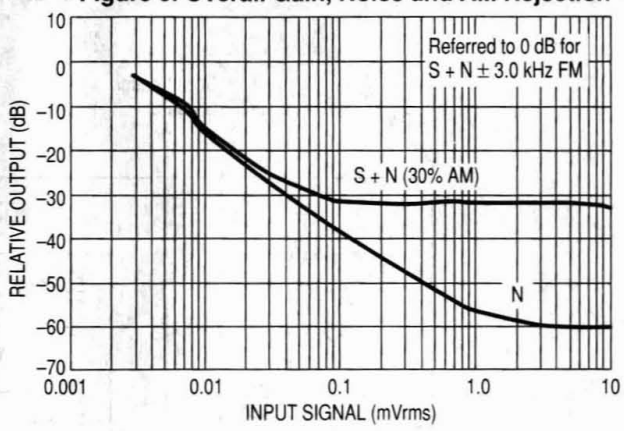


Figure 7. Filter Amp Response

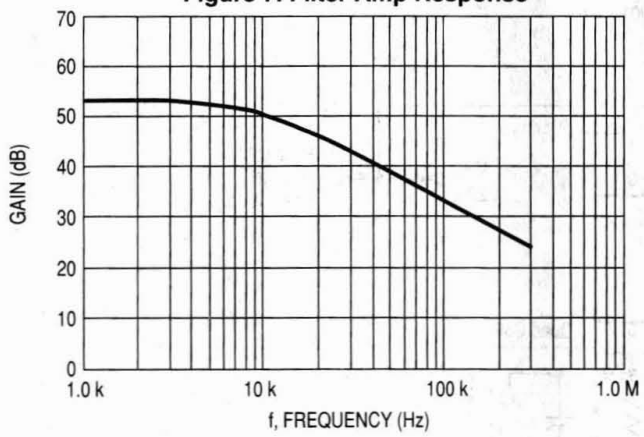


Figure 8. Filter Amp Gain

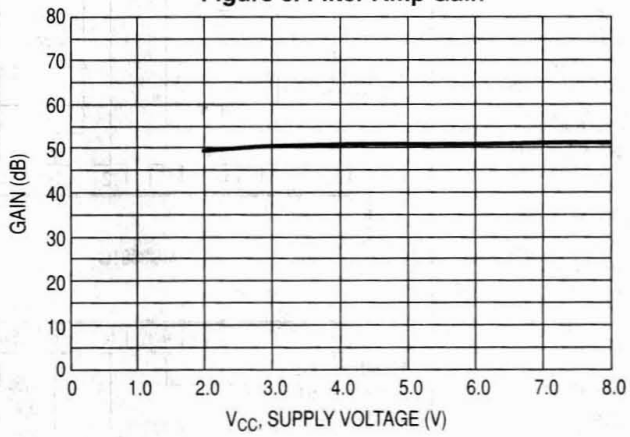


Figure 9. Supply Current

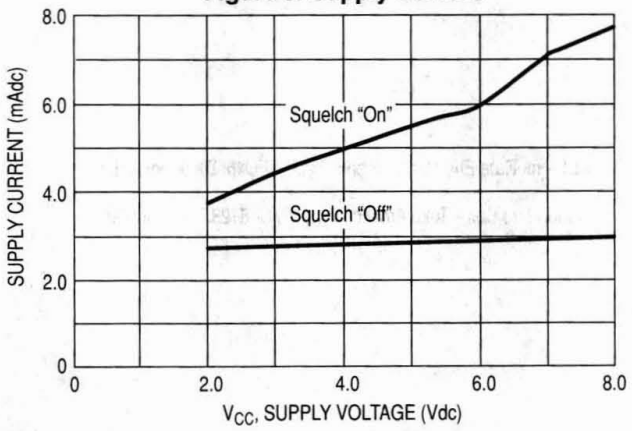
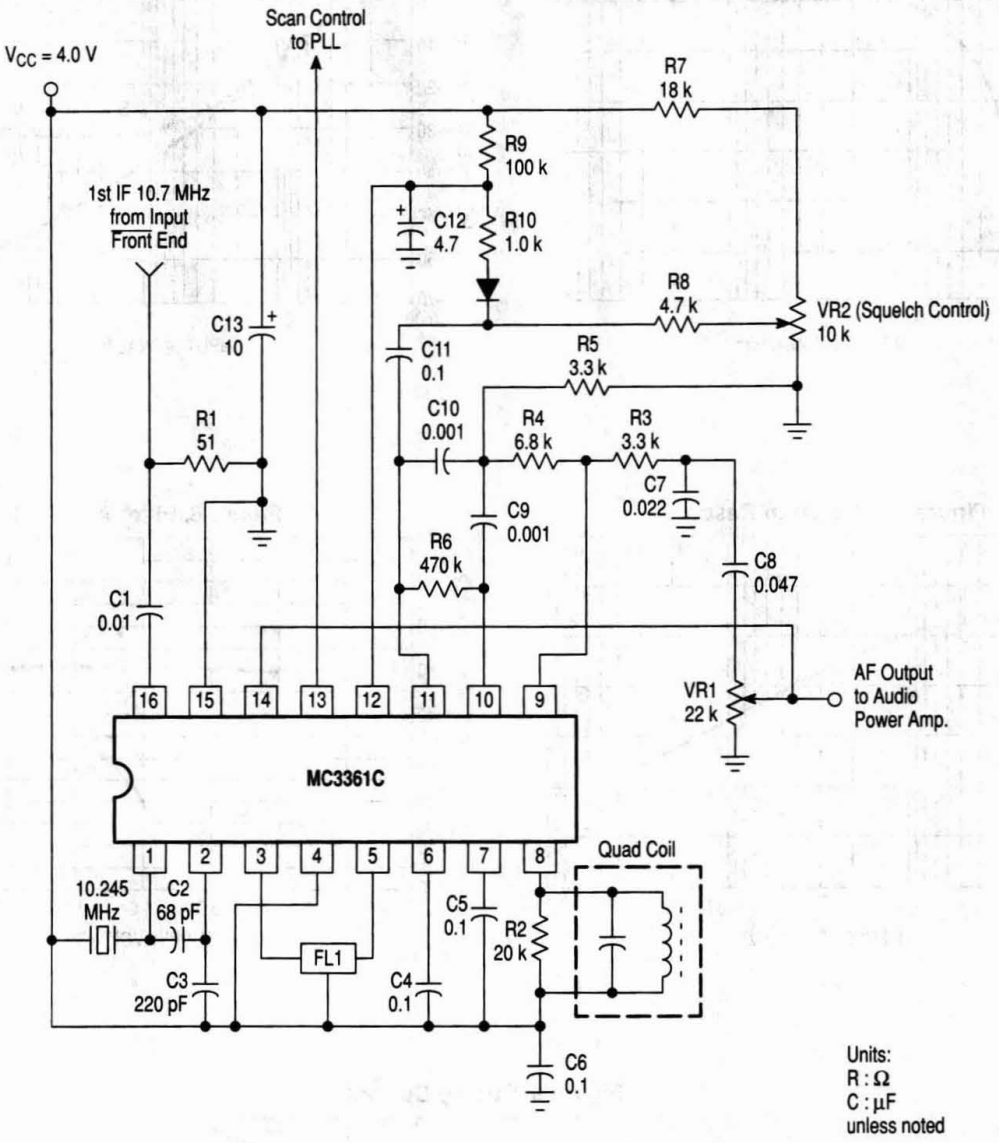


Figure 10. Simplified Application



FL1 – muRata Erie North America Type CFU455D2 or equivalent

Quadrature Coil – Toko America Type 7MC–8128Z or equivalent

MOTOROLA

MC3371
MC3372

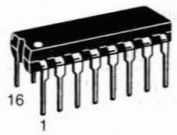
Low Power Narrowband FM IF

LOW POWER FM IF

The MC3371 and MC3372 perform single conversion FM reception and consist of an oscillator, mixer, limiting IF amplifier, quadrature discriminator, active filter, squelch switch, and meter drive circuitry. These devices are designed for use in FM dual conversion communication equipment. The MC3371/MC3372 are similar to the MC3361/MC3357 FM IFs, except that a signal strength indicator replaces the scan function controlling driver which is in the MC3361/MC3357. The MC3371 is designed for the use of parallel LC components, while the MC3372 is designed for use with either a 455 kHz ceramic discriminator, or parallel LC components.

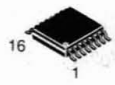
These devices also require fewer external parts than earlier products. The MC3371 and MC3372 are available in dual–in–line and surface mount packaging.

- Wide Operating Supply Voltage Range: V_{CC} = 2.0 to 9.0 V
- Input Limiting Voltage Sensitivity of –3.0 dB
- Low Drain Current: I_{CC} = 3.2 mA, @ V_{CC} = 4.0 V, Squelch Off
- Minimal Drain Current Increase When Squelched
- Signal Strength Indicator: 60 dB Dynamic Range
- Mixer Operating Frequency Up to 100 MHz
- Fewer External Parts Required than Earlier Devices



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

MAXIMUM RATINGS

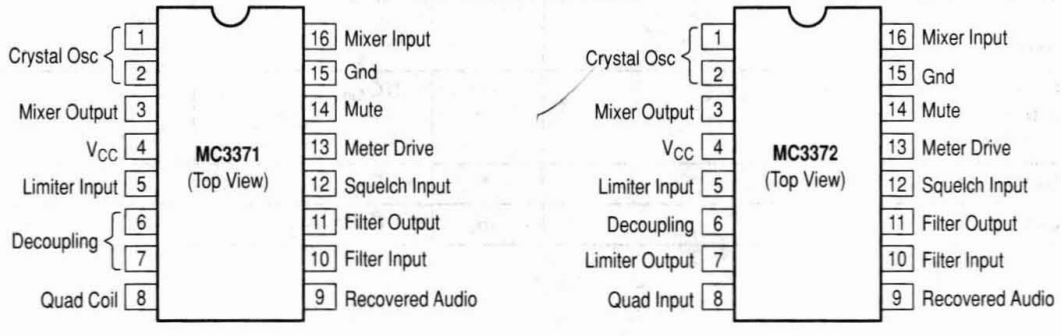
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
RF Input Voltage (V_{CC} ≥ 4.0 Vdc)	16	V16	1.0	Vrms
Detector Input Voltage	8	V8	1.0	Vpp
Squelch Input Voltage (V_{CC} ≥ 4.0 Vdc)	12	V12	6.0	Vdc
Mute Function	14	V_{14}	–0.7 to 10	V_{pk}
Mute Sink Current	14	I14	50	mA
Junction Temperature	–	T_J	150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3371D	T_A = –30° to +70°C	SO–16
MC3371DTB		TSSOP–16
MC3371P		Plastic DIP
MC3372D		SO–16
MC3372DTB		TSSOP–16
MC3372P		Plastic DIP

PIN CONNECTIONS



RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Supply Voltage (@ T_A = 25°C) (–30°C ≤ T_A ≤ +75°C)	4	V_{CC}	2.0 to 9.0 2.4 to 9.0	Vdc
RF Input Voltage	16	V_{rf}	0.0005 to 10	mVrms
RF Input Frequency	16	f_{rf}	0.1 to 100	MHz
Oscillator Input Voltage	1	V_{local}	80 to 400	mVrms
Intermediate Frequency	–	f_{if}	455	kHz
Limiter Amp Input Voltage	5	V_{if}	0 to 400	mVrms
Filter Amp Input Voltage	10	V_{fa}	0.1 to 300	mVrms
Squelch Input Voltage	12	V_{sq}	0 or 2	Vdc
Mute Sink Current	14	I_{sq}	0.1 to 30	mA
Ambient Temperature Range	–	T_A	–30 to +70	°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 58.1125 MHz, df = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, f_{local} = 57.6575 MHz, V_{local} = 0 dBm, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input for 12 dB SINAD Matched Input – (See Figures 11, 12 and 13) Unmatched Input – (See Figures 1 and 2)	–	V_{SIN}	 – –	 1.0 5.0	 – 15	µVrms
Input for 20 dB NQS	–	V_{NQS}	–	3.5	–	µVrms
Recovered Audio Output Voltage V_{rf} = –30 dBm	–	AF_O	120	200	320	mVrms
Recovered Audio Drop Voltage Loss Vrf = –30 dBm, V_{CC} = 4.0 V to 2.0 V	–	AF_{loss}	–8.0	–1.5	–	dB
Meter Drive Output Voltage (No Modulation) V_{rf} = –100 dBm V_{rf} = –70 dBm V_{rf} = –40 dBm	13	M_{Drv} MV1 MV2 MV3	 – 1.1 2.0	 0.3 1.5 2.5	 0.5 1.9 3.1	Vdc
Filter Amp Gain R_s = 600 Ω , f_s = 10 kHz, V_{fa} = 1.0 mVrms	–	$A_{V(Amp)}$	47	50	–	dB
Mixer Conversion Gain V_{rf} = –40 dBm, R_L = 1.8 kΩ	–	$A_{V(Mix)}$	14	20	–	dB
Signal to Noise Ratio V_{rf} = –30 dBm	–	s/n	36	67	–	dB
Total Harmonic Distortion V_{rf} = –30 dBm, BW = 400 Hz to 30 kHz	–	THD	–	0.6	3.4	%
Detector Output Impedance	9	Z_O	–	450	–	Ω
Detector Output Voltage (No Modulation) V_{rf} = –30 dBm	9	DV_O	–	1.45	–	Vdc
Meter Drive V_{rf} = –100 to –40 dBm	13	M_O	–	0.8	–	µA/dB
Meter Drive Dynamic Range RF_{In} IF_{In} (455 kHz)	13	MVD	 – –	 60 80	 – –	dB
Mixer Third Order Input Intercept Point f1 = 58.125 MHz f2 = 58.1375 MHz	–	ITO_{Mix}	–	–22	–	dBm
Mixer Input Resistance	16	R_{in}	–	3.3	–	kΩ
Mixer Input Capacitance	16	C_{in}	–	2.2	–	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (No Input Signal)	4					mA
Squelch Off, V_{sq} = 2.0 Vdc		Icc1	–	3.2	4.2	
Squelch On, V_{sq} = 0 Vdc		Icc2	–	3.6	4.8	
Squelch Off, V_{CC} = 2.0 to 9.0 V		dIcc1	–	1.0	2.0	
Detector Output (No Input Signal)	9	V9				Vdc
DC Voltage, V8 = V_{CC}			0.9	1.6	2.3	
Filter Output (No Input Signal)	11					Vdc
DC Voltage		V11	1.5	2.5	3.5	
Voltage Change, V_{CC} = 2.0 to 9.0 V		dV11	2.0	5.0	8.0	
Trigger Hysteresis	–	Hys	34	57	80	mV

Figure 1. MC3371 Functional Block Diagram and Test Fixture Schematic

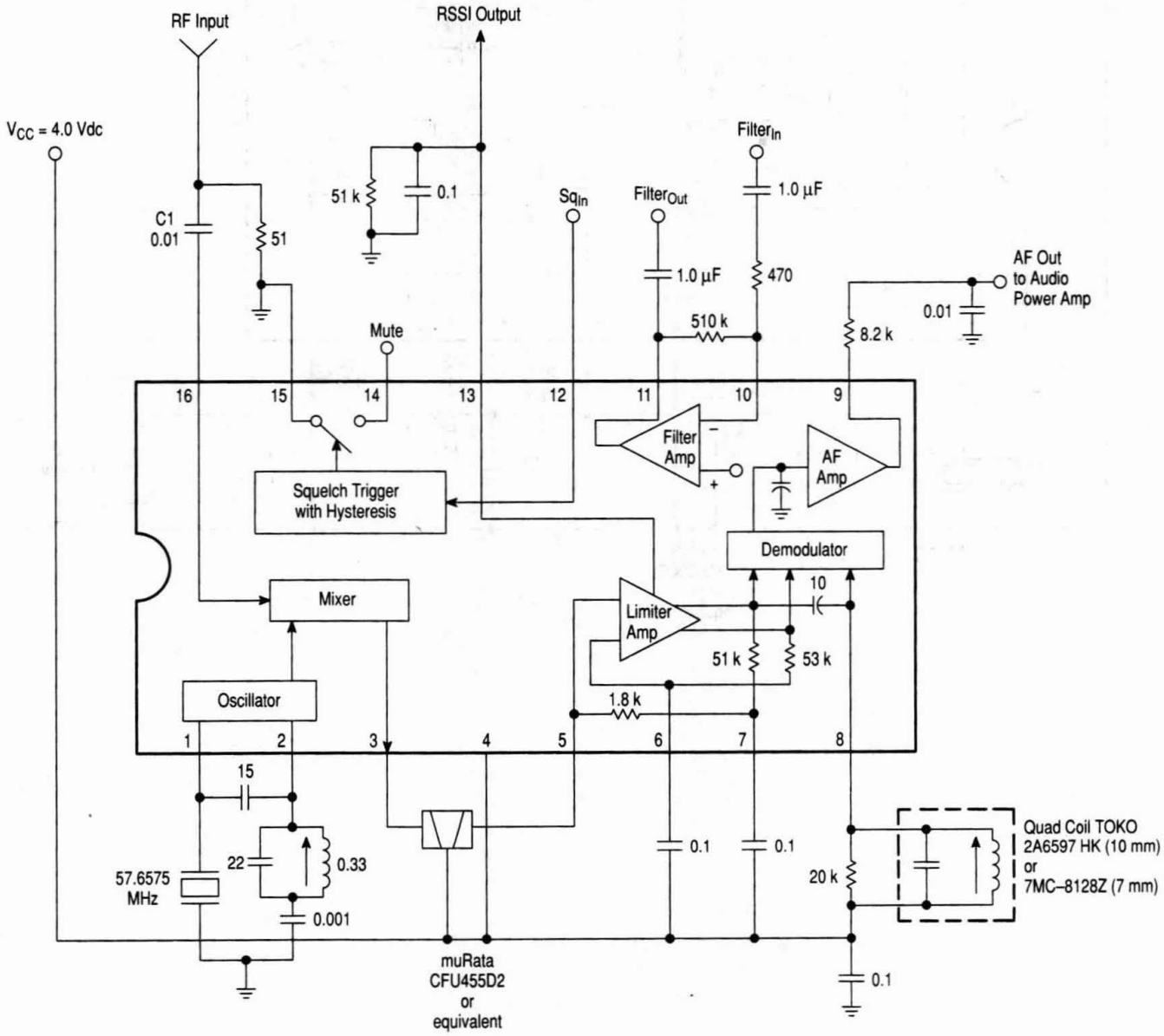
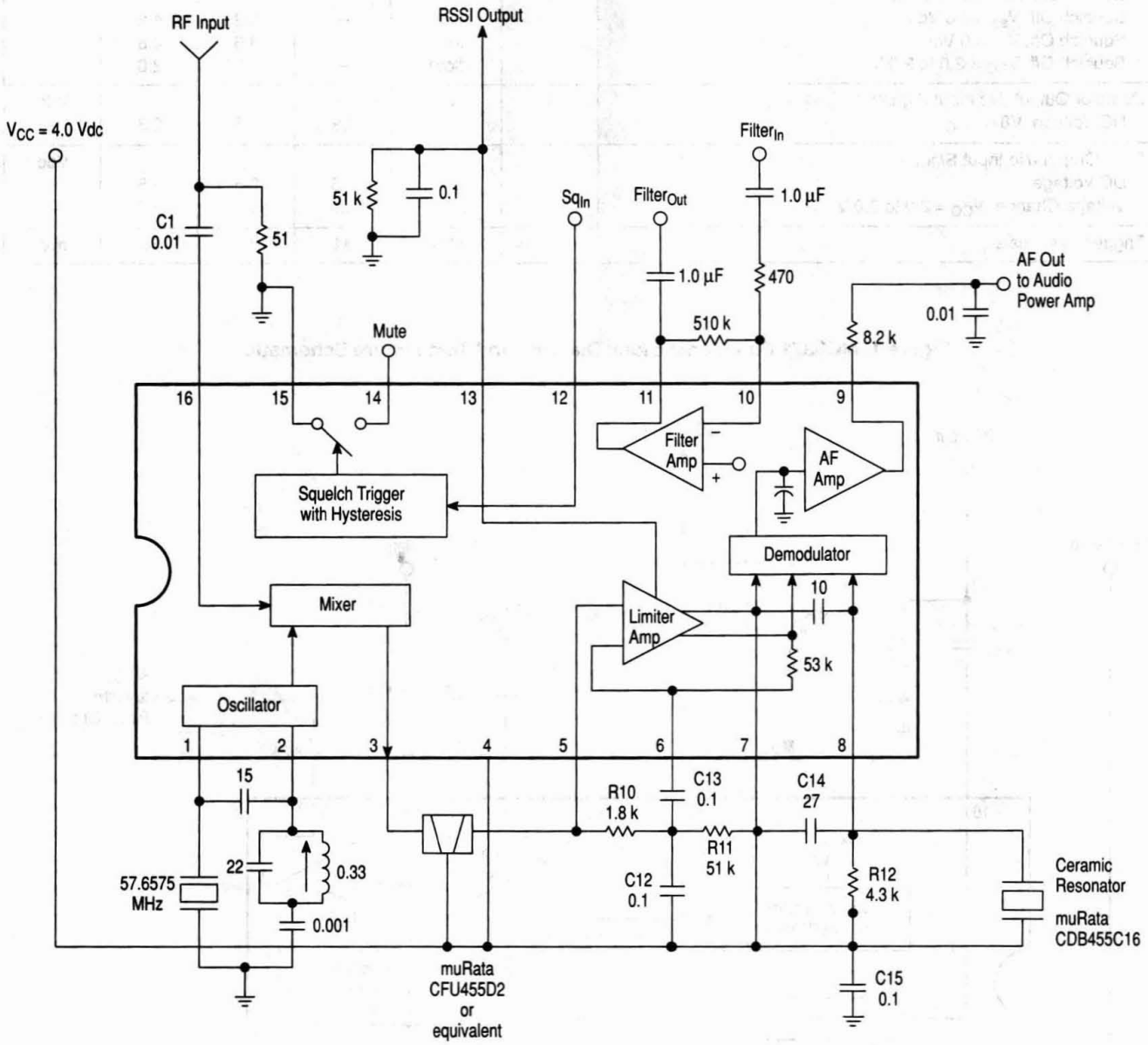


Figure 2. MC3372 Functional Block Diagram and Test Fixture Schematic



TYPICAL CURVES

(Unmatched Input)

Figure 3. Total Harmonic Distortion versus Temperature

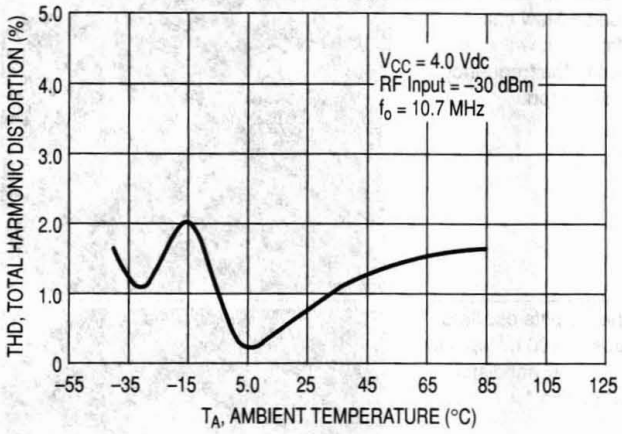


Figure 4. RSSI versus RF Input

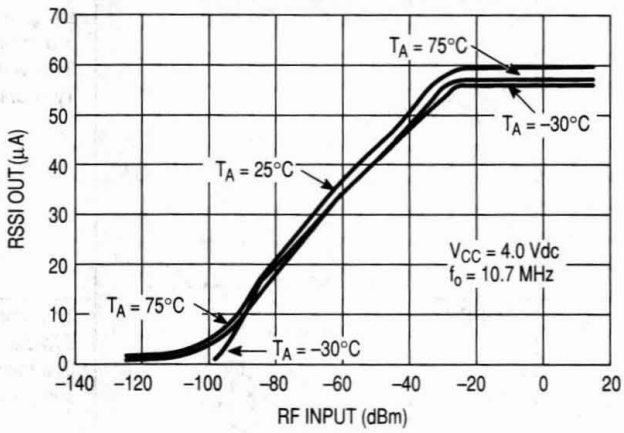


Figure 5. RSSI Output versus Temperature

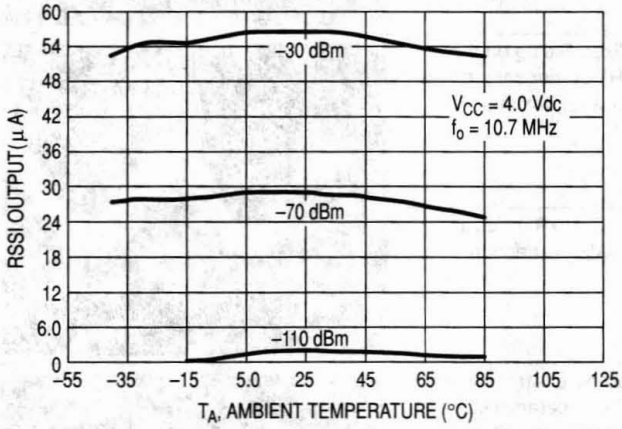


Figure 6. Mixer Output versus RF Input

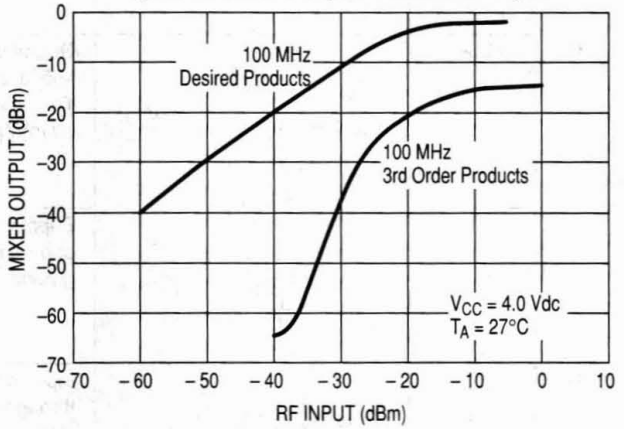


Figure 7. Mixer Gain versus Supply Voltage

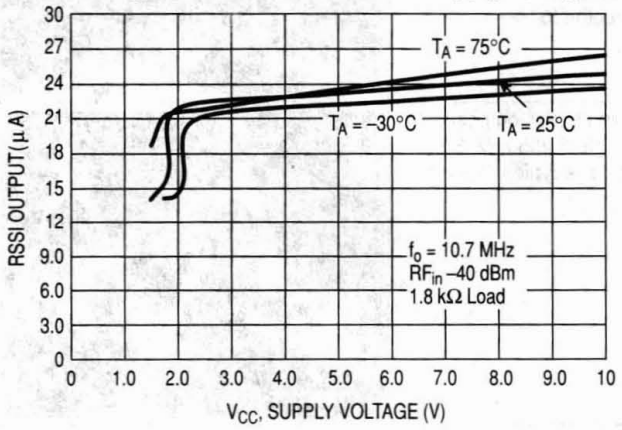
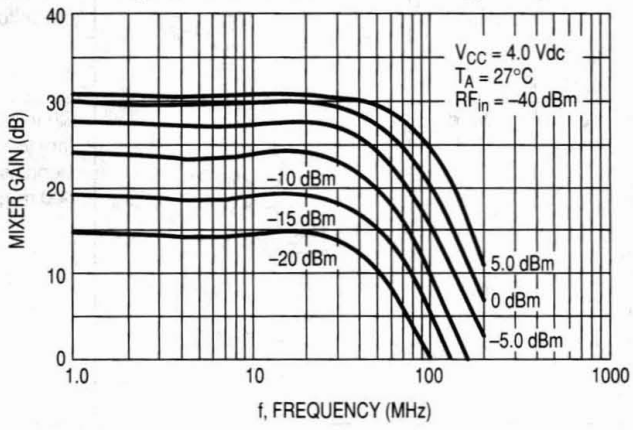
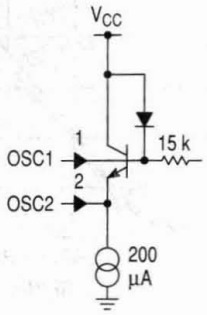
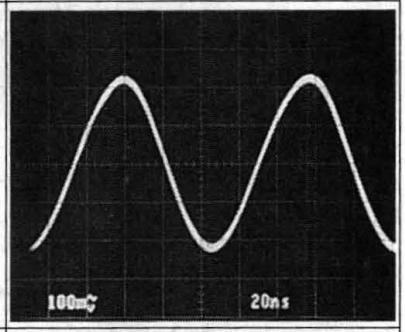
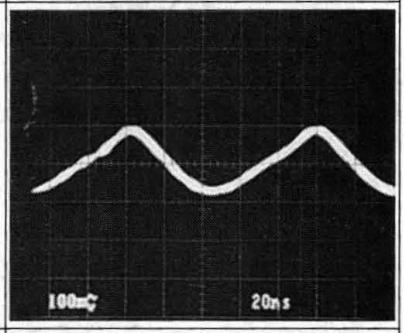
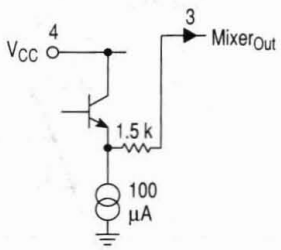
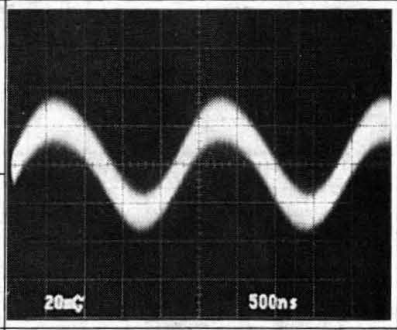
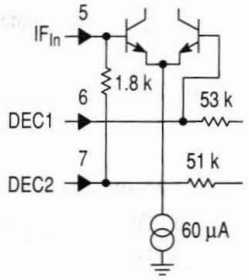
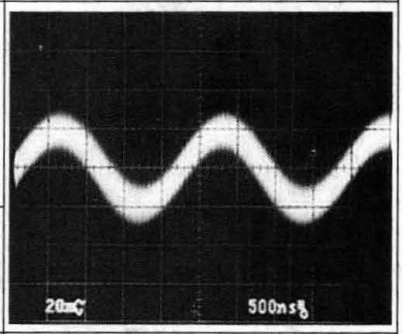
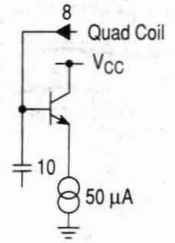
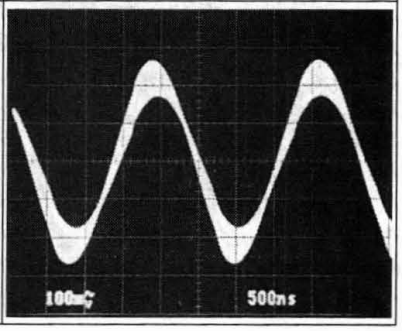


Figure 8. Mixer Gain versus Frequency



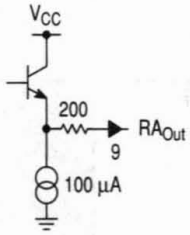
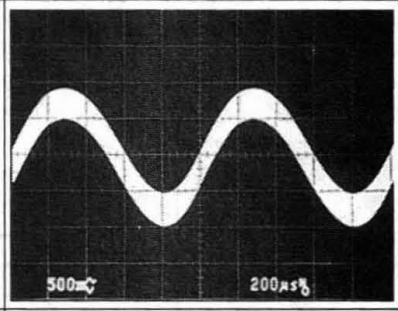
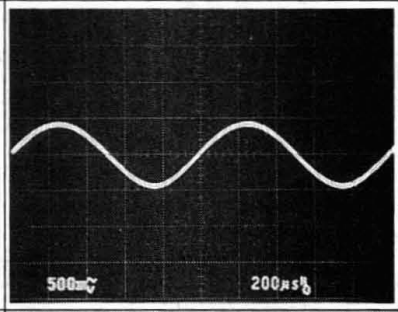
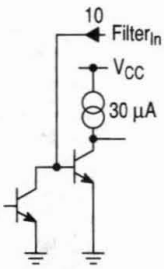
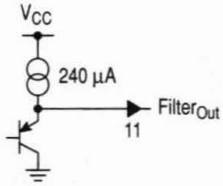
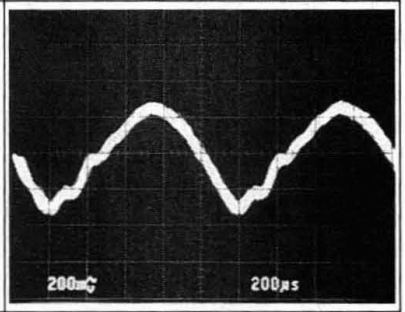
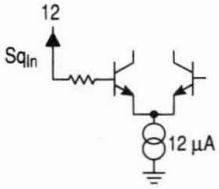
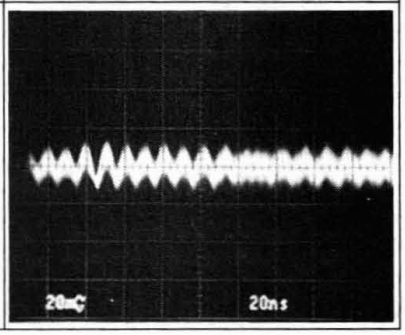
MC3371 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
1	OSC1		The base of the Colpitts oscillator. Use a high impedance and low capacitance probe or a "sniffer" to view the wave–form without altering the frequency. Typical level is 450 mVpp.	
2	OSC2		The emitter of the Colpitts oscillator. Typical signal level is 200 mVpp. Note that the signal is somewhat distorted compared to that on Pin 1.	
3	MX_{Out}		Output of the Mixer. Riding on the 455 kHz is the RF carrier component. The typical level is approximately 60 mVpp.	
4	V_{CC}		Supply Voltage –2.0 to 9.0 Vdc is the operating range. V_{CC} is decoupled to ground.	
5	IF_{In}		Input to the IF amplifier after passing through the 455 kHz ceramic filter. The signal is attenuated by the filter. The typical level is approximately 50 mVpp.	
6 7	DEC1 DEC2		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	
8	Quad Coil		Quadrature Tuning Coil. Composite (not yet demodulated) 455 kHz IF signal is present. The typical level is 500 mVpp.	

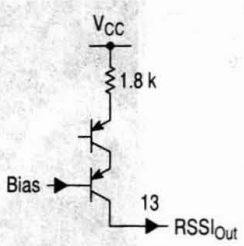
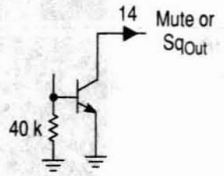
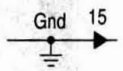
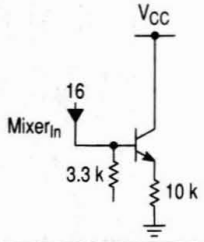
MC3371 PIN FUNCTION DESCRIPTION (continued)

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier component. The typical level is 1.4 Vpp.	
			The filtered recovered audio has the carrier component removed and is typically 800 mVpp.	
10	Fil_{In}		Filter Amplifier Input	
11	Fil_{Out}		Filter Amplifier Output. The typical signal level is 400 mVpp.	
12	Sq_{In}		Squelch Input. See discussion in application text.	

MC3371 PIN FUNCTION DESCRIPTION (continued)

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
13	RSSI		RSSI Output. Referred to as the Received Signal Strength Indicator or RSSI. The chip sources up to 60 µA over the linear 60 dB range. This pin may be used many ways, such as: AGC, meter drive and carrier triggered squelch circuit.	
14	MUTE		Mute Output. See discussion in application text.	
15	Gnd		Ground. The ground area should be continuous and unbroken. In a two–sided layout, the component side has the ground plane. In a one–sided layout, the ground plane fills around the traces on the circuit side of the board and is not interrupted.	
16	MIX_{In}		Mixer Input – Series Input Impedance: @ 10 MHz: 309 – j33 Ω @ 45 MHz: 200 – j13 Ω	

*Other pins are the same as pins in MC3371.

MC3372 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3372 at f_{RF} = 45 MHz (see Figure 13).

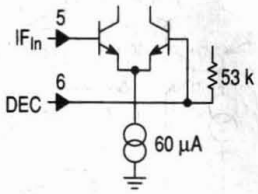
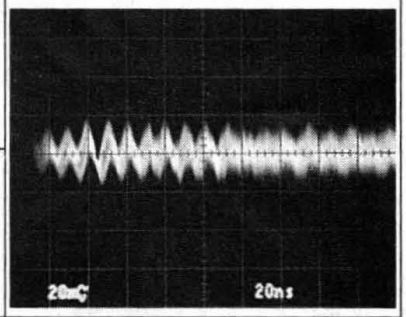
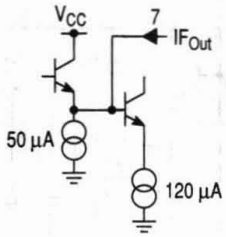
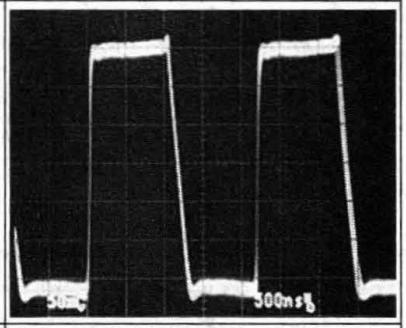
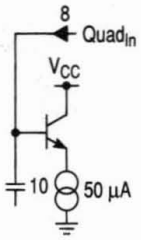
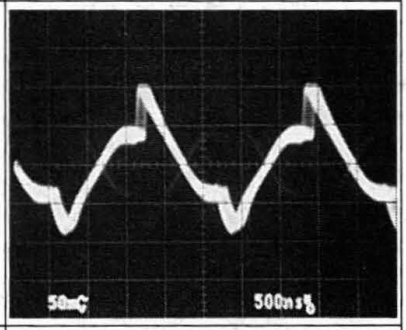
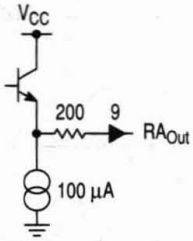
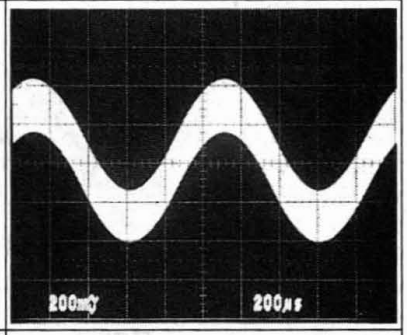
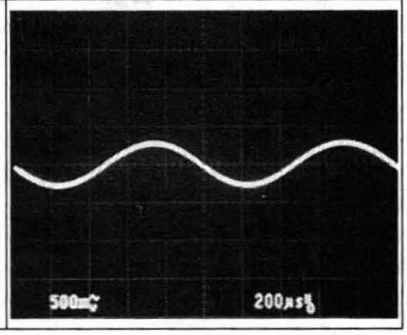
Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
5	IF_{In}		IF Amplifier Input	
6	DEC1		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	
7	IF_{Out}		IF Amplifier Output Signal level is typically 300 mVpp.	
8	$Quad_{In}$		Quadrature Detector Input. Signal level is typically 150 mVpp.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier components. Typical level is 800 mVpp.	
			The filtered recovered audio has the carrier signal removed and is typically 500 mVpp.	

Figure 9. MC3371 Circuit Schematic

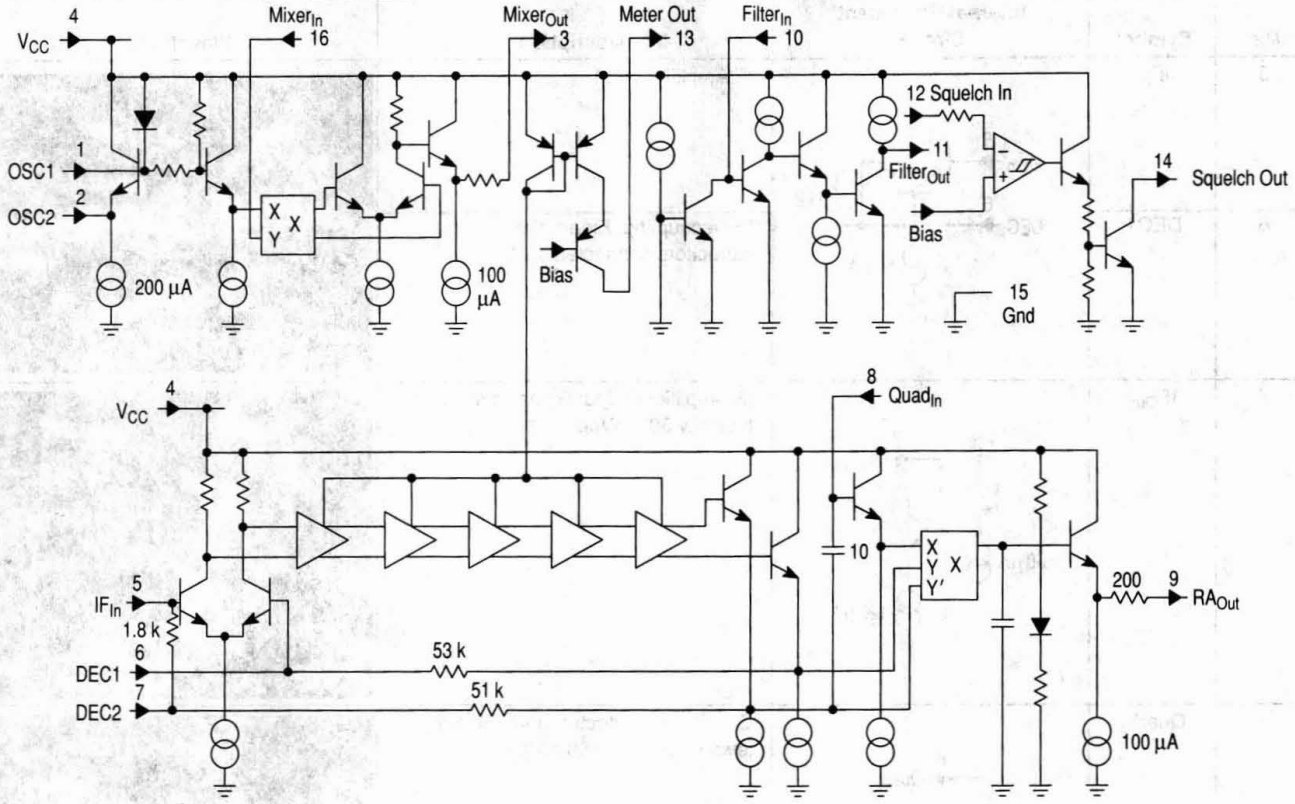
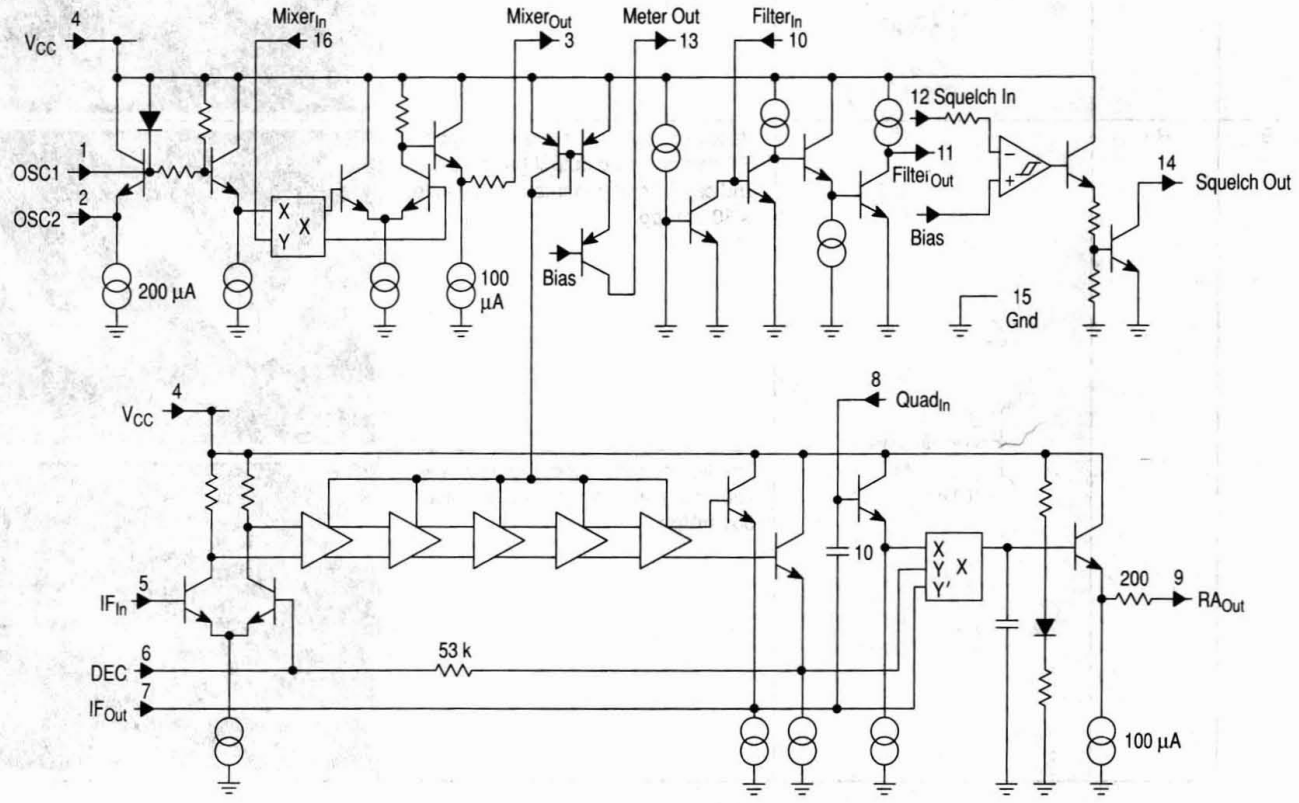


Figure 10. MC3372 Circuit Schematic



CIRCUIT DESCRIPTION

The MC3371 and MC3372 are low power narrowband FM receivers with an operating frequency of up to 60 MHz. Its low voltage design provides low power drain, excellent sensitivity, and good image rejection in narrowband voice and data link applications.

This part combines a mixer, an IF (intermediate frequency) limiter with a logarithmic response signal strength indicator, a quadrature detector, an active filter and a squelch trigger circuit. In a typical application, the mixer amplifier converts an RF input signal to a 455 kHz IF signal. Passing through an external bandpass filter, the IF signal is fed into a limiting amplifier and detection circuit where the audio signal is recovered. A conventional quadrature detector is used.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch switch is used to mute the audio when noise or a tone is present. The input signal level is monitored by a meter drive circuit which detects the amount of IF signal in the limiting amplifier.

APPLICATIONS INFORMATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1 and 2 respectively. This oscillator can be run under crystal control. For fundamental mode crystals use crystal characterized parallel resonant for 32 pF load. For higher frequencies, use 3rd overtone series mode type crystals. The coil (L2) and resistor RD (R13) are needed to ensure proper and stable operation at the LO frequency (see Figure 13, 45 MHz application circuit).

The mixer is doubly balanced to reduce spurious radiation. Conversion gain stated in the AC Electrical Characteristics table is typically 20 dB. This power gain measurement was made under stable conditions using a 50 Ω source at the input and an external load provided by a 455 kHz ceramic filter at the mixer output which is connected to the V_{CC} (Pin 4) and IF input (Pin 5). The filter impedance closely matches the 1.8 kΩ internal load resistance at Pin 3 (mixer output). Since the input impedance at Pin 16 is strongly influenced by a 3.3 kΩ internal biasing resistor and has a low capacitance, the useful gain is actually much higher than shown by the standard power gain measurement. The Smith Chart plot in Figure 17 shows the measured mixer input impedance versus input frequency with the mixer input matched to a 50 Ω source impedance at the given frequencies. In order to assure stable operation under matched conditions, it is necessary to provide a shunt resistor to ground. Figures 11, 12 and 13 show the input networks used to derive the mixer input impedance data.

Following the mixer, a ceramic bandpass filter is recommended for IF filtering (i.e. 455 kHz types having a bandwidth of ±2.0 kHz to ±15 kHz with an input and output impedance from 1.5 kΩ to 2.0 kΩ). The 6 stage limiting IF amplifier has approximately 92 dB of gain. The MC3371 and MC3372 are different in the limiter and quadrature detector circuits. The MC3371 has a 1.8 kΩ and a 51 kΩ resistor providing internal dc biasing and the output of the limiter is internally connected, both directly and through a 10 pF capacitor to the quadrature detector; whereas, in the MC3372 these components are not provided internally. Thus, in the MC3371, no external components are necessary to match the 455 kHz ceramic filter, while in the MC3372, external 1.8 kΩ and 51 kΩ biasing resistors are needed between Pins 5 and 7, respectively (see Figures 12 and 13).

In the MC3371, a parallel LCR quadrature tank circuit is connected externally from Pin 8 to V_{CC} (similar to the MC3361). In the MC3372, a quadrature capacitor is needed externally from Pin 7 to Pin 8 and a parallel LC or a ceramic discriminator with a damping resistor is also needed from Pin 8 to V_{CC} (similar to the MC3357). The above external quadrature circuitry provides 90° phase shift at the IF center frequency and enables recovered audio.

The damping resistor determines the peak separation of the detector and is somewhat critical. As the resistor is decreased, the separation and the bandwidth is increased but the recovered audio is decreased. Receiver sensitivity is dependent on the value of this resistor and the bandwidth of the 455 kHz ceramic filter.

On the chip the composite recovered audio, consisting of carrier component and modulating signal, is passed through a low pass filter amplifier to reduce the carrier component and then is fed to Pin 9 which has an output impedance of 450 Ω. The signal still requires further filtering to eliminate the carrier component, deemphasis, volume control, and further amplification before driving a loudspeaker. The relative level of the composite recovered audio signal at Pin 9 should be considered for proper interaction with an audio post amplifier and a given load element. The MC13060 is recommended as a low power audio amplifier.

The meter output indicates the strength of the IF level and the output current is proportional to the logarithm of the IF input signal amplitude. A maximum source current of 60 μA is available and can be used to drive a meter and to detect a carrier presence. This is referred to as a Received Strength Signal Indicator (RSSI). The output at Pin 13 provides a current source. Thus, a resistor to ground yields a voltage proportional to the input carrier signal level. The value of this resistor is estimated by (V_{CC}(Vdc) – 1.0 V)/60 μA; so for V_{CC} = 4.0 Vdc, the resistor is approximately 50 kΩ and provides a maximum voltage swing of about 3.0 V.

A simple inverting op amp has an output at Pin 11 and the inverting input at Pin 10. The noninverting input is connected to 2.5 V. The op amp may be used as a noise triggered squelch or as an active noise filter. The bandpass filter is designed with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal is checked for a tone signal or for the presence of noise above the normal audio band. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that the audio mute (Pin 14) is open or connected to ground. If Pin 12 is pulled down to 0.9 V or below by the noise or tone detector, Pin 14 is internally shorted to ground. There is about 57 mV of hyteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to the appropriate point in the audio path between Pin 9 and an audio amplifier. The voltage at Pin 14 should not be lower than –0.7 V; this can be assured by connecting Pin 14 to the point that has no dc component.

Another possible application of the squelch switch may be as a carrier level triggered squelch circuit, similar to the MC3362/MC3363 FM receivers. In this case the meter output can be used directly to trigger the squelch switch when the RF input at the input frequency falls below the desired level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 13) and ground (Pin 15).

Figure 11. Typical Application for MC3371 at 10.7 MHz

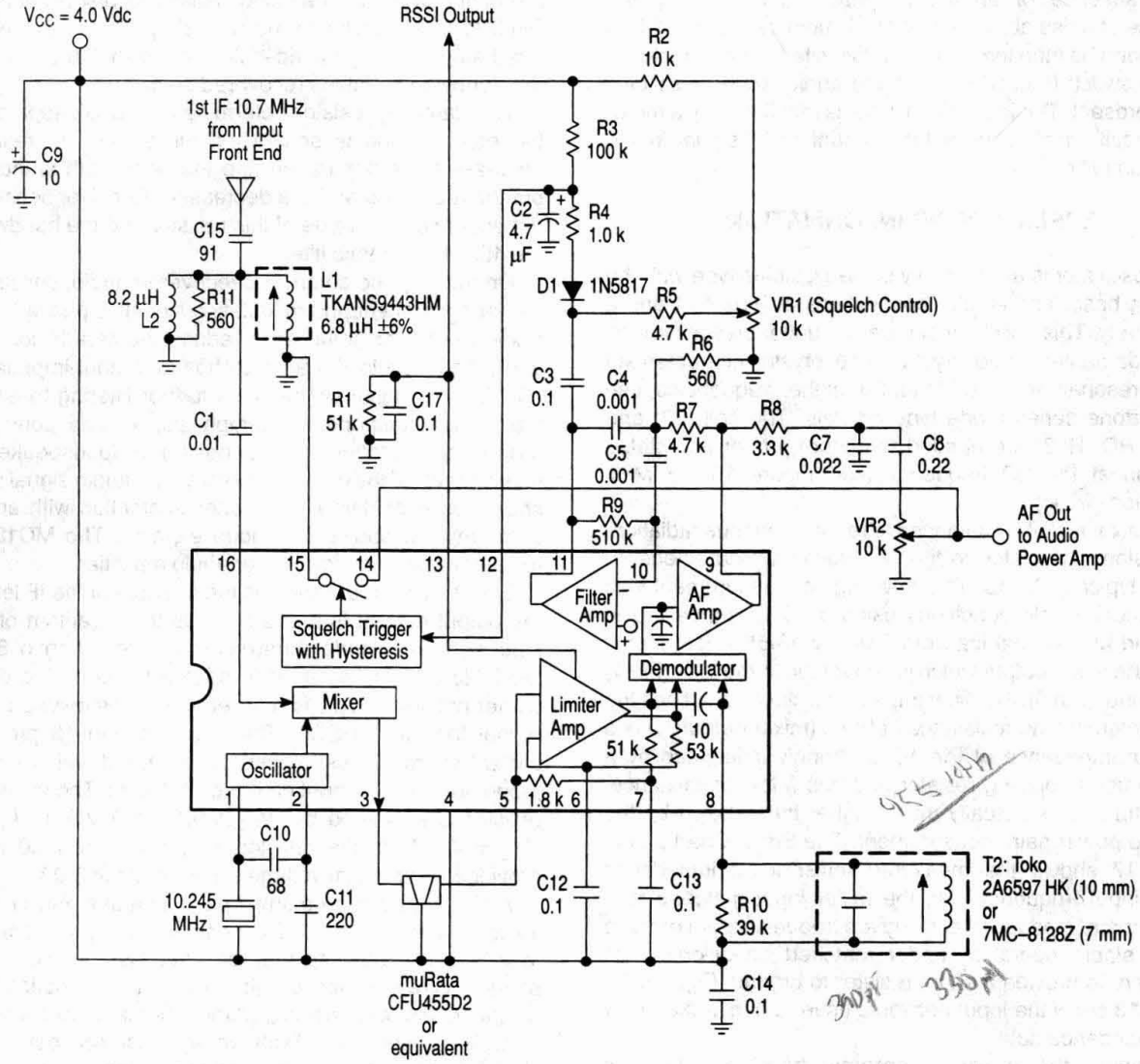


Figure 12. Typical Application for MC3372 at 10.7 MHz

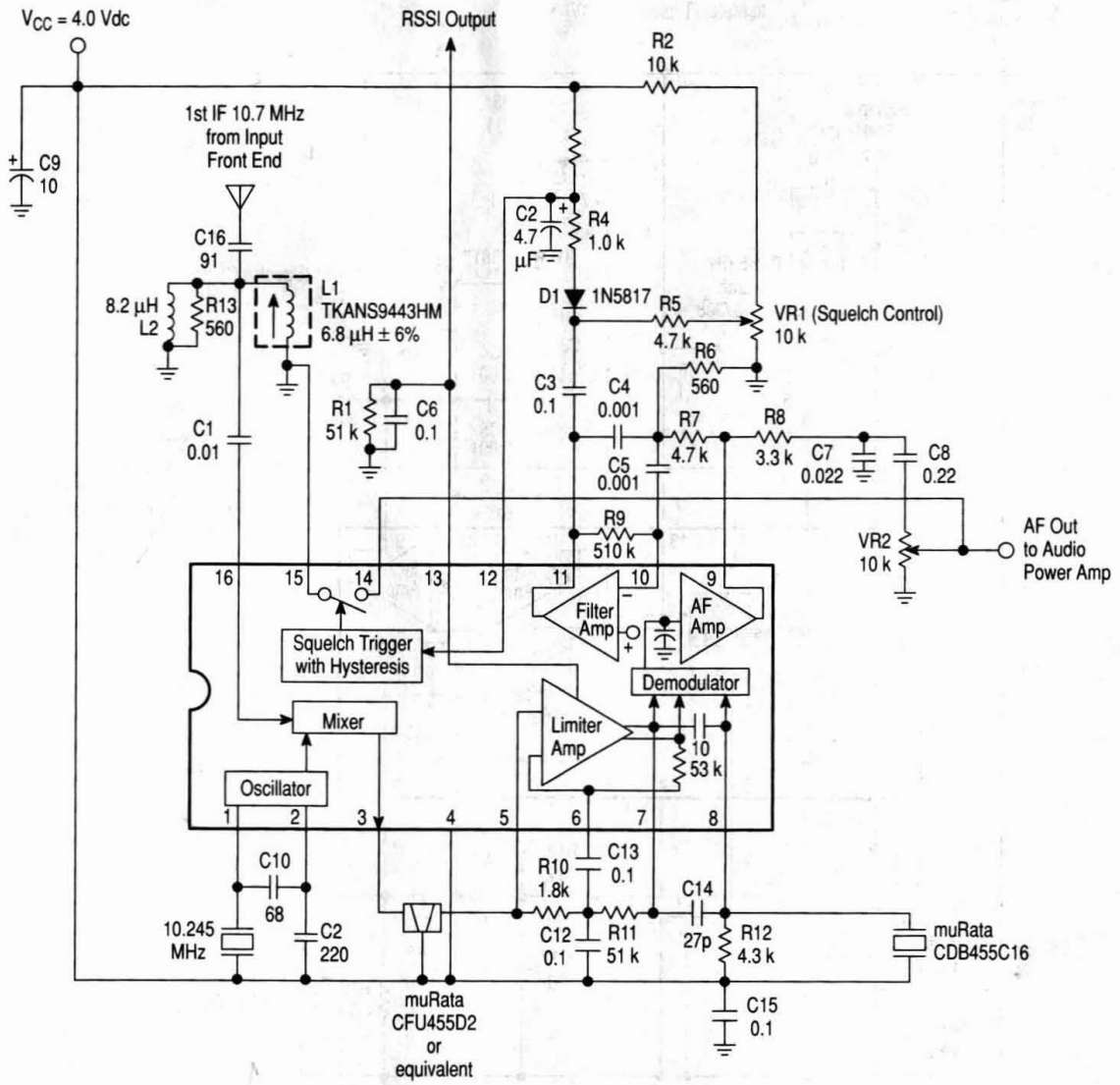


Figure 13. Typical Application for MC3372 at 45 MHz

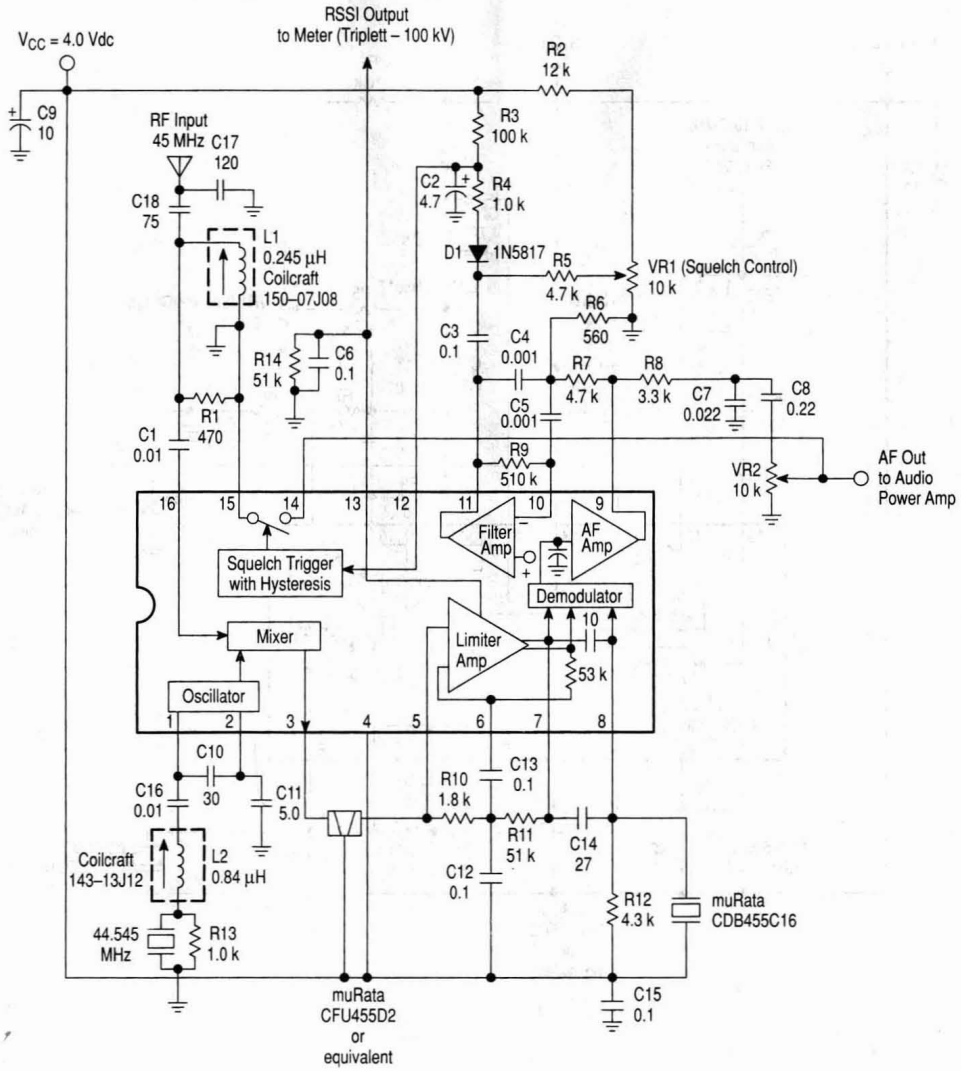


Figure 14. RSSI Output versus RF Input

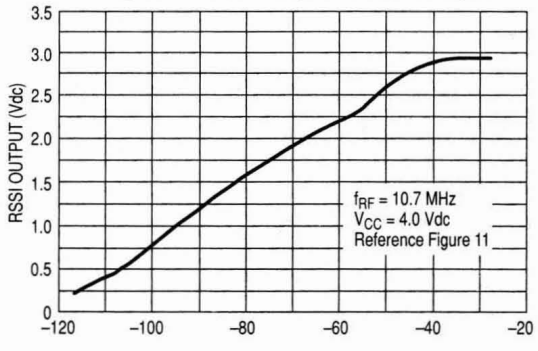


Figure 15. RSSI Output versus RF Input

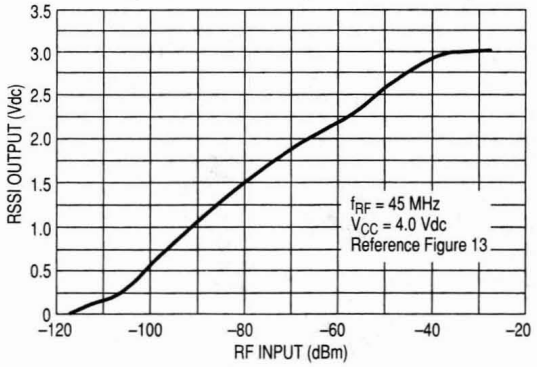
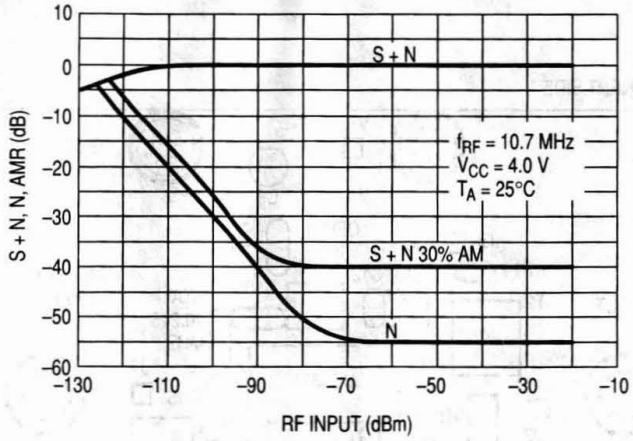


Figure 16. S + N, N, AMR versus Input



* Reference Figures 11, 12 and 13

Figure 17. Mixer Input Impedance versus Frequency

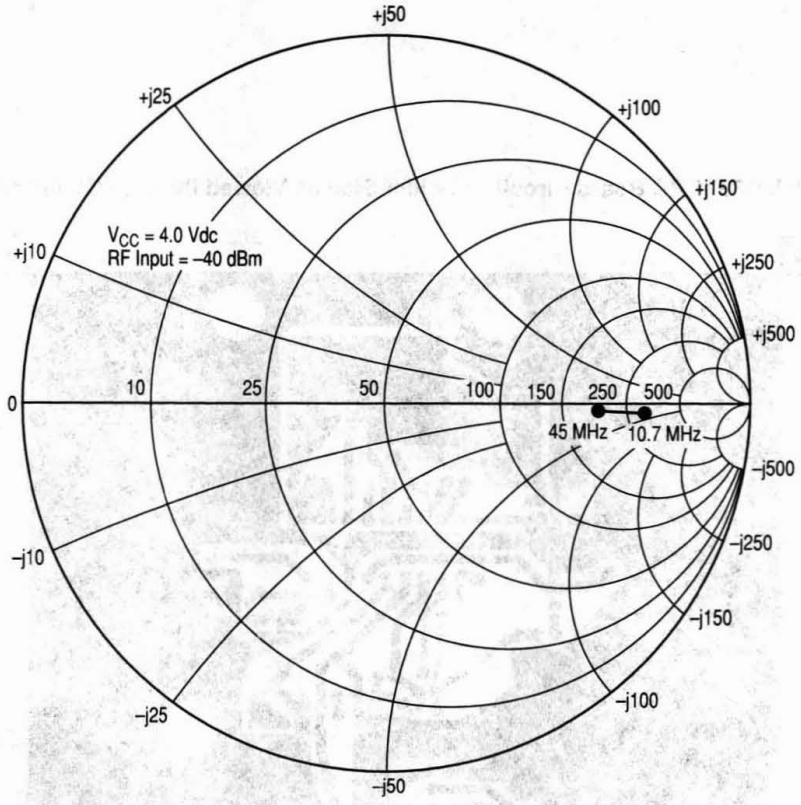


Figure 18. MC3371 PC Board Component View with Matched Input at 10.7 MHz

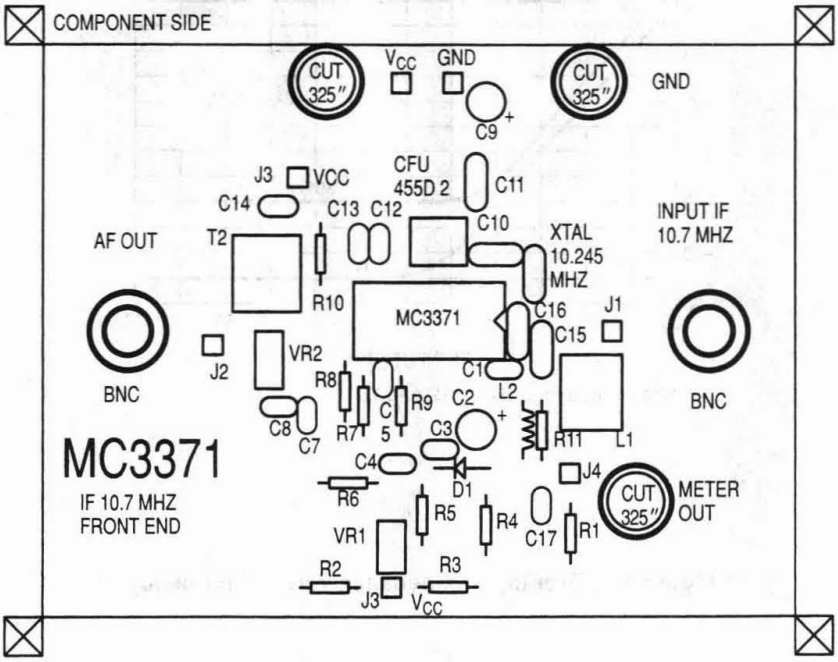
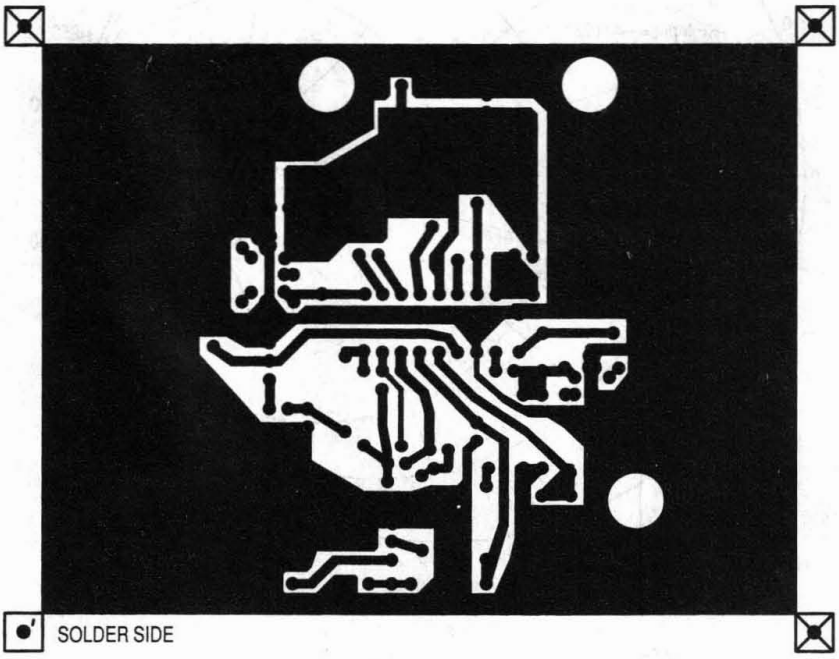


Figure 19. MC3371 PC Board Circuit or Solder Side as Viewed through Component Side



Above PC Board is laid out for the circuit in Figure 11.

Figure 20. MC3372P PC Board Component View with Matched Input at 10.7 MHz

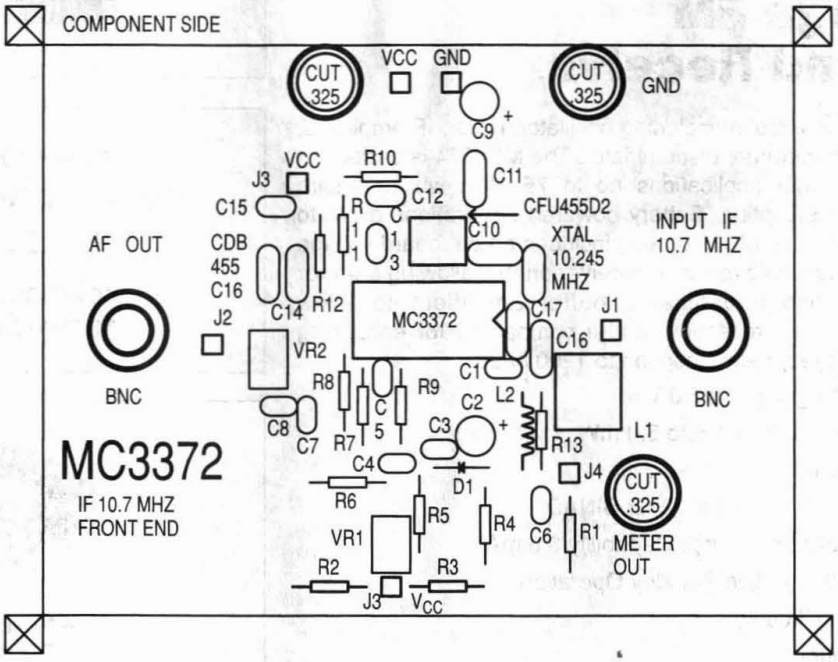
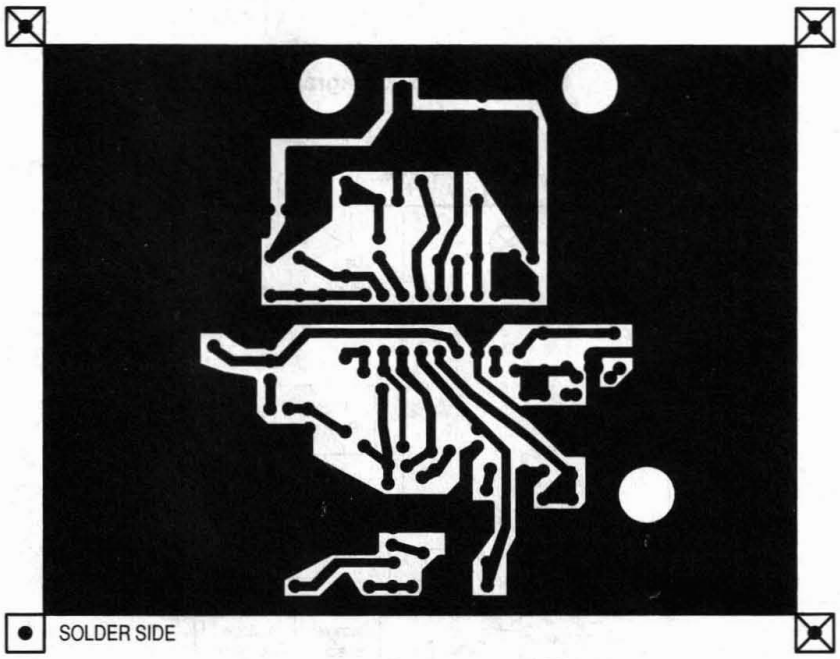


Figure 21. MC3372P PC Board Circuit or Solder Side as Viewed through Component Side



Above PC Board is laid out for the circuit in Figure 12.

MOTOROLA

Low Voltage FM Narrowband Receiver

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3374 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3374 also includes an on–board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down Sleep–Mode™, two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception to 1200 baud.

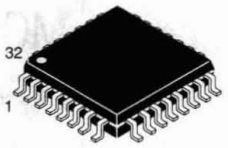
- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: 0.5 μVrms for 12 dB SINAD
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer
- Data Buffer
- FSK Data Shaping Comparator
- Standard 32–Lead QFP Surface Mount Package

Sleep–Mode is a trademark of Motorola, Inc.

MC3374

LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SEMICONDUCTOR TECHNICAL DATA

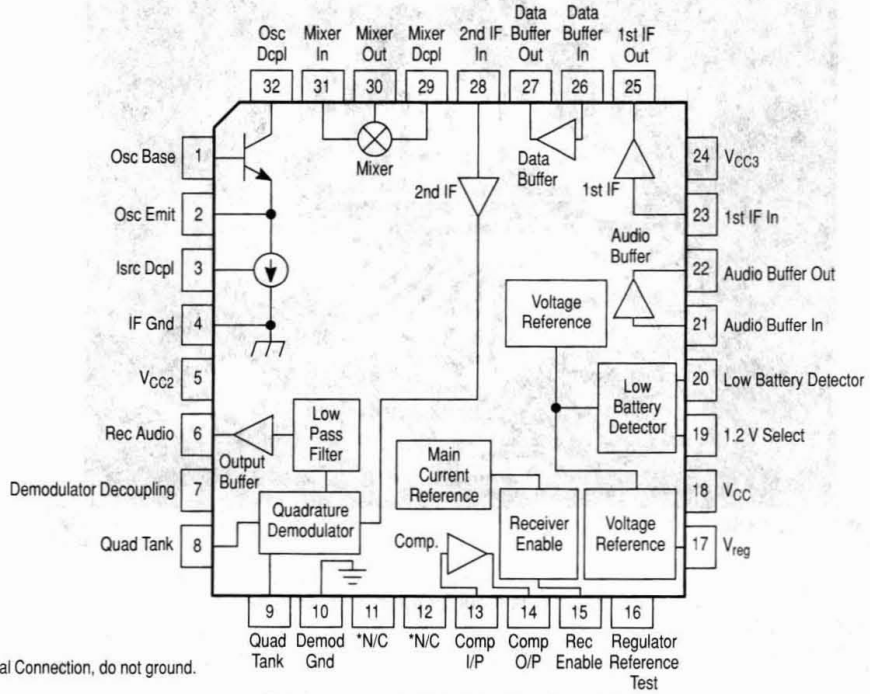


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC3374FTB	T_A = –10° to +70°C	TQFP–32

Simplified Block Diagram



*Internal Connection, do not ground.

This device contains 87 active transistors

MAXIMUM RATINGS (Voltage with respect to Pins 4 and 10; T_A = 25°C.)

Rating	Pin	Value	Unit
Supply Voltage	18	5.0	Vdc
RF Input Signal	31	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	13	1.0	Vrms
Junction Temperature	–	150	°C
Storage Temperature	–	–65 to +150	°C

Device should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Unit
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	15	V_{CC}	Vdc
1.2 V Select Voltage	19	Open or V_{CC}	Vdc
RF Input Signal Level	31	0.001 to 100	mVrms
RF Input Frequency	31	0 to 75	MHz
Intermediate Frequency (IF)	–	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	13	10 to 300	mVrms
Ambient Temperature	–	–10 to 70	°C

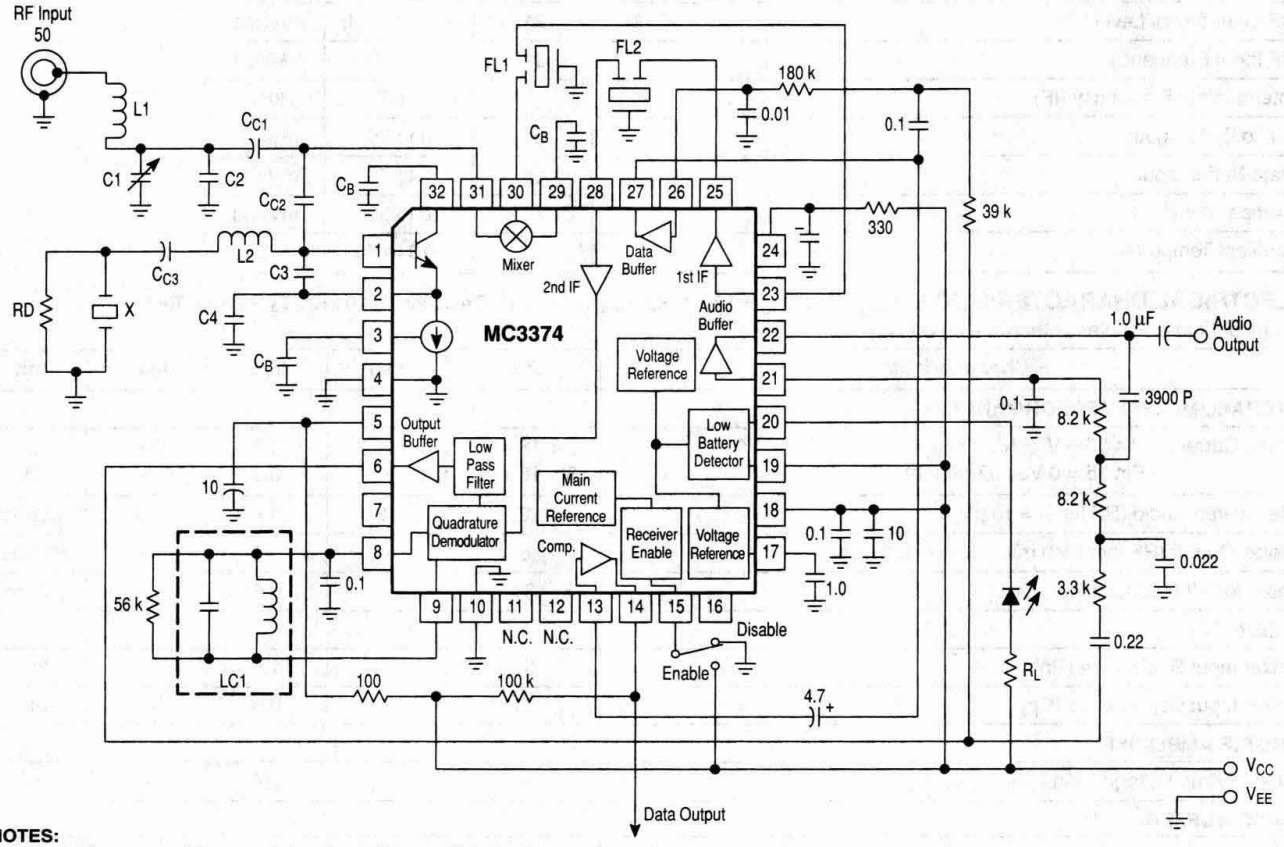
ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
OVERALL MC3374 PERFORMANCE					
Drain Current – Pin 15 = V_{CC} (Enabled) – Pin 15 = 0 Vdc (Disabled)	5 + 18 + 24 5 + 18 + 24	– –	1.6 0.5	3.0 –	mA µA
Recovered Audio (RF Input = 10 µV)	6	13	18	30	mVrms
Noise Output (RF Input = 0 mV, 300 Hz–5.0 kHz)	6	–	1.0	–	mVrms
Input for –3.0 dB Limiting	31	–	0.6	–	µVrms
MIXER					
Mixer Input Resistance (Rp)	31	–	1.5	–	kΩ
Mixer Input Capacitance (Cp)	31	–	9.0	–	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	–	–	27	–	dB
AUDIO BUFFER					
Voltage Gain	–	3.0	4.0	4.7	V/V
Input Resistance	21	–	110	–	kΩ
Maximum Input for Undistorted Output (<5% THD)	21	–	64	–	mVrms
Maximum Output Swing (<5% THD)	22	–	690	–	mV_{pp}
Output Resistance	22	–	780	–	Ω
DATA BUFFER					
Voltage Gain	–	1.4	2.7	4.3	V/V
Input Resistance	26	–	9.8	–	MΩ
Maximum Input for Undistorted Output (<5% THD)	26	–	100	–	mVrms
Maximum Output Swing (<5% THD)	27	–	800	–	mV_{pp}
Output Resistance	27	–	690	–	Ω

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
COMPARATOR					
Minimum Input for Triggering (R_L = 100 kΩ)	13	–	7.0	–	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	13	–	25	–	kHz
Rise Time (10–90%; R_L = 100 kΩ)	14	–	5.0	–	µs
Fall Time (90–10%; R_L = 100 kΩ)	14	–	0.4	–	µs
LOW BATTERY DETECTOR					
Low Battery Trip Point	19	–	1.2	–	Vdc
Low Battery Output – V_{CC} = 0.9 V – V_{CC} = 1.3 V	20 20	– –	0.2 V_{CC}	– –	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 4)	17	0.95	1.07	1.15	Vdc
Source Capability	17	–	–	3.0	mA

Figure 1. MC3374 Pager IF Application Circuit



NOTES:

1. FL1 and FL2 are 455 kHz ceramic bandpass filters, which should have input and output impedances of 1.5 kΩ to 2.0 kΩ. Suggested part numbers are MuRata CFU455X or CFW455x – the 'X' suffix denotes bandwidth.
2. LC1 is a 455 kHz LC resonator. Recommended part numbers are Toko America RMC2A6597HM or 5SVLC–0637BGT (smaller). The evaluation board layout shown provides for use of either resonator. Ceramic discriminator elements cannot be used with the MC3374 due to their low input impedance. The damping resistor value can be raised to increase the recovered audio or lowered to increase the quadrature detector's bandwidth and linearity – practical limits are approximately 27 kΩ to 75 kΩ. Typically the quadrature detector's bandwidth should match the low IF filter's bandwidth.
3. The data buffer is set up as a low–pass filter with a corner frequency of approximately 200 Hz. The audio buffer is a bandpass filter with corner frequencies of 300 Hz and 3.0 kHz. The audio amplifier provides bass suppression.
4. C_{C1} and C_{C3} are RF coupling capacitors and should have ≤ 20 Ω impedance at the desired input and oscillator frequencies.
5. C_{C2} provides "light coupling" of the oscillator signal into the mixer, and should have a 3.0 kΩ to 5.0 kΩ impedance at the desired local oscillator frequency.
6. Capacitors labelled C_B are bypass capacitors and should have 20 Ω impedance at the desired RF and local oscillator frequencies.
7. The network of L1, C1 and C2 provides impedance matching of the mixer input (nominally 3.0 kΩ shunted by 9.0 pF) to 50 Ω at the desired RF/IF input frequency. This will allow for bench testing of the receiver from typical RF signal generators or radio service monitors, but additional or different matching will be required to maximize receiver sensitivity when used in conjunction with an antenna, RF preamplifier or mixer.

In. Freq.	L1	L2	C1	C2	C3	C4	C_{C1}/C_{C3}	C_{C2}	C_B	RD
10.7 MHz	6.8 µH	Short	2–82 pF	10 pF	120 pF	50 pF	1.0 nF	5.0 pF	0.1 µF	Open
45 MHz	0.68 µH	1.2 µH	5–25 pF	Open	30 pF	5.0 pF	1.0 nF	1.0 pF	1.0 nF	1.0 k
72 MHz	0.22 µH	0.22 µH	5–25 pF	Open	18 pF	3.0 pF	470 pF	1.0 pF	470 pF	1.0 k

Figure 2. Recovered Audio versus Supply

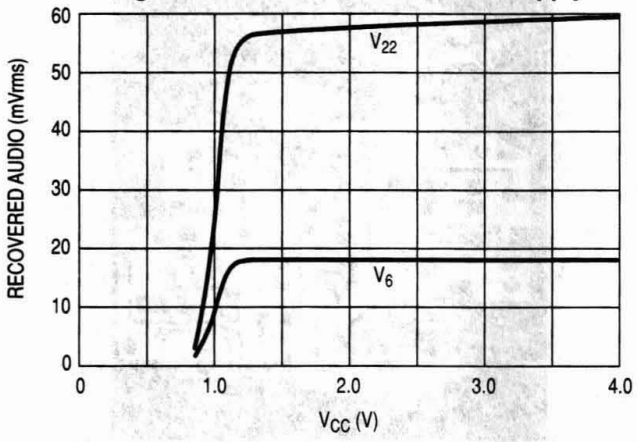


Figure 3. S+N, N versus Input

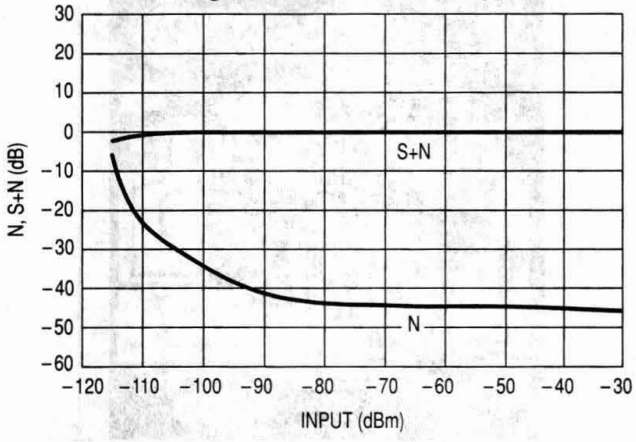


Figure 4. V_{REG} versus Supply

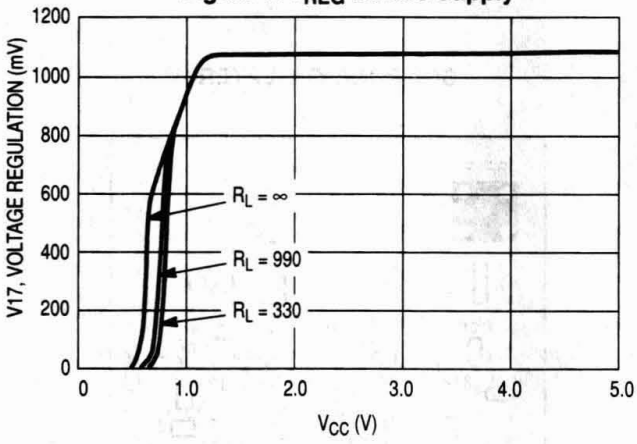


Figure 5. Regulated Output and Recovered Audio versus Temperature

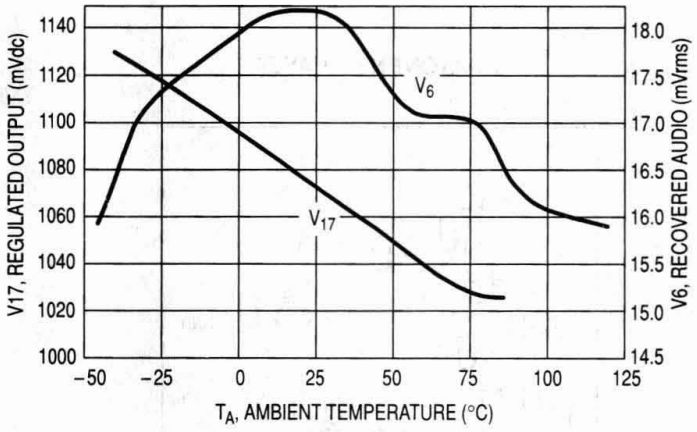


Figure 6. Buffer Amplifier Gains versus Temperature

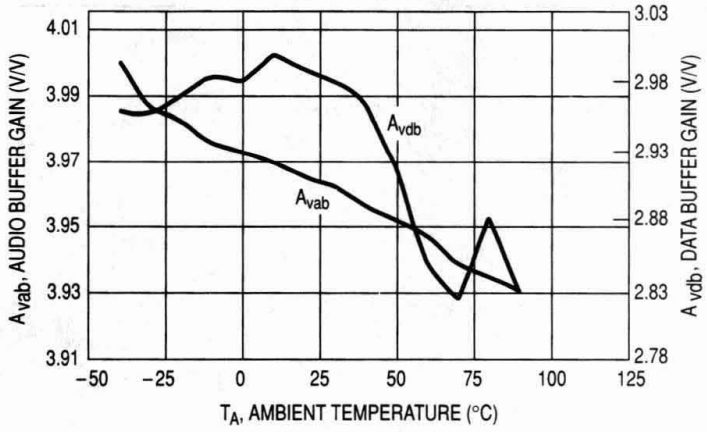
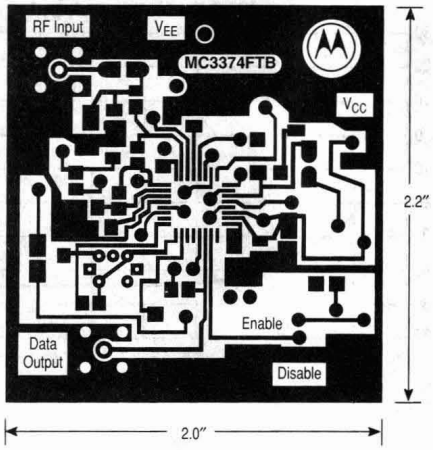
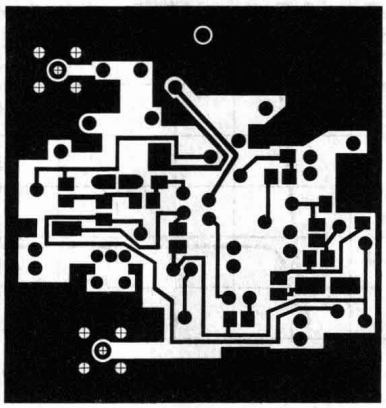


Figure 7. MC3374 Pager Receiver PCB Artwork

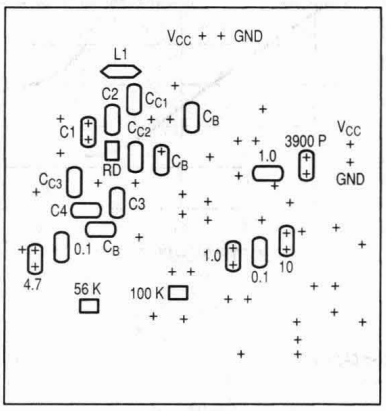
COPPER 1 LAYER
(Actual View of Surface Mount Side)



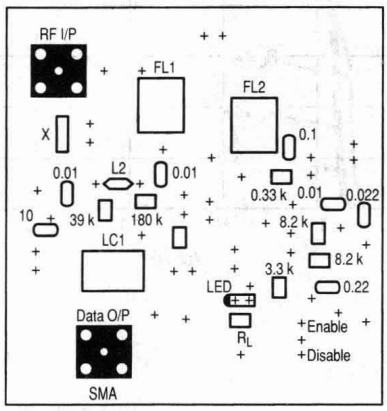
COPPER 2 LAYER
(Caution: Reversed View of Through–Hole Side)



COMPONENT 1 LAYER



COMPONENT 2 LAYER



NOTE: + = Through Hole

CIRCUIT DESCRIPTION

The MC3374 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts this frequency to 455 kHz. The signal is then filtered by a 455 kHz ceramic filter and applied to the first intermediate frequency (IF) amplifier input, before passing through a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Modulation is recovered by a conventional quadrature detector. The typical modulation bandwidth available is 3.0 to 5.0 kHz.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3374 is an FM utility receiver to be used for voice and/or narrowband data reception. It is especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

The MC3374 can be used as a high performance FM IF for the use in low power dual conversion receivers. Because of the MC3374's extremely good sensitivity (0.6 μV for 20 dB (S+N/N, see Figure 3)), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference. An RF preamplifier will likely be needed to overcome preselector losses.

The oscillator is a Colpitts type which must be run under crystal control. For fundamental mode crystals choose resonators, parallel resonant, for a 32 pF load. For higher frequencies, use a 3rd overtone series mode type. The coil L2 and RD resistor are needed to ensure proper operation.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 1. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally. A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 8) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor (see Figure 1), determines the peak separation of the detector (and thus its bandwidth). Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a noninverting amplifier with a nominal voltage gain of 2.7 V/V. This buffer needs its dc bias (approximately 250 mV) provided externally or else debiasing will occur. A 2nd order Sallen–Key low pass filter, as shown in Figure 1, connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post detection filtering. The buffer can also be used as an active filter.

The audio buffer is a noninverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self–biasing so its input should be ac coupled. The two buffers, when applied as active filters, can be used together to allow simultaneous audio and very low speed data reception. Another possible configuration is to receive audio only and include a noise–triggered squelch.

The comparator is a noninverting type with an open collector output. Typically, the pull–up resistor used between Pin 14 and V_{CC} is 100 kΩ. With R_L = 100 kΩ the comparator is capable of operation up to 25 kHz. The circuit is self–biasing, so its input should be ac coupled.

The regulator is a 1.07 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μF capacitor to maintain stability of the MC3374.

All three V_{CC}s on the MC3374 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 1. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

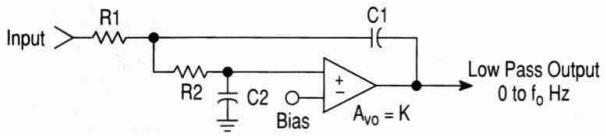
The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3374 supply voltage drops below 1.2 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3374 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 15 is a receiver enable which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μA.

APPENDIX

Design of 2nd Order Sallen–Key Low Pass Filters



The audio and data buffers can easily be configured as active low pass filters using the circuit configuration shown above. The circuit has a center frequency (f_o) and quality factor (Q) given by the following:

$$f_o = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2C2}{R1C1}} + \sqrt{\frac{R1C2}{R2C1}} + (1-K)\sqrt{\frac{R1C1}{R2C2}}}$$

If possible, let R1 = R2 or C1 = C2 to simplify the above equations. Be sure to avoid a negative Q value to prevent instability. Setting $Q = 1/\sqrt{2} = 0.707$ yields a maximally flat filter response.

Data Buffer Design

The data buffer is designed as follows:

f_o = 200 Hz
C1 = C2 = 0.01 µF
Q = 0.707 (target)

K = 2.7 (data buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi C1\sqrt{R1R2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2}{R1}} + (2-K)\sqrt{\frac{R1}{R2}}}$$

Iteration yields R2 = 4.2 (R1) to make Q = 0.707.
Substitution into the equation for f_o yields:
R1 = 38 kΩ (use 39 kΩ)
R2 = 4.2(R1) = 180 kΩ
C1 = C2 = 0.01 µF

Audio Buffer Design

The audio buffer is designed as follows:

f_o = 3000 Hz
R1 = R2 = 8.2 kΩ
Q = 0.707 (target)

K = 3.9 (audio buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi R1\sqrt{C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{C2}{C1}} + (1-K)\sqrt{\frac{C1}{C2}}}$$

Iteration yields C2 = 2.65 (C1) to make Q = 0.707.
Substitution into the equation for f_o yields:
C1 = 3900 pF
C2 = 2.65(C1) = 0.01 µF
R1 = R2 = 8.2 kΩ

MOTOROLA

MC3418

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

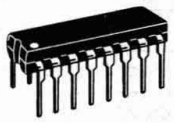
LASER–TRIMMED IC

SEMICONDUCTOR TECHNICAL DATA

Continuously Variable Slope Delta Modulator/Demodulator

Providing a simplified approach to digital speech encoding/decoding, the MC3418 CVSD is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

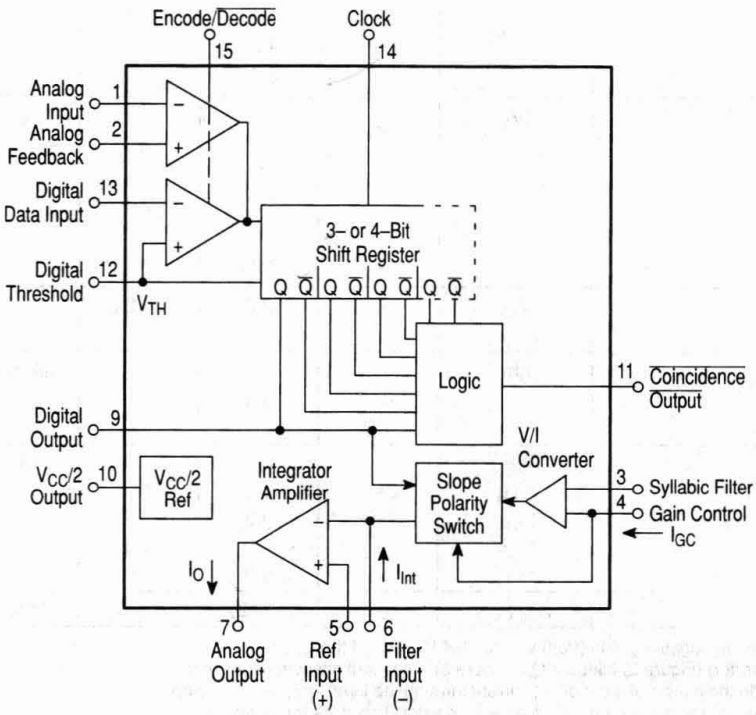
- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ Reference Provided On–Chip)
- MC3418 has a 4–Bit Algorithm (Commercial Telephone)



P SUFFIX
PLASTIC PACKAGE
CASE 648

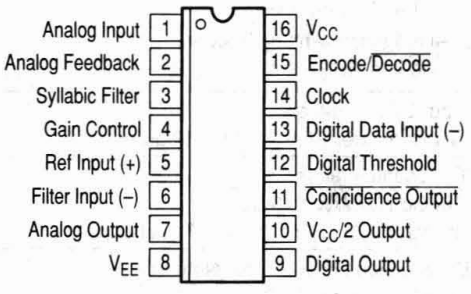
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

Representative Block Diagram



This device contains 144 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3418DW	T_A = 0° to +70°C	SO–16L
MC3418P		Plastic DIP

MAXIMUM RATINGS (All voltages referenced to V_{EE}, T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	–0.4 to V_{CC}	Vdc
Logic Input Voltage Clock, Digital Data, Encode/$\overline{\text{Decode}}$	V_{Logic}	 –0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	–0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	–0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	–0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(ref)}$	V_{CC}/2 – 1.0 to V_{CC}	Vdc
V_{CC}/2 Output Current	I_{ref}	–25	mA

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0 to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) @ Idle Channel	I_{CC}				mA
V_{CC} = 5.0 V		–	3.7	5.5	
V_{CC} = 15 V		–	6.0	11	
Gain Control Current Range (Figure 2)	I_{GCR}	0.002	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) 4.75 V ≤ V_{CC} ≤ 16.5 V	V_I	1.3	–	V_{CC} – 1.3	Vdc
Analog Output Range (Pin 7) 4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ±5.0 mA	V_O	1.3	–	V_{CC} – 1.3	Vdc
Input Bias Currents (Figure 3) Comparator in Active Region	I_{IB}				µA
Analog Input (I1)		–	0.25	1.0	
Analog Feedback (I2)		–	0.25	1.0	
Syllabic Filter Input (I3)		–	0.06	0.3	
Reference Input (I5)		–	–0.06	–0.3	
Input Offset Current Comparator in Active Region Analog Input/Analog Feedback |I1 – I2| (Figure 3) Analog Input/Analog Feedback |I5 – I6| (Figure 4)	I_{IO}	 – –	 0.05 0.01	 0.4 0.1	µA
Input Offset Voltage V/I Converter (Pins 3 and 4) (Figure 5)	V_{IO}	–	2.0	6.0	mV
Transconductance V/I Converter, 0 to 3.0 mA Integrator Amplifier, 0 to ±5.0 mA Load	gm	 0.1 1.0	 0.3 10	 – –	mA/mV
Propagation Delay Times (Note 1) Clock Trigger to Digital Output C_L = 25 pF to Gnd Clock Trigger to Coincidence Output C_L = 25 pF to Gnd, R_L = 4.0 kΩ to V_{CC}	 t_{PLH} t_{PHL} t_{PLH} t_{PHL}	 – – – –	 1.0 0.8 1.0 0.8	 2.5 2.5 3.0 2.0	µs
Coincidence Output Voltage – Low Logic Stage	$V_{OL(Con)}$	–	0.12	0.25	Vdc

NOTES: 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.
2. Dynamic total loop offset (ΣVoffset) equals VIO (comparator) (Figure 3) minus VIOX (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 32 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one–half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to ensure good idle channel performance.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0 to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
$I_{OL(Con)}$ = 3.0 mA					
Coincidence Output Leakage Current – High Logic State V_{OH} = 15 V, 0°C ≤ T_A ≤ 70°C	$I_{OH(Con)}$	–	0.01	0.5	µA
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	1.2	–	V_{CC} – 2.0	Vdc
Digital Threshold Input Current 1.2 V ≤ V_{th} ≤ V_{CC} – 2.0 V V_{IL} Applied to Pins 13, 14 and 15 V_{IH} Applied to Pins 13, 14 and 15	$I_{I(th)}$	 – –	 – –10	 5.0 –50	µA
Maximum Integrator Amplifier Output Current	I_O	±5.0	–	–	mA
V_{CC}/2 Generator Maximum Output Current (Source Only)	I_{ref}	10	–	–	mA
V_{CC}/2 Generator Output Impedance (0 to –10 mA)	z_{ref}	–	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance (4.75 V ≤ V_{CC} ≤ 16.5 V)	εr	–	–	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15) Low Logic State High Logic State	 V_{IL} V_{IH}	 V_{EE} V_{th} + 0.4	 – –	 V_{th} – 0.4 18	Vdc
Dynamic Total Loop Offset Voltage (Note 2) (Figures 3, 4 and 5) I_{GC} = 12 µA, V_{CC} = 12 V T_A = 25°C 0°C ≤ T_A ≤ + 70°C I_{GC} = 12 µA, V_{CC} = 5.0 V T_A = 25°C 0°C ≤ T_A ≤ + 70°C	ΣV_{offset}	 – – – –	 ±0.5 ±0.75 ±1.0 ±1.3	 ±3.0 ±3.8 ±3.5 ±4.3	mV
Digital Output Voltage I_{OL} = 3.6 mA I_{OH} = –0.35 mA	 V_{OL} V_{OH}	 – V_{CC} – 1.0	 0.1 V_{CC} – 0.2	 0.4 –	Vdc
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	3.2	–	V_{CC}	Vdc
Integrating Current (Figure 2) I_{GC} = 12 µA I_{GC} = 1.5 mA I_{GC} = 3.0 mA	$\lvert I_{Int} \rvert$	 8.0 1.42 2.75	 10 1.5 3.0	 12 1.58 3.25	 µA mA mA
Dynamic Integrating Current Match (Figure 6) I_{GC} = 1.5 mA	$V_{O(Ave)}$	–	±100	±280	mV
Input Current – High Logic State (V_{IH} = 18 V) Digital Data Input Clock Input Encode/Decode Input	I_{IH}	 – – –	 – – –	 5.0 5.0 5.0	µA
Input Current – Low Logic State (V_{IL} = 0 V) Digital Data Input Clock Input Encode/Decode Input Clock Input, V_{IL} = 0.4 V	I_{IL}	 –10 –360 –36 –72	 – – – –	 – – – –	µA

NOTES: 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.
2. Dynamic total loop offset (ΣVoffset) equals VIO (comparator) (Figure 3) minus VIOX (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 32 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one–half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to ensure good idle channel performance.

DEFINITION AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the noninverting input to the analog signal comparator. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7

or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to $V_{CC}/2$ at Pin 10 or ground.

The analog input comparator has bias currents of 1.0 μA max, thus the driving impedances at Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6.0 to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V – I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_x resistance. Figure 7 shows the relationship between I_{GC} (x–axis) and the integrating current, I_{Int} (y–axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_x resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should always be between 8.0 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600 Ω load referenced to $V_{CC}/2$ to +6.0 dBm and can otherwise be treated as an op amp output. Pins 5, 6 and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and noninverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid–supply reference is provided for use in single supply applications. The internal regulator is a current source and must be loaded with a resistor to ensure its sinking capability. If a +6.0 dBmo signal is expected across a 600 Ω input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is possible only if Pin 10 sources 3.66 mA into a resistor normally and will source the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. The MC3418 contains a 4–bit register. Pin 11 is an open collector NPN device and requires a pull–up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is R_SC_S while the decay constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3.0 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4.0 kΩ to 12 V and C_L = 25 pF to ground.

Pin 12 — Digital Threshold

This input sets the switching threshold for Pins 13, 14 and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 — Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip–flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 — Clock Input

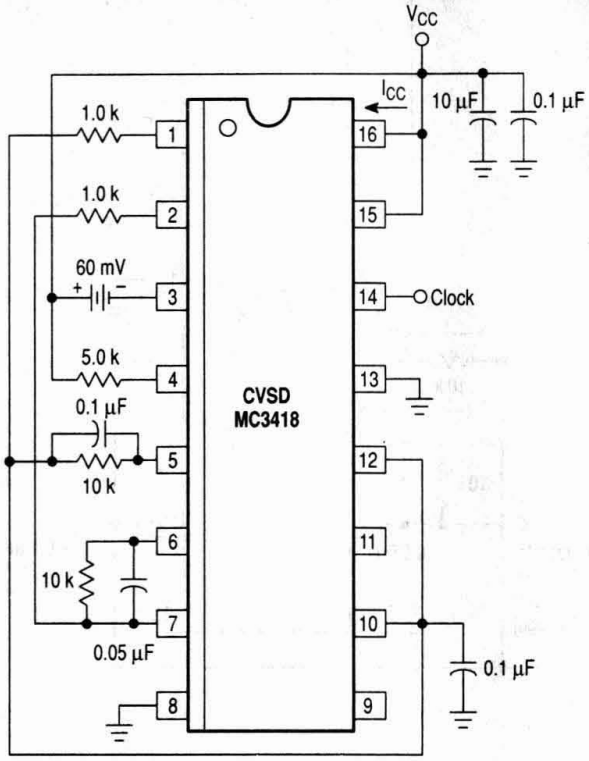
The clock input determines the data rate of the codec circuit. A 32 k bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum high time for the clock input is 300 ns and minimum low time is 900 ns.

Pin 15 — $\overline{\text{Encode/Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC

as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non–voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

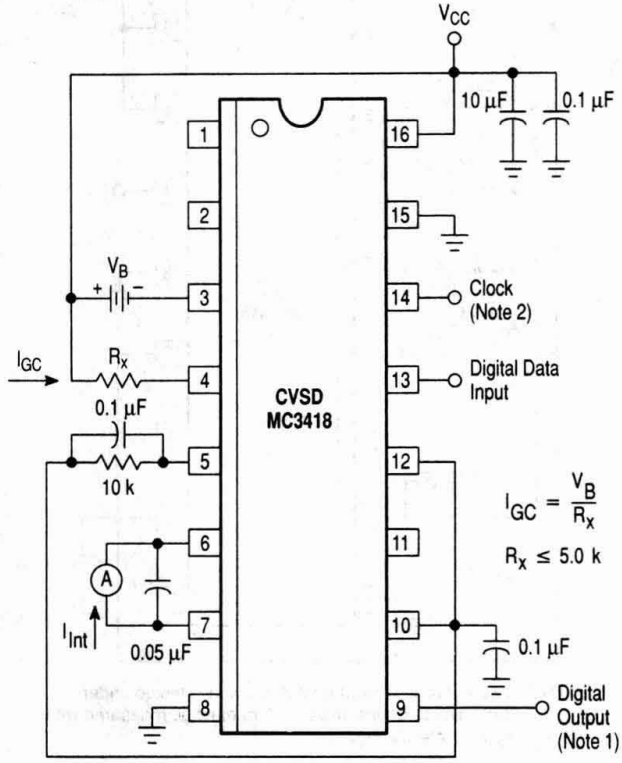
Figure 1. Power Supply Current



Pin 16 — V_{CC}

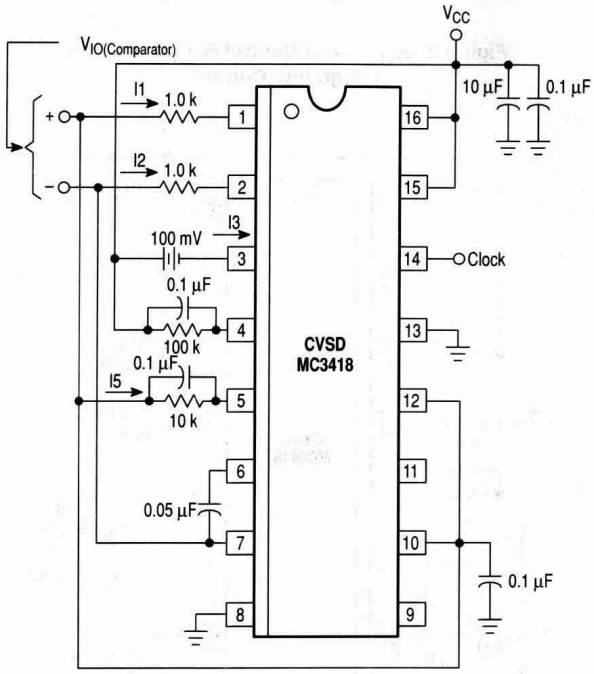
The power supply range is from 4.75 to 16.5 V between Pin V_{CC} and V_{EE}.

Figure 2. I_{GCR} – Gain Control Range and I_{Int} – Integrating Current



NOTES: 1. Digital Output = $\overline{\text{Digital Data Input}}$
2. For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

Figure 3. Input Bias Currents, Analog Comparator Offset Voltage and Current



NOTE: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

Figure 4. Integrator Amplifier Offset Voltage and Current

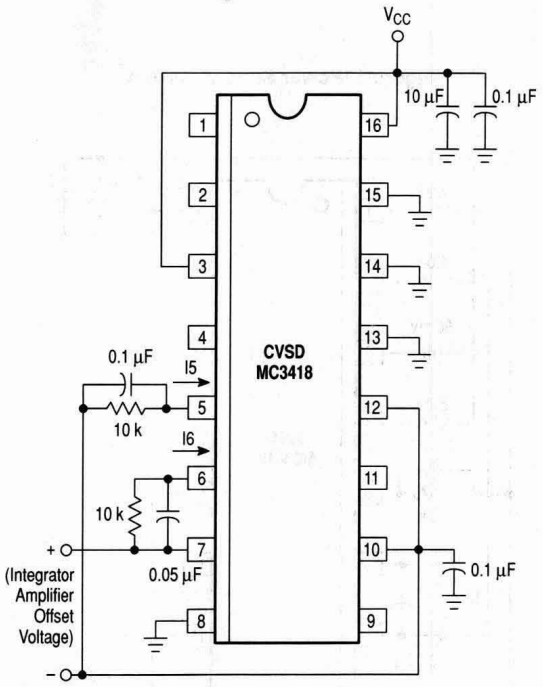
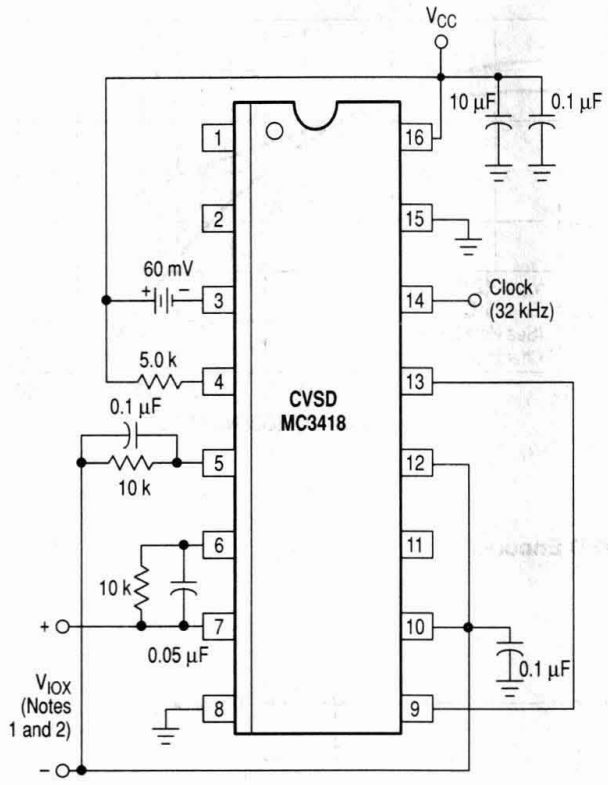
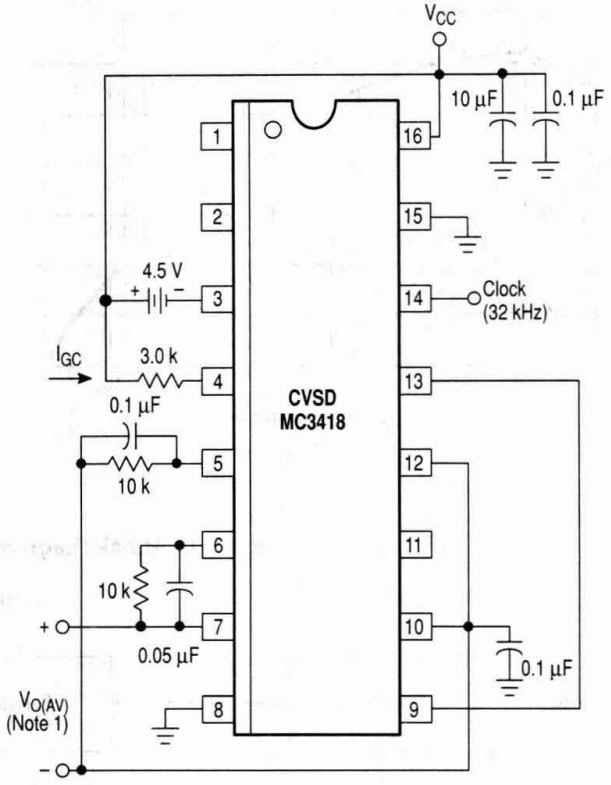


Figure 5. V/I Converter Offset Voltage, V_{IO} and V_{IOX}



NOTES: 1. Integrator amplifier offset voltage plus slope polarity switch mismatch.
2. V_{IOX} is the average voltage of the triangular wave form observed at the measurement points.

Figure 6. Dynamic Integrating Current Match



NOTES: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at t the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 2 in the Electrical Characteristics table.
3. See Figures 8 and 9.

TYPICAL PERFORMANCE CURVES

Figure 7. Typical I_{Int} versus I_{GC} (Mean ±2 σ)

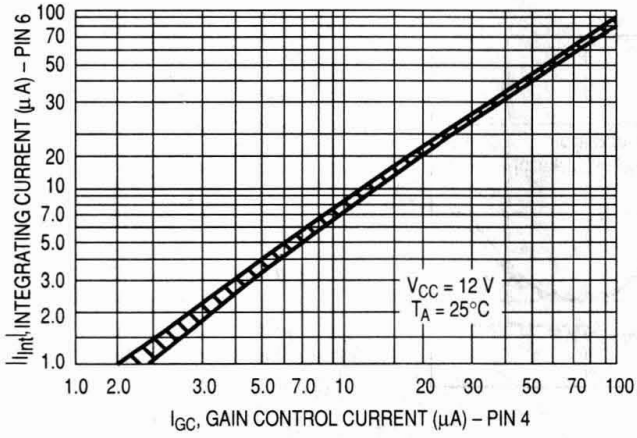


Figure 8. Normalized Dynamic Integrating Current Match versus V_{CC}

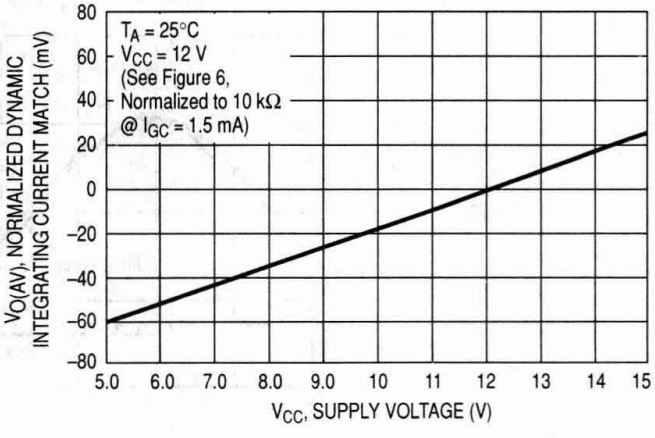


Figure 9. Normalized Dynamic Integrating Current Match versus Clock Frequency

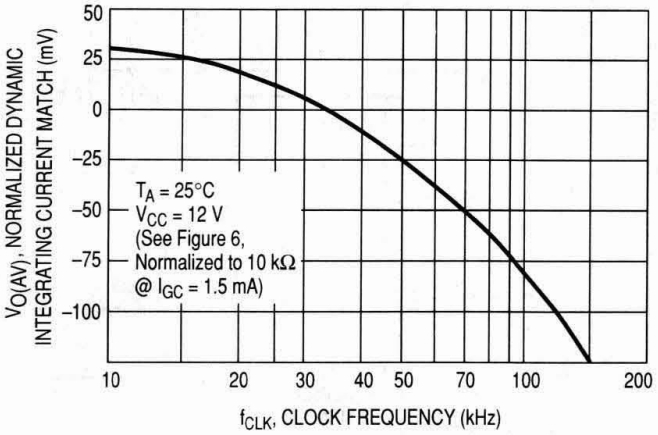


Figure 10. Dynamic Total Loop Offset versus Clock Frequency

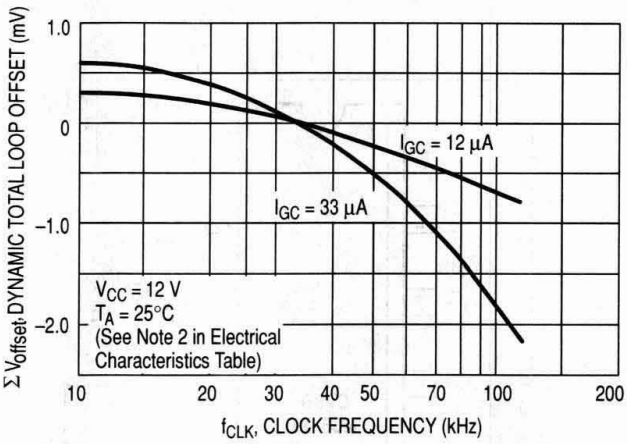


Figure 11. Block Diagram of the CVSD Encoder

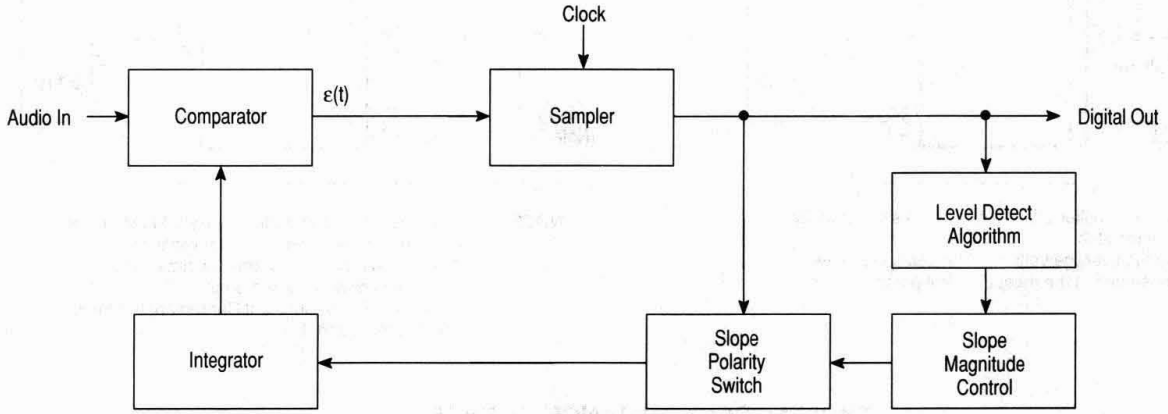


Figure 12. CVSD Waveforms

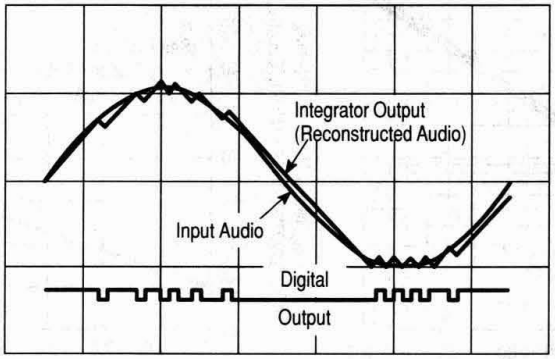


Figure 13. Block Diagram of the CVSD Decoder

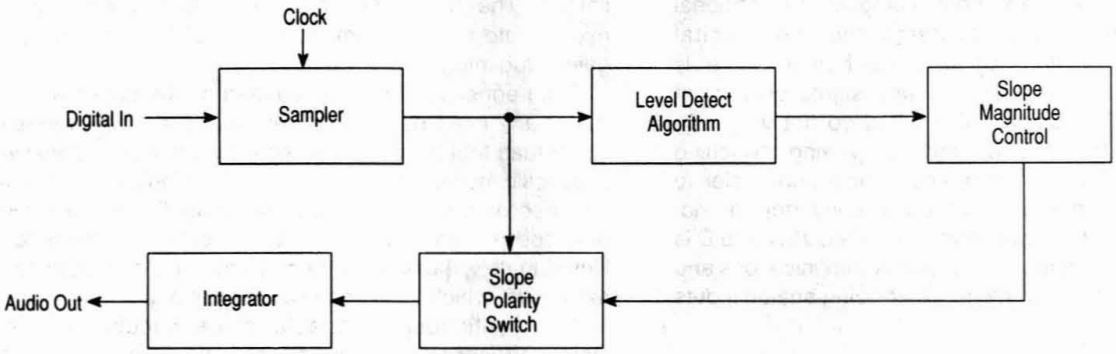
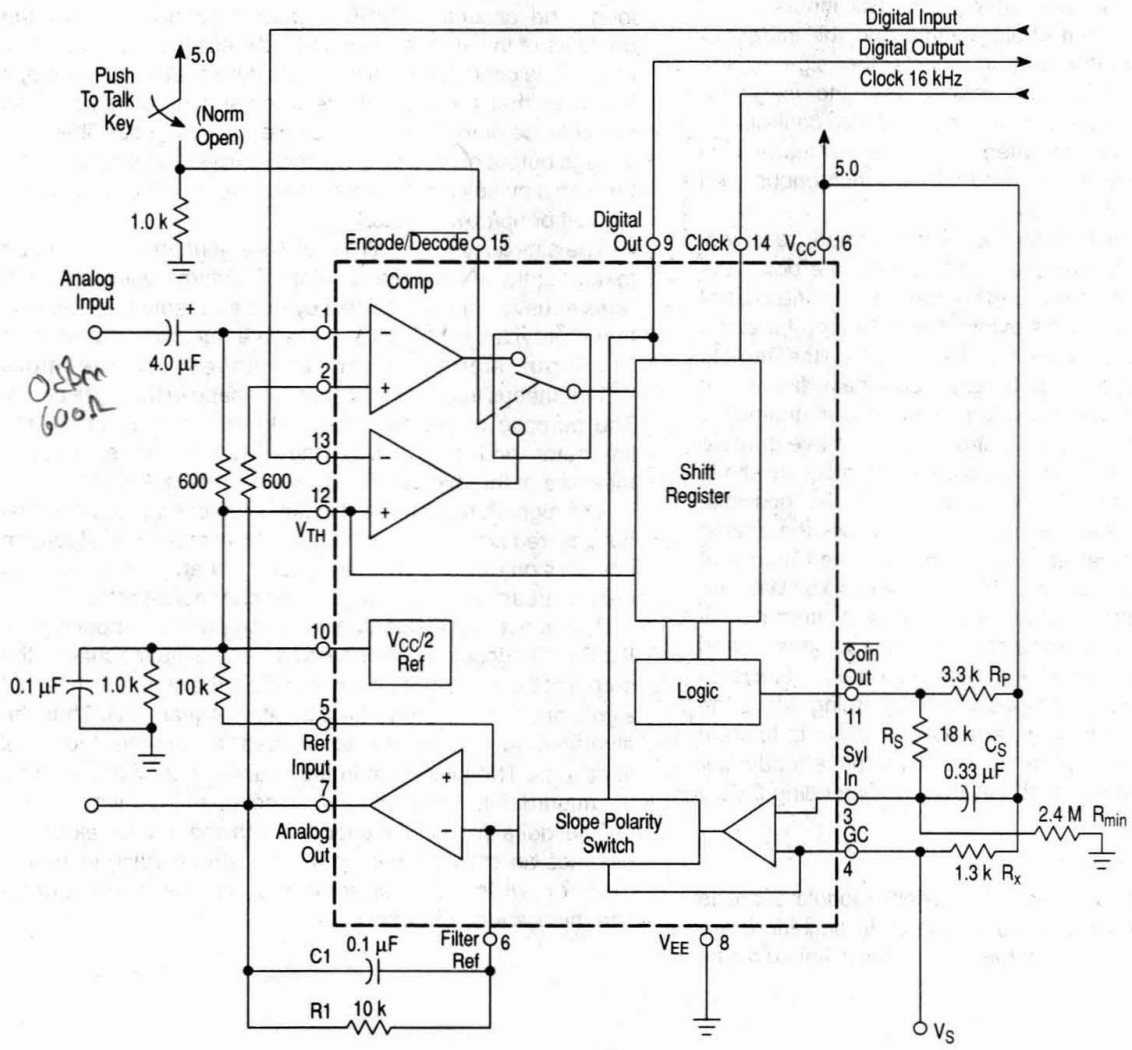


Figure 14. 16 kHz Simplex Voice Codec (Single–Pole Companding and Single Integration)



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band–limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4.0 kHz and clock rates from 8.0 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly, a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 4–bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single–pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all 1s, all 0s algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm operates only on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3418 is shown in Figure 14. This IC is a general purpose CVSD building block which allows the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application, and they are as follows:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single–pole networks. The selection of items 1 through 4 govern the codec performance.

Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13 and 14) from analog signal paths (Pins 1 to 7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications, the circuit in Figure 14 may be operated anywhere from 9.6 to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 16. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4–wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32 k bits and above. Other codecs may use bit rates up to 200 k bits/sec.

Shift Register Length (Algorithm)

The MC3418 has a 4–bit algorithm well suited for 32 kHz and higher clock rates. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal history. At 16 kHz and below, the 4–bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3418 is intended for high performance, high bit rate systems.

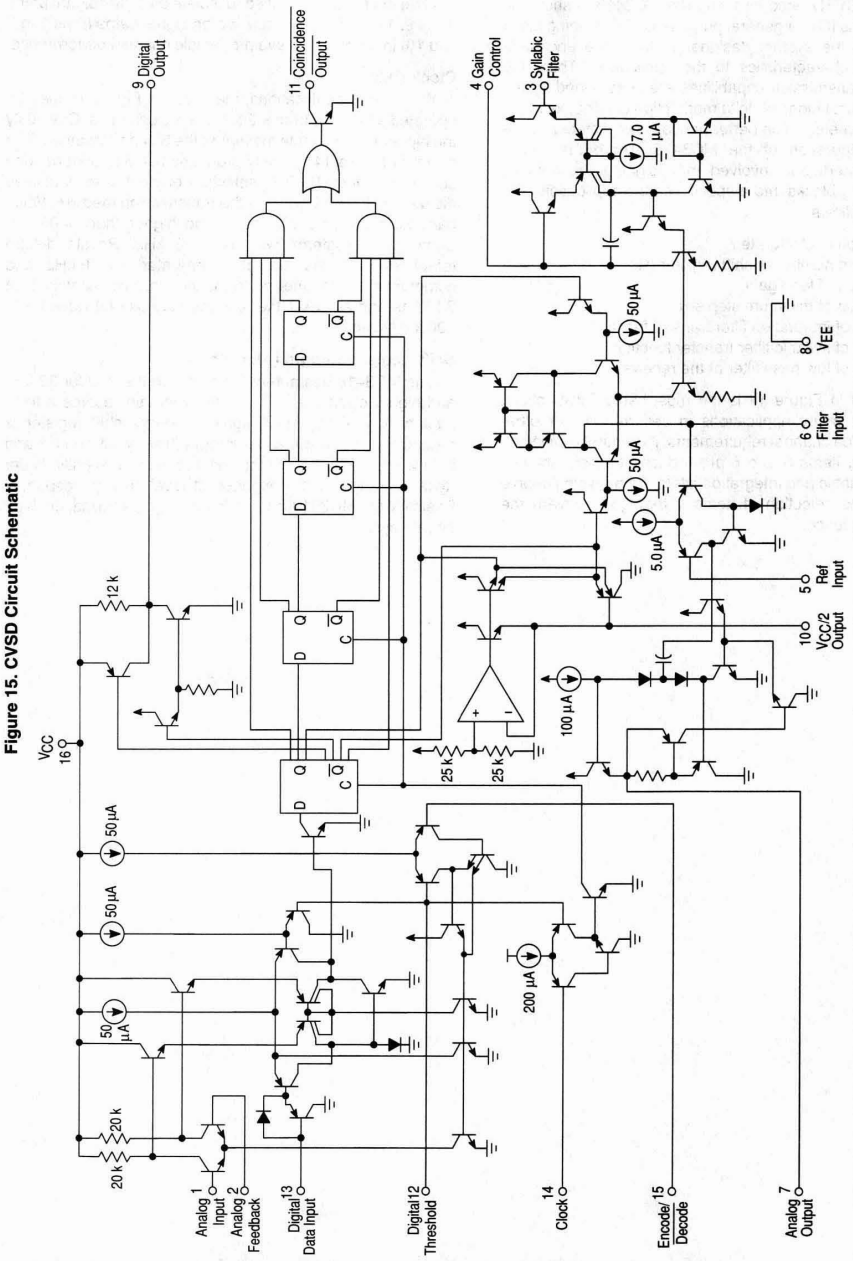
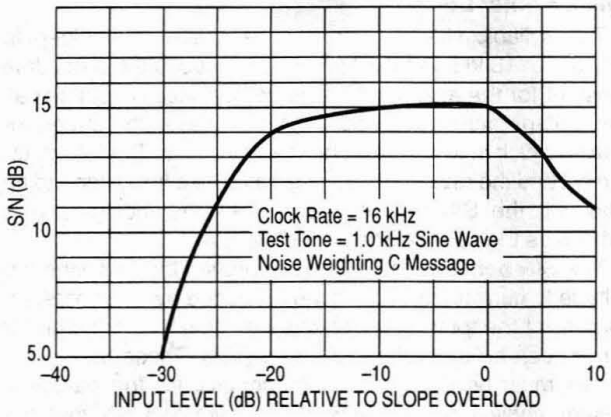


Figure 15. CVSD Circuit Schematic

Figure 16. Signal–to–Noise Performance with Single Integration, Single–Pole and Companding at 16 k Bits (Typical)



Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_x. R_x must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1.0 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6.0 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single–pole of 160 Hz is used.

$R1 = 10\ k\Omega,\ C1 = 0.1\ \mu F$

$$\frac{V_O}{I_i} = \frac{1}{C\left(S + \frac{1}{RC}\right)} = \frac{K}{S + \omega_o}$$

$$\omega_o = 2\ \pi f$$

$$10^3 = \omega_o = 2\ \pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single–pole response from 300 to 3.0 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_O}{R1} + \left(C1 \times \frac{dV_O}{dt}\right)$$

Now a 0 dBmo sine wave has a peak value of 1.0954 V. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1.0 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2\ (10\ k\Omega)} + \frac{0.1\ \mu F\ (1.1)}{0.125\ ms} = 0.935\ mA$$

* The maximum voltage across R1 when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_x = 0.25\left(V_{CC}\right)\frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one–zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3418 is tested to ensure that a 20 mVpp minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one–zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1 – 0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_O}{R1} + C\frac{dV_O}{dt}$$

For values of V_O near $V_{CC}/2$ the V_O/R term is negligible; thus:

$$I_i = C_S\frac{\Delta V_O}{\Delta T}$$

where ΔT is the clock period and ΔV_O is the desired peak–to–peak value of the idle output. For a 16 k bit system using the circuit in Figure 14:

$$I_i = \frac{0.1\ \mu F\ 20\ mV}{62.5\ \mu s} = 33\ \mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_x.

$I_iR_x = V_S min$; for 33 μA, $V_S min = 41.6\ mV$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_S min \quad R_{min} \simeq 2.4\ M\Omega$$

Having established these four parameters – clock rate, number of shift register bits, loop gain, and minimum step size – the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

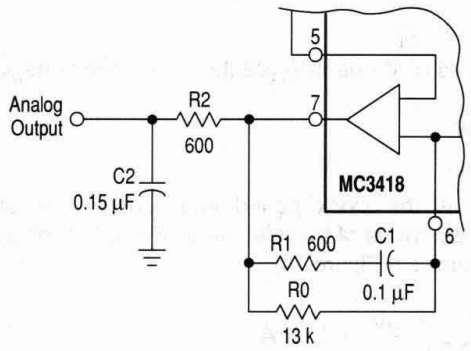
Integration Filter Design

The circuit in Figure 14 uses a single–pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1.0 or 2.0 dB by using a two–pole integration network. The improved circuit is shown in Figure 17.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1.0 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1.0 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low–pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2.0 kHz, and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz, and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low–pass filter which breaks at about 2.5 kHz.) The two–pole network in Figure 17 has a transfer function of:

$$\frac{V_O}{I_i} = \frac{R0R1\left(S + \frac{1}{R1C1}\right)}{R2C2(R0 + R1)\left(S + \frac{1}{(R0+R1)C1}\right)S + \left(\frac{1}{R2C2}\right)}$$

Figure 17. Improved Filter Configuration



NOTE: These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 17 represent one implementation of the telephony filter requirement.

The selection of the two–pole filter network affects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_O}{R0} + \left(\frac{R2C2}{R0} + \frac{R1C1}{R0} + C1\right)\frac{\Delta V_O}{\Delta T} +$$

$$\left(R2C2C1 + \frac{R1C1R2C2}{R0}\right)\frac{\Delta V_O{}^2}{\Delta T^2}$$

The calculation of desired gain resistor R_x then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single–pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

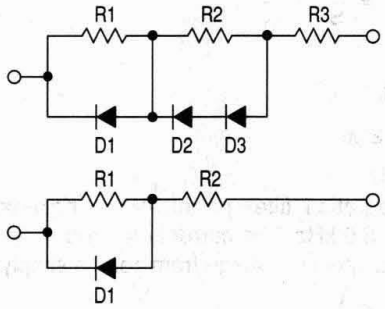
The S/N performance may be improved by modifying the voltage to current transformation produced by R_x. If different portions of the total R_x are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_x$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_x in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor–diode networks are shown in Figure 18.

Figure 18. Resistor–Diode Networks



If the performance of more complex diode networks is desired, the circuit in Figure 19 should be used. It simulates the companding characteristics of nonlinear R_x elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 21 provides excellent performance for 12 to 40 kHz systems.

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5.0 mV minimum step size and a typical 1.0% current match from 15 μA to 3.0 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the 4–bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 19, a telephone quality codec can be mass produced.

The circuit in Figure 19 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1.0 kHz test tone at a 37.7 k bit rate. At 37.7 k bits, 40 voice channels may be multiplexed on a standard 1.544 MB T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators, and small PABX installations.

The Active Companding Network

The unique feature of the codec in Figure 19 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 19, the voltage swing of Pin 11 is 6.0 V. The operating companding ratio is analoged by the voltage between Pins 10 and 4 by means of the virtual short across Pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 V below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ – 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6.0 V).

The present step size of the operating codec is directly related to the voltage across R_x, which established the integrator current. In Figure 19, the voltage across R_x is amplified by the differential amplifier A2 whose output is single ended with respect to Pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 V. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at Pin 4 is amplified by A1. The output of A1 changes the voltage across R_x in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at Pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_x, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on Pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_x and the gain of A2 and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at Pin 4 goes to zero and the voltage across R_x goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_x. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and Pin 4 and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 20. A smooth 2.0 dB drop is realized from 12 dBm to –24 under the control of A1. At –24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

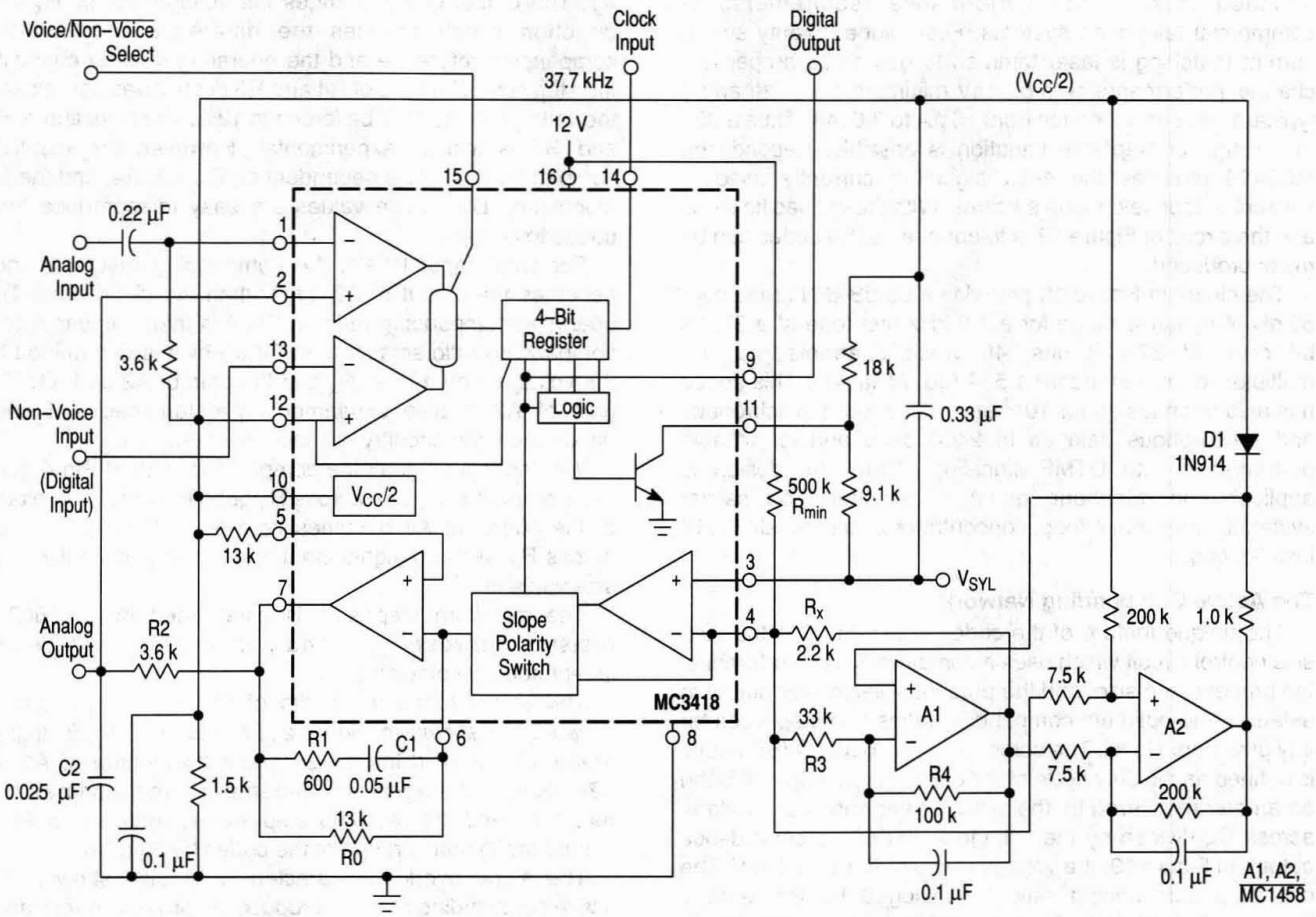
The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_x. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 19 is designed specifically for 37.7 k bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 19 represents a significant step forward in the art and cost of CVSD codec designs.

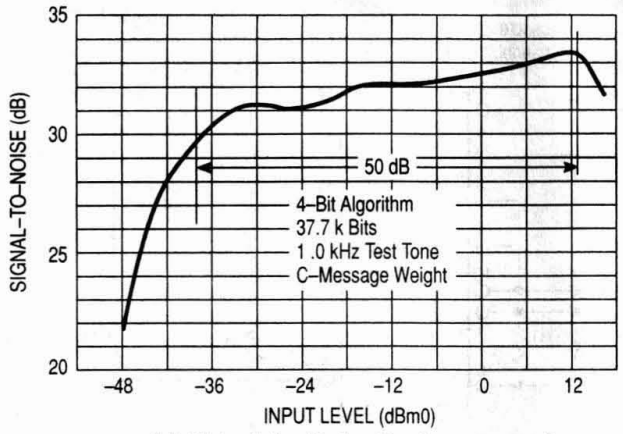
*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 19, 0.050 μF would work well.

Figure 19. Telephone Quality Deltamod Coder*

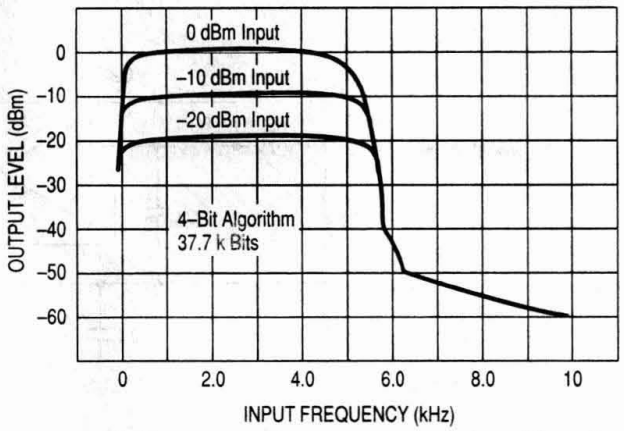


* Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.

Figure 20. Signal–to–Noise Performance and Frequency Response*



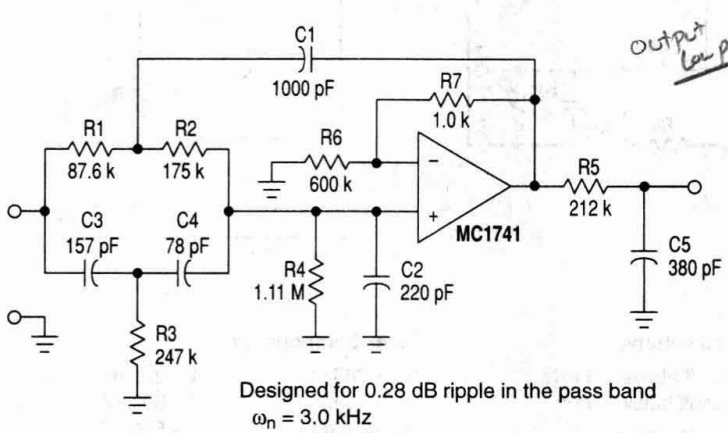
(a) Signal–to–Noise Performance of Telephony Quality Deltamodulator



(b) Frequency Response versus Input Level (Slope Overload Characteristic)

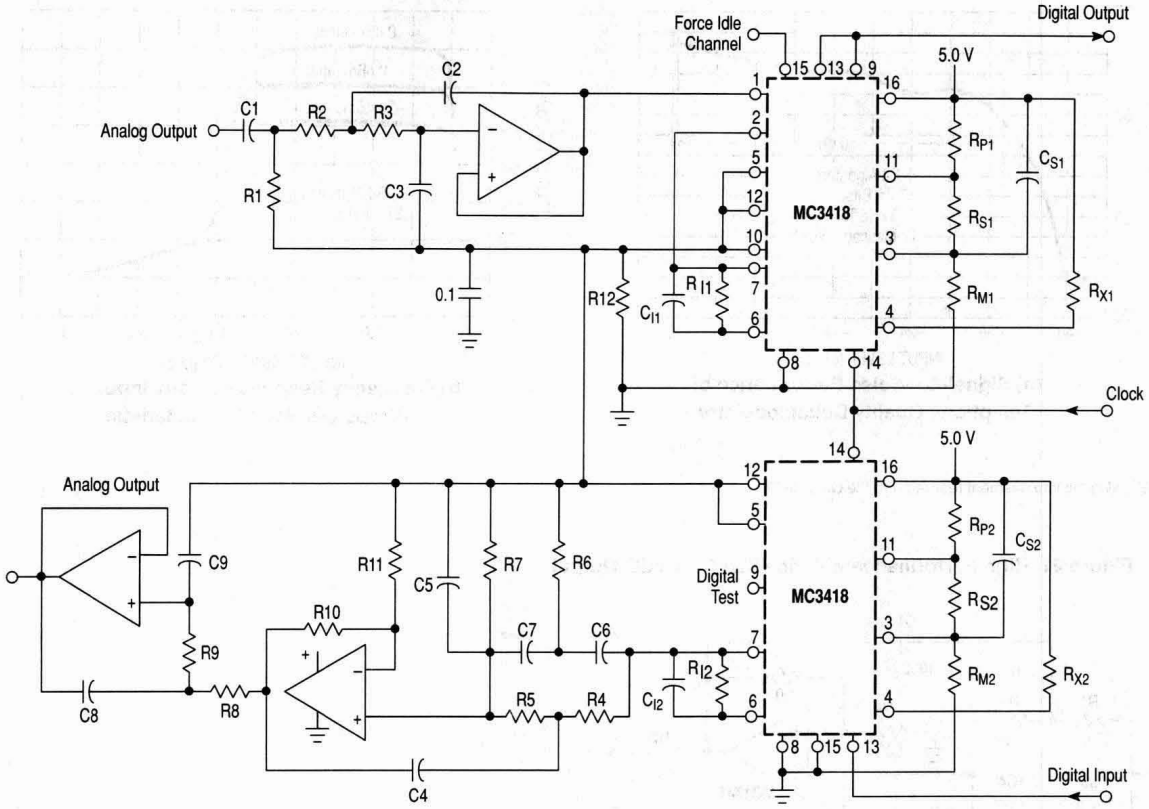
*Showing the improvement realized with the circuit in Figure 19.

Figure 21. High Performance Elliptic Filter for CVSD Output



Designed for 0.28 dB ripple in the pass band
ω_n = 3.0 kHz
ω_s = ≅ 6.0 kHz
AdB at ω_s and above 29.5 dB

Figure 22. Full Duplex/32 k Bit CVSD Voice Codec



Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1.0 kΩ

R_{M1}, R_{M2} – 15 MΩ
Minimum step size = 6.0 mV

C_{S1}, C_{S2} – 0.05 µF
C_{I1}, C_{I2} – 0.05 µF

2 MC3418
1 MC3403 (or MC3406)

NOTE: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6.0 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9.0 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 Ω
R11 – 72 kΩ

C1 – 3.3 µF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

NOTE: All Res. 0.1% to 1%
All Cap. 0.1%

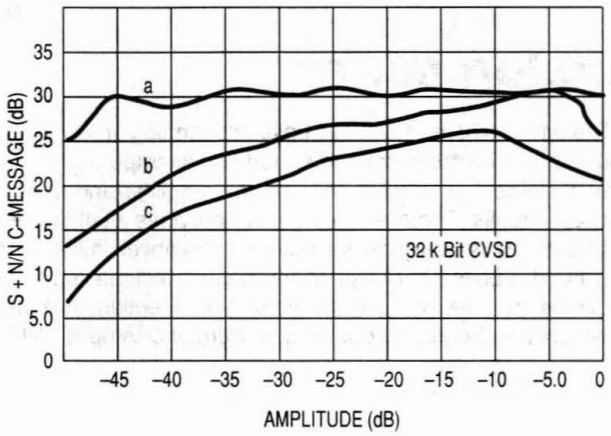
COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required, and the cost objectives. To illustrate the choices available, the data in Figure 23 compares the signal–to–noise ratios and dynamic range of various codec design options at 32 k bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non–voice applications of the MC3418 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

Figure 23. Comparative Codec Performance – Signal–to–Noise Ratio for 1.0 kHz Test Tone



NOTE: These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a – Complex companding and double integration (Figure 19)
Curve b – Double integration (Figure 14 using Figure 17)
Curve c – Single integration (Figure 14) with 6.0 mV stepsize

MOTOROLA

MC12002

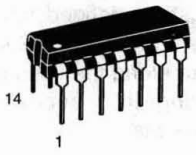
Analog Mixer

The MC12002 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

This circuit is designed for use as a balanced mixer in high-frequency wide-band circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.

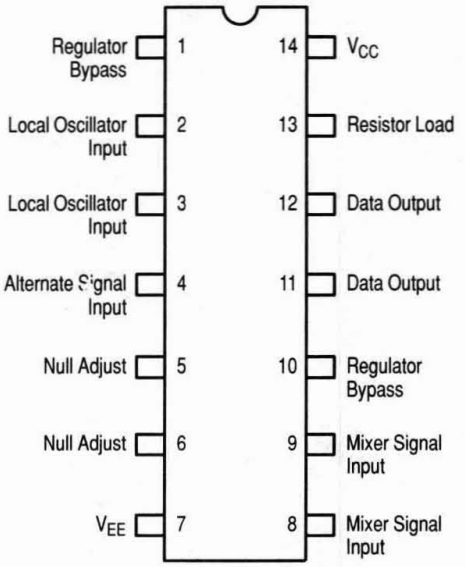
ANALOG MIXER

SEMICONDUCTOR TECHNICAL DATA



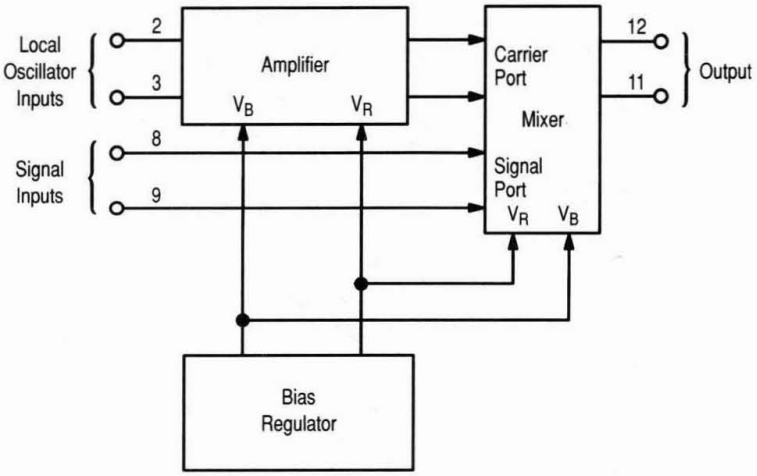
P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



(Top View)

Figure 1. Logic Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12002P	T_A = –30° to +85°C	Plastic

ELECTRICAL CHARACTERISTICS

										TEST VOLTAGE VALUES				
										Volts				
										V_{IHmax}	V_{ILmin}	V_{CC}		
										+2.9	+2.0	+5.0		
			Test Limits							VOLTAGE APPLIED TO PINS LISTED BELOW				
		Pin Under	−30°C		+25°C		+85°C							
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	V_{IHmax}	V_{ILmin}	V_{CC}	Gnd	
Power Supply Drain	I_{CC}	14	—	—	—	16	—	—	mAdc	—	—	11,12,14	5,6,7	
Input Current	I_{inH}	2	—	—	—	0.75	—	—	mAdc	2	—	11,12,14	5,6,7	
		3	—	—	—	0.75	—	—	mAdc	3	—	11,12,14	5,6,7	
		8	—	—	—	0.75	—	—	mAdc	8	—	11,12,14	5,6,7	
		9	—	—	—	0.75	—	—	mAdc	9	—	11,12,14	5,6,7	
	I_{inL}	2	—	—	−0.7	—	—	—	mAdc	—	2	11,12,14	5,6,7	
		3	—	—	−0.7	—	—	—	mAdc	—	3	11,12,14	5,6,7	
		8	—	—	−0.7	—	—	—	mAdc	—	8	11,12,14	5,6,7	
		9	—	—	−0.7	—	—	—	mAdc	—	9	11,12,14	5,6,7	
Output Current	IO_1	11	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7	
		12	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7	
	IO_2	11	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7	
		12	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7	
	I_{out}	11	—	—	4.2	7.8	—	—	mAdc	2,9	—	11,12,14	5,6,7	
		11	—	—	4.2	7.8		—	mAdc	3,8	—	11,12,14	5,6,7	
		12	—	—	4.2	7.8		—	mAdc	2,8	—	11,12,14	5,6,7	
		12	—	—	4.2	7.8		—	mAdc	3,9	—	11,12,14	5,6,7	
Differential Current	ΔIO_1	11,12	−100	+100	−100	+100	−100	+100	µAdc	—	—	11,12,14	7	
	ΔIO_2	11,12	−200	+200	−200	+200	−200	+200	µAdc	—	—	11,12,14	5,6,7	
Bias Voltage	V_{Bias}	1	2.33	2.53	2.32	2.52	2.3	2.5	Vdc	—	—	11,12,14	5,6,7	
		4	390	590	400	600	410	610	mVdc	—	—	11,12,14	5,6,7	
		5	275	415	285	425	295	435	mVdc	—	—	11,12,14	7	
		6	275	415	285	425	295	435	mVdc	—	—	11,12,14	7	
		10	1.26	1.46	1.185	1.385	1.105	1.305	Vdc	—	—	11,12,14	5,6,7	
										Pulse In	Pulse Out	−3.0 V	Gnd	V_{EE}
AC Gain (See Figure 1)	A_V	11	—	—	5.0	—	—	—	V/V	2	11	9	14	7
(Frequency = 100 MHz) *Note		11	—	—	0.28	—	—	—	V/V	8	11	3	14	7

NOTE: *Note: AC Gain is a function of collector load impedance.

Figure 2. Analog Mixer Circuit Schematic

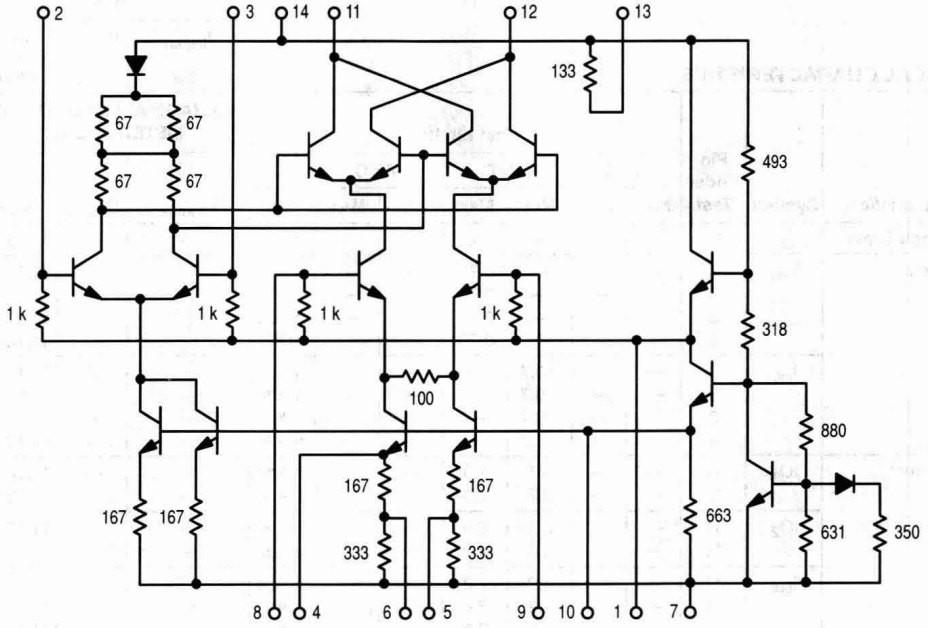
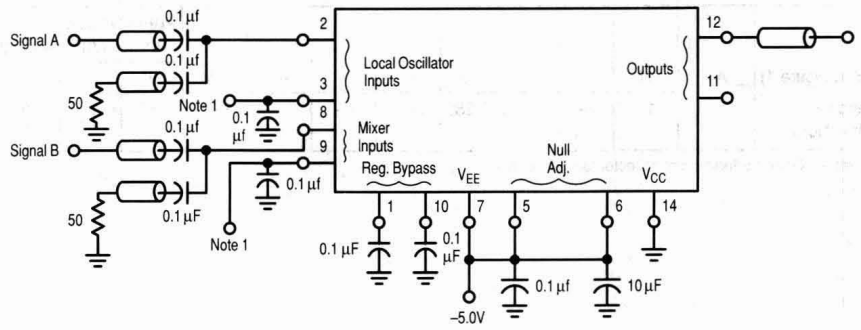


Figure 3. AC Gain Test



Note 1:
V_{IL} = –3.0 V on pin 3 when pin 8 is under test.
V_{IL} = –3.0 V on pin 9 when pin 2 is under test.

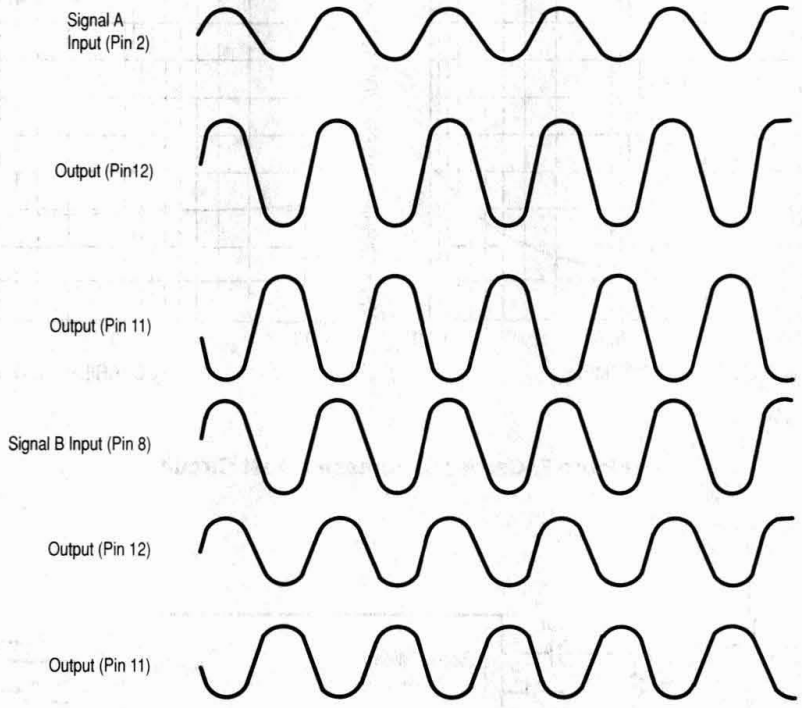
Signal A = 30 mVpp

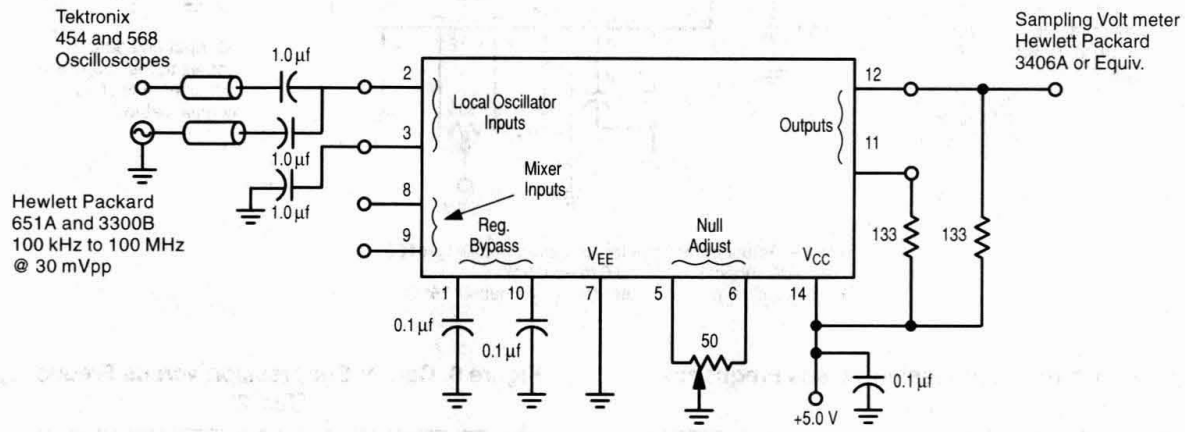
Signal B = 300 mVpp

Freq. = 100 MHz

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
The unused output is connected to a 50-ohm resistor to ground.

Figure 4. Carrier Feedthrough Test Circuits





Notes:
Test 1 – Adjust potentiometer for carrier null at f_c = 100 kHz.
Test 2 – Connect pins 5 and 6 to Gnd.

All Input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Figure 5. Carrier Feedthrough versus Frequency
(Test 1)

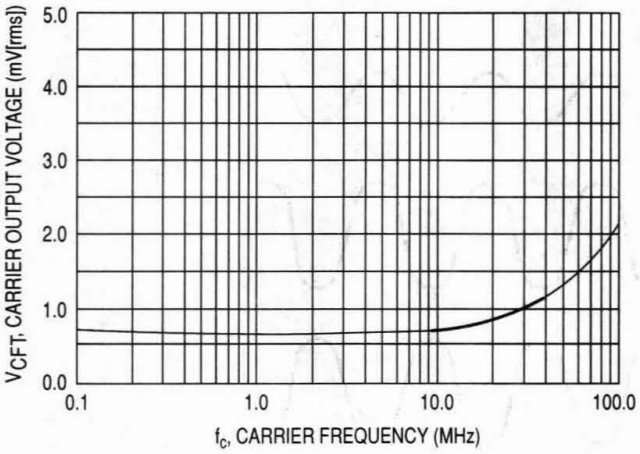


Figure 6. Carrier Feedthrough versus Frequency
(Test 2)

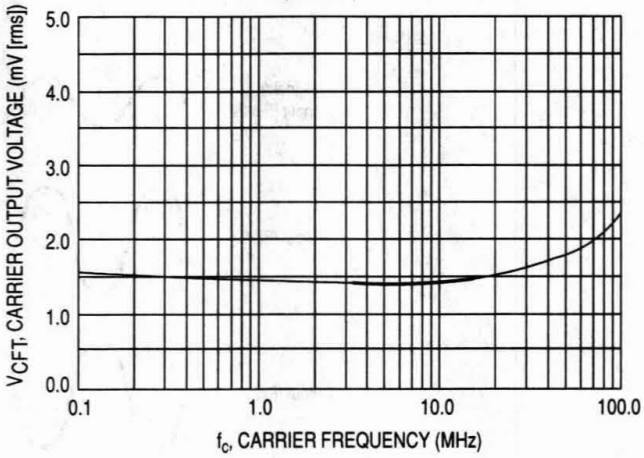
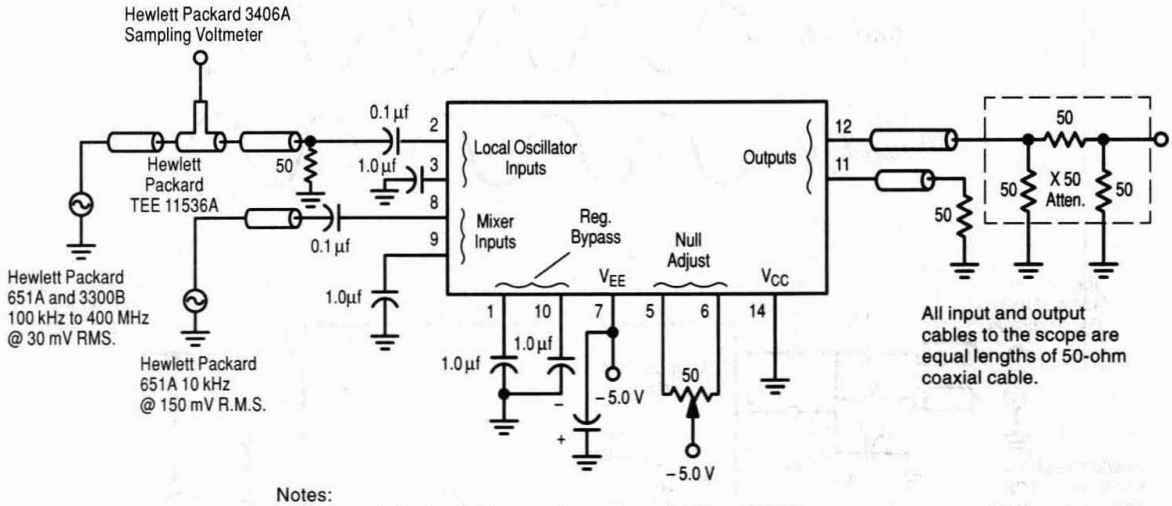


Figure 7. Carrier Suppression Test Circuit



Notes:
Test 1 – Adjust potentiometer for carrier null @ f_c = 100 kHz
Test 2 – Connect pins 5 and 6 to –5.0 volts
Test 3 – Adjust potentiometer for carrier null @ 25° C

Figure 8. Carrier Suppression versus Frequency
(Test 1)

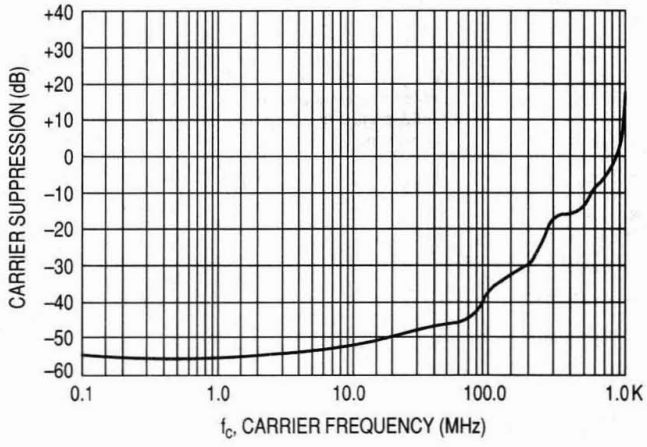


Figure 9. Carrier Suppression versus Frequency
(Test 2)

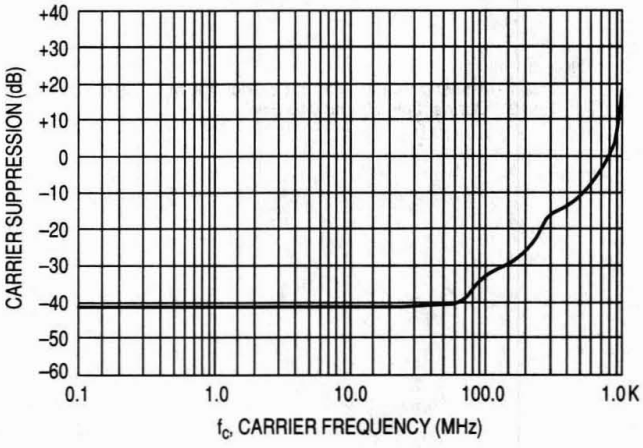


Figure 10. Carrier Suppression versus Temperature

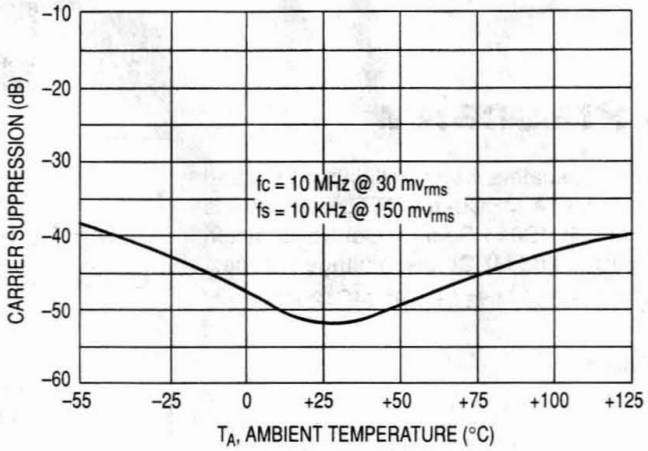
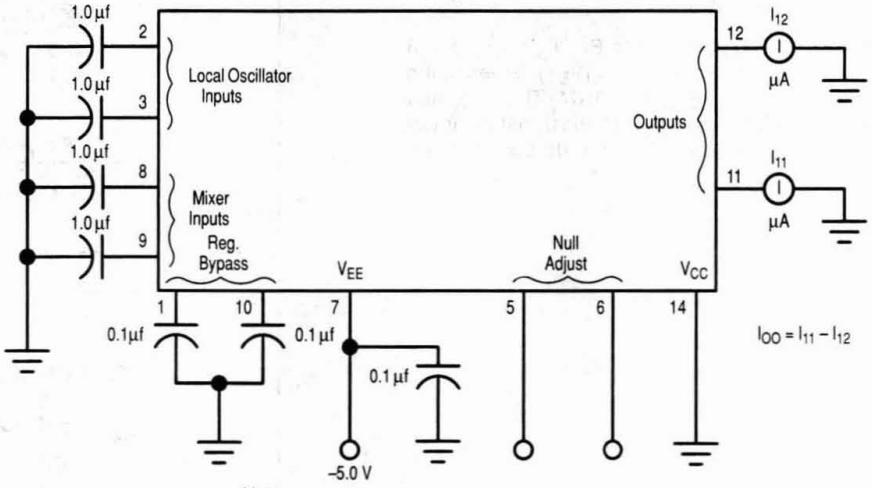


Figure 11. Output Offset Current (I_{00}) versus Temperature



Notes:
Test 1 – Pins 5 and 6 left open
Test 2 – Pins 5 and 6 are tied to –5.0 volts

Figure 12. Output Offset Current versus Temperature

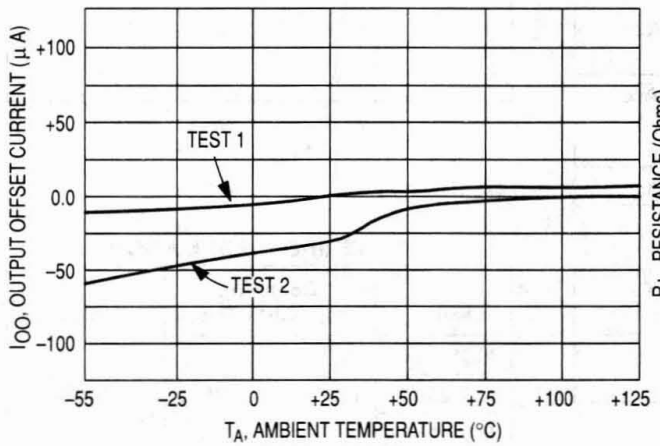
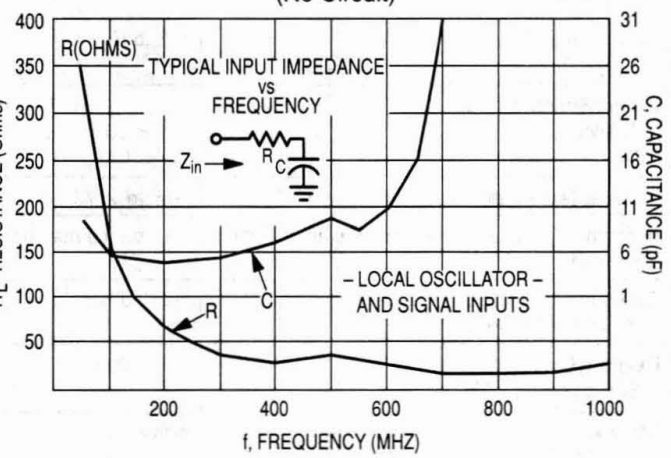


Figure 13. Typical Input Impedance versus Frequency
(No Circuit)



MOTOROLA

MC12009
MC12011
MC12013

MECL PLL COMPONENTS
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

Dual Modulus Prescaler

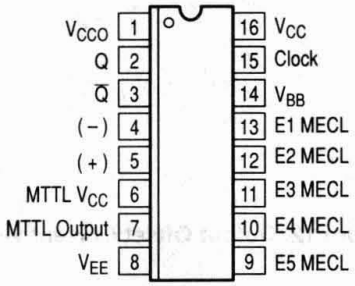
These devices are two–modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL–to–MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- MC12009 480 MHz (÷5/6), MC12011 550 MHz (÷8/9), MC12013 550 MHz (÷10/11)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- 5.0 or –5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ohms and 4 pF
- V_{BB} Reference Voltage
- 310 Milliwatts (Typ)

* When using a 5.0 V supply, apply 5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using –5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply –5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impaired)			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	–8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current Continuous Surge	I_O	 < 50 < 100	mAdc
Storage Temperature Range	T_{stg}	–65 to +175	°C
(Recommended Maximum Ratings above which performance may be degraded)			
Operating Temperature Range MC12009, MC12011, MC12013	T_A	–30 to +85	°C
DC Fan–Out (Note 1) (Gates and Flip–Flops)	n	70	—

NOTES: 1. AC fan–out is limited by desired system performance.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12009P	T_A = – 35° to +85°C	Plastic
MC12011P		
MC12013P		

Figure 1. Logic Diagrams

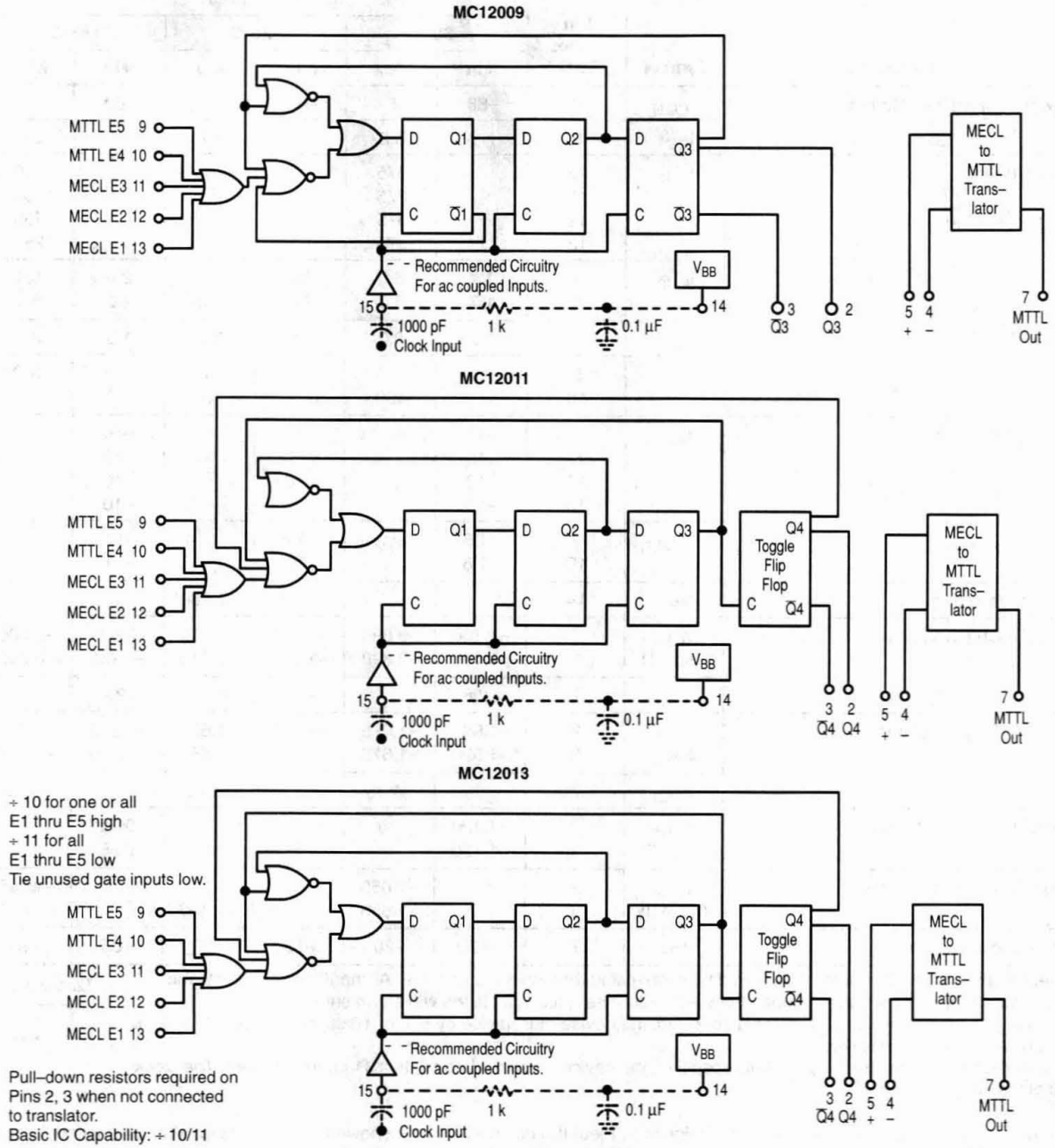
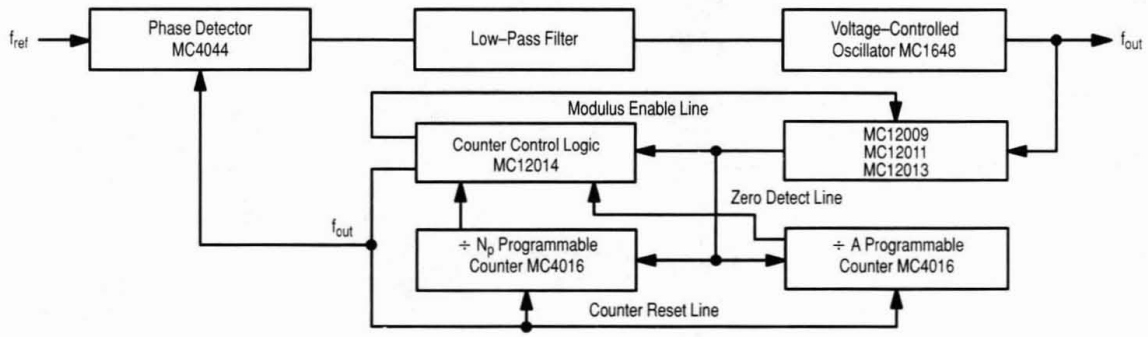


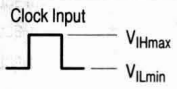
Figure 2. Typical Frequency Synthesizer Application



ELECTRICAL CHARACTERISTICS (Supply Voltage = –5.2 V, unless otherwise noted.)

Characteristic	Symbol	Pin Under Test	Test Limits						Unit
			–30°C		+25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{CC1}	8	–88		–80		–80		mAdc
	I_{CC2}	6		5.2		5.2		5.2	mAdc
Input Current	I_{inH1}	15 11 12 13		375 375 375 375		250 250 250 250		250 250 250 250	µAdc
	I_{inH2}	4 5	1.7 1.7	6.0 6.0	2.0 2.0	6.0 6.0	2.0 2.0	6.4 6.4	mAdc
	I_{inH3}	5	0.7	3.0	1.0	3.0	1.0	3.6	
	I_{inH4}	9 10		100 100		100 100		100 100	µAdc
Leakage Current	I_{inL1}	15 11 12 13	–10 –10 –10 –10		–10 –10 –10 –10		–10 –10 –10 –10		µAdc
	I_{inL2}	9 10	–1.6 –1.6		–1.6 –1.6		–1.6 –1.6		mAdc
Reference Voltage	V_{BB}	14			–1.360	–1.160			Vdc
Logic '1' Output Voltage	V_{OH1} (Note 1)	2 3	–1.100 –1.100	–0.890 –0.890	–1.000 –1.000	–0.810 –0.810	–0.930 –0.930	–0.700 –0.700	Vdc
	V_{OH2}	7	–2.8		–2.6		–2.4		
Logic '0' Output Voltage	V_{OL1} (Note 1)	2 3	–1.990 –1.990	–1.675 –1.675	–1.950 –1.950	–1.650 –1.650	–1.925 –1.925	–1.615 –1.615	Vdc
	V_{OL2}	7		–4.26		–4.40		–4.48	
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2 3	–1.120 –1.120		–1.020 –1.020		–0.950 –0.950		Vdc
Logic '0' Threshold Voltage	V_{OLA} (Note 3)	2 3		–1.655 –1.655		–1.630 –1.630		–1.595 –1.595	Vdc
Short Circuit Current	I_{OS}	7	–65	–20	–65	–20	–65	–20	mAdc

1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 5, 8 or 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 6, 9 or 11 during this test. The clock input is the waveform shown.

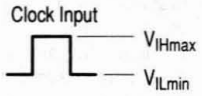


Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to –2.0 V. Test procedures are shown for only one gate. The other gates are tested in the same manner.

ELECTRICAL CHARACTERISTICS (Supply Voltage = –5.2 V, unless otherwise noted.) (continued)

			TEST VOLTAGE/CURRENT VALUES						
			Volts						
@ Test Temperature			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{ILH}	
–30°C			–0.890	–1.990	–1.205	–1.500	–2.8	–4.7	
+25°C			–0.810	–1.950	–1.105	–1.475	–2.8	–4.7	
+85°C			–0.700	–1.925	–1.035	–1.440	–2.8	–4.7	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	
Power Supply Drain Current	I_{CC1}	8							1,16
	I_{CC2}	6	4	5					6
Input Current	I_{inH1}	15 11 12 13	15 11 12 13						1,16 1,16 1,16 1,16
	I_{inH2}	4 5	5 5	4 4					6 6
	I_{inH3}	5	4	5					6
	I_{inH4}	9 10					9 10		1,16 1,16
Leakage Current	I_{inL1}	15 11 12 13							1,16 1,16 1,16 1,16
	I_{inL2}	9 10						9 10	1,16 1,16
Reference Voltage	V_{BB}	14							1,16
Logic '1' Output Voltage	V_{OH1} (Note 1.)	2 3		11,12,13 11,12,13				9,10 9,10	1,16 1,16
	V_{OH2}	7	5	4					6
Logic '0' Output Voltage	V_{OL1} (Note 1.)	2 3		11,12,13 11,12,13				9,10 9,10	1,16 1,16
	V_{OL2}	7	4	5					6
Logic '1' Threshold Voltage	V_{OHA} (Note 2.)	2 3			11,12,13 11,12,13				1,16 1,16
Logic '0' Threshold Voltage	V_{OLA} (Note 3.)	2 3				11,12,13 11,12,13			1,16 1,16
Short Circuit Current	I_{OS}	7	5	4				7	6

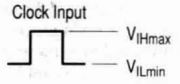
1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 5, 8 or 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 6, 9 or 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (Supply Voltage = –5.2 V, unless otherwise noted.) (continued)

			TEST VOLTAGE/CURRENT VALUES						
			Volts			mA			
@ Test Temperature			V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	
–30°C			–3.2	–4.4	–5.2	–0.25	16	–0.40	
+25°C			–3.2	–4.4	–5.2	–0.25	16	–0.40	
+85°C			–3.2	–4.4	–5.2	–0.25	16	–0.40	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd
			V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	
Power Supply Drain Current	I_{CC1}	8			8				1,16
	I_{CC2}	6			8				6
Input Current	I_{inH1}	15			8				1,16
		11	9,10		8				1,16
		12	9,10		8				1,16
		13	9,10		8				1,16
	I_{inH2}	4			8				6
		5			8				6
	I_{inH3}	5			8				6
	I_{inH4}	9			8				1,16
		10			8				1,16
Leakage Current	I_{inL1}	15			8,15				1,16
		11			8,11				1,16
		12			8,12				1,16
		13			8,13				1,16
	I_{inL2}	9			8				1,16
		10			8				1,16
Reference Voltage	V_{BB}	14			8	14			1,16
Logic '1' Output Voltage	V_{OH1} (Note 1.)	2			8				1,16
		3			8				1,16
	V_{OH2}	7			8			7	6
Logic '0' Output Voltage	V_{OL1} (Note 1.)	2			8				1,16
		3			8				1,16
	V_{OL2}	7			8		7		6
Logic '1' Threshold Voltage	V_{OHA} (Note 2.)	2	9,10		8				1,16
		3	9,10		8				1,16
Logic '0' Threshold Voltage	V_{OLA} (Note 3.)	2		9,10	8				1,16
		3		9,10	8				1,16
Short Circuit Current	I_{OS}	7			8				6

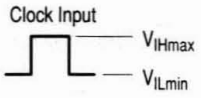
1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 5, 8 or 10 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 6, 9 or 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (Supply Voltage = 5.0 V, unless otherwise noted.)

Characteristic	Symbol	Pin Under Test	Test Limits						Unit
			–30°C		+25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{CC1}	8	–88		–80		–80		mAdc
	I_{CC2}	6		5.2		5.2		5.2	mAdc
Input Current	I_{inH1}	15 11 12 13		375 375 375 375		250 250 250 250		250 250 250 250	µAdc
	I_{inH2}	4 5	1.7 1.7	6.0 6.0	2.0 2.0	6.0 6.0	2.0 2.0	6.4 6.4	mAdc
	I_{inH3}	5	0.7	3.0	1.0	3.0	1.0	3.6	
	I_{inH4}	9 10			100 100	100 100		100 100	µAdc
Leakage Current	I_{inL1}	15 11 12 13	–10 –10 –10 –10		–10 –10 –10 –10		–10 –10 –10 –10		µAdc
	I_{inL2}	9 10	–1.6 –1.6		–1.6 –1.6		–1.6 –1.6		mAdc
Reference Voltage	V_{BB}	14			3.67	3.87			Vdc
Logic '1' Output Voltage	V_{OH1} (Note 4.)	2 3	3.900 3.900	4.110 4.110	4.000 4.000	4.190 4.190	4.070 4.070	4.300 4.300	Vdc
	V_{OH2}	7	2.4		2.6		2.8		
Logic '0' Output Voltage	V_{OL1} (Note 4.)	2 3	3.070 3.070	3.385 3.385	3.110 3.110	3.410 3.410	3.135 3.135	3.445 3.445	Vdc
	V_{OL2}	7		0.94		0.80		0.72	
Logic '1' Threshold Voltage	V_{OHA} (Note 5.)	2 3	3.880 3.880		3.980 3.980		4.050 4.050		Vdc
Logic '0' Threshold Voltage	V_{OLA} (Note 6.)	2 3		3.405 3.405		3.430 3.430		3.465 3.465	Vdc
Short Circuit Current	I_{OS}	7	–65	–20	–65	–20	–65	–20	mAdc

4. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
5. In addition to meeting the output levels specified, the device must divide by 5, 8 or 10 during this test. The clock input is the waveform shown.
6. In addition to meeting the output levels specified, the device must divide by 6, 9 or 11 during this test. The clock input is the waveform shown.

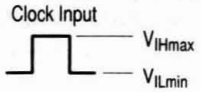


Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to –2.0 V. Test procedures are shown for only one gate. The other gates are tested in the same manner.

ELECTRICAL CHARACTERISTICS (Supply Voltage = 5.0 V, unless otherwise noted.) (continued)

			TEST VOLTAGE/CURRENT VALUES						
			Volts						
@ Test Temperature			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{ILH}	
–30°C			+4.110	+3.070	+3.795	+3.500	+2.4	+0.5	
+25°C			+4.190	+3.110	+3.895	+3.525	+2.4	+0.5	
+85°C			+4.300	+3.135	+3.965	+3.560	+2.4	+0.5	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V_{EE}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	
Power Supply Drain Current	I_{CC1}	8							8
	I_{CC2}	6	4	5					8
Input Current	I_{inH1}	15 11 12 13	15 11 12 13						8 8 8 8
	I_{inH2}	4 5	5 5	4 4					8 8
	I_{inH3}	5	4	5					8
	I_{inH4}	9 10					9 10		8 8
Leakage Current	I_{inL1}	15 11 12 13							8,15 8,11 8,12 8,13
	I_{inL2}	9 10						9 10	8 8
Reference Voltage	V_{BB}	14							8
Logic '1' Output Voltage	V_{OH1} (Note 4.)	2 3		11,12,13 11,12,13				9,10 9,10	8 8
	V_{OH2}	7	5	4					8
Logic '0' Output Voltage	V_{OL1} (Note 4.)	2 3		11,12,13 11,12,13				9,10 9,10	8 8
	V_{OL2}	7	4	5					8
Logic '1' Threshold Voltage	V_{OHA} (Note 5.)	2 3			11,12,13 11,12,13				8 8
Logic '0' Threshold Voltage	V_{OLA} (Note 6.)	2 3				11,12,13 11,12,13			8 8
Short Circuit Current	I_{OS}	7	5	4				7	8

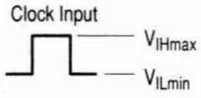
4. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
5. In addition to meeting the output levels specified, the device must divide by 5, 8 or 10 during this test. The clock input is the waveform shown.
6. In addition to meeting the output levels specified, the device must divide by 6, 9 or 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (Supply Voltage = 5.0 V, unless otherwise noted.) (continued)

			TEST VOLTAGE/CURRENT VALUES						
			Volts			mA			
@ Test Temperature			V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	
–30°C			+2.0	+0.8	+5.0	–0.25	16	–0.40	
+25°C			+2.0	+0.8	+5.0	–0.25	16	–0.40	
+85°C			+2.0	+0.8	+5.0	–0.25	16	–0.40	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**						**(V_{EE}) Gnd**
			V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	
Power Supply Drain Current	I_{CC1}	8			1,16				8
	I_{CC2}	6			6				8
Input Current	I_{inH1}	15			1,16				8
		11	9,10		1,16				8
		12	9,10		1,16				8
		13	9,10		1,16				8
	I_{inH2}	4			6				8
		5			6				8
	I_{inH3}	5			6				8
	I_{inH4}	9			1,16				8
		10			1,16				8
Leakage Current	I_{inL1}	15			1,16				8,15
		11			1,16				8,11
		12			1,16				8,12
		13			1,16				8,13
	I_{inL2}	9			1,16				8
		10			1,16				8
Reference Voltage	V_{BB}	14			1,16	14			8
Logic '1' Output Voltage	V_{OH1} (Note 4.)	2			1,16				8
		3			1,16				8
	V_{OH2}	7			6			7	8
Logic '0' Output Voltage	V_{OL1} (Note 4.)	2			1,16				8
		3			1,16				8
	V_{OL2}	7			6		7		8
Logic '1' Threshold Voltage	V_{OHA} (Note 5.)	2	9,10		1,16				8
		3	9,10		1,16				8
Logic '0' Threshold Voltage	V_{OLA} (Note 6.)	2		9,10	1,16				8
		3		9,10	1,16				8
Short Circuit Current	I_{OS}	7			6				8

4. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
5. In addition to meeting the output levels specified, the device must divide by 5, 8 or 10 during this test. The clock input is the waveform shown.
6. In addition to meeting the output levels specified, the device must divide by 6, 9 or 11 during this test. The clock input is the waveform shown.



SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013									TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:								
			−30°C			+25°C			+85°C											
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Pulse Gen.1	Pulse Gen.2	Pulse Gen.3	V_{IHmin} †	V_{ILmin} †	V_F −3.0 V	V_{EE} −3.0 V	V_{CC} +2.0
Propagation Delay (See Figures 3 and 5)	t_{15+2+}	2	—	—	8.1	—	—	8.1	—	—	8.9	ns	15	—	—	—	11,12,13	9,10	8	1,6,16
	t_{15+2-}	2	—	—	7.5	—	—	7.5	—	—	8.2		15	—	—	—	11,12,13	9,10	8	1,6,16
	t_{5+7+}	7	—	—	8.4	—	—	8.1	—	—	8.9		A	—	—	—	—	—	8	1,6,16
	t_{5-7-}	7	—	—	6.5	—	—	6.5	—	—	7.1		A	—	—	—	—	—	8	1,6,16
Setup Time (See Figures 4 and 5)	t_{setup1}	11	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	*	—	—	*	9,10	8	1,6,16
	t_{setup2}	9	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	—	*	—	11,12,13	*	8	1,6,16
Release Time (See Figures 4 and 5)	t_{rel1}	11	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	*	—	—	*	9.10	8	1,6,16
	t_{rel2}	9	5.0	—	—	5.0	—	—	5.0	—	—	ns	15	—	*	—	11,12,13	*	8	1,6,16
Toggle Frequency (See Figure 6)	f_{max}	2										MHz								
MC12009 : 5/6			440	—	—	480	—	—	440	—	—		—	—	—	11	—	—	8	16
MC12011 : 8/9			500	—	—	550	—	—	500	—	—		—	—	—	11	—	—	8	16
MC12013 : 10/11			500	—	—	550	—	—	500	—	—		—	—	—	11	—	—	8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

	−30°C	+25°C	+85°C	
†V_{IHmin}	+1.03	+1.115	+1.20	Vdc
†V_{ILmin}	+0.175	+0.200	+0.235	Vdc

Figure 3. AC Voltage Waveforms

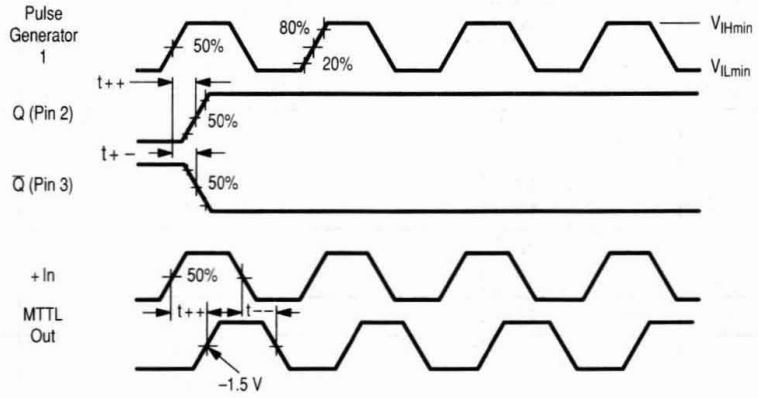
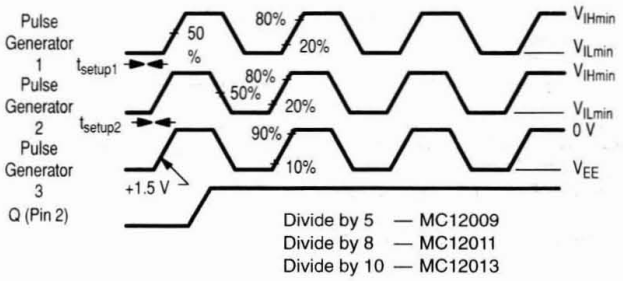


Figure 4. Setup and Release Time Waveforms



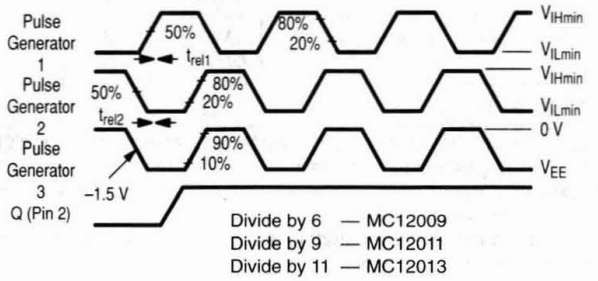
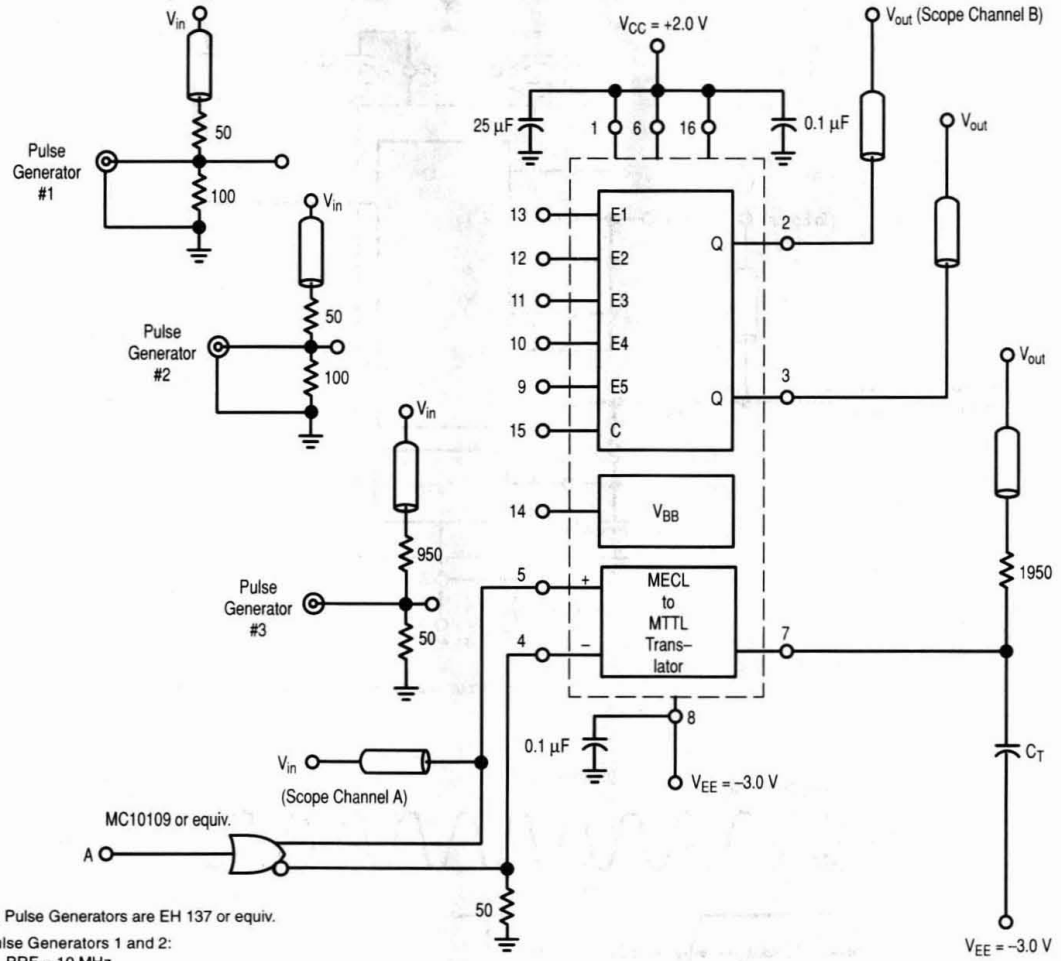


Figure 5. AC Test Circuit



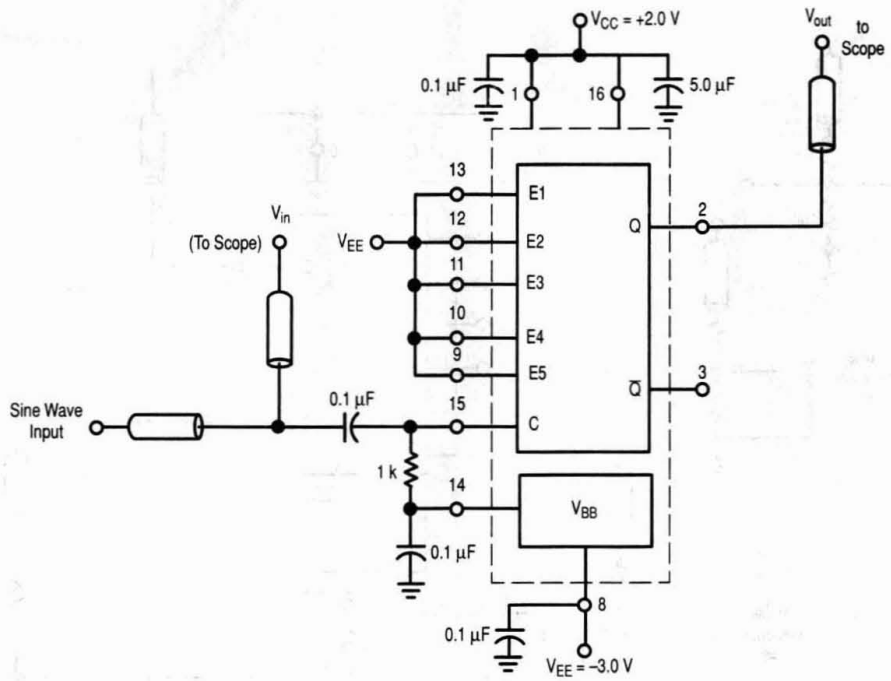
All Pulse Generators are EH 137 or equiv.

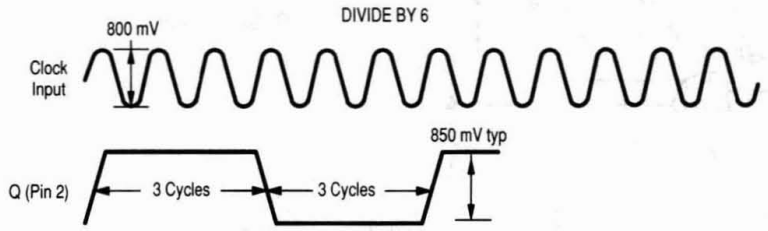
Pulse Generators 1 and 2:
PRF = 10 MHz
PW = 50% Duty Cycle
t+ = t– = 2.0 ± 0.2 ns

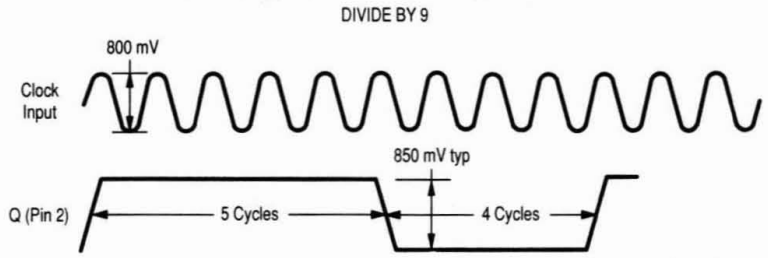
Pulse Generator 3:
PRF = 2.0 MHz
PW = 50% Duty Cycle
t+ = t– = 5.0 ± 0.5 ns

All resistors are + 1%.
All input and output cables to the scope are equal lengths of 50–ohm coaxial cable.
The 1950–ohm resistor at Pin 7 and the scope termination impedance constitute a 40 : 1 attenuator probe.
C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.
Unused output connected to a 50–ohm resistor to ground.

Figure 6. Maximum Frequency Test Circuit







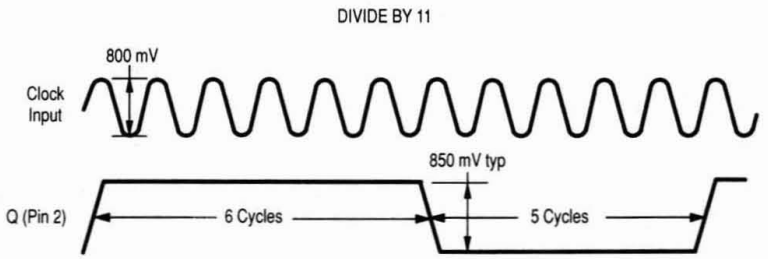


Figure 7. State Diagram

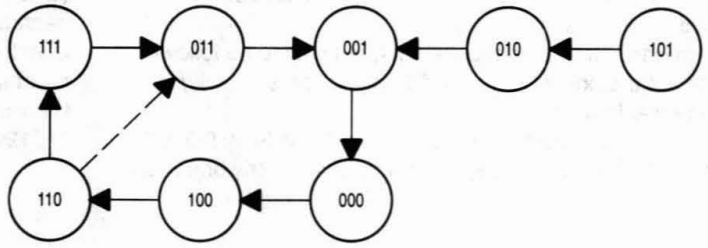
DIVIDE BY 5/6 (MC12009/MC12509)

Q1	Q2	Q3
1	1	1
0	1	1
0	0	1
0	0	0
1	0	0
1	1	0

Enable = 0

Enable = 1

— — — Enable = 1



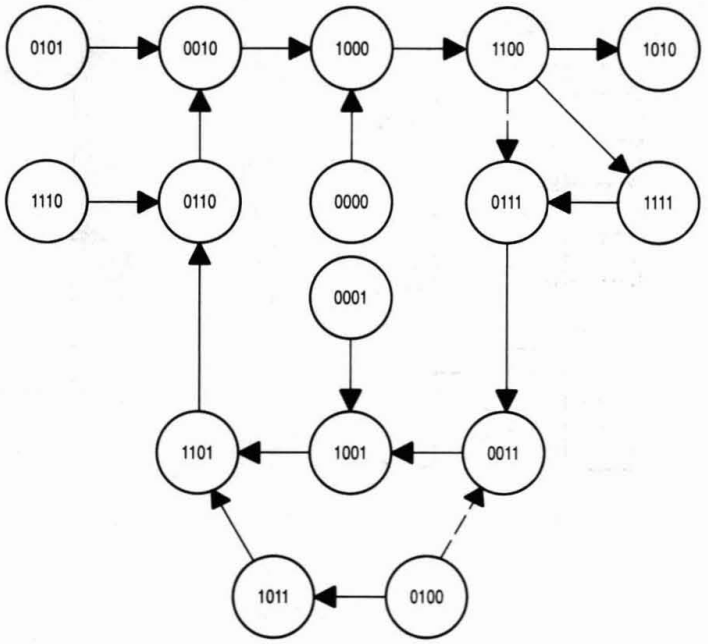
DIVIDE BY 8/9 (MC12011)

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1

— — — Enable = 1.



DIVIDE BY 10/11 (MC12013)

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

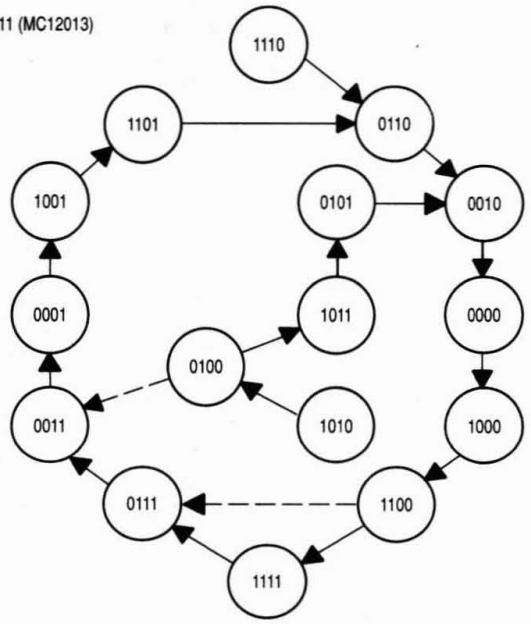
Enable = 0

Enable = 1

NOTES:

— — — Enable = 1.

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.



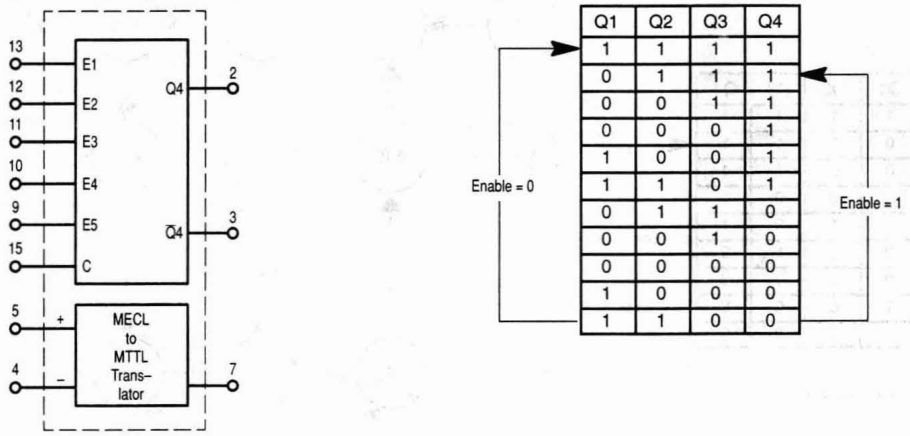
APPLICATIONS INFORMATION

The primary application of these devices is as a high–speed variable modulus prescaler in the divide by N section of a phase–locked loop synthesizer used as the local oscillator of two–way radios.

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

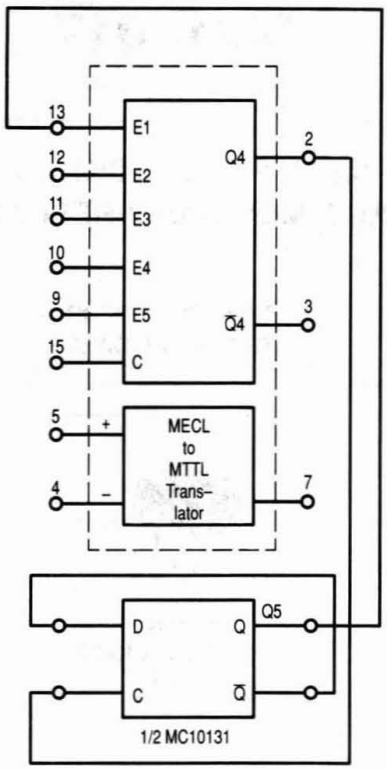
In their basic form, these devices will divide by 5/6, 8/9, or 10/11. Division by 5, 8, or 10 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 6, 9, or 11 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low). With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.) A few of the many configurations are shown below, only for the MC12013.

Figure 8. Divide By 10/11 (MC12013)



Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Figure 9. Divide By 20/21 (MC12013)



COUNT	Q1	Q2	Q3	Q4	Q4
31	1	1	1	1	1
30	0	1	1	1	1
28	0	0	1	1	1
24	0	0	0	1	1
25	1	0	0	1	1
27	1	1	0	1	1
22	0	1	1	0	1
20	0	0	1	0	1
16	0	0	0	0	1
17	1	0	0	0	1
19	1	1	0	0	1
14	0	1	1	1	0
12	0	0	1	1	0
8	0	0	0	1	0
9	1	0	0	1	0
11	1	1	0	1	0
6	0	1	1	0	0
4	0	0	1	0	0
0	0	0	0	0	0
1	1	0	0	0	0
3	1	1	0	0	0

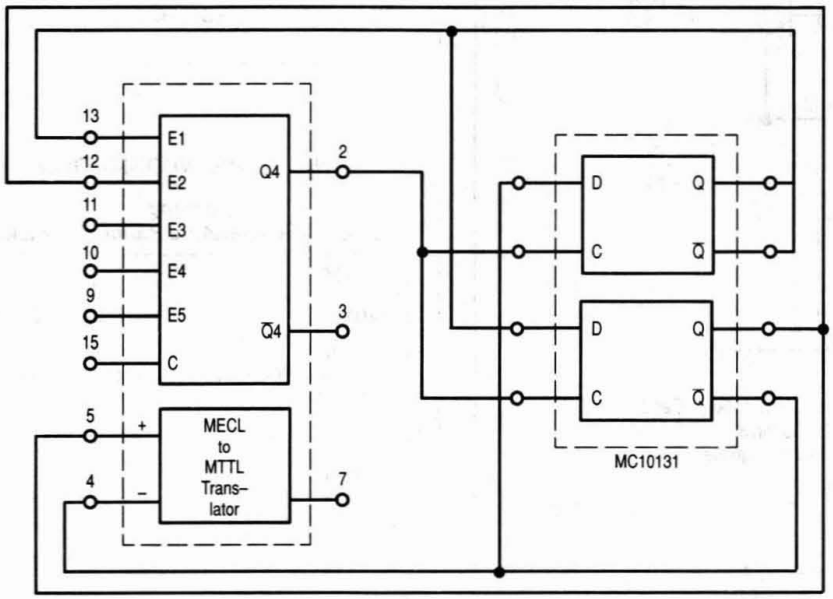
E2 + E3 + E4 + E5 = 0

E2 + E3 + E4 + E5 = 1

To obtain an MTTL output, connect Pins 5 and 4 to Pins 2 and 3 respectively. Termination resistors for the MECL outputs are not shown, but are required except for the flip–flop driving the translator section.

The ÷ 20/21 counter may also be built using an MTTL flip–flop by connecting Pins 5 and 4 to Pins 2 and 3 respectively, and driving the MTTL flip–flop with Pin 7. MC12013 inputs E4 and E5 are used rather than E1. With E1 + E2 + E3 = 0, operation remains as shown.

Figure 10. Divide By 40/41 (MC12013)



For ÷ 40 : E4 + E5 = 1
For ÷ 41 : E4 + E5 = 0

Termination resistors for MECL outputs are not shown, but are required except for the flip–flop driving the translator section.

MOTOROLA

MC12015
MC12016
MC12017

Dual Modulus Prescaler

MECL PLL COMPONENTS
DUAL MODULUS PRESCALER

SEMICONDUCTOR
TECHNICAL DATA

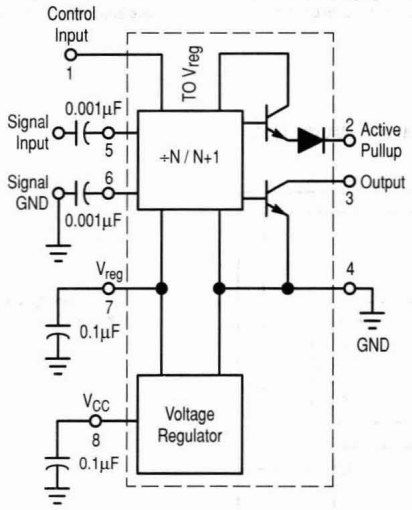
The MC12015, MC12016 and MC12017 are dual modulus prescalers which will drive divide by 32 and 33, 40 and 41, and 64 and 65, respectively. An internal regulator is provided to allow these devices to be used over a wide range of power–supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc ±10% at Pin 7, or by applying an unregulated voltage source from 5.5Vdc to 9.5 Vdc to Pin 8.

- 225 MHz Toggle Frequency
- Low–Power 7.5 mA Maximum at 6.8 V
- Control Input and Output Are Compatible With Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

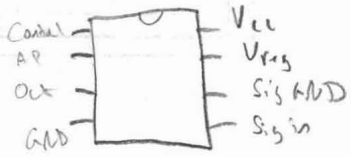
SIMPLIFIED BLOCK DIAGRAM



1. V_{reg} at Pin 7 is not guaranteed to be between 4.5 and 5.5V when V_{CC} is being applied to Pin 8
2. Pin 7 is not to be used as a source of regulated output voltage

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12015D	T_A = –40° to +85°C	SO–8
MC12016D		
MC12017D		
MC12015P		Plastic
MC12016P		
MC12017P		



MAXIMUM RATINGS [tblhead]

Rating	Symbol	Value	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5 V; V_{reg} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input) 	 f_{max} f_{min}	 225 –	 – –	 – 35	MHz
Supply Current	I_{CC}	–	6.0	7.8	mA
Control Input HIGH (÷32, 40 or 64)	V_{IH}	2.0	–	–	V
Control Input LOW (÷33, 41 or 65)	V_{IL}	–	–	0.8	V
Output Voltage HIGH (I_{source} = 50μA) [Nofe 1]	V_{OH}	2.5	–	–	V
Output Voltage LOW (I_{sink} = 2mA) [Note 1]	V_{OL}	–	–	0.5	V
Input Voltage Sensitivity 35 MHz 50 to 225 MHz	V_{in}	 400 200	 – –	 800 800	mVpp
PLL Response Time [Notes 2 and 3]	t_{PLL}	–	–	t_{out} to 70	ns

NOTES: 1. Pin 2 connected to Pin 3.
2. t_{PLL} = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
3. t_{out} = period of output waveform.

MOTOROLA

MC12018

520 MHz Dual Modulus Prescaler

The MC12018 is a dual modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc ±10% at Pin 7, or by applying an unregulated voltage source from 5.5 Vdc to 9.5 Vdc to Pin 8.

- 520 MHz Toggle Frequency
- Low–Power 8.0 mA Typical
- Control Input Is Compatible With Standard CMOS and TTL
- Supply Voltage 4.5 V to 9.5 V
- On–Chip 10 kΩ Resistor from Positive Edge to Ground

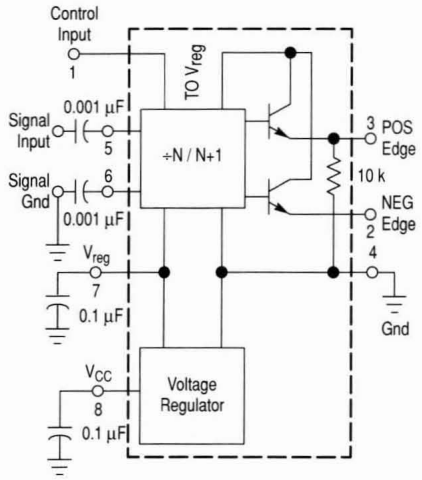
MECL PLL COMPONENTS
÷128/129 DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

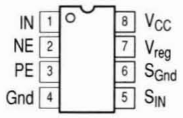
P SUFFIX
PLASTIC PACKAGE
CASE 626

SIMPLIFIED BLOCK DIAGRAM



1. V_{reg} at Pin 7 is not guaranteed to be between 4.5 and 5.5 V when V_{CC} is being applied to Pin 8
2. Pin 7 is not to be used as a source of regulated output voltage
3. 10 kΩ pulldown recommended with negative edge output (Pin 2)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12018D	T_A = – 40° to +85°C	SO–8
MC12018P		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

NOTE; ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5 V; V_{reg} = 4.5 to 5.5 V; T_A = –40 to 85°C), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input) f_{max} f_{min}		520 –	– –	– 75	MHz
Supply Current	I_{CC}	–	8.0	10.7	mA
Control Input HIGH (÷128)	V_{IH}	2.0	–	–	V
Control Input LOW (÷129)	V_{IL}	–	–	0.8	V
Differntial Output Voltage (I_{source} = –200μA)	V_{out}	0.8	1.0	–	V
Input Voltage Sensitivity 75MHz 125–520MHz	V_{in}	 400 200	 – –	 800 800	mV_{PP}
PLL Response Time (Notes 1 and 2)	t_{PLL}	–	–	t_{out}–50	ns

NOTES: 1. t_{PLL} = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

MOTOROLA

MC12019

Dual Modulus Prescaler

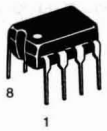
The MC12019 is a divide by 20 and 21 dual modulus prescaler. It will divide by 20 when the modulus control input is HIGH and divide by 21 when the modulus control input is LOW.

- 225 MHz Toggle Frequency
- Low-Power 7.5 mA Maximum at 5.5 V
- Control Input is Compatible with Standard Motorola CMOS Synthesizers
- Emitter Follower Output

MECL PLL COMPONENTS
÷20/21 DUAL MODULUS PRESCALER

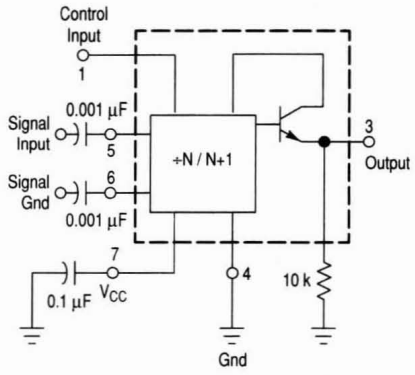
SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

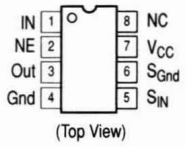


P SUFFIX
PLASTIC PACKAGE
CASE 626

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12019D	T_A = – 40° to +85°C	SO–8
MC12019P		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 7	V_{CC}	8.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

NOTE; ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max} f_{min}	225 –	– –	– 20	MHz
Supply Current	I_{CC}	–	–	7.5	mA
Control Input HIGH (÷20)	V_{IH}	2.0	–	–	V
Control Input LOW (÷21)	V_{IL}	–	–	0.8	V
Output Swing Voltage (10 kΩ to ground)	V_{out}	600	–	1200	mVpp
Input Voltage Sensitivity 20 MHz to 225 MHz	V_{in}	200	–	800	mV_{PP}
PLL Response Time (Notes 1 and 2)	t_{PLL}	–	–	t_{out}–70	ns

NOTES: 1. t_{PLL} = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

MOTOROLA

MC12022A
MC12022B

Consider MC12052A for New Designs

1.1GHz Dual Modulus Prescaler

MECL PLL COMPONENTS
÷64/65, ÷128/129
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12022A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

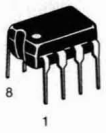
The MC12022B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low–Power 7.5 mA Typical
- Operating Temperature Range of –40 to +85°C
- Short Setup Time (t_{set}) 16ns Maximum @ 1.1 GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL. Maximum Input Voltage Should Be Limited to 6.5 Vdc

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626

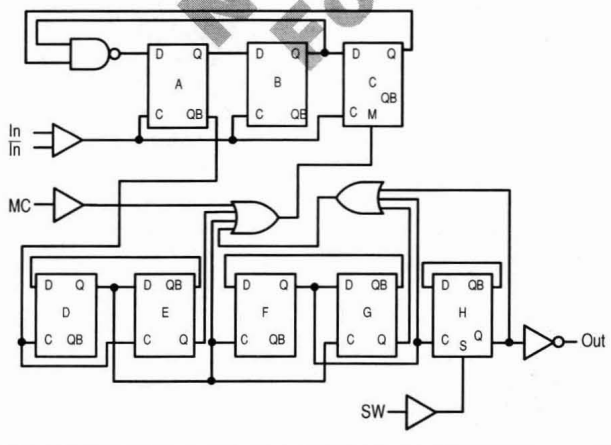
FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

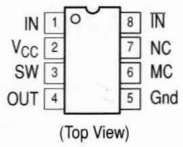
NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

Not Recommended For New Designs

Figure 1. Logic Diagram (MC12022A)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12022AD	T_A = – 40° to +85°C	SO–8
MC12022AP		Plastic
MC12022BD		SO–8
MC12022BP		Plastic

MAXIMUM RATINGS

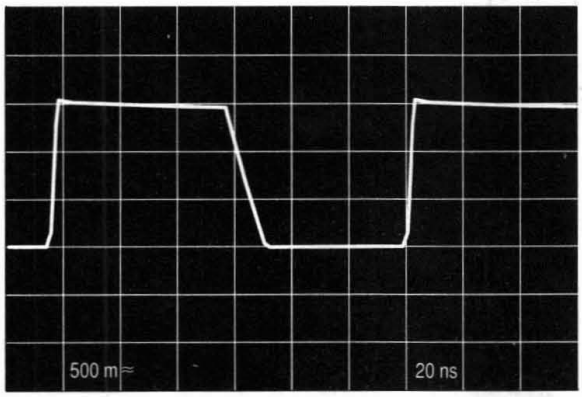
Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to + 7.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE; ESD data available upon request.

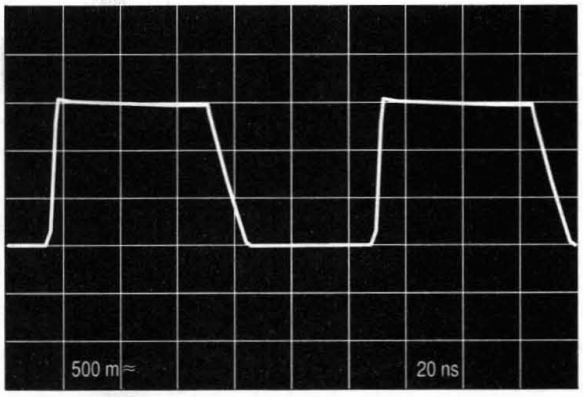
ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40°C to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.6	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	7.5	10	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (C_L = 12 pF; R_L = 2.2 kΩ)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1500 1500	mVpp
Output Current (C_L = 12 pF; R_L = 2.2 kΩ)	I_O	–	1.5	4.0	mA

Figure 2. Typical Output Waveforms

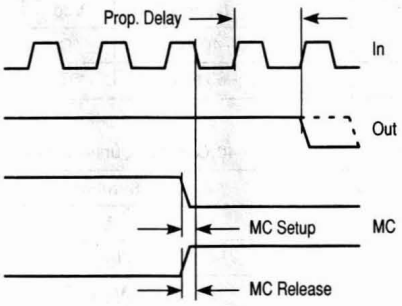


(÷64, 500MHz Input Frequency, V_{CC} = 5.0V, T_A = 25°C, Output Loaded)



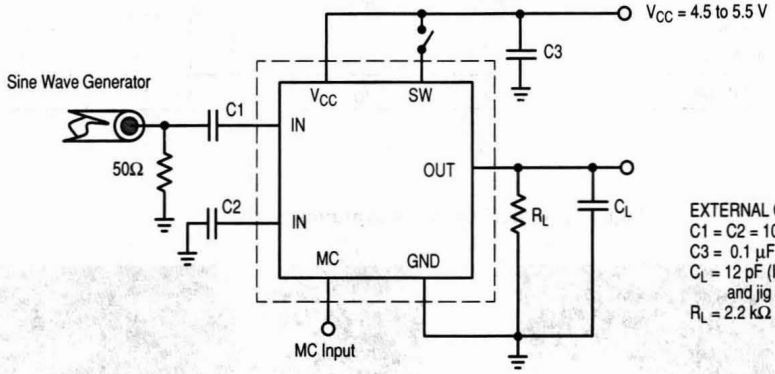
(÷128, 1.1GHz Input Frequency, V_{CC} = 5.0V, T_A = 25°C, Output Loaded)

Figure 3. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 4. AC Test Circuit



EXTERNAL COMPONETS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 12 pF (Including Scope and jig capacitance)
R_L = 2.2 kΩ

Figure 5. Input Signal Amplitude versus Input Frequency
Divide Ratio = 8; V_{CC} = 5.0V; T_A = 25°C

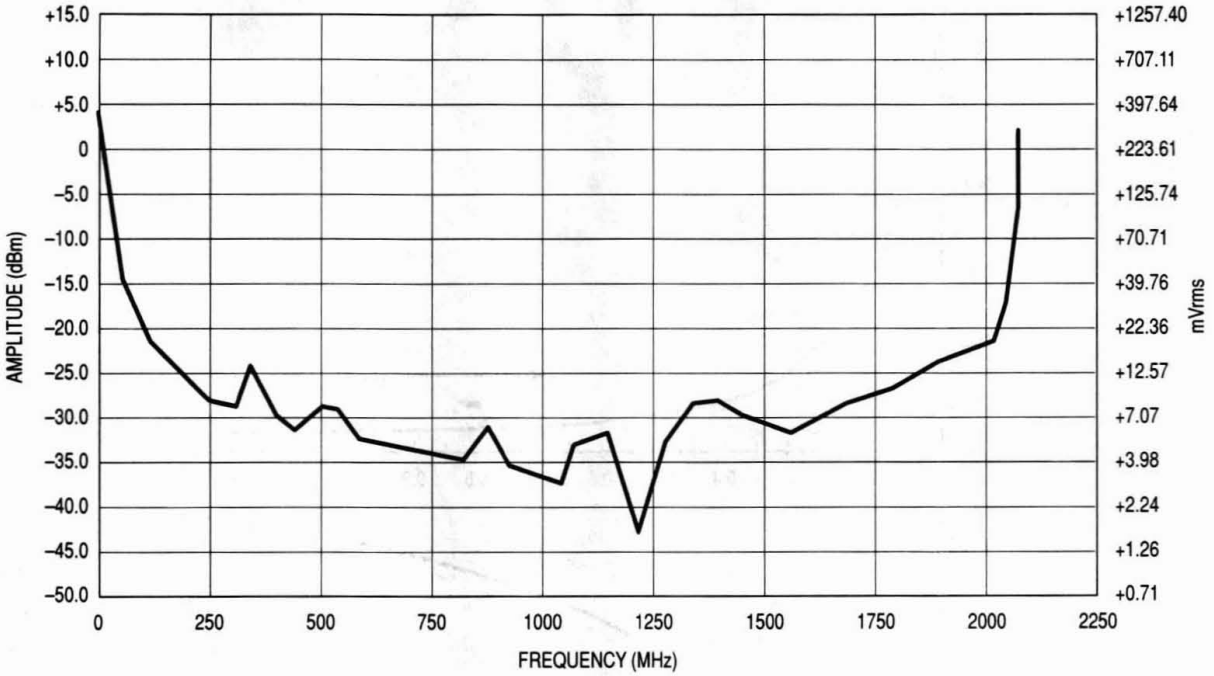


Figure 6. Output Amplitude versus Input Frequency

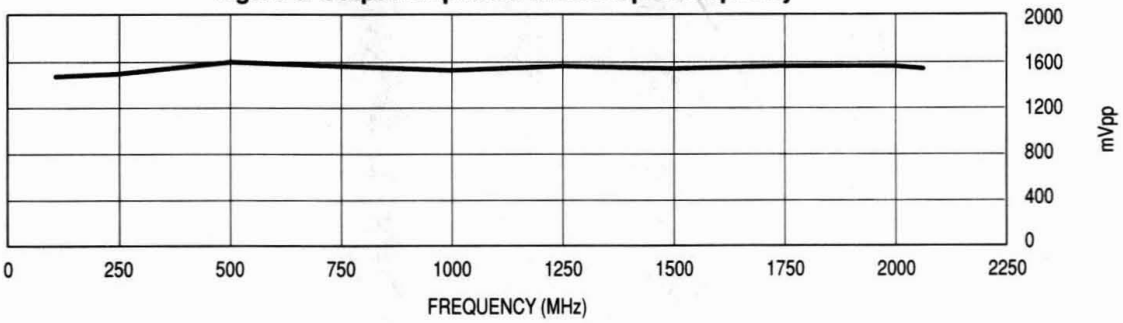
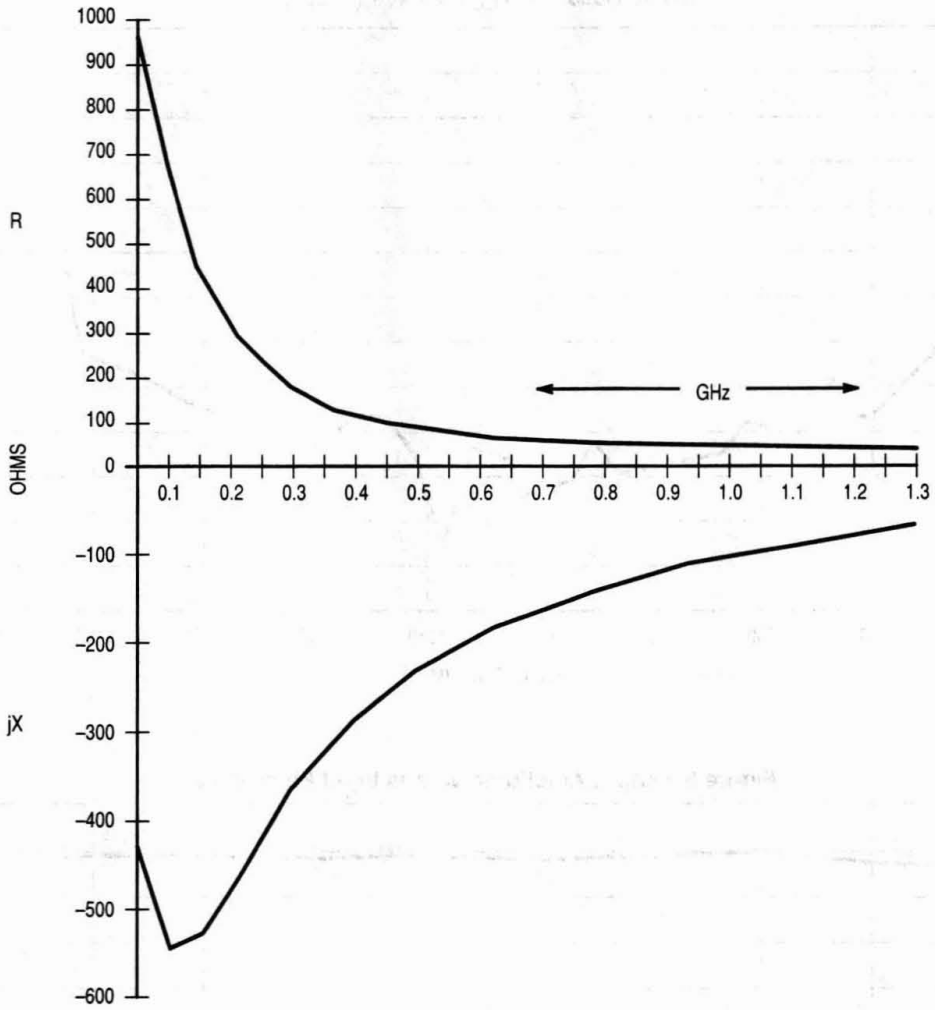


Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

1.1 GHz Low-Voltage Dual Modulus Prescaler

MC12022LVA MC12022LVB

MECL PLL COMPONENTS ÷64/65, ÷128/129 DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12022LVA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12022LVB can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

NOTE: The "B" Version Is Not Recommended for New Designs

- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.0 V
- Low–Power 4.0 mA Typical at V_{CC} = 2.7 V
- Operating Temperature Range of –40 to 85°C
- Short Setup Time (t_{set}) 16ns Maximum @ 1.1 GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

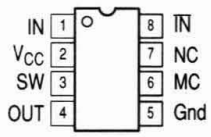
NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grouunding this pin, but this is not recommended due to increased power soncumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

NOTE: * Equivalent to a two–input NAND gate

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12022LVAD	T_A = – 40° to +85°C	SO–8
MC12022LVAP		Plastic
MC12022LVBD		SO–8
MC12022LVBP		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE; ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40°C to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	4.7	6.5	mA
Supply Current Output Unloaded (Pin 2) at 5.0 Vdc	I_{CCH}		5.8	8.0	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (C_L = 12 pF; R_L = 1.1 kΩ at 2.7 Vdc)	V_{out}	0.8	1.0	–	V_{pp}
Output Voltage Swing (C_L = 12 pF; R_L = 2.2 kΩ at 5.0 Vdc)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	$V_{in(min)}$	100 400	– –	1500 1500	mVpp
Output Current (C_L = 12 pF; R_L = 2.2 kΩ at 2.7 Vdc)	I_O	–	1.2	4.0	mA
Output Current (C_L = 12 pF; R_L = 2.2 kΩ at 5.0 Vdc)	I_O	–	1.2	4.0	mA

Figure 1. Logic Diagram (MC12022LVA)

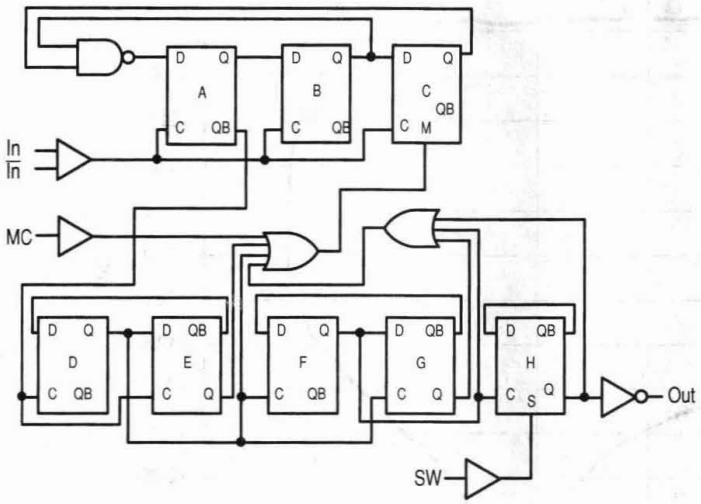
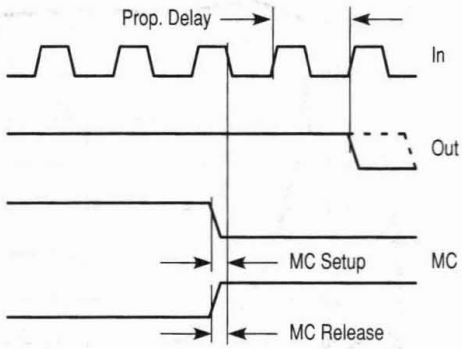
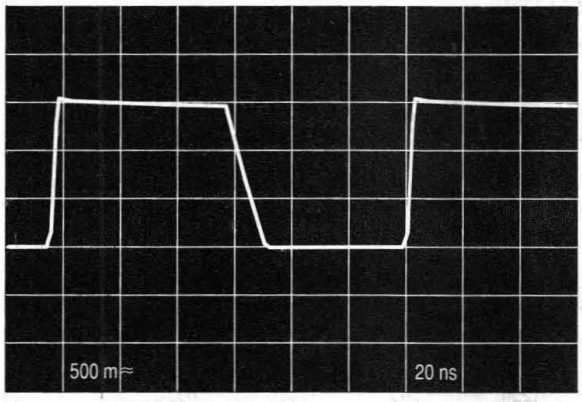


Figure 2. Modulus Setup Time

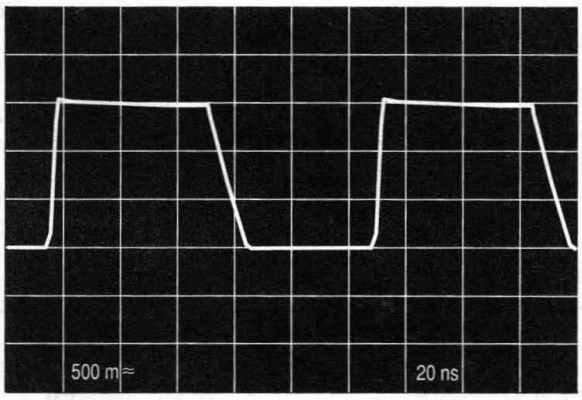


Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. Typical Output Waveforms

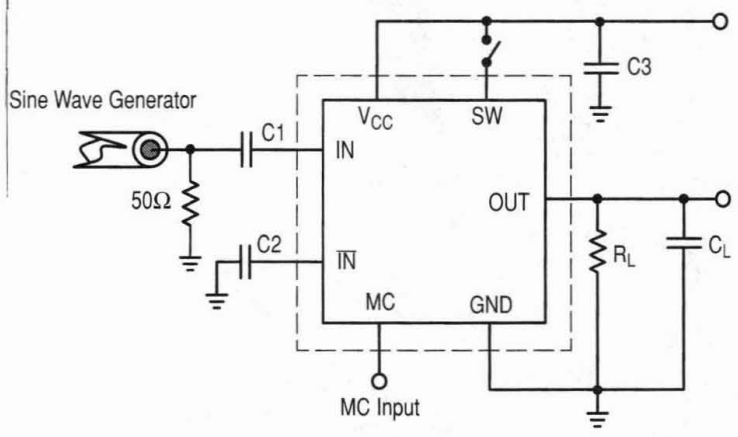


(÷64, 500MHz Input Frequency, V_{CC} = 5.0V, T_A = 25°C, Output Loaded)



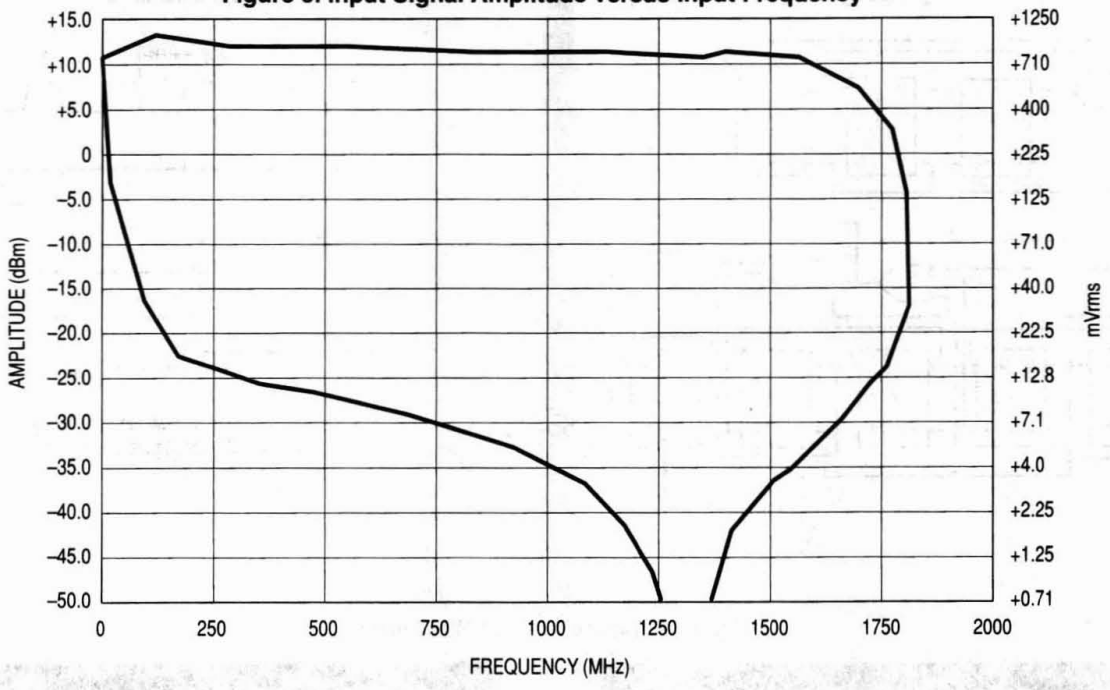
(÷128, 1.1GHz Input Frequency, V_{CC} = 5.0V, T_A = 25°C, Output Loaded)

Figure 4. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000pF
C3 = 0.1μF
C_L = 12pF (Including Scope and jig capacitance)
R_L = 2.2kΩ (at +5.0Vdc)
R_L = 1.1kΩ (at +2.7Vdc)

Figure 5. Input Signal Amplitude versus Input Frequency



Divide Ratio = 128; V_{CC} = 5.0 V; T_A = 25°C

Figure 6. Output Amplitude versus Input Frequency

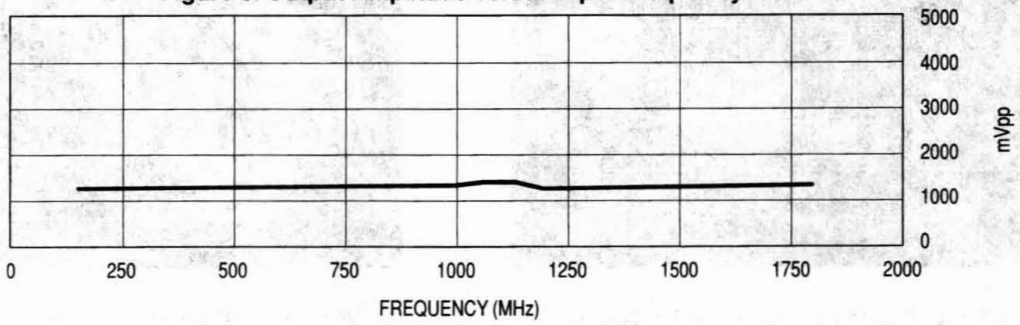
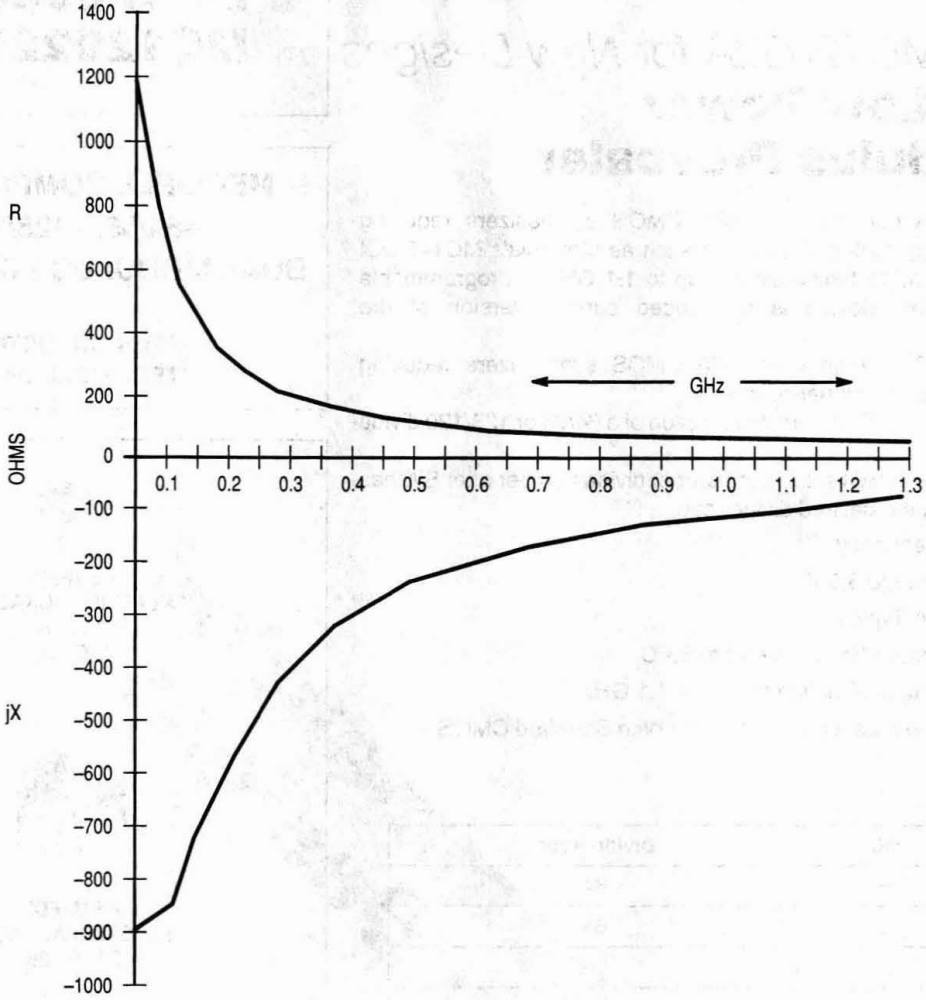


Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

Consider MC12052A for New Designs

1.1 GHz Low Power Dual Modulus Prescaler

The MC12022SLA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps. This device is a reduced current version of the MC12022A/B.

The MC12022SLB can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low–Power 4.0 mA Typical
- Operating Temperature Range of –40 to 85°C
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grouunding this pin, but this is not recommended due to increased power soncumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

NOTE: * Equivalent to a two–input NAND gate

Not Recommended For New Designs

MC12022SLA
MC12022SLB

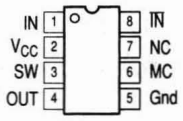
MECL PLL COMPONENTS
÷64/65, ÷128/129
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

P SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12022SLAD	T_A = – 40° to +85°C	SO–8
MC12022SLAP		Plastic
MC12022SLBD		SO–8
MC12022SLBP		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE; ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40°C to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2) at 5.0 Vdc	I_{CC}	–	3.8	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} – 0.5V	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (C_L = 8.0 pF; R_L = 14.4 kΩ)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	$V_{in(min)}$	100 400	– –	1500 1500	mVpp
Output Current (C_L = 8.0 pF; R_L = 4.4 kΩ, V_{CC} = 5.0 V)	I_O	–	.75	4.0	mA

Figure 1. Logic Diagram (MC12022SLA)

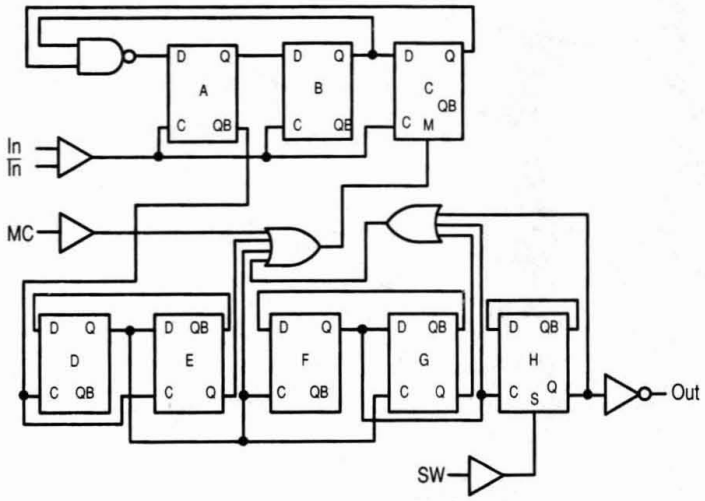
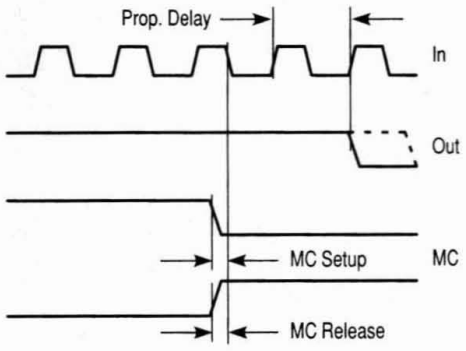
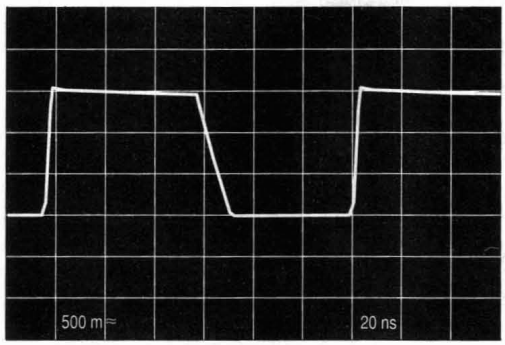


Figure 2. Modulus Setup Time

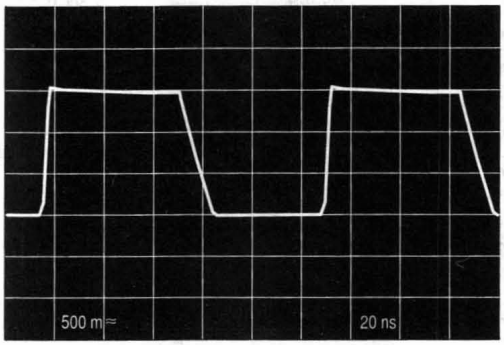


Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. Typical Output Waveforms

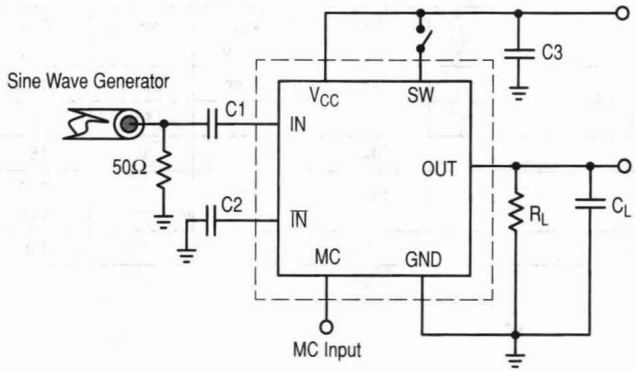


(÷64, 500MHz Input Frequency, V_{CC} = 5.0V, T_A = 25°C, Output Loaded)



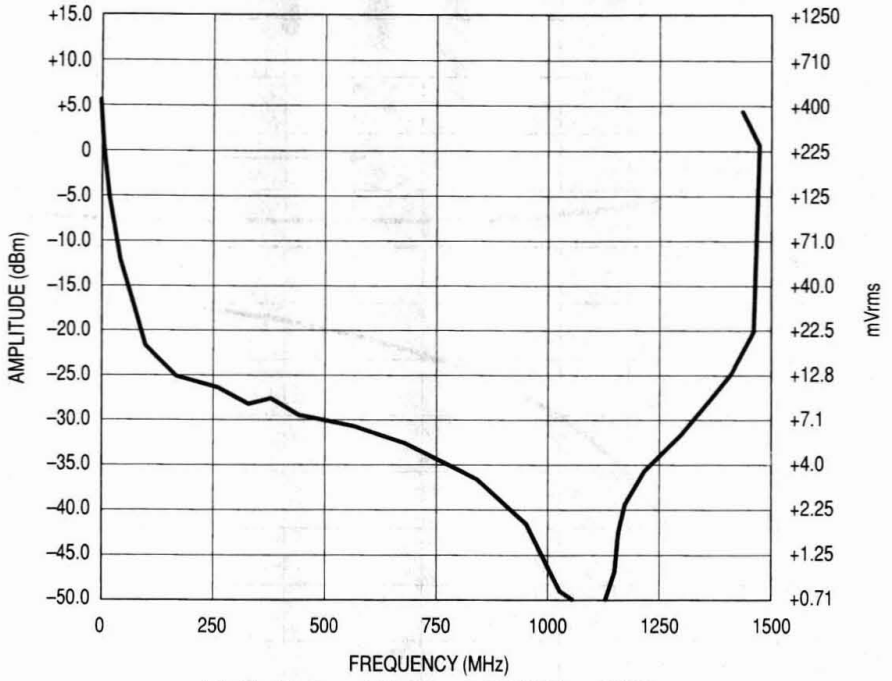
(÷128, 1.1GHz Input Frequency, V_{CC} = 5.0V, T_A = 25°C, Output Loaded)

Figure 4. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and jig capacitance)
R_L = 4.4 kΩ (at 5.0 Vdc)

Figure 5. Input Signal Amplitude versus Input Frequency



Divide Ratio = 128; V_{CC} = 5.0V; T_A = 25°C

Figure 6. Output Amplitude versus Input Frequency

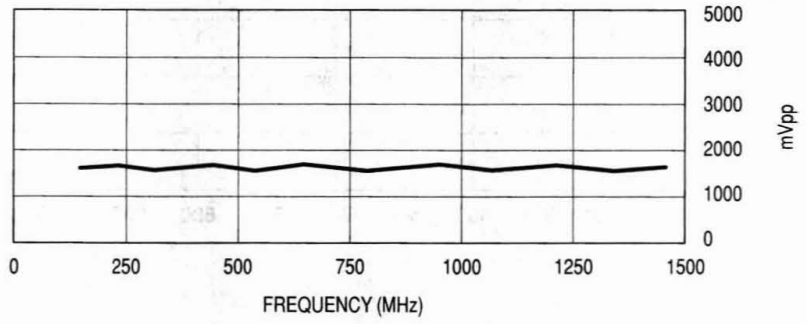
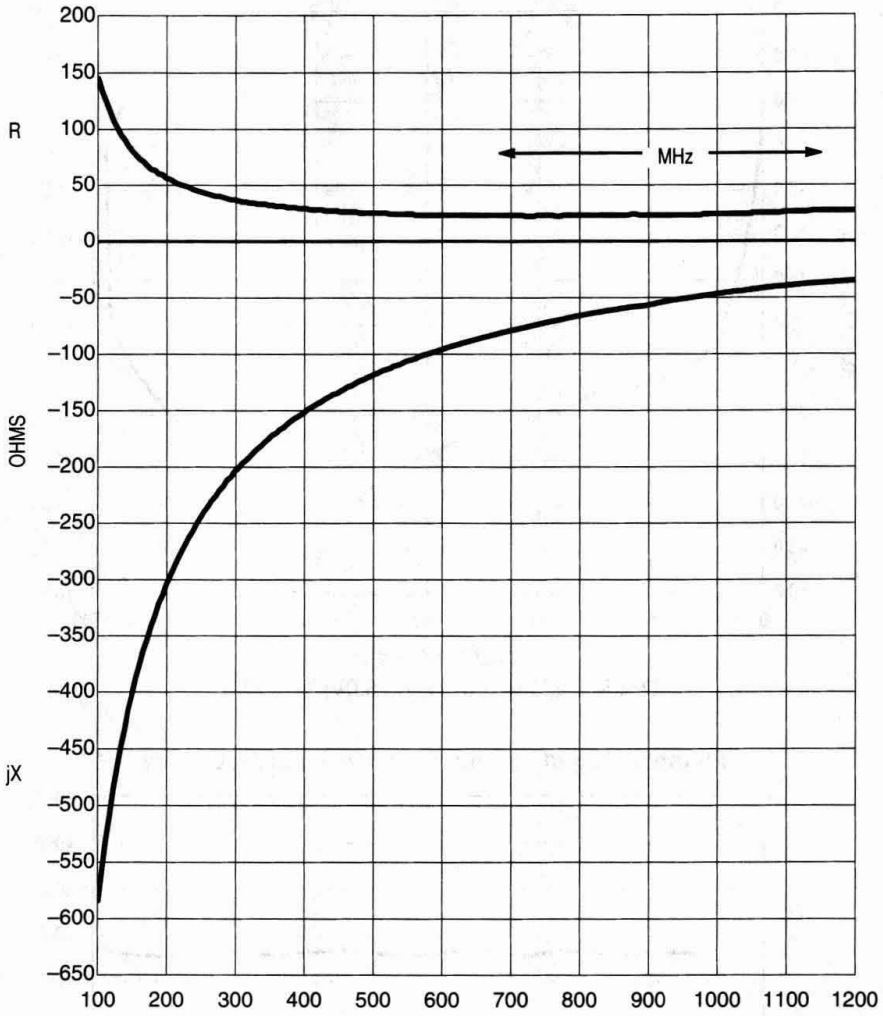


Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12023

225 MHz Prescaler

The MC12023 is a prescaler which will divide by 64. This device may be operated over a supply voltage range of 3.2 to 5.5 V.

- 225 MHz Toggle Frequency
- Low-Power 4.8 mA Maximum at 5.5 V
- Operating Supply Voltage of 3.2 to 5.5 V
- Connecting Pins 2 and 3 Allows Driving One TTL Load

MECL PLL COMPONENTS
÷64 PRESCALER

SEMICONDUCTOR
TECHNICAL DATA

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	0 to 8.0	Vdc
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	–65 to 175	°C

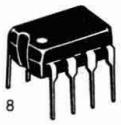
NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.2 to 5.5V; T_A = 0 to +70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input) 35 MHz 50–225 MHz	f_{max} f_{min}	225 –	– –	– 35	MHz
Supply Current at 5.5 V	I_{CC}	–	3.50[3]	4.8	mA
Output Voltage HIGH[1] (V_{CC} = 3.2 V)[2]	V_{OH}	1.2	1.4	–	V
Output Voltage HIGH[1] (V_{CC} = 5.0 V)[2]	V_{OH}	2.5	–	–	V
Output Voltage LOW[1] (I_{sink} = 2.0 mA)	V_{OL}	–	–	0.5	V
Input Voltage Sensitivity 35 MHz 50–225 MHz	V_{in}	 400 200	 – –	 800 800	mV_{PP}

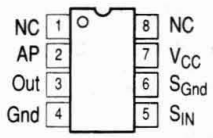
NOTES: 1. Pin 2 connected to Pin 3
2. I_{source} = 50 µA
3. V_{CC} = 4.5 V

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



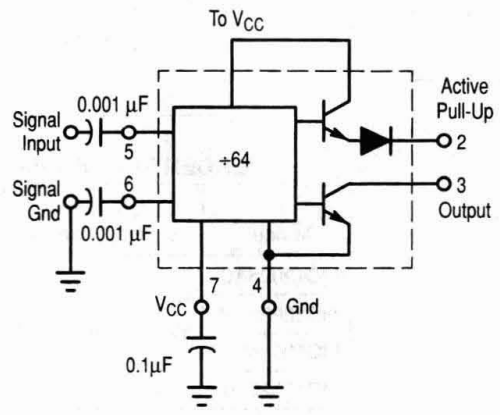
P SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



(Top View)

Figure 1. Prescaler Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12023D	T_A = 0° to 70°C	SO–8
MC12023P		Plastic

MOTOROLA

1.1 GHz Dual Modulus Prescaler

MC12026A
MC12026B

MECL PLL COMPONENTS
÷8/9, ÷16/17
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12026 is a high frequency, low voltage dual modulus prescaler used in phase–locked loop (PLL) applications.

The MC12026A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12026B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

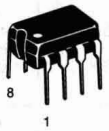
A Divide Ratio Control (SW) permits selection of an 8/9 or 16/17 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

NOTE: The "B" Version Is Not Recommended for New Designs

- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 4.0 mA Typical
- Operating Temperature Range of –40 to 85°C
- The MC12026 is Pin Compatible With the MC12022
- Short Setup Time (t_{set}) 6ns Typical @ 1.1 GHz
- Modulus Control Input Level is Compatible With Standard CMOS and TTL

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



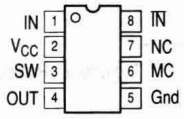
P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	8
H	L	9
L	H	16
L	L	17

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grouunding this pin, but this is not recommended due to increased power soncumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Characteristics	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc
Maximum Output Current, Pin 4	I_O	10.0	mA

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12026AD	T_A =–40° to +85°C	SO–8
MC12026AP		Plastic
MC12026BD		SO–8
MC120226BP		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sin Wave)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	4.0	5.3	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	GND	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	–
Output Voltage Swing (R_L = 560 Ω; I_O = 5.5 mA)[1] (R_L = 1.1 kΩ; I_O = 2.9 mA)[2]	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out[3]	t_{SET}	–	6	9	ns
Input Voltage Sensitivity 100–25 0MHz 250–1100 MHz	V_{in}	 400 100	 – –	 1000 1000	mVpp

notes: 1. Divide Ratio of ÷8/9 at 1.1 GHz, C_L = 8.0 pF
2. Divide Ratio of ÷16/17 at 1.1 GHz, C_L = 8.0 pF
3. Assuming R_L = 560 Ω at 1.1 GHz

Figure 1. Logic Diagram (MC12026A)

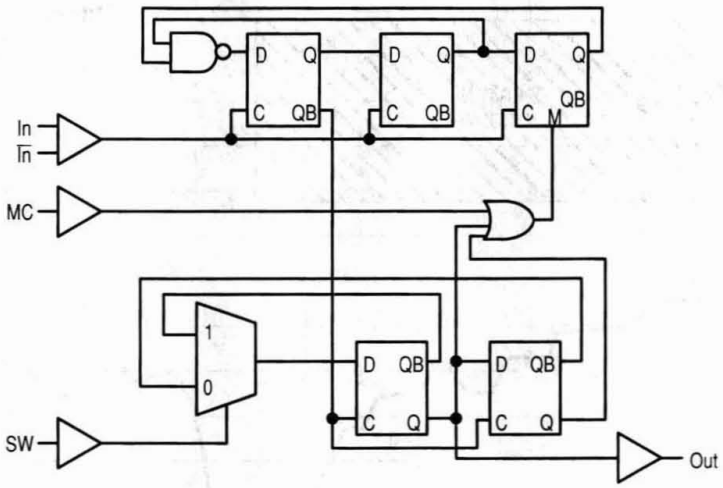
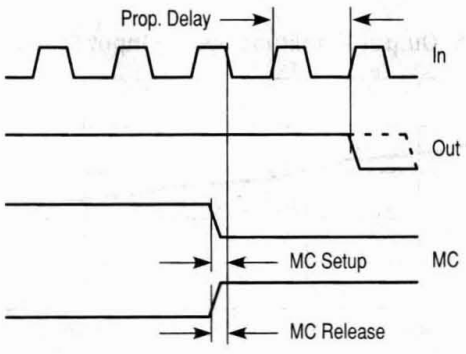


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit

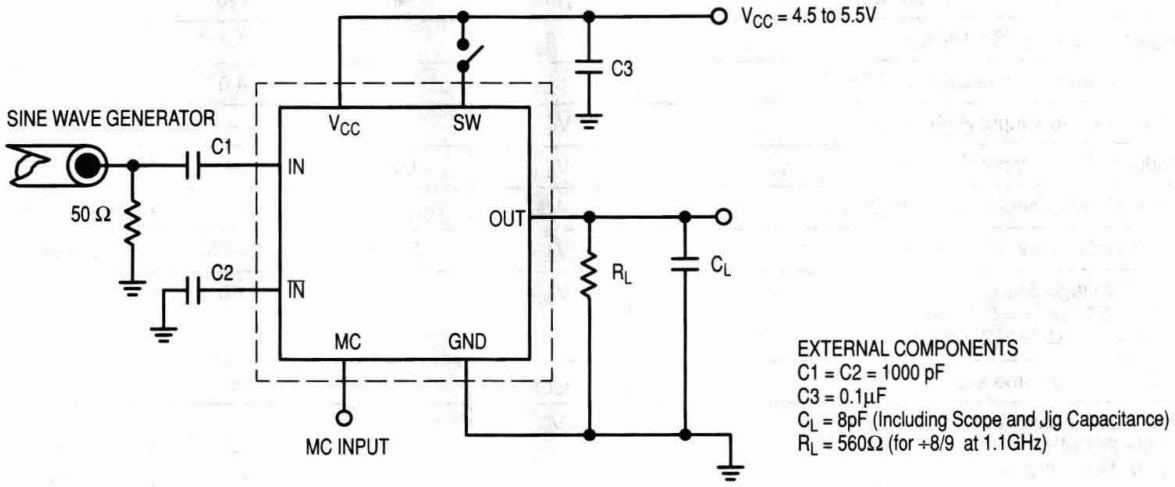
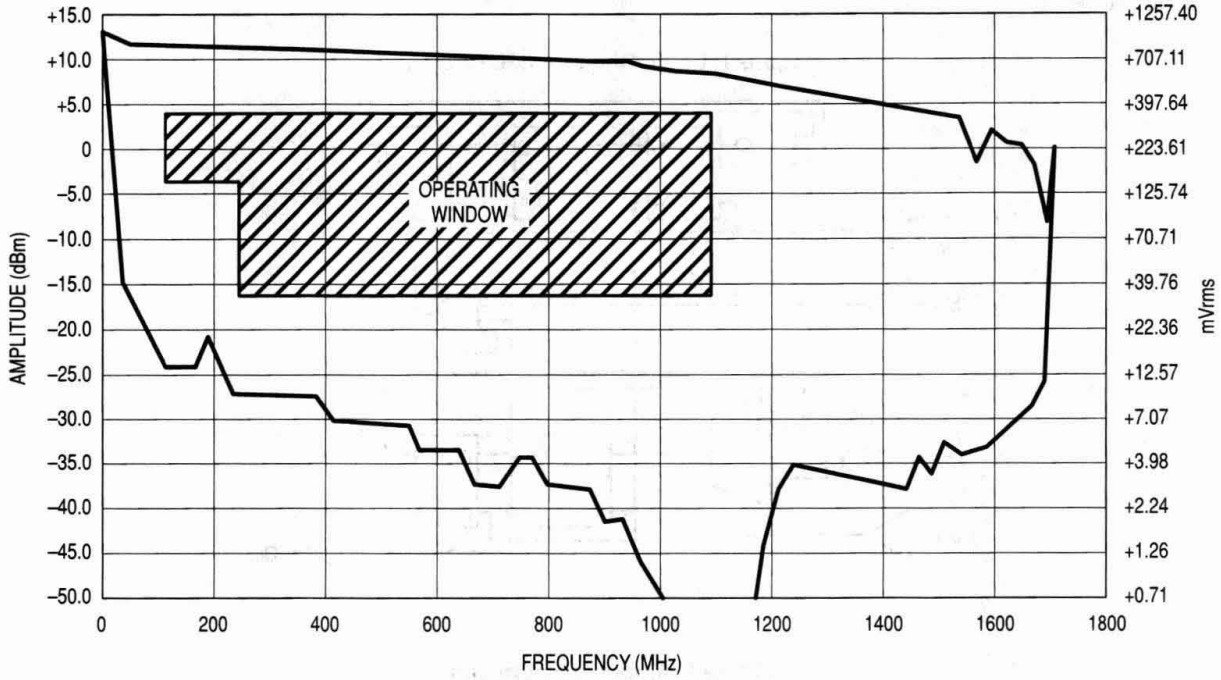


Figure 4. Input Signal Amplitude versus Input Frequency



Divide Ratio = 8; V_{CC} = 5.0 V; T_A = 25°C

Figure 5. Output Amplitude versus Input Frequency

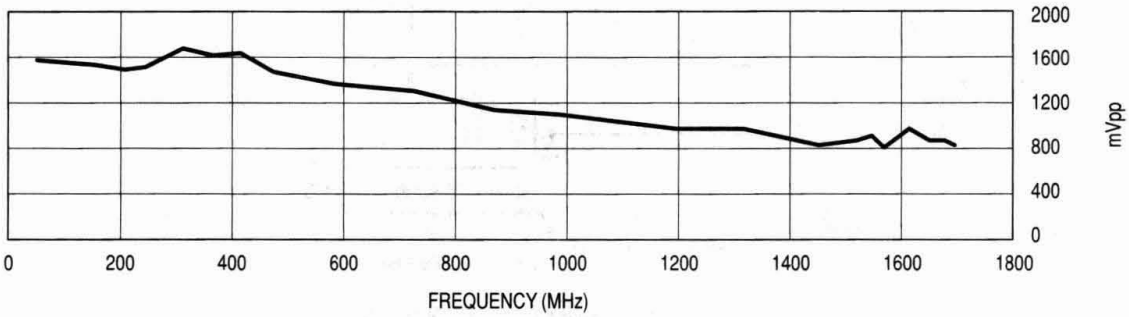
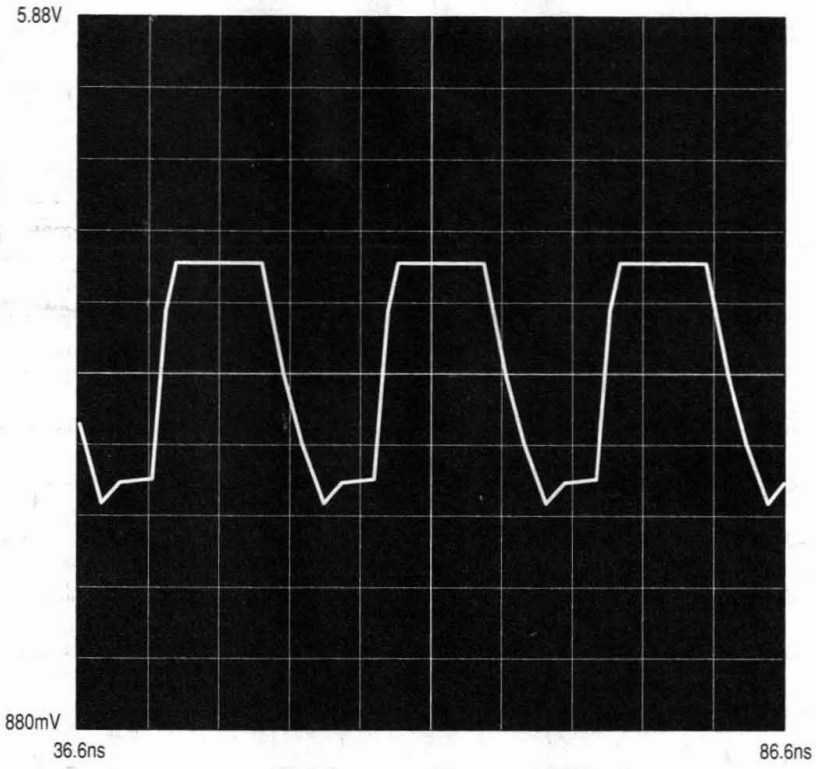
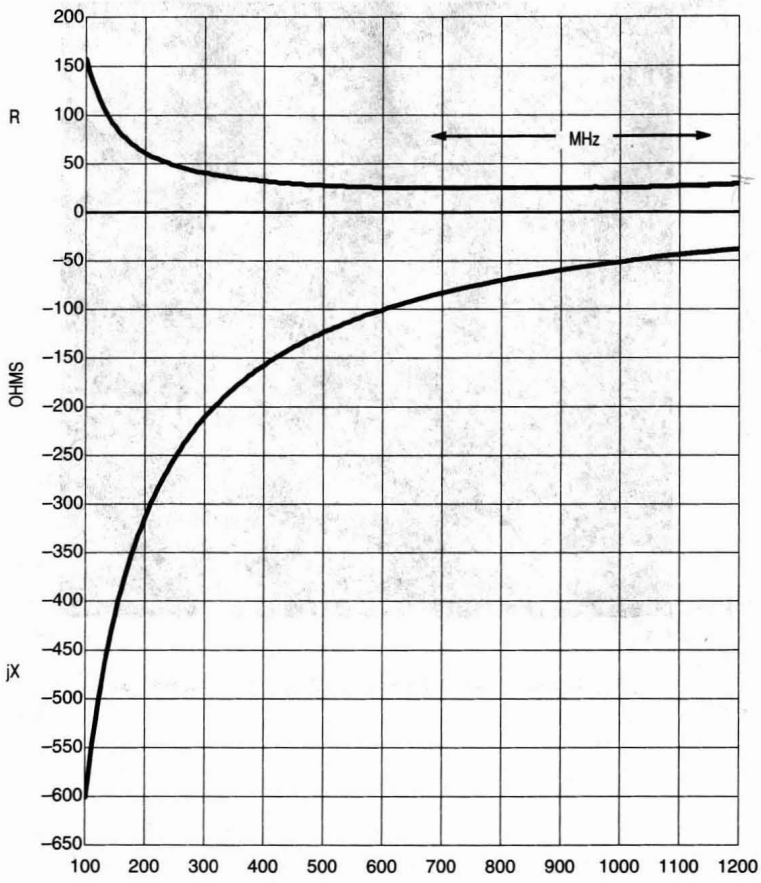


Figure 6. Typical Output Waveform



(÷8, 1.1 GHz Input Frequency, V_{CC} = 5.0, T_A = 25°C, Output Loaded With 8.0pF)

Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

1.1 GHz Dual Modulus Prescaler

MC12028A
MC12028B

MECL PLL COMPONENTS
÷64/65, ÷128/129
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12028A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12028B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

NOTE: The "B" Version Is Not Recommended for New Designs

- 1.1 GHz Toggle Frequency
- MC12028A for Positive Edge Triggered Synthesizers
- 6.5 mA Maximum, –40 to 85°C, V_{CC} = 5.5 Vdc
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Low–Power 4.0 mA Typical

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grouunding this pin, but this is not recommended due to increased power soncumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

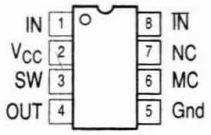
NOTE: * Equivalent to a two–input NAND gate

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12028AD	T_A = –40° to +85°C	SO–8
MC12028AP		Plastic
MC12028BD		SO–8
MC120228BP		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	4.0	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	—
Output Voltage Swing (C_L = 12 pF; R_L = 2.2 kΩ)	V_{out}	1.0	1.6		V_{pp}
Modulus Setup Time MC to Out	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1500 1500	mVpp
Output Current (C_L = 12 pF; R_L = 2.2 kΩ)	I_O	–	1.5	4.0	mA

Figure 1. Logic Diagram (MC12028A)

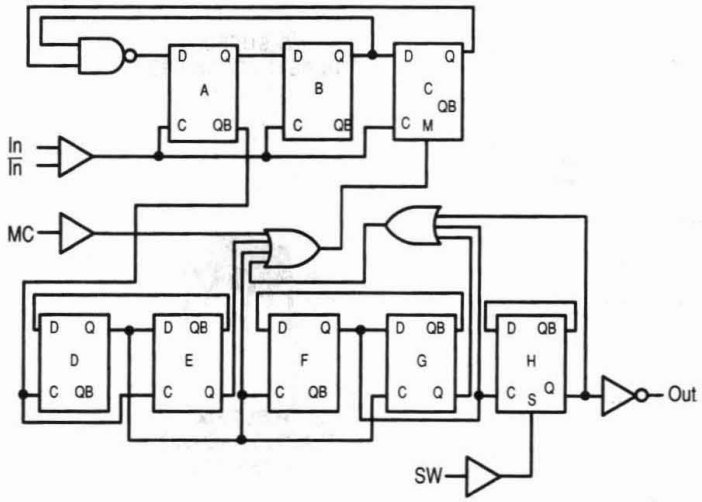
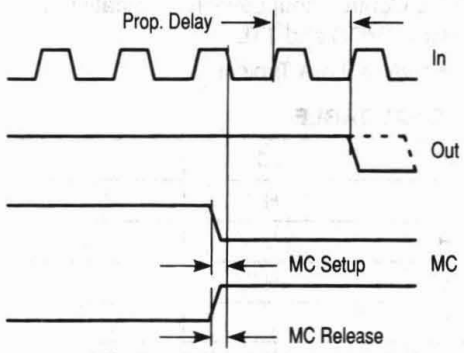


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. Typical Output Waveform

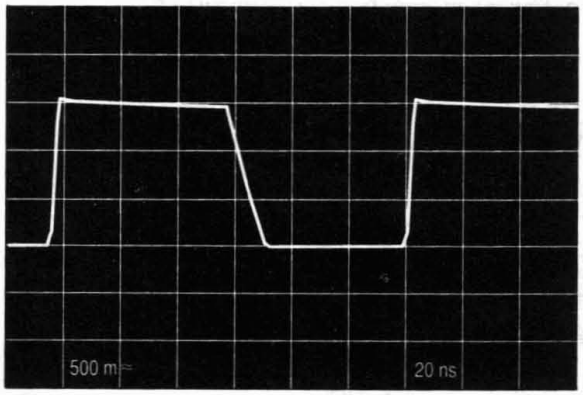


Figure 4. AC Test Circuit

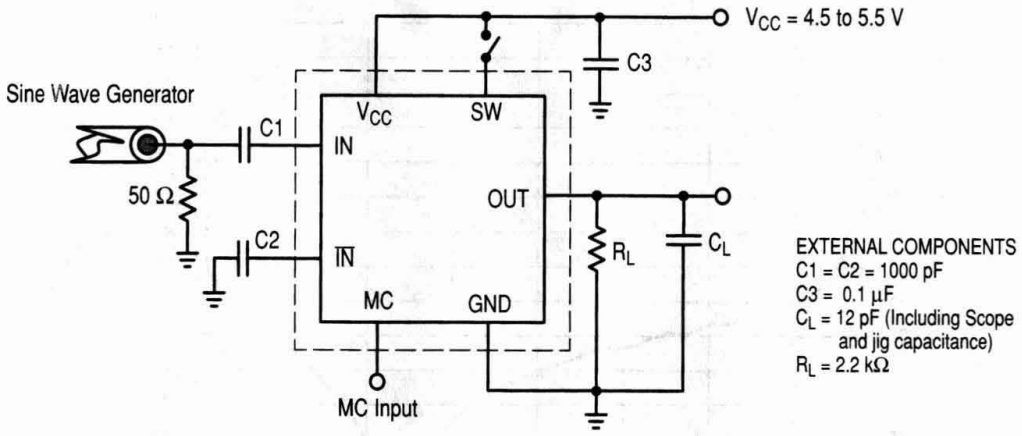


Figure 5. Typical Input Impedance versus Input Frequency

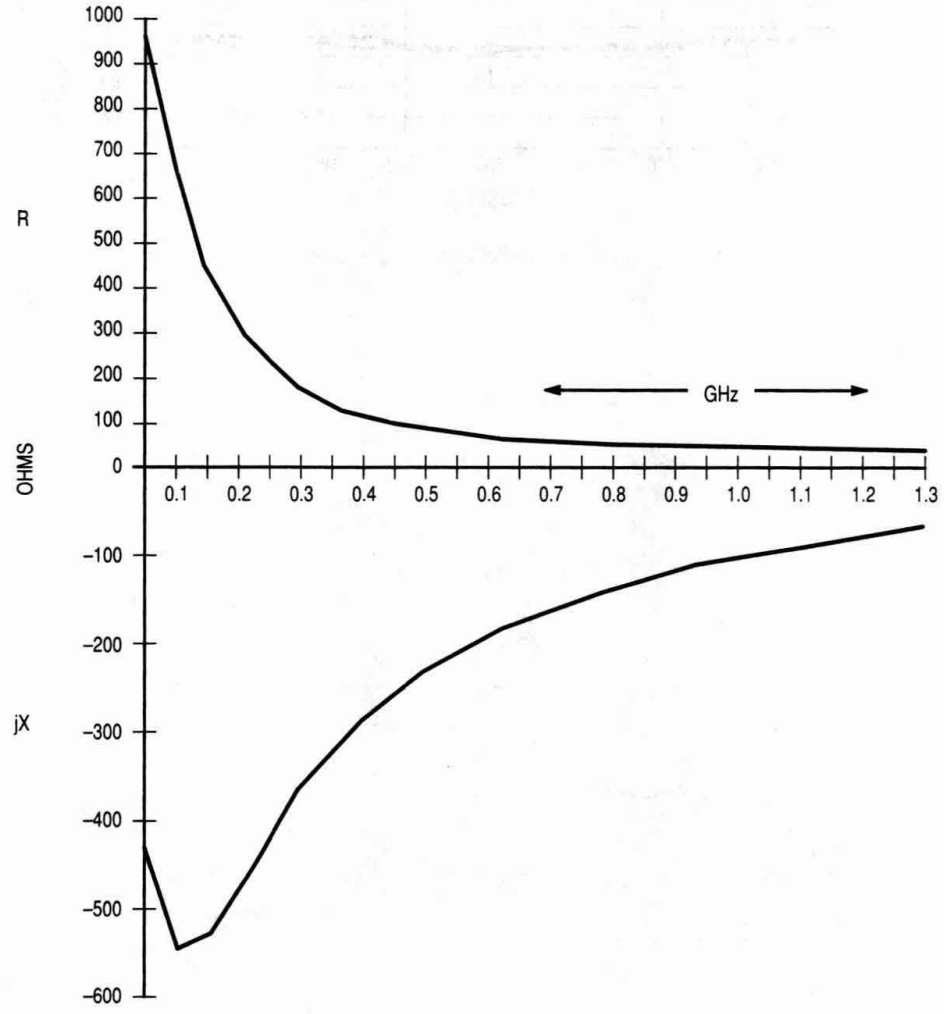
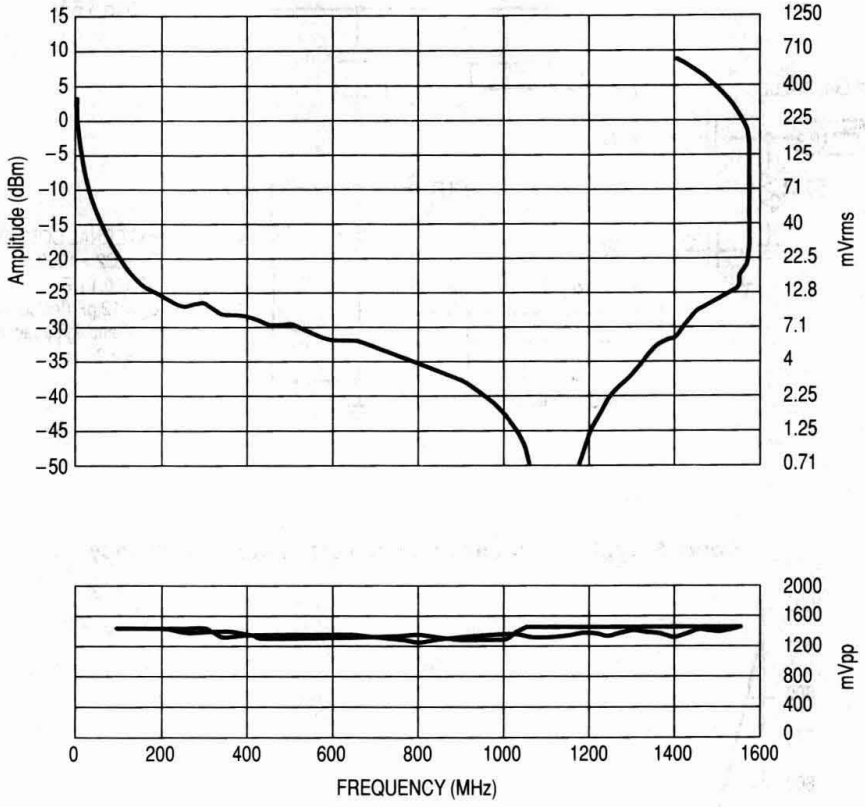


Figure 6. Input Signal Amplitude versus Input Frequency



Divide Ratio = 32

MOTOROLA

MC12032A
MC12032B

Consider MC12054A for New Design
2.0GHz Dual Modulus Prescaler

MECL PLL COMPONENTS
÷64/65, ÷128/129
DUAL MODULUS PRESCALER

SEMICONDUCTOR
TECHNICAL DATA

The MC12032A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

The MC12032B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

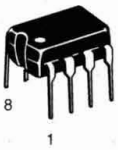
A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

NOTE: The "B" Version Is Not Recommended for New Designs

- 2.0 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- MC12032A for Positive Edge Triggered Synthesizers
- 12 mA Maximum, –40 to 85°C, V_{CC} = 5.5 Vdc
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Low–Power 8.5 mA Typical

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grouunding this pin, but this is not recommended due to increased power soncumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

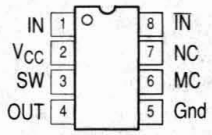
NOTE: * Equivalent to a two–input NAND gate

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12032AD	T_A =–40° to +85°C	SO–8
MC12032AP		Plastic
MC12032BD		SO–8
MC120328BP		Plastic

Not Recommended For New Designs

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.5	2.4	2.0	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	8.5	12	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	—
Output Voltage Swing (C_L = 12 pF; R_L = 2.2 kΩ)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out	t_{set}	–	8.0	10	ns
Input Voltage Sensitivity 500–2000 MHz	$V_{in(min)}$	100	–	1500	mVpp
Output Current (C_L = 12 pF; R_L = 2.2 kΩ)	I_O	–	1.5	4.0	mA

Figure 1. Logic Diagram (MC12032A)

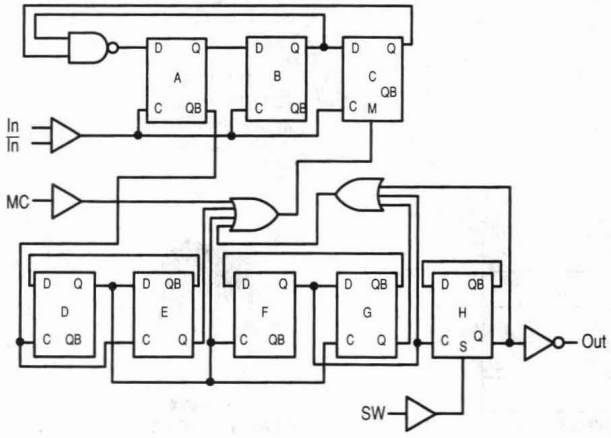
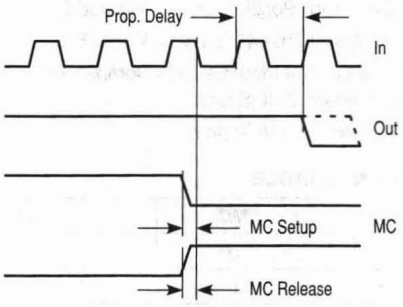
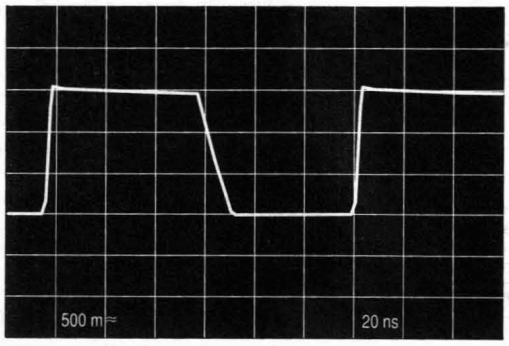


Figure 2. Modulus Setup Time

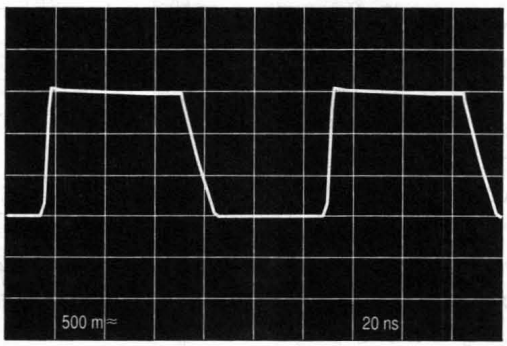


Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. Typical Output Waveforms



(÷64, 500 MHz Input Frequency, V_{CC} = 5.0 V, T_A = 25°C, Output Loaded)



(÷128, 1.1 GHz Input Frequency, V_{CC} = 5.0 V, T_A = 25°C, Output Loaded)

Figure 4. AC Test Circuit

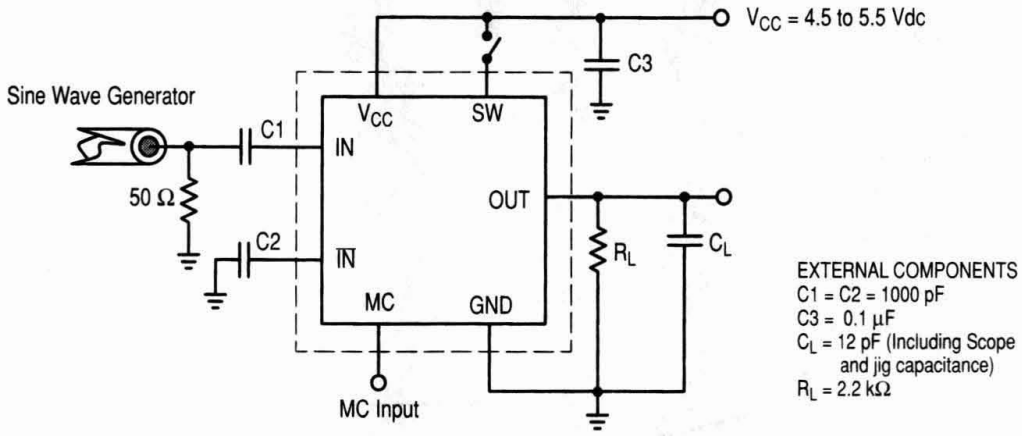
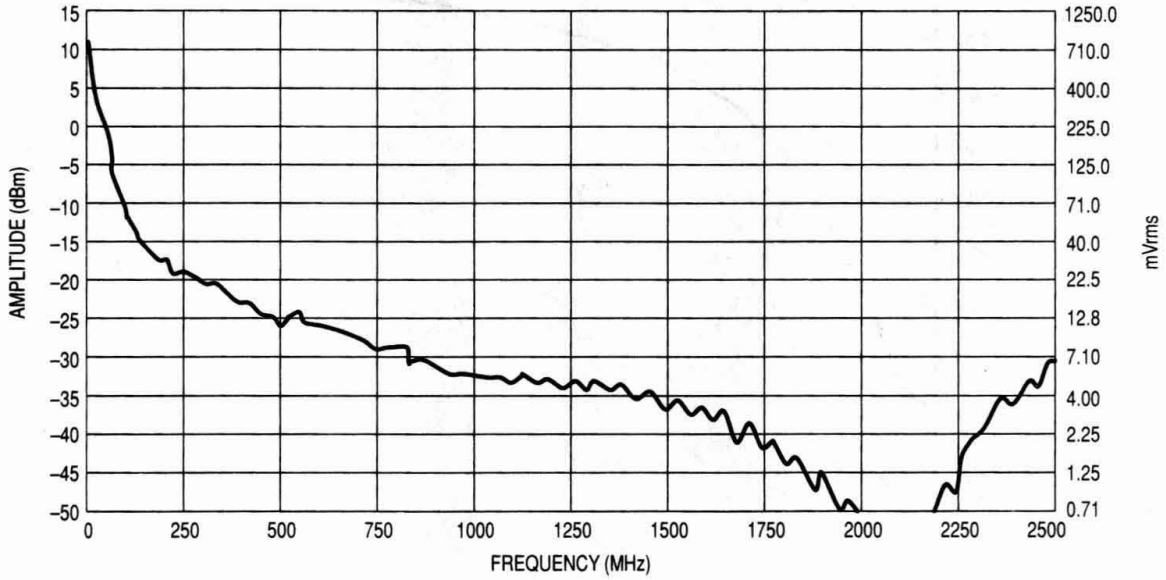


Figure 5. Input Signal Amplitude versus Input Frequency



Divide Ratio = 128

Figure 6. Output Amplitude versus Input Frequency

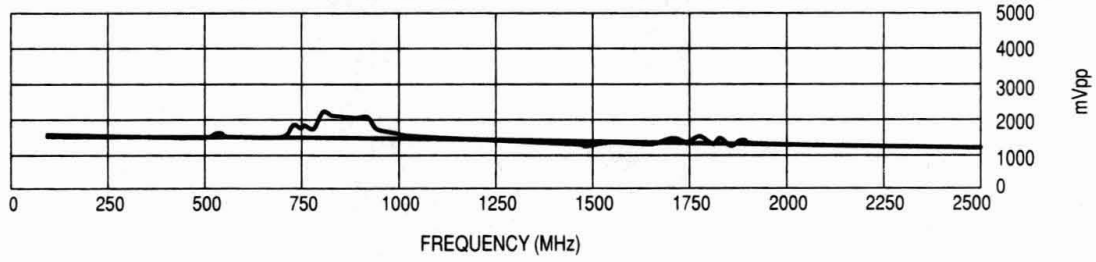
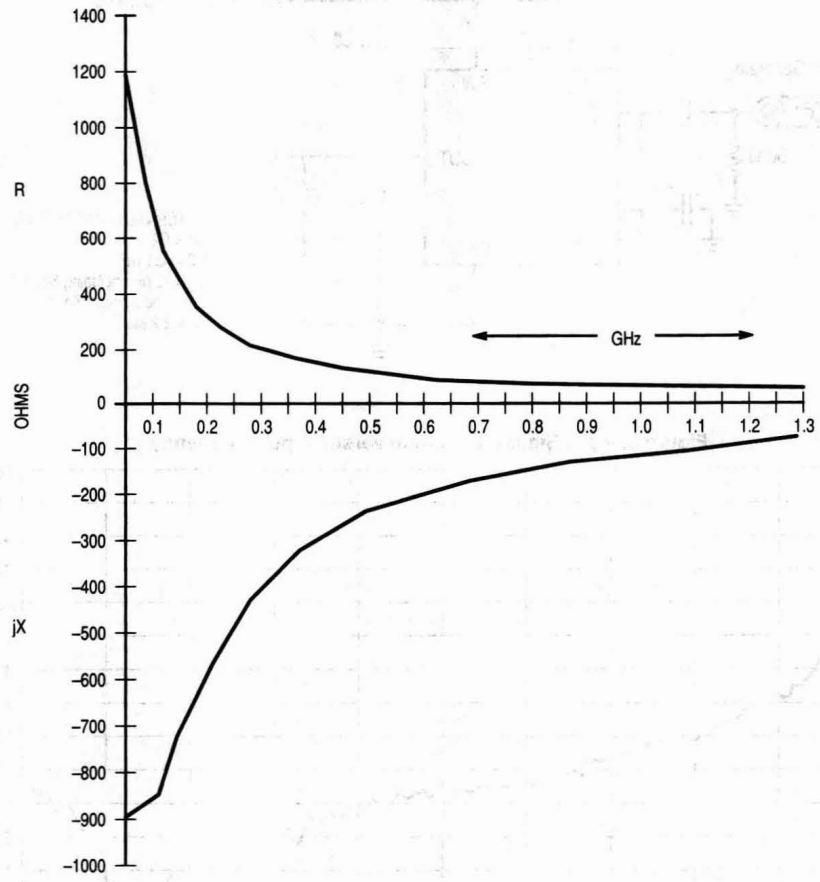


Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

2.0 GHz Low Voltage Dual Modulus Prescaler

MC12033A
MC12033B

MECL PLL COMPONENTS
÷32/33, ÷64/65
LOW VOLTAGE
DUAL MODULUS PRESCALER

SEMICONDUCTOR
TECHNICAL DATA

The MC12033 is a high frequency low voltage dual modulus prescaler used in phase–locked loop (PLL) applications. A high frequency input signal up to 2.0 GHz is provided for cordless and cellular communication services such as DECT, PHS, and PCS. The MC12033 can be operated down to a minimum supply voltage of 2.7 V required for battery operated portable systems.

The MC12033A can be used with CMOS synthesizer requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signal up to 2.0 GHz in programmable frequency steps. The MC12033B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

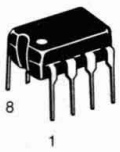
A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

NOTE: The "B" Version Is Not Recommended for New Designs

- 2.0 GHz Toggle Frequency
- Supply Voltage 2.7 V to 5.0 Vdc
- Low Power 10.0 mA Typical at V_{CC} = 2.7 V
- Operating Temperature Range of –40 to 85°C
- The MC12033 is Pin Compatible With the MC12022
- Short Setup Time (t_{set}) 8ns Typical at 2.0 GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

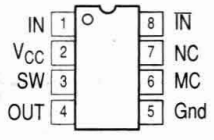
NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grouunding this pin, but this is not recommended due to increased power soncumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	Tstg	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc
Maximum Output Current, Pin 4	I_O	10.0	mA

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12033AD	T_A = –40° to +85°C	SO–8
MC12033AP		Plastic
MC12033BD		SO–8
MC12033BP		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.0 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		ft	0.5	2.4	2.0	GHz
Supply Current Output (Pin 2)	V_{CC} = 2.7 V V_{CC} = 5.0 V	I_{CC}	– –	10.0 13.0	12.5 16.0	mA
Modulus Control Input HIGH (MC)		V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input LOW (MC)		V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input HIGH (SW)		V_{IH2}	V_{CC}	V_{CC}	V_{CC}	V
Divide Ratio Control Input LOW (SW)		V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (Note 1)	C_L = 8.0 pF; R_L = 600 Ω	V_{OUT}	0.8	1.2	–	V_{pp}
Modulus Setup Time MC to OUT @ 2000 MHz		t_{set}	–	8.0	10	ns
Input Voltage Sensitivity	500–2000 MHz	V_{IN}	100	–	1000	mVpp
Output Current (Note 2)	V_{CC} = 2.7V, C_L = 8.0 pF, R_L = 600 Ω V_{CC} = 5.0 V, C_L = 8.0 pF, R_L = 1.5 kΩ	I_O	– –	2.4 2.4	4.0 4.0	mA

NOTES: 1. Valid over voltage range 2.7 to 5.0 V; R_L = 600 Ω @ V_{CC} = 2.7 V; R_L = 1.5 kΩ @ V_{CC} = 5.0 V
2. Divide ratio of ÷32/33 @ 2.0 GHz

Figure 1. Logic Diagram (MC12033A)

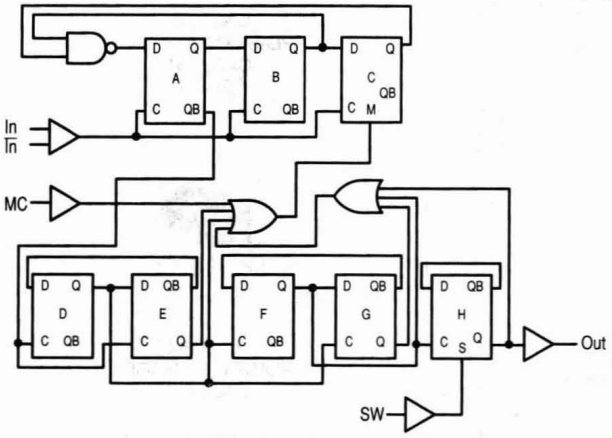
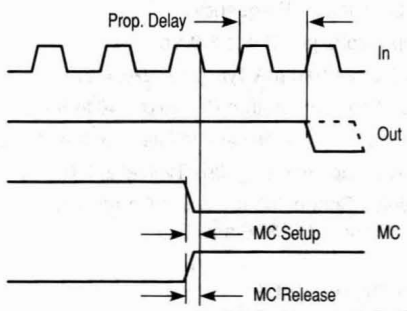
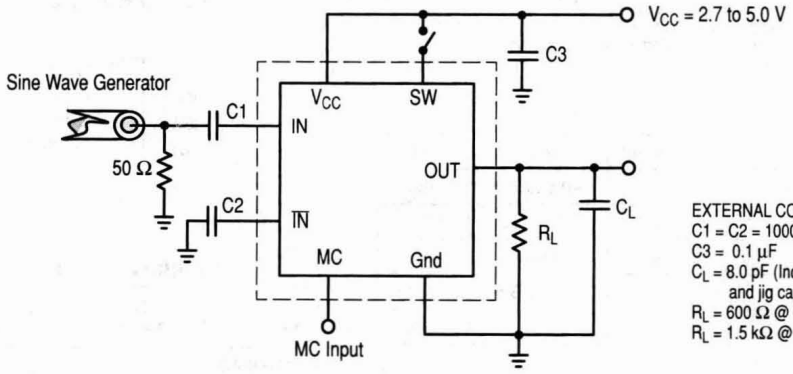


Figure 2. Modulus Setup Time



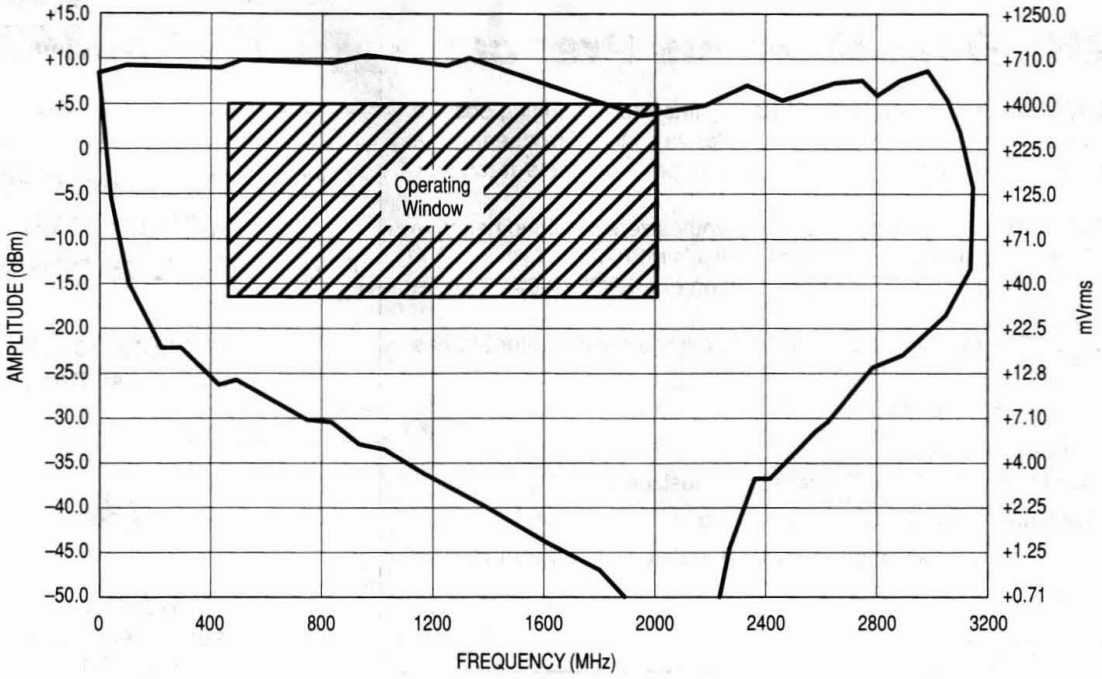
Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



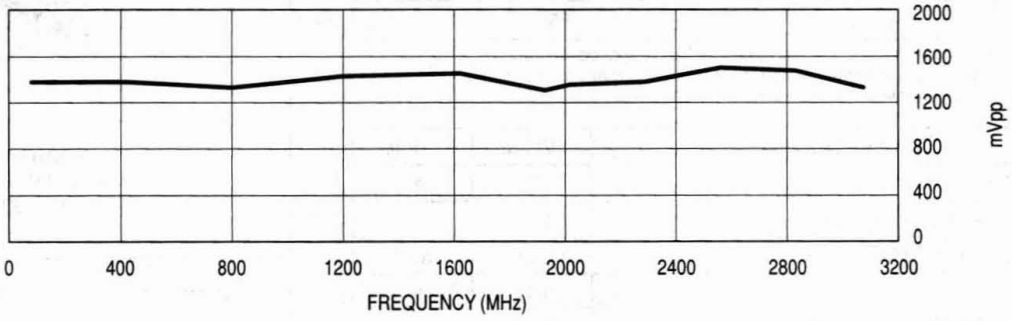
EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and jig capacitance)
R_L = 600 Ω @ V_{CC} = 2.7 V
R_L = 1.5 kΩ @ V_{CC} = 5.0 V

Figure 4. Input Signal Amplitude versus Input Frequency



Divide Ratio = 64; V_{CC} = 5.0 V; T_A = 25°C

Figure 5. Output Amplitude versus Input Frequency



MOTOROLA

2.0GHz Dual Modulus Prescaler

MC12034A
MC12034B

MECL PLL COMPONENTS
÷32/33, ÷64/65
DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12034A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

The MC12034B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- MC12034A for Positive Edge Triggered Synthesizers
- 12mA Maximum, –40 to 85°C, V_{CC} = 5.5 Vdc
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Low–Power 8.5 mA Typical

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

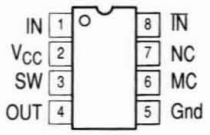
SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

Design Criteria	Value	Unit
Internal Gate Count *	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

NOTE: *Equivalent to a two–input NAND gate.

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to +7.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Modulus Control Input, Pin 6	MC	–0.5 to +6.5	Vdc

NOTES: 1. ESD data available upon request.
2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12034AD	T_A = –40° to +85°C	SO–8
MC12034AP		Plastic
MC12034BD		SO–8
MC120348BP		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 Vdc, T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	f_t	0.5	2.4	2.0	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	8.5	12	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	–
Output Voltage Swing (C_L = 12 pF, R_L = 1.1 kΩ)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out	t_{SET}	–	8.0	10.0	ns
Input Voltage Sensitivity 500–2000 MHz	V_{in}	100	–	1500	mVpp
Output Current (C_L = 12 pF, R_L = 1.1 kΩ)	I_O	–	–	3.5	mA

Figure 1. Logic Diagram (MC12034A)

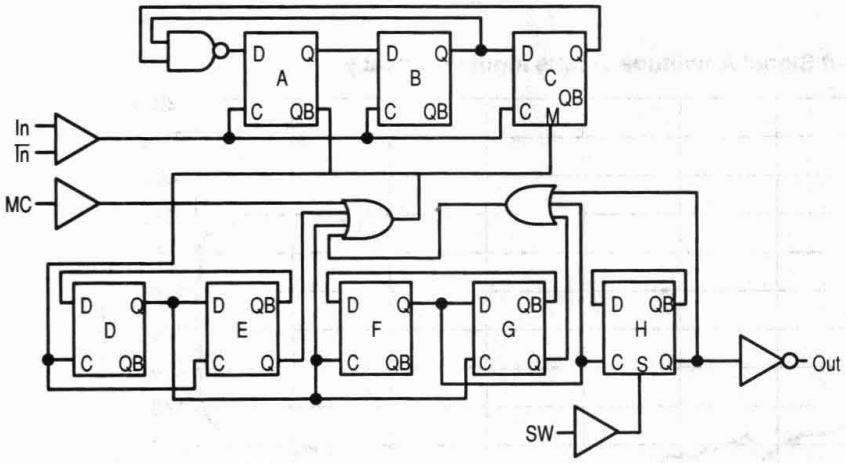
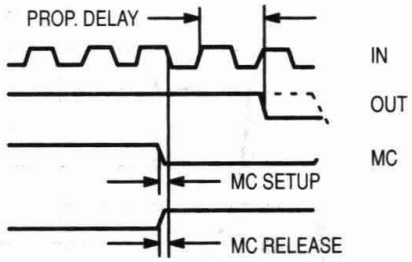


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

Figure 3. Typical Output Waveform

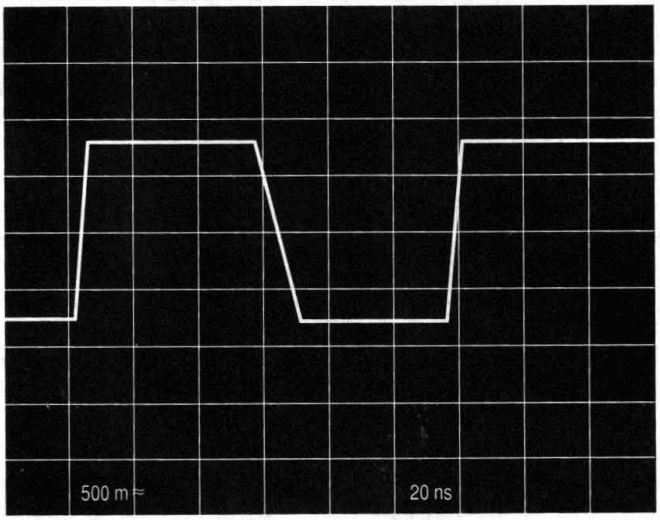


Figure 4. AC Test Circuit

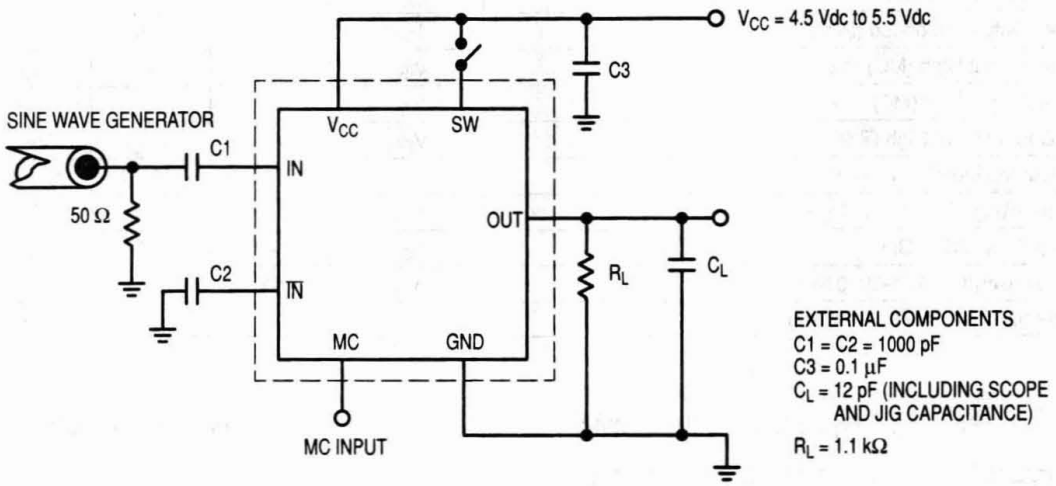
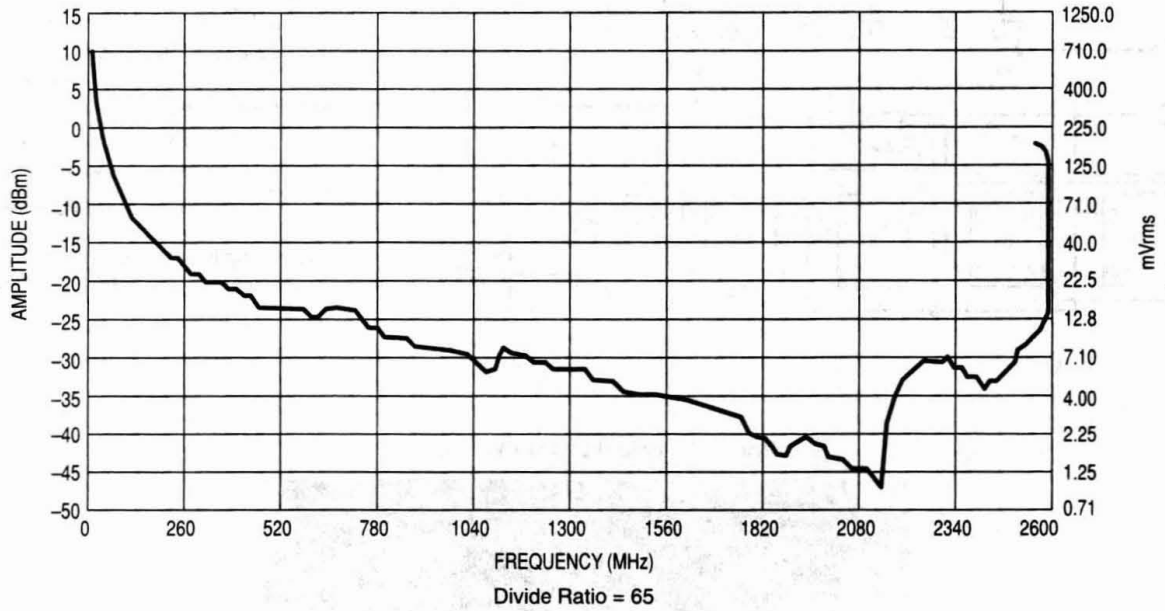
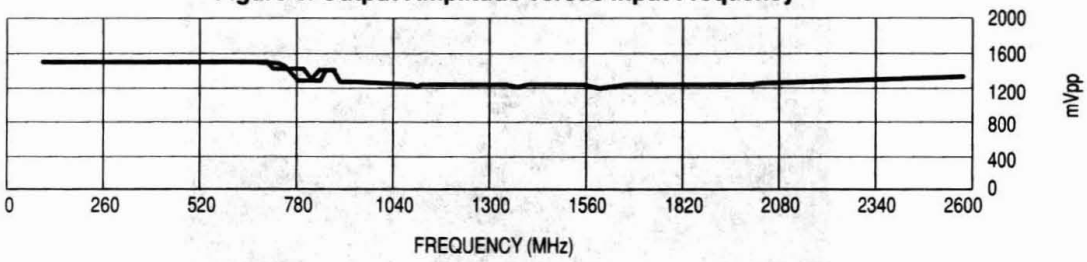


Figure 5. Input Signal Amplitude versus Input Frequency



Divide Ratio = 65

Figure 6. Output Amplitude versus Input Frequency



MOTOROLA

1.1 GHz Low Power Dual Modulus Prescaler

MC12038A

MECL PLL COMPONENTS ÷127/128, ÷255/256 DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12038A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 127/128 or 255/256 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low–Power 4.8 mA Typical
- Operating Temperature Range of –40 to 85°C
- Short Setup Time (t_{set}) 16ns Maximum @ 1.1 GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- On–Chip Output Termination

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	127
H	L	128
L	H	255
L	L	256

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

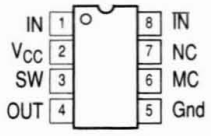
NOTE: * Equivalent to a two–input NAND gate

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12038AD	T_A = – 40° to +85°C	SO–8
MC12038AP		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2) at 5.0 Vdc	I_{CC}	–	4.8	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (C_L = 8.0 pF)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	$V_{in(min)}$	100 400	– –	1500 1500	mVpp

Figure 1. Logic Diagram (MC12038A)

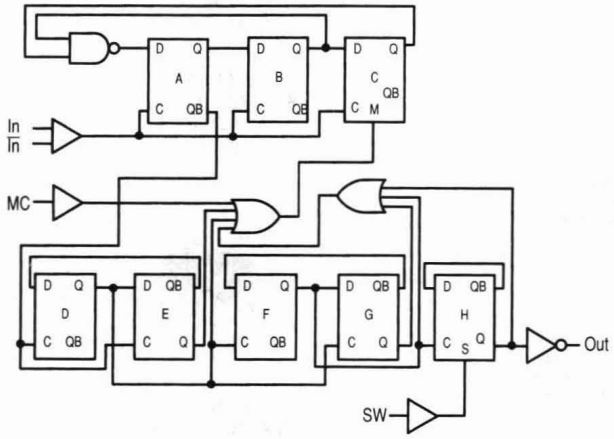
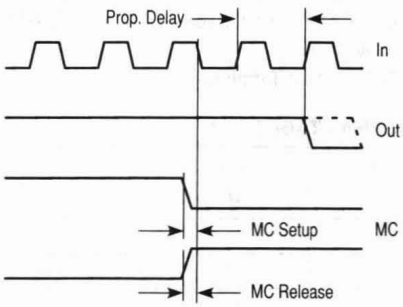
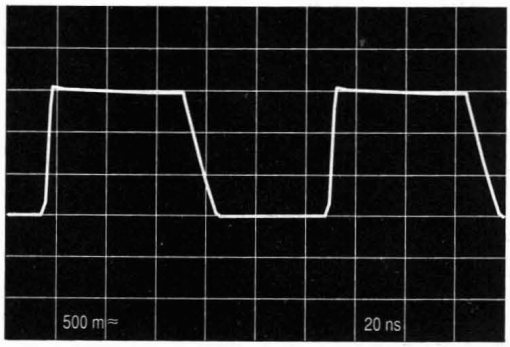


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. Typical Output Waveforms



(÷128, 1.1 GHz Input Frequency, V_{CC} = 5.0 V, T_A = 25°C, Output Loaded)

Figure 4. AC Test Circuit

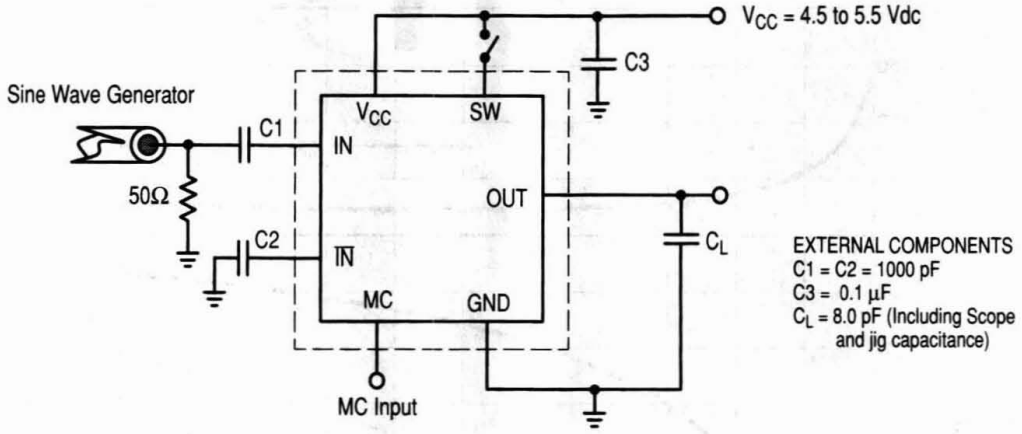
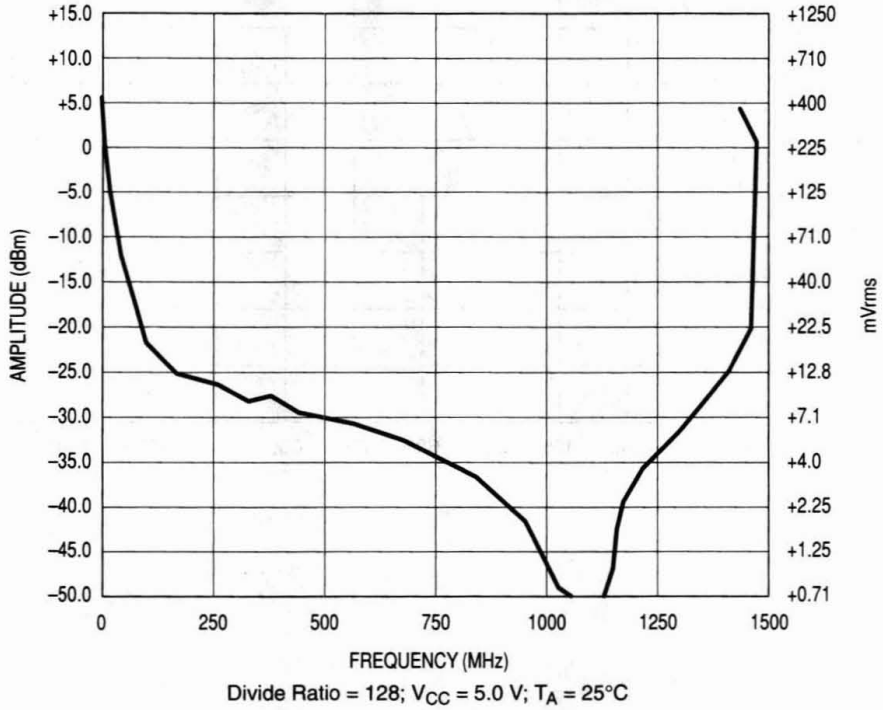


Figure 5. Input Signal Amplitude versus Input Frequency



Divide Ratio = 128; V_{CC} = 5.0 V; T_A = 25°C

Figure 6. Output Amplitude versus Input Frequency

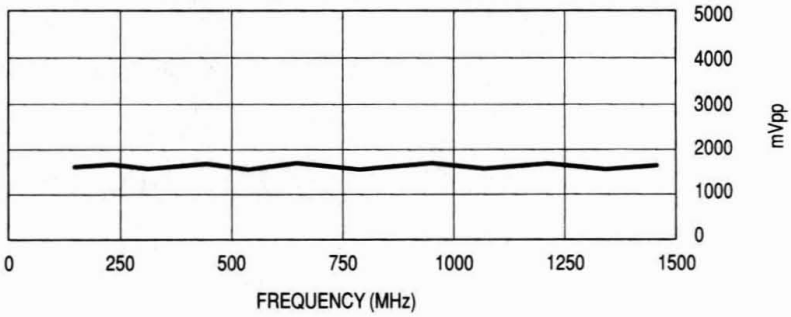
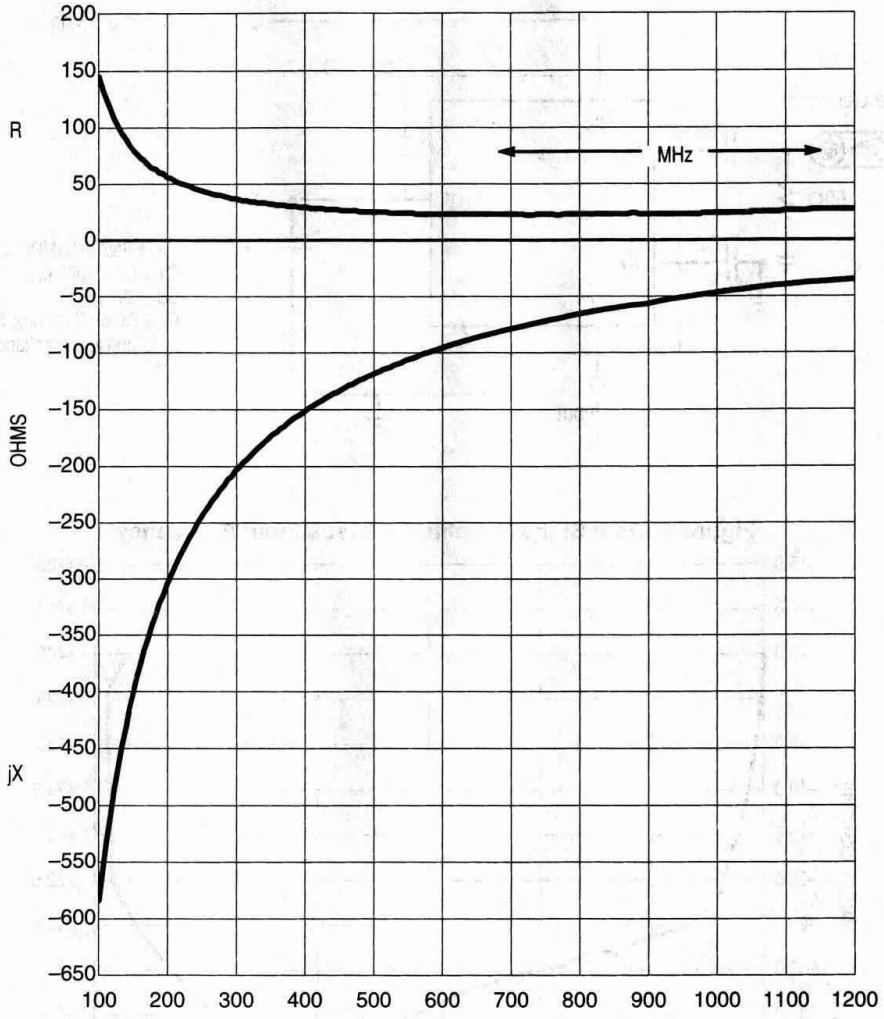


Figure 7. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12040

Phase-Frequency Detector

The MC12040 is a phase–frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648, MC12147, MC12148 or MC12149), it is useful in a broad range of phase–locked loop applications.

- Operating Frequency = 80 MHz Typical

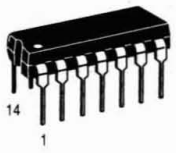
Pin Conversion Table

14 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 PIN PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

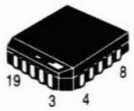
PHASE–FREQUENCY DETECTOR

SEMICONDUCTOR TECHNICAL DATA

Inputs		Outputs			
R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1



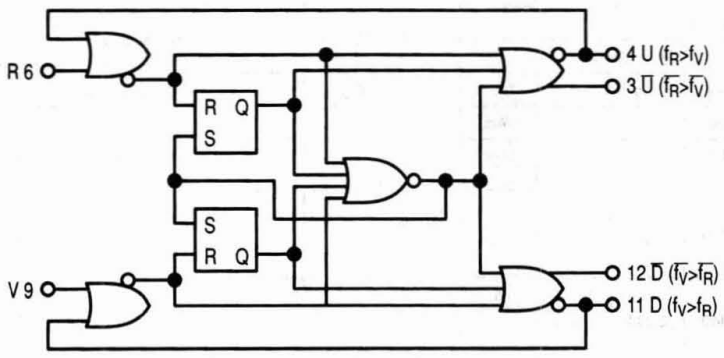
P SUFFIX
PLASTIC PACKAGE
CASE 646



FN SUFFIX
PLASTIC PACKAGE
CASE 775
(PLCC)

Not Recommended for New Designs

LOGIC DIAGRAM

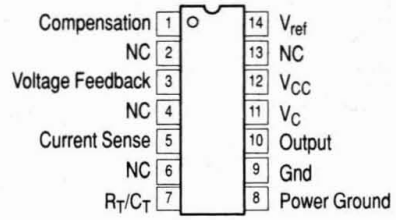


V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

PIN CONNECTIONS



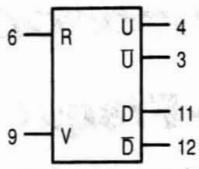
(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12040P	T_A = 0° to +75°C	Plastic

ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to –2.0 V for –5.2 V tests.



NOTE: For more information on using an ECL device in a +5V system, refer to Motorola Application Note AN1406/D, "Designing with PECL (ECL at +5.0V)"

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	–0.840	–1.870	–1.145	–1.490	–5.2
25°C	–0.810	–1.850	–1.105	–1.475	–5.2
75°C	–0.720	–1.830	–1.045	–1.450	–5.2

Supply Voltage = –5.2V

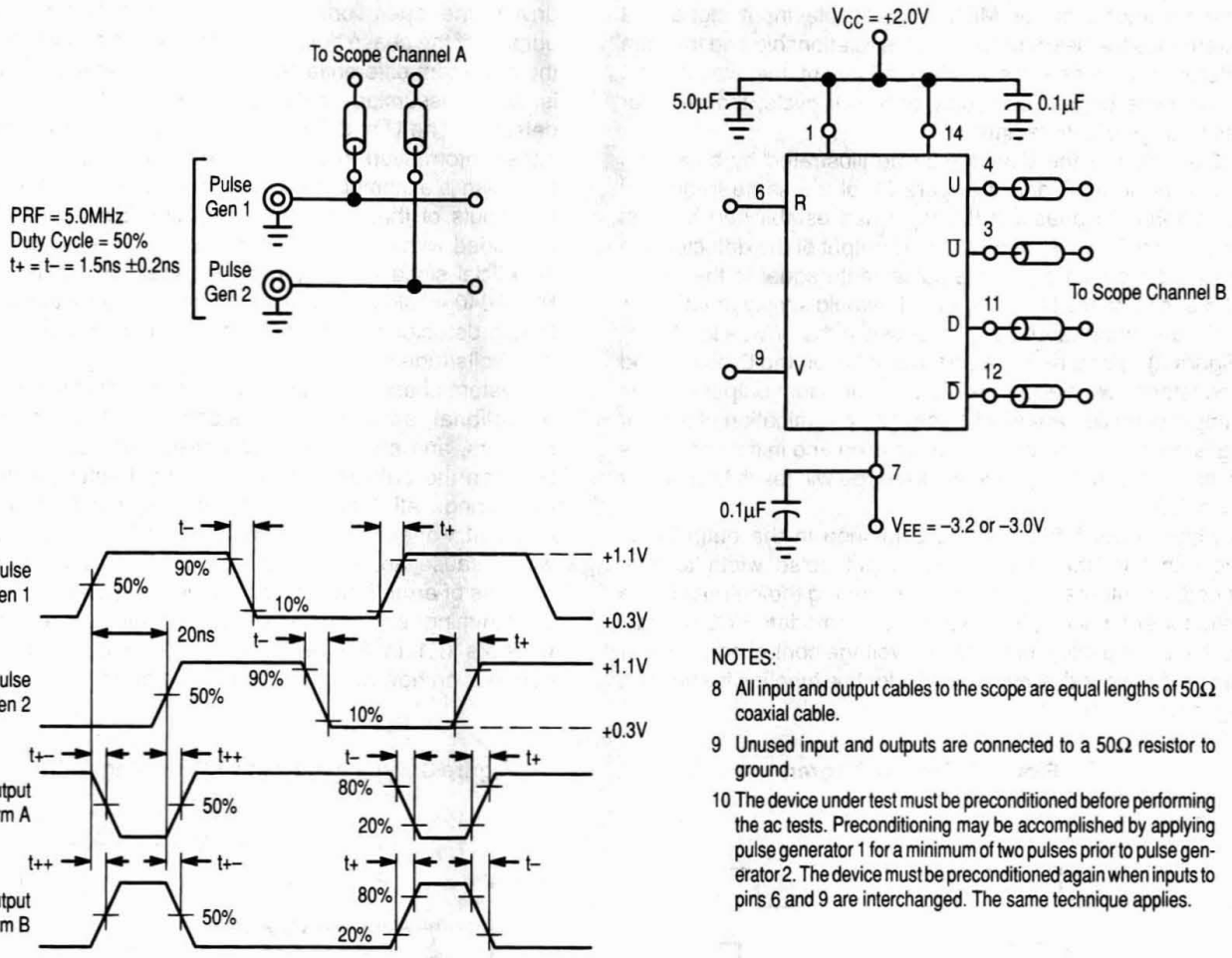
Symbol	Characteristics	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
I_E	Power Supply Drain	7			–120	–60			mAdc					7	1,14
I_{INH}	Input Current	6 9				350 350			µAdc	6 9				7 7	1,14 1,14
V_{OH}[1]	Logic "1" Output Voltage	3 4 11 12	–1.000	–0.840	–0.960	–0.810	–0.900	–0.720	Vdc					7	1,14
V_{OL}[1]	Logic "0" Output Voltage	3 4 11 12	–1.870	–1.635	–1.850	–1.620	–1.830	–1.595	Vdc					7	1,14
V_{OHA}[2]	Logic "1" Input Voltage	3 4 11 12	–1.020		–0.980		–0.920		Vdc			6.9		7	1,14
V_{OLA}[2]	Logic "0" Input Voltage	3 4 11 12		–1.615		–1.600		–1.575	Vdc			9 6 9 6	6 9 6 9	7	1,14

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

Supply Voltage = +5.0V

Symbol	Characteristics	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
I_E	Power Supply Drain	7			–115	–60			mAdc					1,14	7
I_{INH}	Input Current	6 9				350 350			µAdc	6 9				1,14 1,14	7 7
V_{OH}[1]	Logic "1" Output Voltage	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc					1,14	7
V_{OL}[1]	Logic "0" Output Voltage	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc					1,14	7
V_{OHA}[2]	Logic "1" Input Voltage	3 4 11 12	3.980		4.020		4.080		Vdc			6.9		1,14	7
V_{OLA}[2]	Logic "0" Input Voltage	3 4 11 12		3.450		3.460		3.490	Vdc			9 6 9 6	6 9 6 9	1,14	7

Figure 1. AC Tests



NOTES:

8 All input and output cables to the scope are equal lengths of 50Ω coaxial cable.

9 Unused input and outputs are connected to a 50Ω resistor to ground.

10 The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.

Symbol	Characteristic	Pin Under Test	Output Waveform	MC12040 0°C Max	MC12040 25°C Max	MC12040 85°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED: Pulse Gen 1	Pulse Gen 2	V_{EE} –3.0 or –3.2V	V_{CC} +2.0V
t_{6+4+}	Propagation Delay	6,4	B	4.6	4.6	5.0	ns	6	9	7	1,14
t_{6+12+}		6,12	A	6.0	6.0	6.6		9	6		
t_{6+3-}		6,3	A	4.5	4.5	4.9		6	9		
t_{6+11-}		6,11	B	6.4	6.4	7.0		9	6		
t_{9+11+}		9,11	B	4.6	4.6	5.0		9	6		
t_{9+3+}		9,3	A	6.0	6.0	6.6		6	9		
t_{9+12-}		9,12	A	4.5	4.5	4.9		9	6		
t_{9+4-}		9,4	B	6.4	6.4	7.0		6	9		
t_{3+}	Output Rise Time	3	A	3.4	3.4	3.8	ns	6	9	7	1,14
t_{4+}		4	B					6	9		
t_{11+}		11	B					9	6		
t_{14+}		14	A					9	6		
t_{3-}	Output Fall Time	3	A	3.4	3.4	3.8	ns	6	9	7	1,14
t_{4-}		4	B					6	9		
t_{11-}		11	B					9	6		
t_{14-}		14	A					9	6		

APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL–compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 2), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 2), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start–up. A stable phase–locked loop will result from either condition.

Phase error information is contained in the output duty cycle–that is, the ratio of the output pulse width to total period. By integrating or low–pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage controlled oscillator can be developed. A circuit useful for this function is shown in Figure 3.

Proper level shifting is accomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector (U and D). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The U and D outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R–C filtering imbedded within the input network (NO TAG) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16mV offset voltage in the amplifier would cause an error of 0.016/ 0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 3). Phase error over temperature depends on how much the offending parameters drift.

Figure 2. Timing Diagram

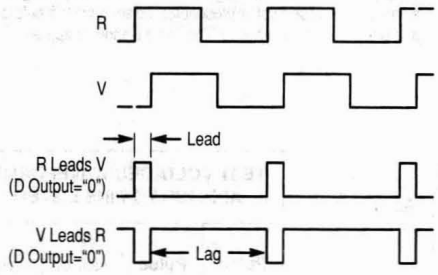
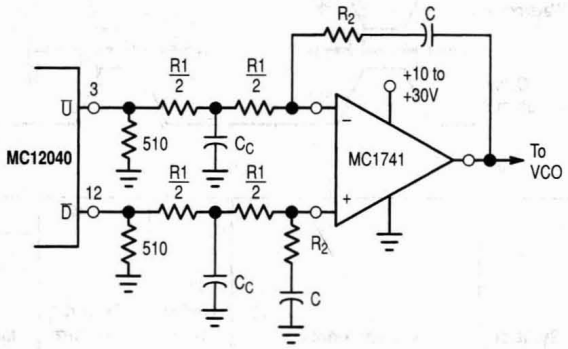


Figure 3. Typical Filter and Summing Network



MOTOROLA

MC12052A

1.1 GHz Super Low Power Dual Modulus Prescaler

MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

The MC12052A is a super low power dual modulus prescaler used in phase–locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 2.7 mW at a minimum supply voltage of 2.7 V.

The MC12052A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- The MC12052 is Pin and Functionally Compatible with the MC12022
- Low Power 1.0 mA Typical
- 2.0 mA Maximum, –40 to 85°C, V_{CC} = 2.7 to 5.5 Vdc
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

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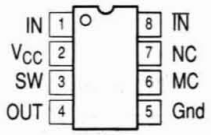
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12052AD	T_A = – 40° to +85°C	SO–8
MC12052ASD		SSOP–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current (Pin 2)	I_{CC}	–	1.0	2.0	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Modulus Control Input Low (MC)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (Note 2) (C_L = 8.0 pF, R_L = 3.3 kΩ)	V_{out}	0.8	1.1	–	V_{PP}
Modulus Setup Time MC to Out @ 1100 MHz	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mV_{PP}
Output Current (Note 1) V_{CC} = 2.7 V, C_L = 8.0 pF, R_L = 3.3 kΩ V_{CC} = 5.0 V, C_L = 8.0 pF, R_L = 7.2 kΩ	I_O	 – –	 0.5 0.5	 3.0 3.0	mA

NOTES: 1. Divide ratio of ÷64/65 @ 1.1 GHz
2. Valid over voltage range 2.7 to 5.5 V; R_L = 3.3 kΩ @ V_{CC} = 2.7 V; R_L = 7.2 kΩ @ V_{CC} = 5.0 V

Figure 1. Logic Diagram (MC12052A)

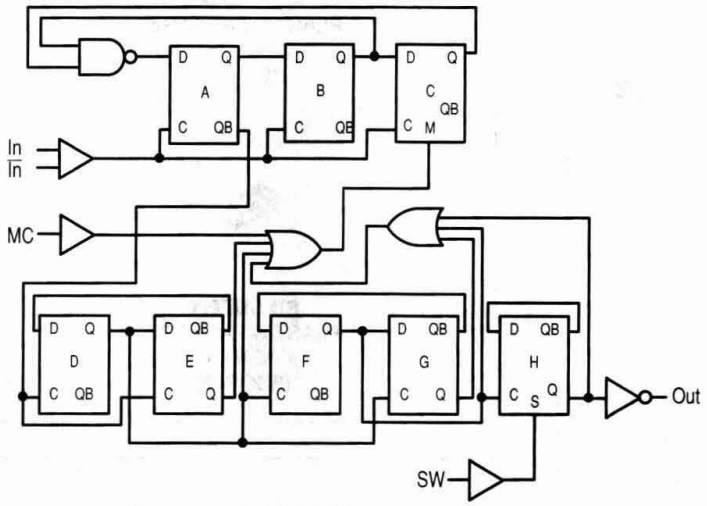
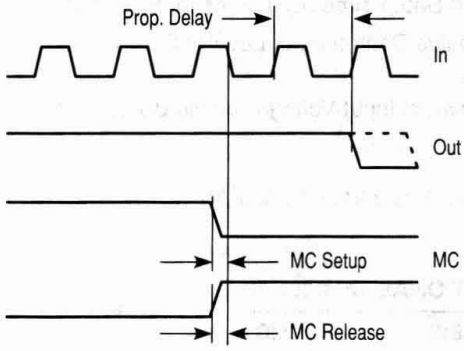
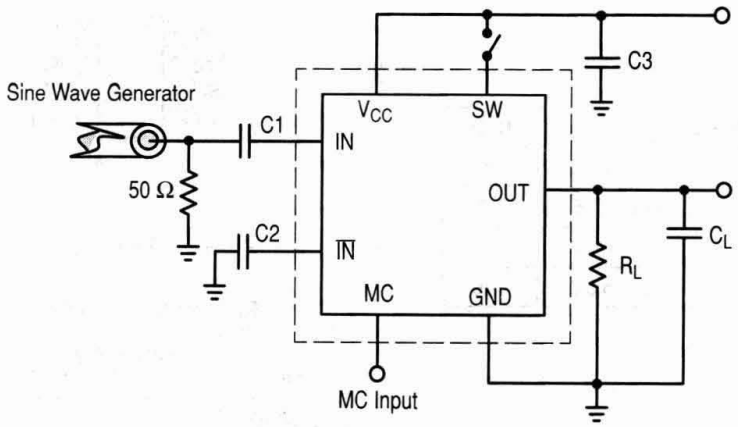


Figure 2. Modulus Setup Time



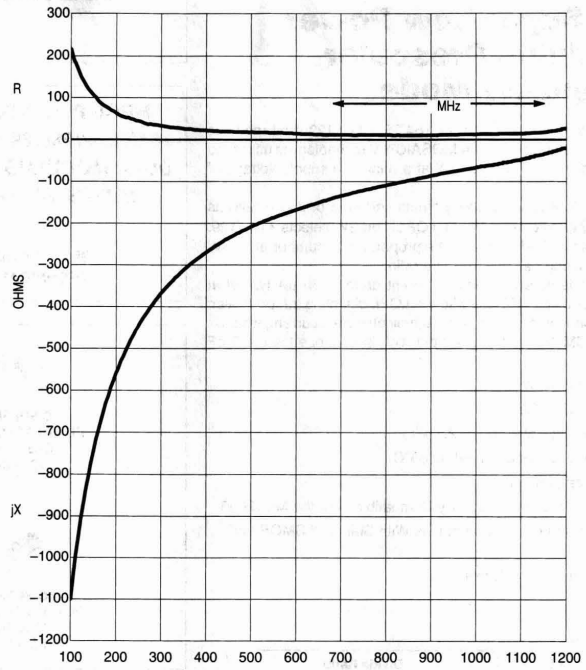
Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0pF (Including Scope and jig capacitance)
R_L = 3.3 kΩ @ V_{CC} = 2.7 V
R_L = 7.2 kΩ @ V_{CC} = 5.0 V

Figure 4. Typical Input Impedance versus Input Frequency



MC12053A

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise notex.)

Characteristic		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)		f_t	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)	V_{CC} = 2.7 V V_{CC} = 5.0 V	I_{CC}	– –	1.60 1.75	2.5 2.5	mA
Stand–By Current	V_{CC} = 2.7 V V_{CC} = 5.0 V	I_{SB}	– –	50 100	250 250	µA
Modulus Control & Stand–By Input HIGH (MC & SB)		V_{IH1}	2.0	–	V_{CC} + 0.5	V
Modulus Control & Stand–By Input LOW (MC & SB)		V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input HIGH (SW)		V_{IH2}	V_{CC} – 0.5	V_{CC}	V_{CC} + 0.5	V
Divide Ratio Control Input LOW (SW)		V_{IH2}	Open	Open	Open	
Output Voltage Swing (Note 1)		V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to OUT at 1100 MHz		t_{set}	–	11	16	ns
Input Voltage Sensitivity	250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp

NOTE: Assumes 8.0 pF high impedance load.

Figure 1. Logic Diagram (MC12053A)

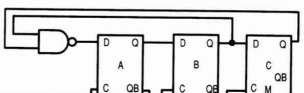
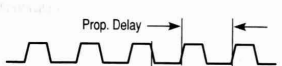


Figure 2. Modulus Setup Time



MOTOROLA

1.1 GHz Super Low Power Dual Modulus Prescaler With Stand-By Mode

MC12053A

MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER WITH STAND–BY MODE

SEMICONDUCTOR TECHNICAL DATA

The MC12053A is a super low power ÷64/65, ÷128/129 dual modulus prescaler. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 4.3 mW at a minimum supply voltage of 2.7 V.

The Divide Ratio Control input, SW, permits selection of divide ratio as desired. A HIGH on SW selects ÷64/65; an OPEN on SW selects ÷128/129. The Modulus Control input, MC, selects the proper divide number after SW has been biased to select the desired divide ratio.

Stand–by mode is featured to reduce current drain to 50 µA typical at 2.7 V when the stand–by pin, SB, is switched LOW, disabling the prescaler. On–chip output termination provides 500 µA (typical) output current, which is sufficient to drive a CMOS synthesizer input high impedance load (8.0 pF typical).

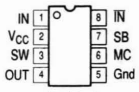
- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.5 V
- Low Power 1.5 mA Typical at V_{CC} = 2.7 V
- Operating Temperature Range of –40 to 85°C
- On–Chip Output Termination
- The MC12053A Is Pin and Functionally Compatible With the MC12036
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

MOSAIC V is a trademark of Motorola

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC} – 0.5 to V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC & SB: H = 2.0 V to V_{CC}, L = Gnd to 0.8 V.

MAXIMUM RATINGS

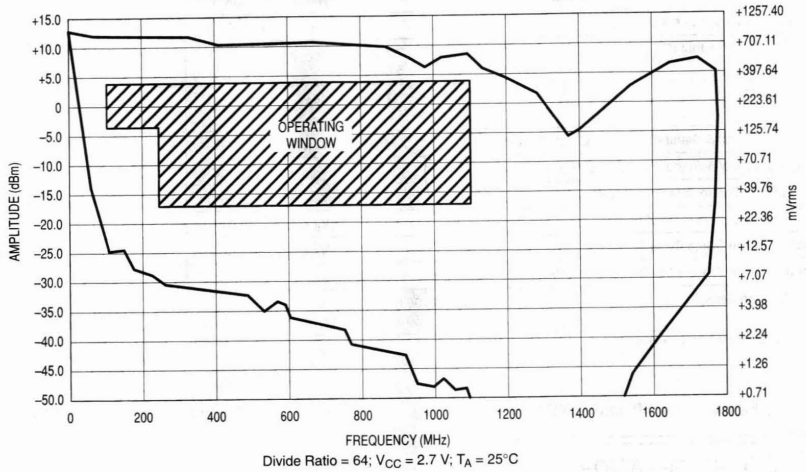
Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to V_{CC}	Vdc
Maximum Output Current, Pin 4	I_O	4.0	mA

NOTE: ESD data available upon request.

ORDERING INFORMATION

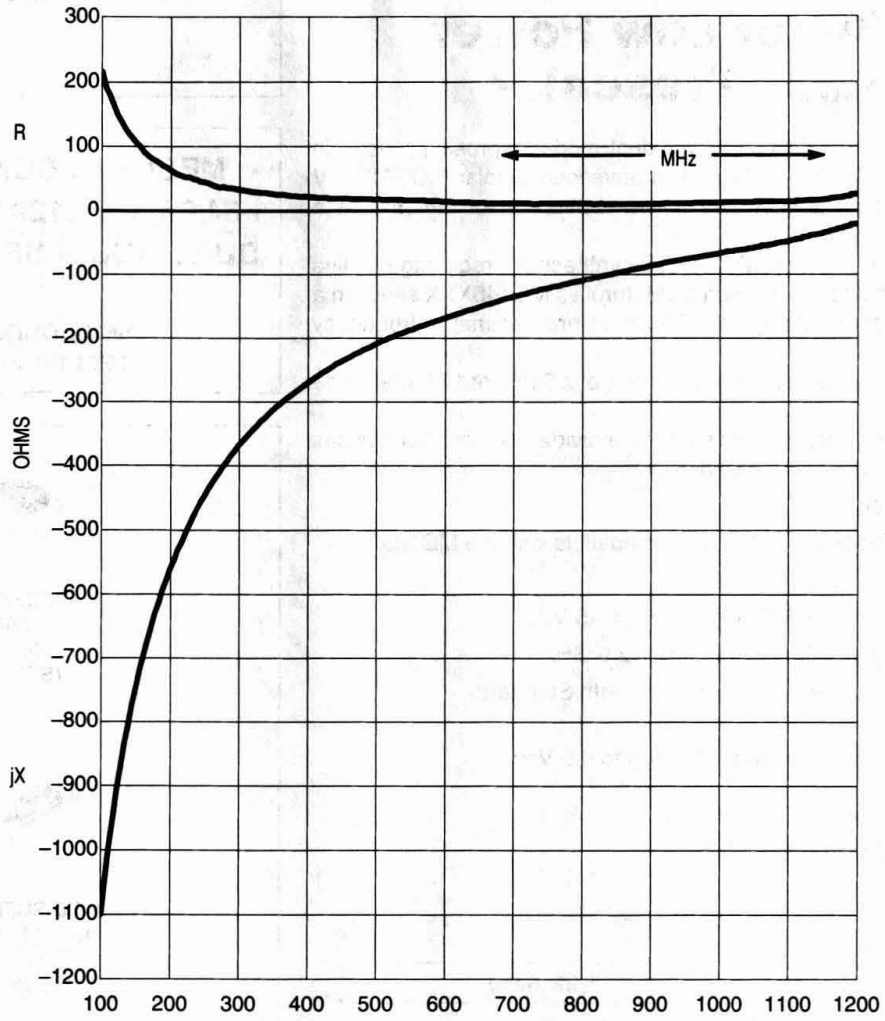
Device	Operating Temp Range	Package
MC12053AD	T_A = – 40° to +85°C	SO–8
MC12053ASD		SSOP–8

Figure 4. Input Signal Amplitude versus Input Frequency



Divide Ratio = 64; V_{CC} = 2.7 V; T_A = 25°C

Figure 6. Typical Input Impedance versus Input Frequency



MOTOROLA

2.0 GHz Super Low Power Dual Modulus Prescaler

The MC12054A is a super low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 5.4 mW at a minimum supply voltage of 2.7 V.

The MC12054A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- The MC12054 is Pin and Functionally Compatible with the MC12031
- Low Power 2.0 mA Typical
- 2.6mA Maximum, –40 to 85°C, V_{CC} = 2.7 to 5.5 Vdc
- Short Setup Time (t_{set}) 10ns Maximum @ 2.0 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

MOSAIC V is a trademark of Motorola

MC12054A

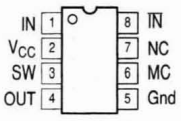
MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12054AD	T_A = – 40° to +85°C	SO–8
MC12054ASD		SSOP–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 Vdc, T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	2.5	2.0	GHz
Supply Current (Pin 2)	I_{CC}	–	2.0	2.6	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Modulus Control Input Low (MC)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (Note 2) (C_L = 8.0 pF, R_L = 1.65 kΩ)	V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to Out @ 2000 MHz	t_{set}	–	8.0	10	ns
Input Voltage Sensitivity 250–2000 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp
Output Current (Note 1) V_{CC} = 2.7 V, C_L = 8.0 pF, R_L = 1.65 kΩ V_{CC} = 5.0 V, C_L = 8.0 pF, R_L = 3.6 kΩ	I_O	 – –	 1.0 1.0	 4.0 4.0	mA

NOTES: 1. Divide ratio of ÷64/65 @ 2.0 GHz
2. Valid over voltage range 2.7 to 5.5 V; R_L = 1.65 kΩ @ V_{CC} = 2.7 V; R_L = 3.6 kΩ @ V_{CC} = 5.0 V

Figure 1. Logic Diagram (MC12054A)

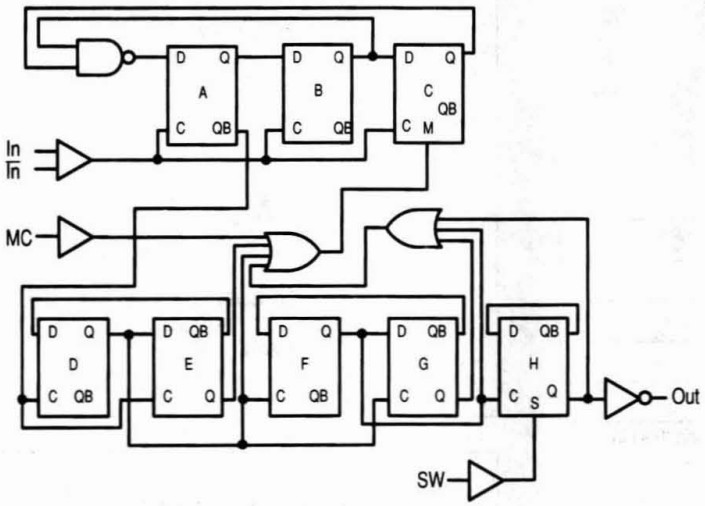
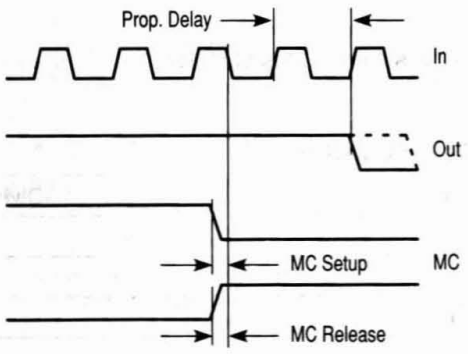
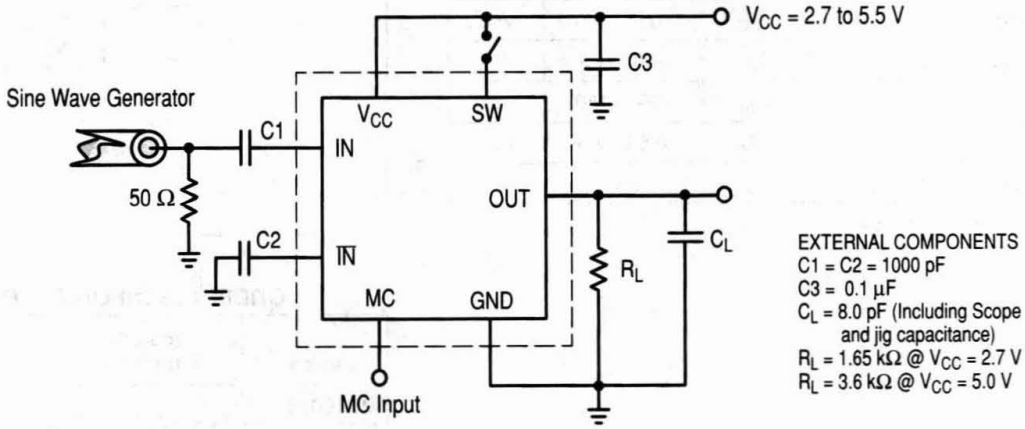


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and jig capacitance)
R_L = 1.65 kΩ @ V_{CC} = 2.7 V
R_L = 3.6 kΩ @ V_{CC} = 5.0 V

MOTOROLA

MC12058

1.1 GHz Low Power Dual Modulus Prescaler

The MC12058 is a low power ÷126/128, ÷254/256 dual modulus prescaler. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 3.0 mW at a minimum supply voltage of 2.7 V. The MC12058 can be operated down to a minimum supply voltage of 2.7 V required for battery operated portable systems.

On–chip output termination provides 250 μA (typical) output current to drive a 8.0 pF (typical) high impedance load. The Divide Ratio Control input, SW, permits selection of divide ratio as desired. A HIGH on SW selects ÷126/128; an OPEN on SW selects ÷254/256. The Modulus Control input, MC, selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage 2.7 to 5.5 V
- Low Power 1.1 mA Typical at V_{CC} = 3.0 V
- Operating Temperature Range of –40 to 85°C
- On–Chip Output Termination

MOSAIC V is a trademark of Motorola

MECL PLL COMPONENTS
÷126/128, ÷254/256
LOW POWER
DUAL MODULUS PRESCALER

SEMICONDUCTOR
TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	126
H	L	128
L	H	254
L	L	256

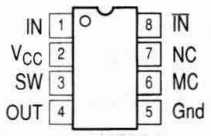
NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to V_{CC}	Vdc
Maximum Output Current, Pin 4	I_O	4.0	mA

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12058D	T_A = – 40° to +85°C	SO–8
MC12058SD		SSOP–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)		f_t	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)		I_{CC}	–	1.1	2.0	mA
Modulus Control Input HIGH (MC)		V_{IH1}	2.0	–	V_{CC} + 0.5	V
Modulus Control Input LOW (MC)		V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input HIGH (SW)		V_{IH2}	V_{CC} – 0.5	V_{CC}	V_{CC} + 0.5	V
Divide Ratio Control Input LOW (SW)		V_{IH2}	Open	Open	Open	–
Output Voltage Swing (Note 1)		V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to OUT at 1100 MHz		t_{set}	–	11	16	ns
Input Voltage Sensitivity	250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp

NOTE: Assumes 8.0 pF high impedance load.

Figure 1. Logic Diagram (MC12058)

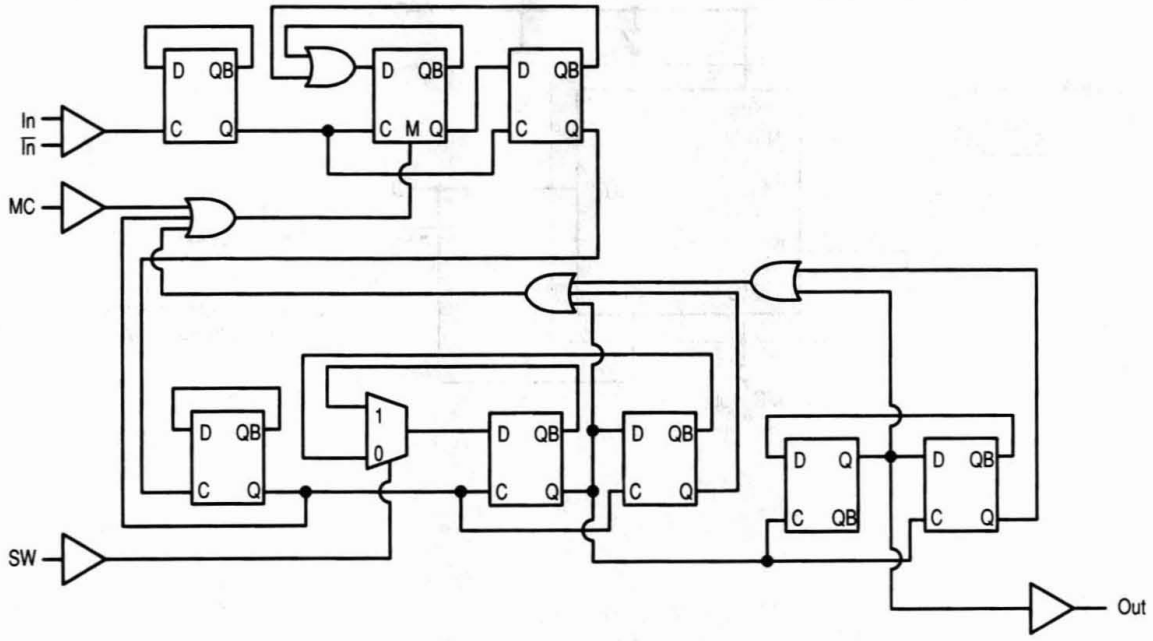
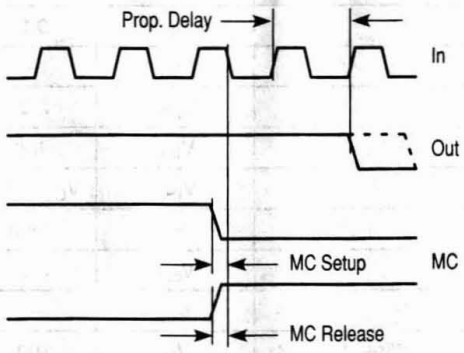
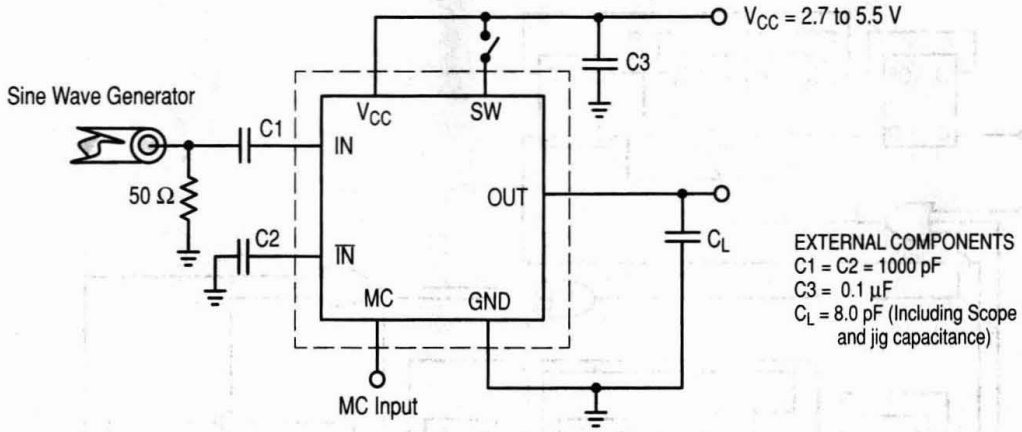


Figure 2. Modulus Setup Time



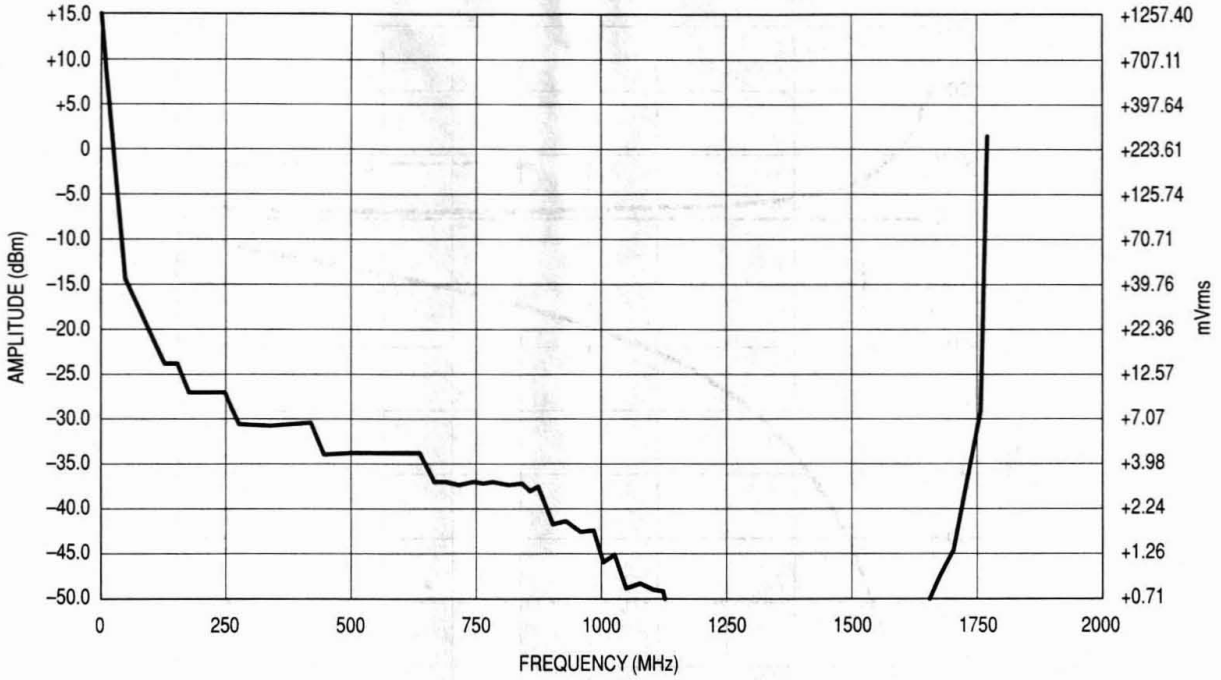
Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and jig capacitance)

Figure 4. Input Signal Amplitude versus Input Frequency



Divide Ratio = 126; V_{CC} = 5.5 V; T_A = 25°C

Figure 5. Output Amplitude versus Input Frequency

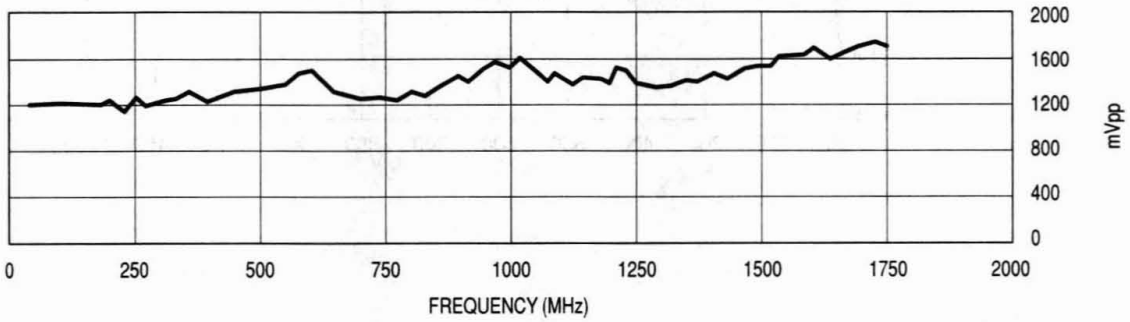
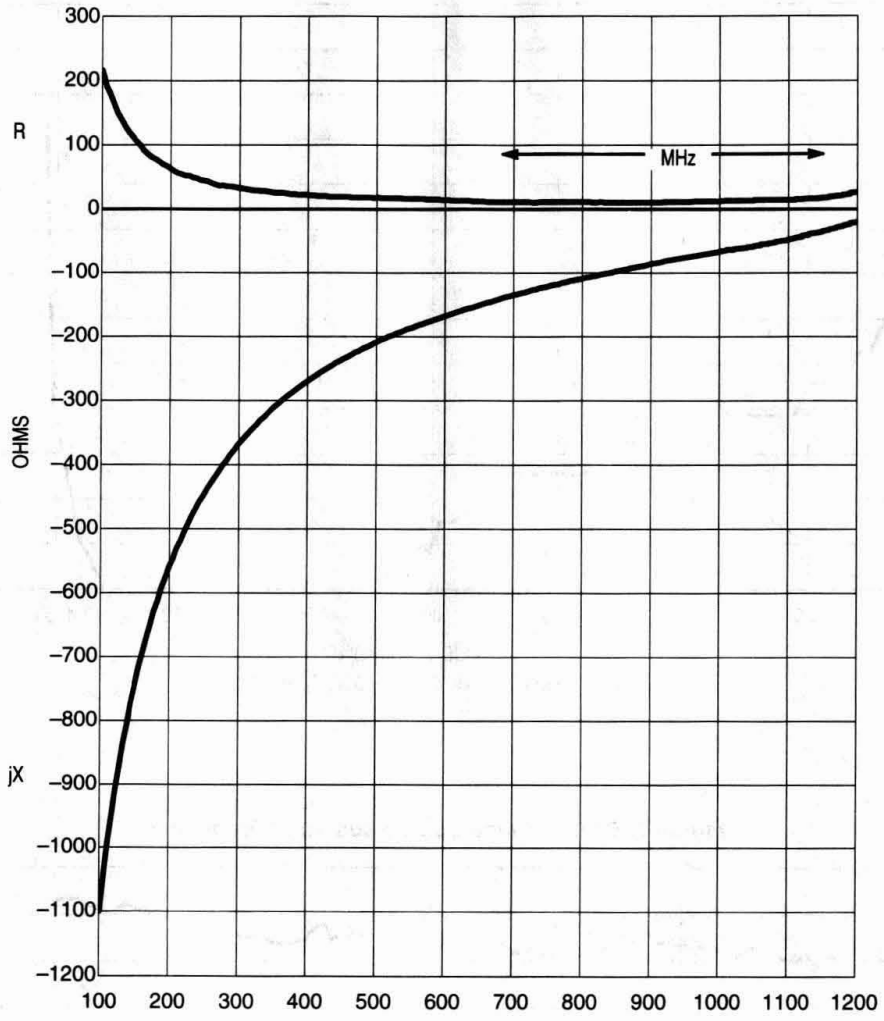


Figure 6. Typical Input Impedance versus Input Frequency



MOTOROLA

MC12061

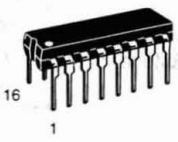
Crystal Oscillator

The MC12061 is for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

- Frequency Range = 2.0 to 20 MHz
- Temperature Range = 0 to + 70°C
- Single Supply Operation: +5.0 Vdc or –5.2 Vdc
- Three Outputs Available:
  11. Complementary Sine Wave (600 mVpp typ)
  12. Complementary MECL
  13. Single Ended TTL

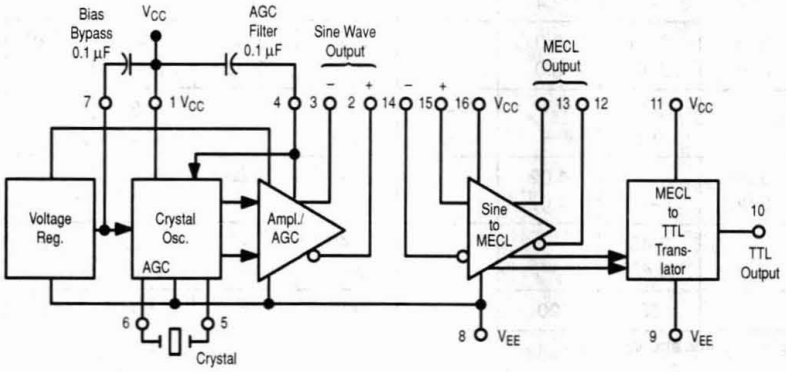
CRYSTAL OSCILLATOR

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

Figure 1. Block Diagram



Note: 0.1 µF power supply pin bypass capacitors not shown.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12061P	T_A = 0° to +70°C	Plastic

TYPICAL CIRCUIT CONFIGURATIONS

Note: 0.1 µF power supply pin bypass capacitors not shown.

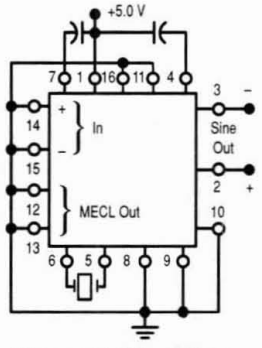


Figure 2. Sine Wave Output

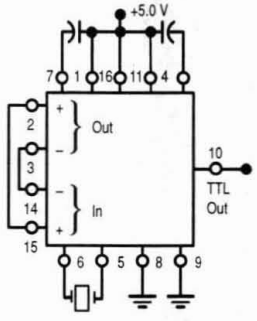


Figure 3. MTTL Output

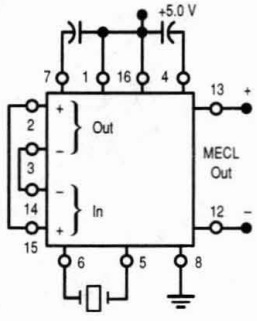


Figure 4. MECL Output
(+5.0 V Supply)

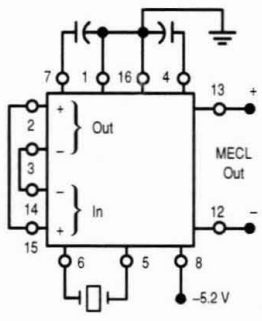


Figure 5. MECL Output
(–5.2 V Supply)

CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12061
Mode of Operation	Fundamental Series Resonance
Frequency Range	2.0 MHz — 20 MHz
Series Resistance, R1	Minimum at Fundamental
Maximum Effective Resistance $R_{E(max)}$	155 ohms

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			0°C		+25°C			+75°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_{CC}	1	–	–	13	16	19	–	–	mAdc
		1	–	–	18	23	28	–	–	
		11	–	–	–	3.0	4.0	–	–	
		16	–	–	13	16	19	–	–	
Input Current	I_{inH}	14	–	–	–	–	250	–	–	µAdc
		15	–	–	–	–	250	–	–	
	I_{inL}	14	–	–	–	–	1.0	–	–	µAdc
		15	–	–	–	–	1.0	–	–	
Differential Offset Voltage	ΔV	4 to 7	–	–	40	–	325	–	–	mAdc
		2 to 3	–	–	–200	0	+200	–	–	
Output Voltage Level	V_{out}	2	–	–	–	3.5	–	–	–	Vdc
		3	–	–	–	3.5	–	–	–	
Logic '1' Output Voltage	V_{OH1} (Note 1)	12	4.0	4.16	4.04	–	4.19	4.1	4.28	Vdc
		13	4.0	4.16	4.04	–	4.19	4.1	4.28	
	V_{OH2}	10	2.4	–	2.4	–	–	2.4	–	
Logic '0' Output Voltage	V_{OL1} (Note 1)	12	2.98	3.43	3.0	–	3.44	3.02	3.47	Vdc
		13	2.98	3.43	3.0	–	3.44	3.02	3.47	
	V_{OL2}	10	–	0.5	–	–	0.5	–	0.5	
		10	–	0.5	–	–	0.5	–	0.5	
Logic '1' Threshold Voltage	V_{OHA}	12	3.98	–	4.02	–	–	4.08	–	Vdc
		13	3.98	–	4.02	–	–	4.08	–	
Logic '0' Threshold Voltage	V_{OLA}	12	–	3.45	–	–	3.46	–	3.49	Vdc
		13	–	3.45	–	–	3.46	–	3.49	
Output Short Circuit Current	I_{OS}	10	20	60	20	–	60	20	60	mAdc

NOTE: 1. Devices will meet standard MECL logic levels using V_{EE} = –5.2 Vdc and V_{CC} = 0.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}
	TEST VOLTAGE/CURRENT VALUES (Volts)					
0°C	4.16	3.19	3.86	3.51	4.0	4.75
+25°C	4.19	3.21	3.90	3.52	4.0	4.75
+75°C	4.28	3.23	3.96	3.55	4.0	4.75

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	
Power Supply Drain Current	I_{CC}	1	–	–	–	–	–	–	8
		1	–	–	–	–	–	–	8
		11	14	15	–	–	–	–	8,9
		16	–	–	–	–	–	–	8
Input Current	I_{inH}	14	14	15	–	–	–	–	8
		15	15	14	–	–	–	–	8
	I_{inL}	14	15	–	–	–	–	–	8,14
		15	14	–	–	–	–	–	8,15
Differential Offset Voltage	ΔV	4 to 7	–	–	–	–	5,6	–	8
		2 to 3	–	–	–	–	4	–	–
Output Voltage Level	V_{out}	2	–	–	–	–	4	–	8
		3	–	–	–	–	4	–	8
Logic '1' Output Voltage	V_{OH1} (Note 1)	12	14	15	–	–	–	–	8
		13	15	14	–	–	–	–	8
	V_{OH2}	10	15	14	–	–	–	11,16	8,9
Logic '0' Output Voltage	V_{OL1} (Note 1)	12	15	14	–	–	–	–	8
		13	14	15	–	–	–	–	8
	V_{OL2}	10	14	15	–	–	–	11,16	8,9
		10	14	15	–	–	–	–	8,9
Logic '1' Threshold Voltage	V_{OHA}	12	–	–	14	15	–	–	8
		13	–	–	15	14	–	–	8
Logic '0' Threshold Voltage	V_{OLA}	12	–	–	15	14	–	–	8
		13	–	–	14	15	–	–	8
Output Short Circuit Current	I_{OS}	10	15	14	–	–	–	11,16	8,9,10

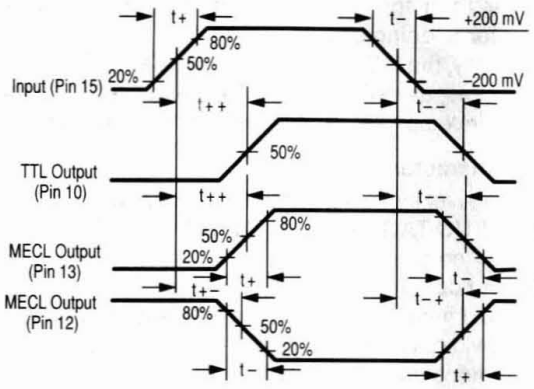
NOTE: 1. Devices will meet standard MECL logic levels using V_{EE} = –5.2Vdc and V_{CC} = 0.

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE/CURRENT VALUES					
			Volts		mA			
@ Test Temperature			V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_{IL}	
0°C			5.0	5.25	16	–0.4	–2.5	
+25°C			5.0	5.25	16	–0.4	–2.5	
+75°C			5.0	5.25	16	–0.4	–2.5	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					Gnd
			V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_{IL}	
Power Supply Drain Current	I_{CC}	1	1	–	–	–	–	8
		1	1	–	–	–	–	8
		11	11,16	–	–	–	–	8,9
		16	16	–	–	–	–	8
Input Current	I_{inH}	14	16	–	–	–	–	8
		15	16	–	–	–	–	8
	I_{inL}	14	16	–	–	–	–	8,14
		15	16	–	–	–	–	8,15
Differential Offset Voltage	ΔV	4 to 7	1	–	–	–	–	8
		2 to 3	–	–	–	–	–	–
Output Voltage Level	V_{out}	2	1	–	–	–	–	8
		3	1	–	–	–	–	8
Logic '1' Output Voltage	V_{OH1} (Note 1)	12	16	–	–	–	12	8
		13	16	–	–	–	13	8
	V_{OH2}	10	–	–	–	10	–	8,9
Logic '0' Output Voltage	V_{OL1} (Note 1)	12	16	–	–	–	12	8
		13	16	–	–	–	13	8
	V_{OL2}	10	–	–	10	–	–	8,9
		10	–	11,16	10	–	–	8,9
Logic '1' Threshold Voltage	V_{OHA}	12	16	–	–	–	12	8
		13	16	–	–	–	13	8
Logic '0' Threshold Voltage	V_{OLA}	12	16	–	–	–	12	8
		13	16	–	–	–	13	8
Output Short Circuit Current	I_{OS}	10	–	–	–	–	–	8,9,10

NOTE: 1. Devices will meet standard MECL logic levels using V_{EE} = –5.2Vdc and V_{CC} = 0.

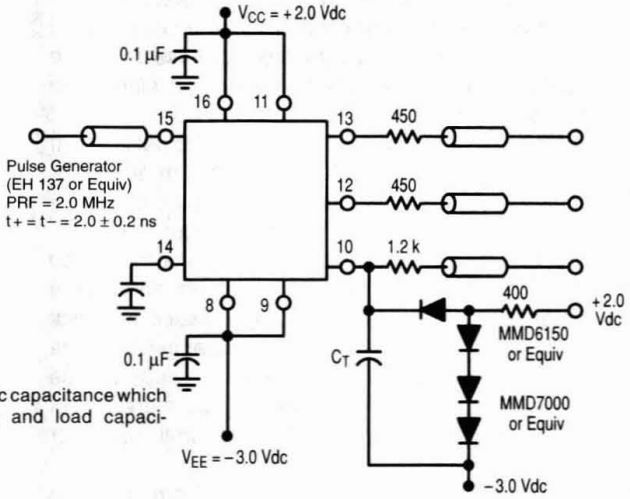
Figure 6. AC Characteristics – MECL and TTL Outputs



All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Unused outputs are connected to a 50 Ω ± 1% resistor to ground.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.



Characteristic	Symbol	Pin Under Test	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Unit	Pulse In	Pulse Out	+2.0 Vdc	–3.0 Vdc	Gnd
Propagation Delay	t_{15+10+}	10	—	22	—	17	25	—	27	ns	15	10	11,16	8,9	14
	t_{15-10-}	10	—	19	—	12	18	—	18			10			
	t_{15+12-}	12	—	5.2	—	4.3	5.5	—	5.8			12			
	t_{15-12+}	12	—	5.0	—	3.7	5.2	—	5.2			12			
	t_{15+13+}	13	—	4.8	—	4.0	5.0	—	5.2			13			
	t_{15-13-}	13	—	5.0	—	4.0	5.0	—	5.1			13			
Rise Time	t_{12+}	12	—	4.0	—	3.0	4.0	—	4.4	ns	15	12	11,16	8,9	14
	t_{13+}	13	—	4.0	—	3.0	4.0	—	4.4	ns	15	13	11,16	8,9	14
Fall Time	t_{12-}	12	—	4.0	—	3.0	4.0	—	4.0	ns	15	12	11,16	8,9	14
	t_{13-}	13	—	4.0	—	3.0	4.0	—	4.0	ns	15	13	11,16	8,9	14

Characteristic	Pin Under Test	+25°C Min	+25°C Typ	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: +2.0 Vdc	–3.0 Vdc
Sine Wave Amplitude	2	650	750	mVp-p	1	8,9
	3	650	750			

Figure 7. AC Test Circuit – Sine Wave Output

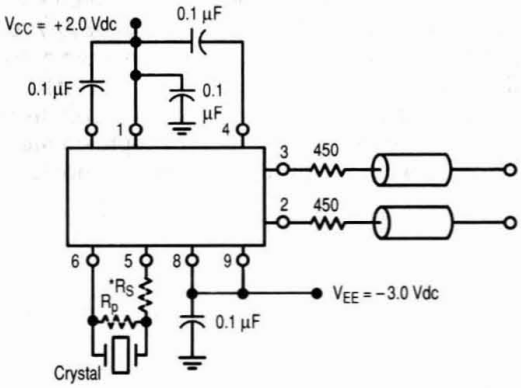
All output cables to the scope are equal lengths of 50 Ω coaxial cable. All unused cables must be terminated with a 50 Ω ± 1% resistor to ground.

450 Ω resistor and the scope termination impedance constitute a 10:1 attenuator probe.

Crystal — Reeves Hoffman Series Mode,
Series Resistance Minimum at Fundamental
f = 10 MHz
R_E = 5 Ω

*R_S = 15 kΩ is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance ≤ 155 Ω

R_p: will improve start up problems value: 200–500 Ω



OPERATING CHARACTERISTICS

The MC12061 consists of three basic sections: an oscillator with AGC and two translators (NO TAG). Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or TTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal — an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The MC12061 is designed to operate from a single supply — either +5.0 Vdc or –5.2 Vdc. Although each translator has separate V_{CC} and V_{EE} supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate V_{EE} pin from the TTL translator helps minimize transient disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to V_{EE} (pin 8). With the translators not powered, supply current drain is typically reduced from 42 mA to 23 mA for the MC12061.

Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup. However, the variation should be within approximately ±0.001% from unit to unit.

Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small — about –0.08 ppm/°C for MC12061 operating at 8.0 MHz (see NO TAG).

Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mV_{p-p} (no load) to 500 mV_{p-p} (120 ohm ac load). Approximately 500 mV_{p-p} can be provided across 50 ohms by slightly increasing the dc current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15 pF) to the 50 ohm load of Figure 9. The dc voltage level at pin 2 or 3 is nominally 3.5 Vdc with V_{CC} = +5.0 Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent. The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approximately load independent except that the higher harmonic levels (greater than the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates, as defined in NO TAG, and the TTL output (pin 10) will drive up to ten gates, as defined in NO TAG.

Noise Characteristics

Noise level evaluation of the sine wave outputs using the circuit of NO TAG, with operation at or 9.0 MHz, indicates the following characteristics:

1. Noise floor (200 kHz from oscillator center frequency) is approximately –122 dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
2. Close-in noise (100 Hz from oscillator center frequency) is approximately –88 dB when referenced to a 1.0 Hz bandwidth.

Figure 8. Frequency Variation Due to Temperature

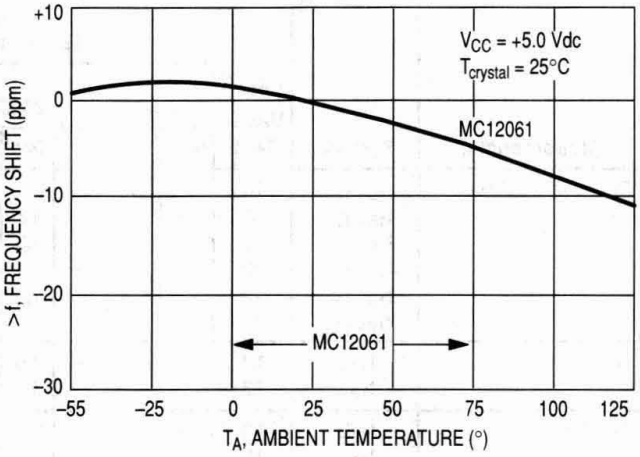
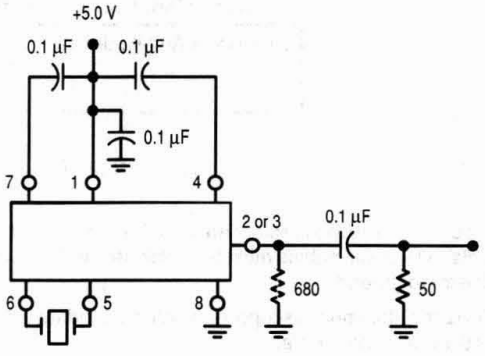


Figure 9. Driving Low Impedance Loads



* See text under signal characteristics.

Figure 10. MECL Translator Load Capability

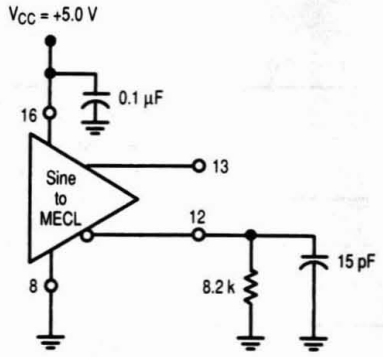


Figure 11. TTL Translator Load Capability

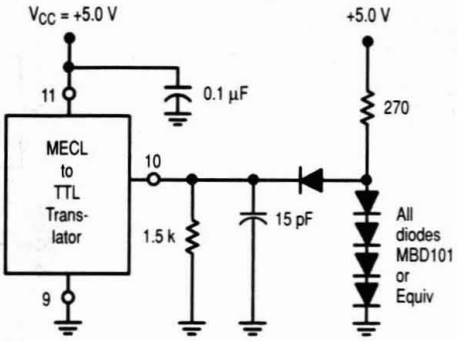
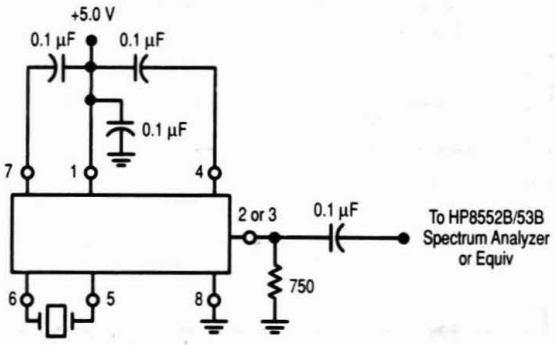


Figure 12. Noise Measurement Test Circuit

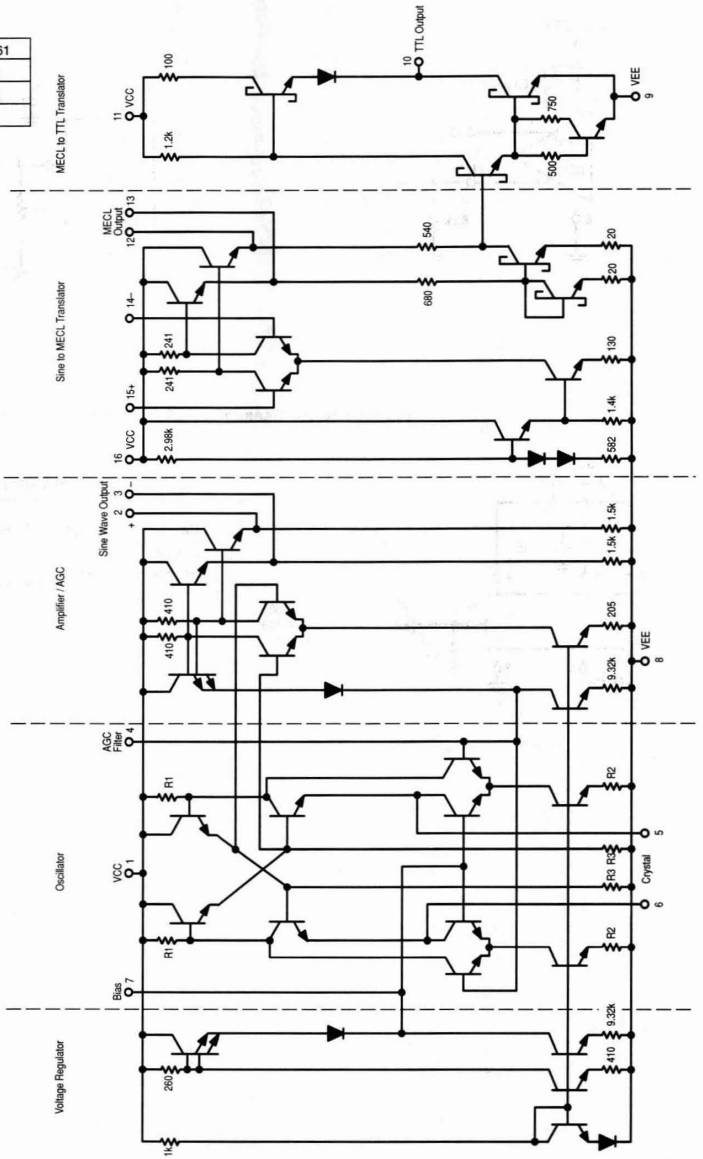


ANALYZER SETTING

Measurement	Sweep	Bandwidth	Video Filter
Noise Floor	50 kHz/div	10 kHz	10 Hz
Close-In Noise	20 kHz/div	10 Hz	10 Hz

Figure 13. Circuit Schematic

RESISTOR	MC12061
R1 (2 Places)	200 Ω
R2 (2 Places)	400 Ω
R3 (2 Places)	2 kΩ



MOTOROLA

1.3 GHz Prescaler

MC12066

MECL PLL COMPONENTS
÷64/256 PRESCALER

SEMICONDUCTOR
TECHNICAL DATA

The MC12066 is a selectable divide by 64/256 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

The MC12066 is pin and functionally compatible to the Plessey SP4666, but with significantly lower power consumption.

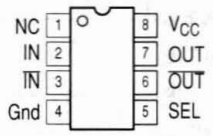
An internal, two stage preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential outputs are provided.

The MC12066 contains an internal low pass filter to reduce harmonic content to a low level. The filter bandwidth is selectable depending on the state of the SEL pin. The typical –3.0 dB bandwidth is 4.3 MHz for ÷256 mode, and 17.2 MHz for ÷64 mode. Figures 2 and 3 illustrate typical device performance.

- 1.3 GHz Toggle Frequency
- Operating Supply Voltage of 2.7 to 5.5 V
- Low–Power 7.5 mA Typical at V_{CC} = 5.0 V
- High Input Sensitivity, 5 mVrms Max at V_{CC} = 2.7 to 5.5, T_A = –40 to 85°C
- 600 mV Minimum Peak–to–Peak Output Swing
- Differential Outputs

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

TRUTH TABLE

SEL	Prescaler
L	256
H	64

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 175	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ[1]	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max}[2] f_{min}	1.3 –	1.6 –	– 50	GHz MHz
Supply Current at 5.5 V	I_{CC}	–	7.5	12	mA
Output Voltage (Load =12 pF)	V_{out}	0.6	1.0	–	V_{pp}
Input Voltage Sensitivity 50–200 MHz 200–1300 MHz	$V_{in\ min}$	 – –	 2.5 0.5	 10 5	mVrms
Input Overload	$V_{in\ max}$	200	400	–	mVrms
Input HIGH Voltage (SEL)	V_{IH}	$0.7V_{CC}$	–	–	V
Input LOW Voltage (SEL)	V_{IL}	–	–	$0.3V_{CC}$	V

NOTES: 1. Typical measured at 25°C, 5.0 V
2. See Figure 2

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12066D	T_A = –40° to +85°C	SO–8

Figure 1. Prescaler Block Diagram

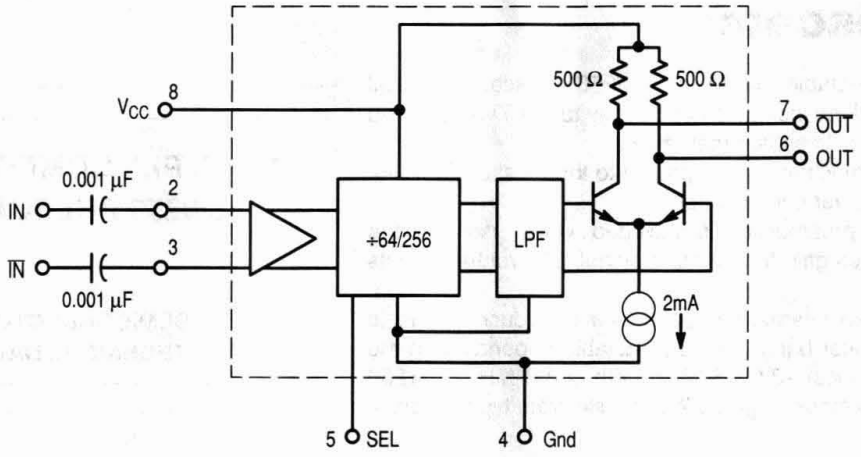


Figure 2. Typical Input Signal Amplitude and Output Peak–to–Peak Amplitude versus Input Frequency With a Divide Ratio of 64

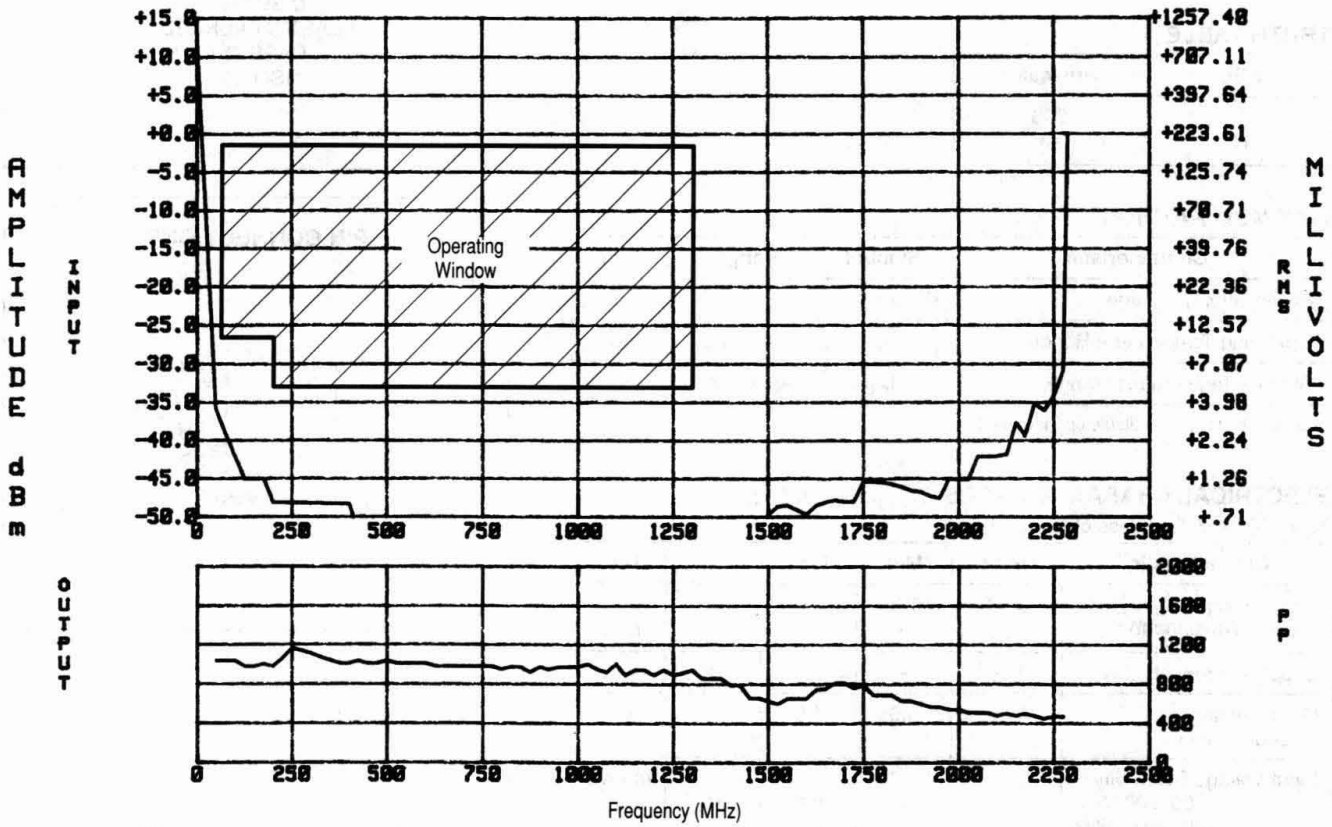


Figure 3. Output Spectrum Illustrating Harmonic Suppression, Input Frequency 900 MHz, ÷64 Divide Ratio

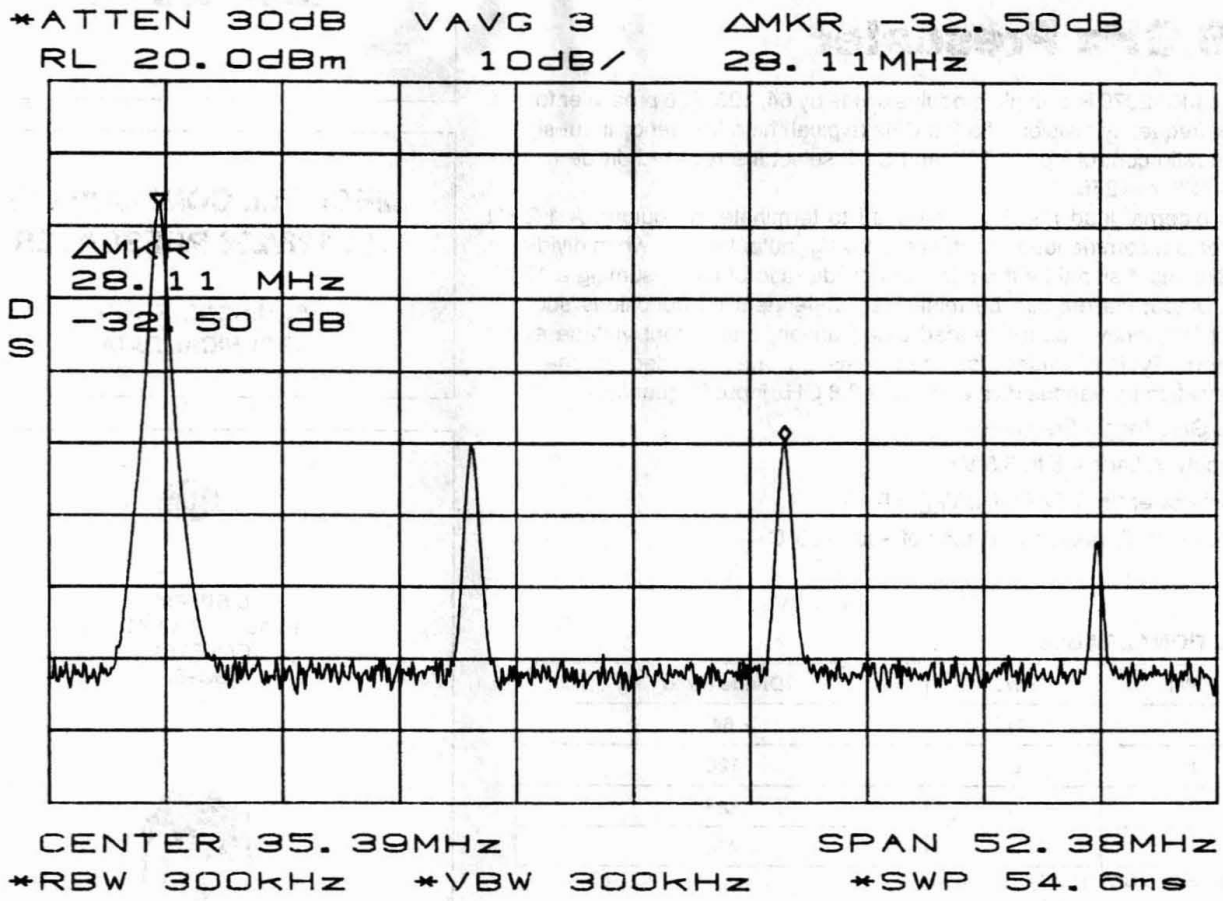
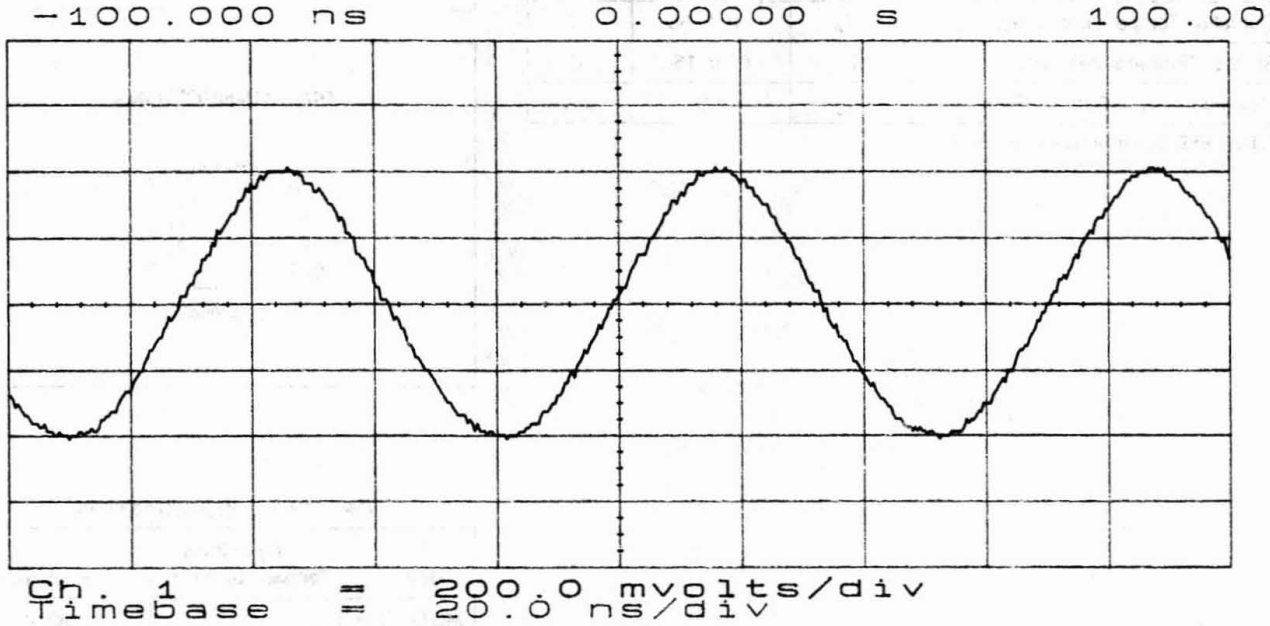


Figure 4. Typical Output Waveform, Input Frequency 900 MHz, ÷64 Divide Ratio



MOTOROLA

2.8 GHz Prescaler

The MC12079 is a single modulus divide by 64, 128, 256 prescaler for low power frequency division of a 2.8 GHz (typical) high frequency input signal. Divide ratio control inputs SW1 and SW2 select the required divide ratio of ÷64, ÷128, or ÷256.

An external load resistor is required to terminate the output. A 1.2 kΩ resistor is recommended to achieve a 1.6 V_{pp} output swing, when dividing a 1.1 GHz input signal by the minimum divide ratio of 64, assuming a 12 pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V_{out} specification for various divide ratios at 2.8 GHz input frequency.

- 2.8 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 9mA Typical at V_{CC} = 5.0 V
- Operating Temperature Range of –40 to 85°C

FUNCTIONAL TABLE

SW1	SW2	Divide Ratio
H	H	64
H	L	128
L	H	128
L	L	256

NOTE: SW1 & SW2: H = V_{CC}, L = Open.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	4.0	mA

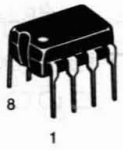
NOTE: ESD data available upon request.

MC12079

MECL PLL COMPONENTS ÷64/128/256 PRESCALER

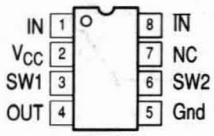
SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12079D	T_A = – 40° to +85°C	SO–8
MC12079P		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		ft	0.25	3.4	2.8	GHz
Supply Current Output (Pin 2)		I_{CC}	–	9.0	11.5	mA
Input Voltage Sensitivity	250–500 MHz 500–2800 MHz	V_{in}	400 100	– –	1000 1000	mVpp
Divide Ratio Control Input High (SW)		V_{IH}	V_{CC}	V_{CC}	V_{CC}	V
Divide Ratio Control Input Low (SW)		V_{IL}	Open	Open	Open	–
Output Voltage Swing (C_L = 12 pF; R_L = 1.2 kΩ; I_O = 2.7 mA)[1] (C_L = 12 pF; R_L = 2.2 kΩ; I_O = 1.5 mA)[2] (C_L = 12 pF; R_L = 3.9 kΩ; I_O = 0.85 mA)[3]		V_{out}	1.0	1.6	–	V_{pp}

NOTES: 1. Divide ratio of ÷64 at 2.8 GHz.
2. Divide ratio of ÷128 at 2.8 GHz.
3. Divide ratio of ÷256 at 2.8 GHz.

Figure 1. Logic Diagram (MC12079)

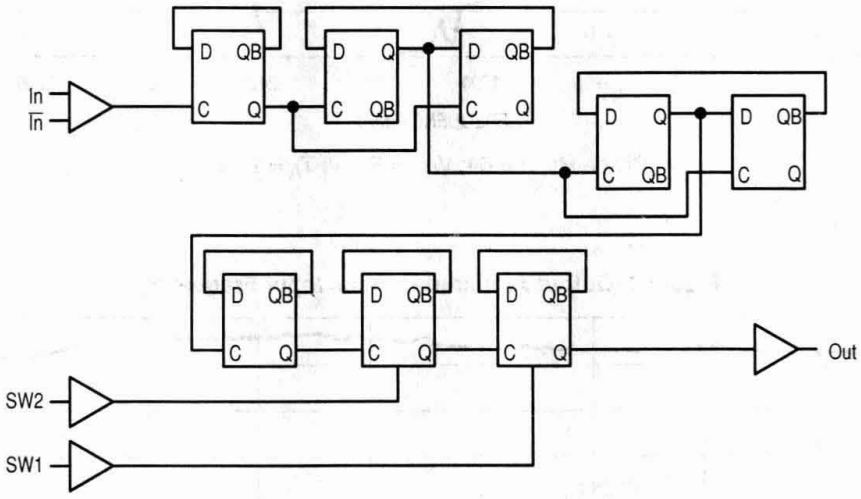
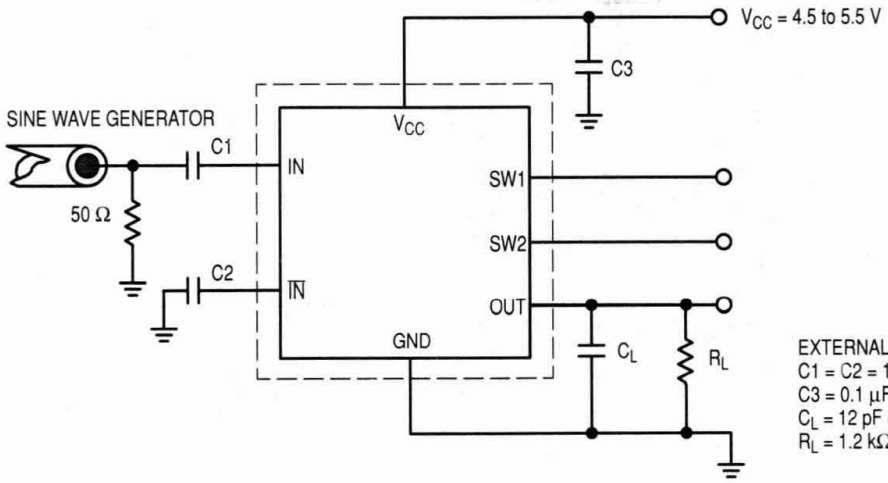
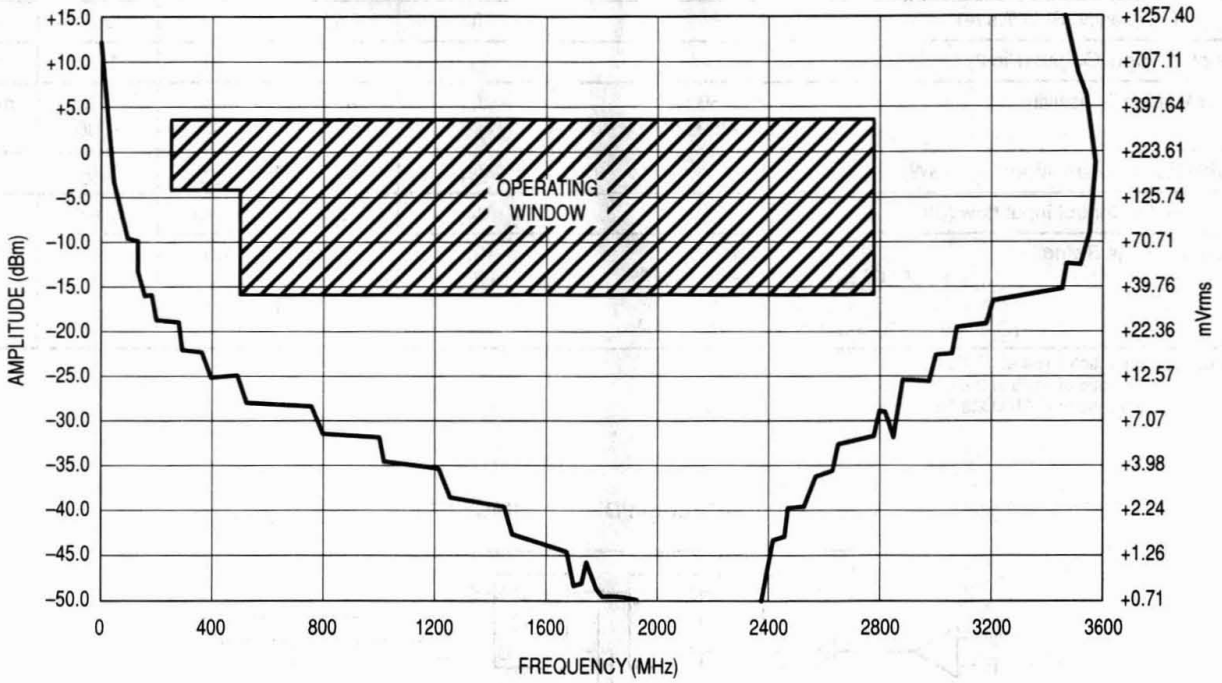


Figure 2. AC Test Circuit



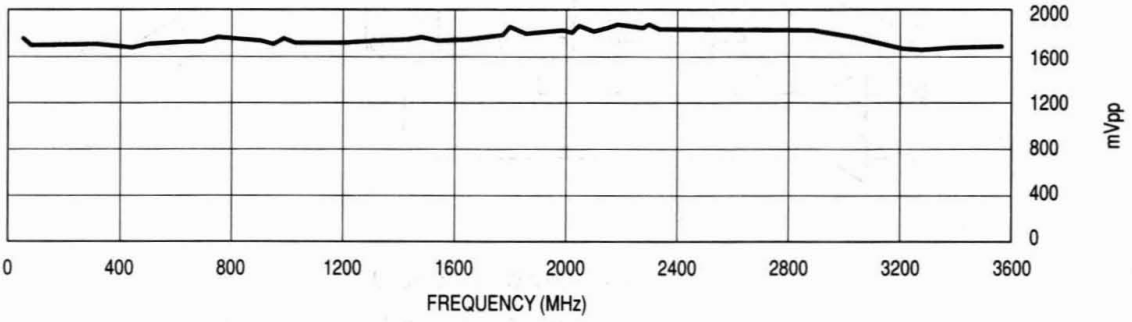
EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 μF
C_L = 12 pF (Including Scope and Jig Capacitance)
R_L = 1.2 kΩ (for ÷64 at 2.8 GHz)

Figure 3. Input Signal Amplitude versus Input Frequency



Divide Ratio = 64; V_{CC} = 5.0 V; T_A = 25°C

Figure 4. Output Amplitude versus Input Frequency



MOTOROLA

1.1 GHz Prescaler

MC12080

MECL PLL COMPONENTS
÷10/20/40/80 PRESCALER

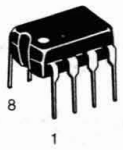
SEMICONDUCTOR
TECHNICAL DATA

The MC12080 is a single modulus divide by 10, 20, 40, 80 prescaler for low power frequency division of a 1.1 GHz high frequency input signal. Divide ratio control inputs SW1, SW2 and SW3 select the required divide ratio of ÷10, ÷20, ÷40, or ÷80.

An external load resistor is required to terminate the output. A 820 Ω resistor is recommended to achieve a 1.2 V_{pp} output swing, when dividing a 1.1 GHz input signal by the minimum divide by ratio of 10, assuming a 8.0 pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V_{out} specification for various divide ratios at 1.1 GHz input frequency.

- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 3.7mA Typical at V_{CC} = 5.0 V
- Operating Temperature Range of –40 to 85°C

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW1	SW2	SW3	Divide Ratio
L	L	L	80
L	L	H	40
L	H	L	40
L	H	H	20
H	L	L	40
H	L	H	20
H	H	L	20
H	H	H	10

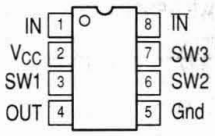
NOTE: SW1, SW2 and SW3: H = V_{CC}, L = Open.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	10	mA

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12080D	T_A = – 40° to +85°C	SO–8
MC12080P		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		ft	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)		I_{CC}	–	3.7	5.0	mA
Input Voltage Sensitivity	100–250 MHz 250–1100 MHz	V_{in}	400 100	– –	1000 1000	mVpp
Divide Ratio Control Input High (SW1, SW2, SW3)		V_{IH}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input Low (SW1, SW2, SW3)		V_{IL}	Open	Open	Open	–
Output Voltage Swing[1]	R_L = 820 Ω, I_O = 4.0 mA for ÷10 R_L = 1.6 kΩ, I_O = 2.1 mA for ÷20 R_L = 3.3 kΩ, I_O = 1.1 mA for ÷40 R_L = 6.2 kΩ, I_O = 0.57 mA for ÷80	V_{out}	0.8	1.2	–	V_{pp}

NOTE: 1. Assumes 8.0 pF load and 1.1 GHz input frequency (typical), I_O at V_{CC} = 5.0 V and T_A = 25°C

Figure 1. Logic Diagram (MC12080)

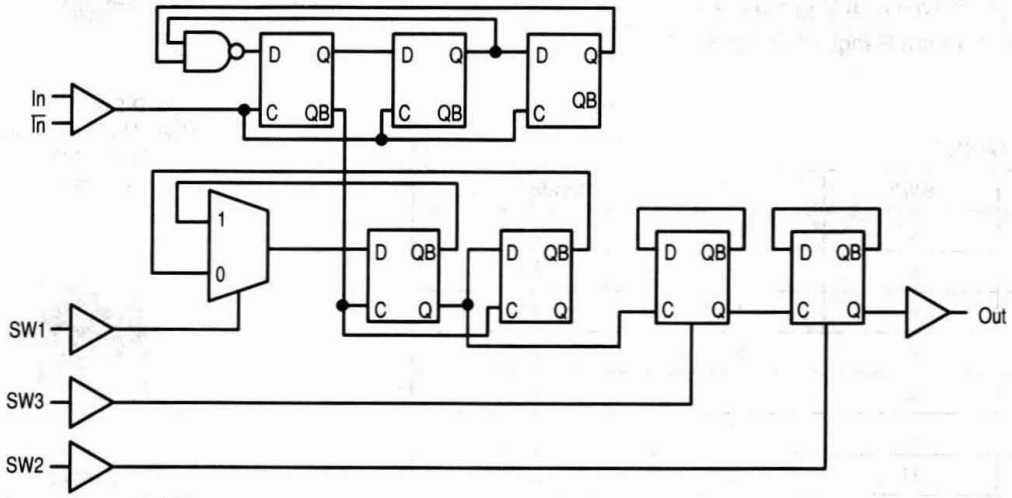
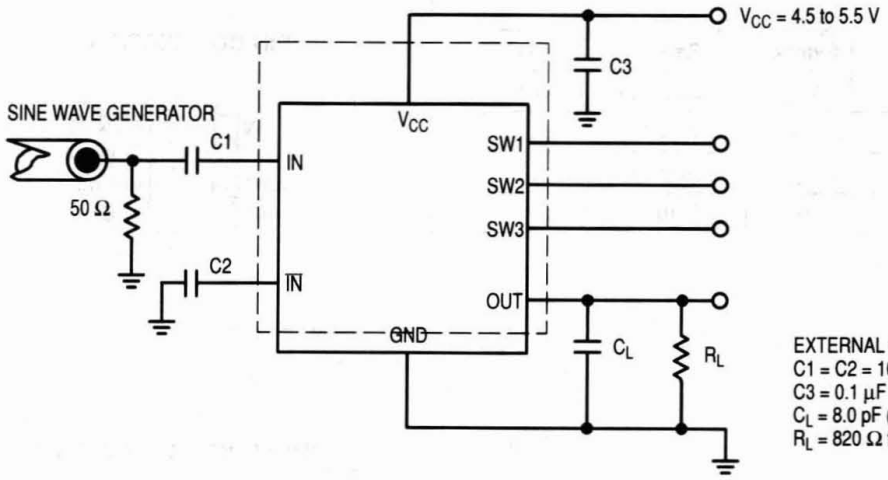
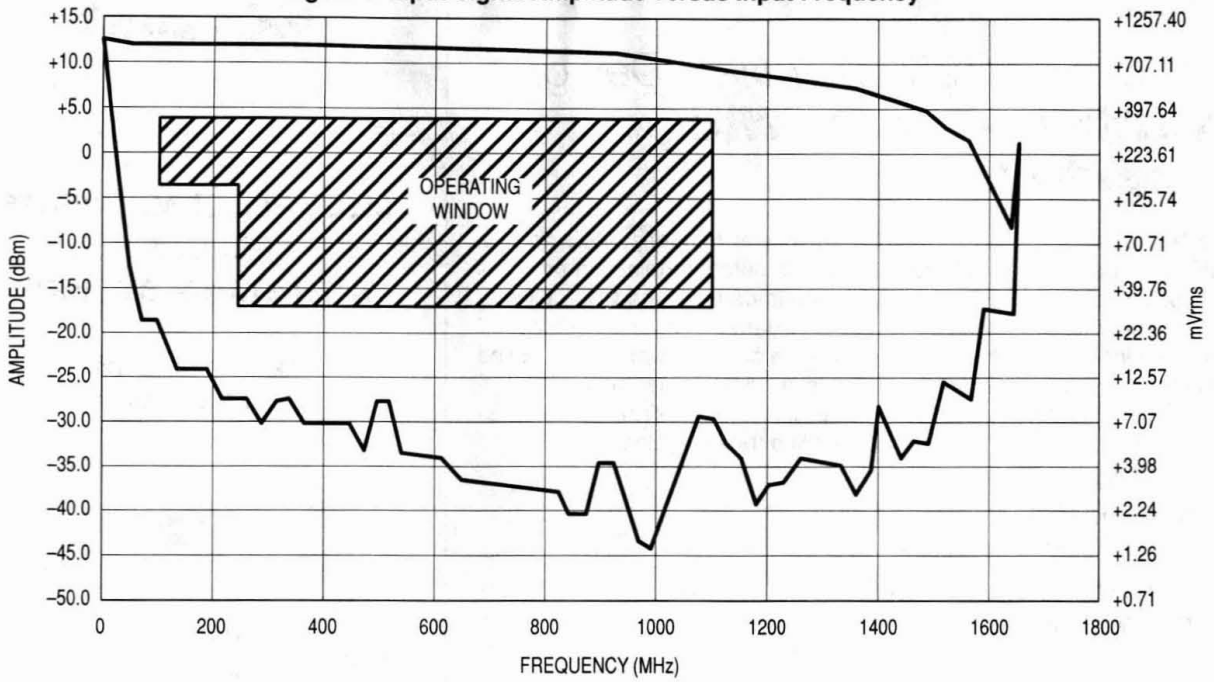


Figure 2. AC Test Circuit



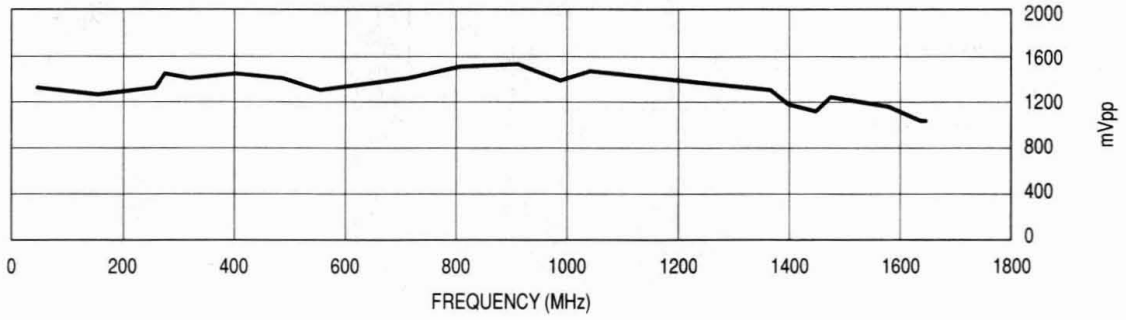
EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and Jig Capacitance)
R_L = 820 Ω for ÷10 at 1.1 GHz

Figure 3. Input Signal Amplitude versus Input Frequency



Divide Ratio = 10; V_{CC} = 5.0 V; T_A = 25°C

Figure 4. Output Amplitude versus Input Frequency



MOTOROLA

MC12083

Consider MC12093 for New Designs

1.1 GHz Prescaler With Stand-By Mode

The MC12083 is a ÷2 prescaler for low power frequency division of a 1.1 GHz high frequency input signal. On–chip output termination provides output current to drive a 2.0 pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added parallel from the OUT Pin to Gnd to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Stand–By mode is featured to reduce current drain to 250 μA typical when the stand–by pin SB is switched LOW disabling the prescaler.

- 1.1 GHz Toggle Frequency
- Supply Voltage 2.7 to 5.5 V
- Low Power 4.5 mA Typical at V_{CC} = 2.7 V
- Operating Temperature –40 to 85°C
- On–Chip Termination

MECL PLL COMPONENTS
÷2 PRESCALER
WITH STAND–BY MODE

SEMICONDUCTOR
TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

P SUFFIX
PLASTIC PACKAGE
CASE 626

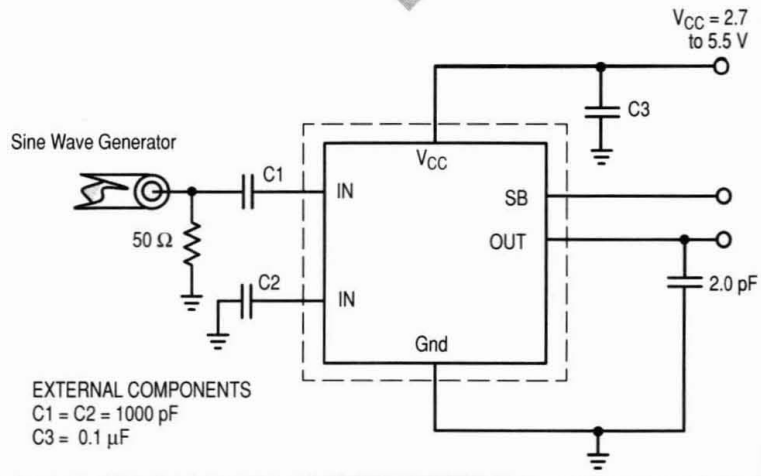
MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	10	mA

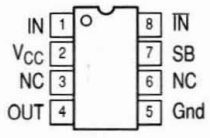
NOTE: ESD data available upon request.

Not Recommended For New Designs

Figure 1. AC Test Circuit



PIN CONNECTIONS



(Top View)

A LOW on the Stand–By Pin 7 disables the device.

ORDERING INFORMATION

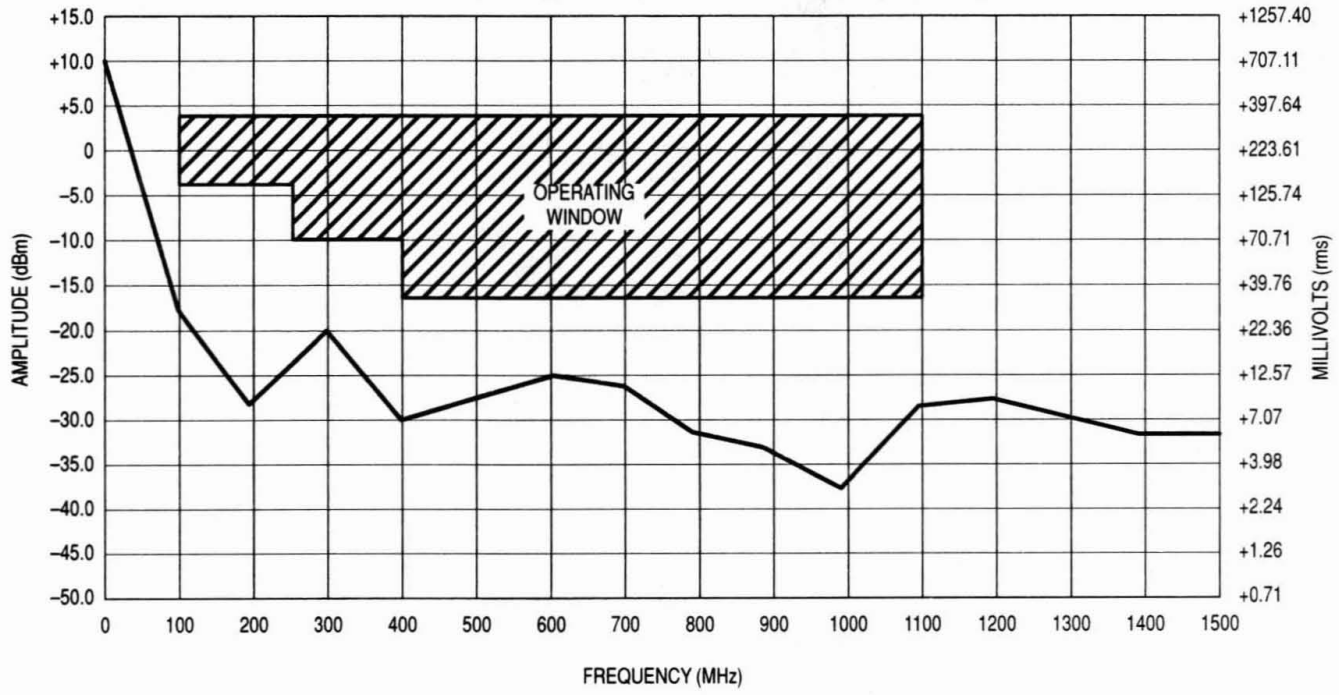
Device	Operating Temperature Range	Package
MC12083D	T_A = – 40° to +85°C	SO–8
MC12083P		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		ft	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)	V_{CC} = 3.0 V V_{CC} = 5.5 V	I_{CC}	– –	4.4 4.8	6.5 6.5	mA
Standby Current	V_{CC} = 3.0 V V_{CC} = 5.5 V	ISB	– –	250 500	350 600	µA
Standby Input HIGH (SB)		V_{IH}	2.0	–	V_{CC}	V
Standby Input LOW (SB)		V_{IL}	Gnd	–	0.8	V
Output Voltage Swing (Note 1) 2.0 pF Load @ 500 MHz Input 2.0 pF Load @ 750 MHz Input 2.0 pF Load @ 1100 MHz Input		V_{OUT}	 700 600 400	 800 700 450	 – – –	mVpp
Input Voltage Sensitivity	100–250 MHz 250–400 MHz 400–1100 MHz	V_{IN}	400 200 100		1000 1000 1000	mVpp

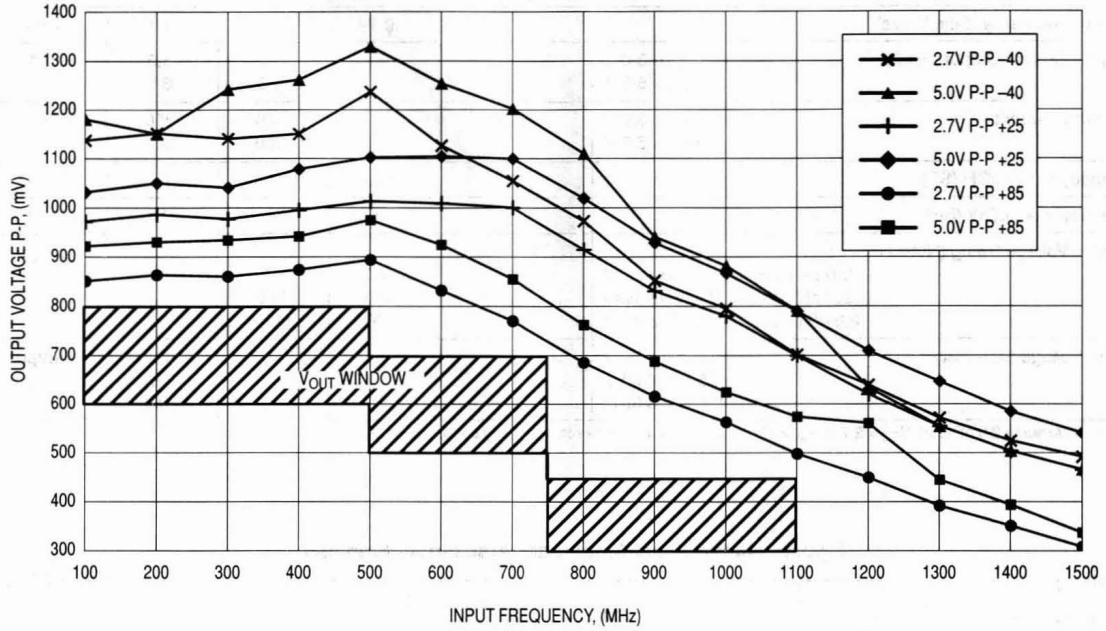
NOTE: 1. Assume 2.0 pF load, V_{CC} = 2.7 V, V_{IN} =minimum specification for each frequency band, T_A = 85°C

Figure 2. Input Signal Amplitude versus Input Frequency



Divide Ratio = 2; V_{CC} = 2.7 V; T_A = 25°C; Output Loaded With 2.0 pF

Figure 3. 12083 Output Peak–to–Peak at 2.0 pF Load



MOTOROLA

MC12089

2.8 GHz Prescaler

The MC12089 is a single modulus divide by 64 and 128 prescaler for low power frequency division of a 2.8 GHz high frequency input signal. The low power (10.2 mA typical at 5.0 V) and high operating frequency features make this prescaler ideal in satellite TV receiver applications.

Divide ratio control input SW selects the required divide ratio of ÷64 or ÷128.

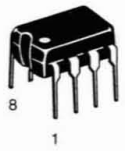
On–chip output termination provides 2.5 mA of output current to drive a 12 pF (typical) high impedance load. The output voltage swing under typical supply voltage and temperature conditions is 1.2 V. If additional drive is required for the prescaler output, an external resistor can be added in parallel from the OUT pin to Gnd to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

- 2.8 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power Dissipation 51 mW Typical
- Operating Temperature Range of –40 to 85°C

MECL PLL COMPONENTS
÷64/128 PRESCALER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626

FUNCTIONAL TABLE

SW	Divide Ratio
H	64
L	128

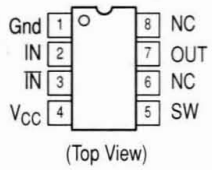
NOTE: H = V_{CC}, L = Open.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 4	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Output Current, Pin 7	I_O	4.0	mA

NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12089D	T_A = – 40° to +85°C	SO–8
MC12089P		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		ft	0.25	3.4	2.8	GHz
Supply Current Output (Pin 2)		I_{CC}	–	10.2	14.5	mA
Input Voltage Sensitivity	250–500 MHz 500–2800 MHz	V_{in}	400 100	– –	1000 1000	mVpp
Divide Ratio Control Input High (SW)		V_{IH}	V_{CC}	V_{CC}	V_{CC}	V
Divide Ratio Control Input Low (SW)		V_{IL}	Open	Open	Open	–
Output Voltage Swing (Note 1)		V_{out}	0.8	1.2	–	V_{pp}

NOTE: 1. Assumes C_L = 12 pF

Figure 1. Logic Diagram (MC12089)

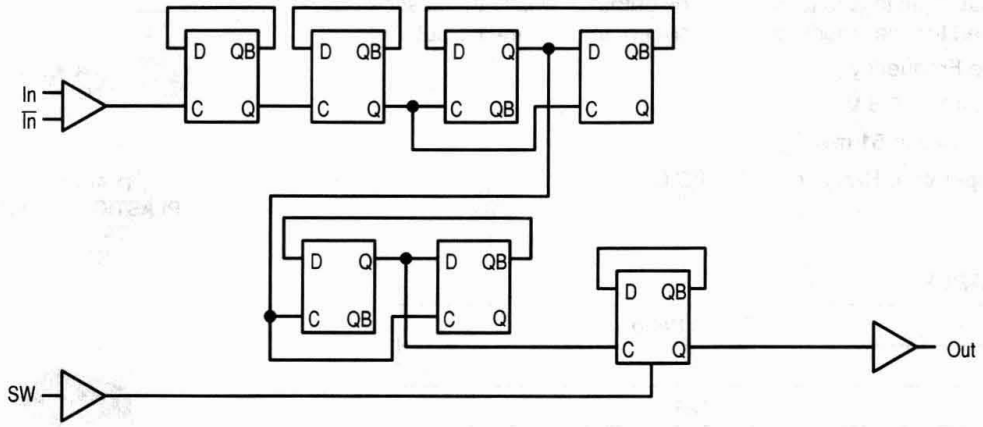
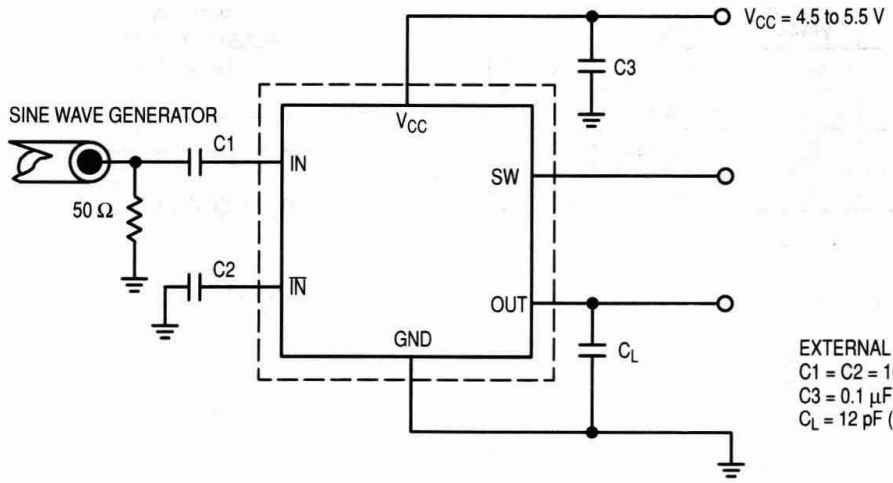
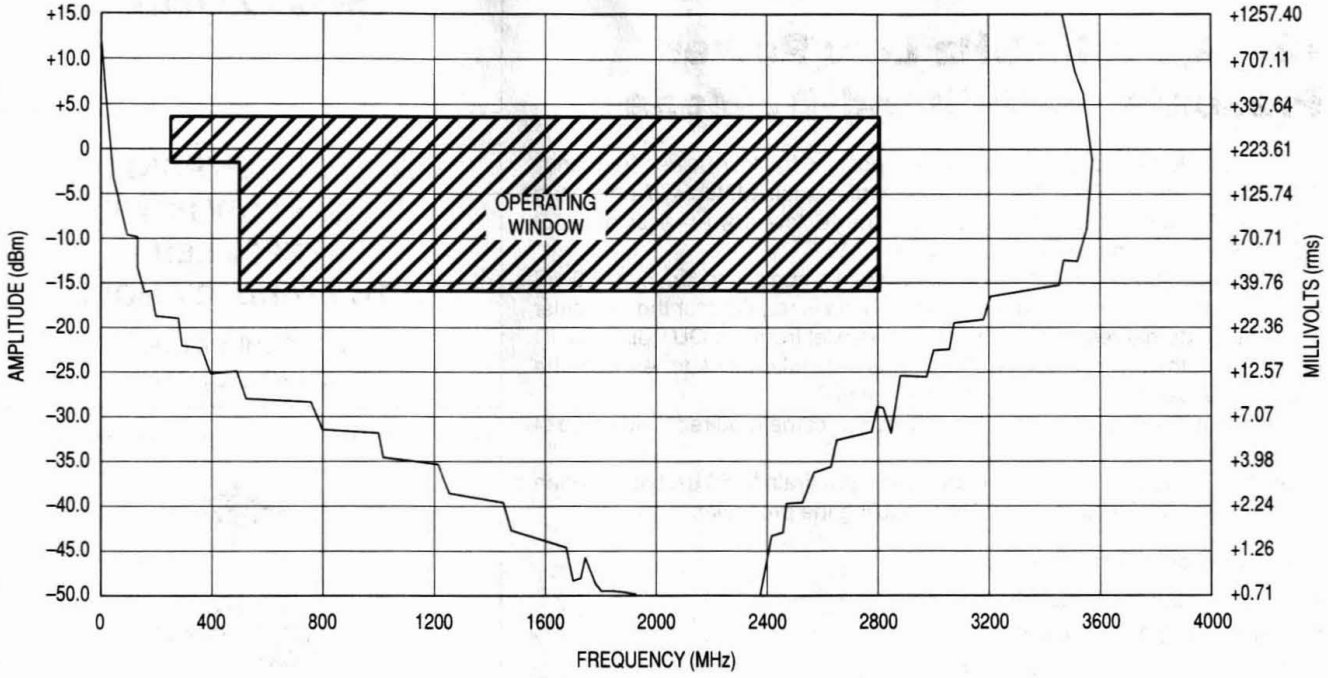


Figure 2. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 12 pF (Including Scope and Jig Capacitance)

Figure 3. Input Signal Amplitude versus Input Frequency



Divide Ratio = 64; V_{CC} = 5.0 V; T_A = 25°C

MOTOROLA

MC12093

÷2, ÷4, ÷8 1.1GHz Low Power Prescaler with Stand-By Mode

The MC12093 is a single modulus prescaler for low power frequency division of a 1.1 GHz high frequency input signal. Motorola's advanced MOSAIC™ V technology is utilized to acheive low power dissipation of 6.75 mW at a minimum supply voltage of 2.7 V.

On–chip output termination provides output current to drive a 2.0 pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Divide ratio control inputs SW1 and SW2 select the required divide ratio of ÷2, ÷4, or ÷8.

Stand–By mode is featured to reduce current drain to 50 µA typical when the standby pin SB is switched LOW disabling the prescaler.

- 1.1 GHz Toggle Frequency
- Supply Voltage 2.7 V to 5.5 Vdc
- Low Power 3.0 mA Typical
- Operating Temperature –40 to 85°C
- Divide by 2, 4 or 8 Selected by SW1 and SW2 Pins
- On–Chip Termination

MOSAIC V is a trademark of Motorola

MECL PLL COMPONENTS
÷2, ÷4, ÷8 LOW POWER PRESCALER WITH STAND–BY MODE

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

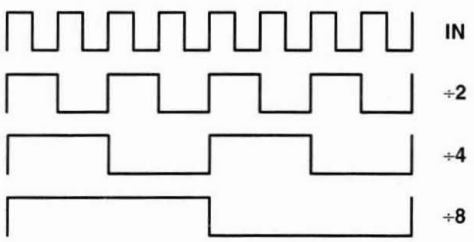
SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

FUNCTIONAL TABLE

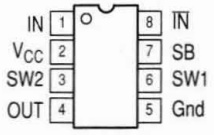
SW	SW2	Divide Ratio
L	L	8
H	L	4
L	H	4
H	H	2

NOTES: 1. SW1 & SW2: H = (V_{CC} – 0.5 V) to V_{CC}; L = Open.
2. SB: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

Function Chart



PIN CONNECTIONS



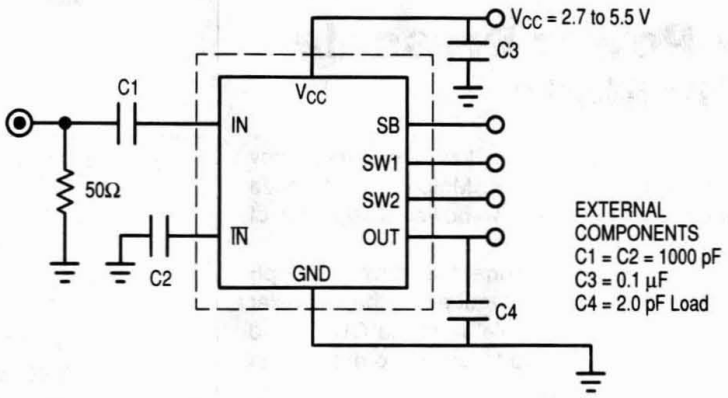
(Top View)

A LOW on the Stand–By Pin 7 disables the device.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12093D	T_A = – 40° to +85°C	SO–8
MC12093SD		SSOP–8

Figure 1. AC Test Circuit



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 6.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	Tstg	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	4.0	mA

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	ft	0.1	1.4	1.1	GHz
Supply Current	I_{CC}	–	3.0	4.5	mA
Stand–By Current	ISB	–	120	200	µA
Stand–By Input HIGH (SB)	V_{IH1}	2.0	–	V_{CC}	V
Stand–By Input LOW (SB)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input HIGH (SW1 & SW2)	V_{IH2}	V_{CC} – 0.5	V_{CC}	V_{CC} + 0.5	V
Divide Ratio Control Input LOW (SW1 & SW2)	V_{IL2}	OPEN	OPEN	OPEN	
Output Voltage Swing (2.0 pF Load)	V_{OUT}				V_{pp}
Output Frequency 12.5–350 MHz (Note 1)		0.6	0.80	–	
Output Frequency 350–400 MHz (Note 2)		0.5	0.70	–	
Output Frequency 400–450 MHz (Note 3)		0.4	0.55	–	
Output Frequency 450–550 MHz (Note 4)		0.3	0.45	–	
Input Voltage Sensitivity 250–1100 MHz	V_{IN}	100	–	1000	mVpp
100–250 MHz		400	–	1000	

NOTES: 1. Input frequency 1.1 GHz, ÷8, minimum output frequency of 12.5 MHz.
2. Input frequency 700–800 MHz, ÷2.
3. Input frequency 800–900 MHz, ÷2.
4. Input frequency 900–1100 MHz, ÷2.

MOTOROLA

MC12095

2.5 GHz Low Power Prescaler With Stand-By Mode

MECL PLL COMPONENTS
÷2, ÷4 LOW POWER PRESCALER WITH STAND–BY MODE

SEMICONDUCTOR TECHNICAL DATA

The MC12095 is a single modulus prescaler for low power frequency division of a 2.5 GHz high frequency input signal. Motorola's advanced MOSAIC™ V technology is utilized to acheive low power dissipation of 24 mW at a minimum supply voltage of 2.7 V.

On–chip output termination provides output current to drive a 2.0 pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added in parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Divide ratio control input (SW) selects the required divide ratio of ÷2 or ÷4. Stand–By mode is available to reduce current drain to 100µA typical when the standby pin SB is switched LOW disabling the prescaler.

- 2.5 GHz Toggle Frequency
- Supply Voltage 2.7 V to 5.5 Vdc
- Low Power 8.7 mA Typical
- Operating Temperature –40 to 85°C
- Divide by 2 or 4 Selected by the SW Pin

NOTE: For applications up to 1.1 GHz, please consult the MC12093 datasheet.

MOSAIC V is a trademark of Motorola

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

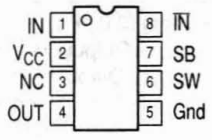
SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

FUNCTIONAL TABLE

SW	Divide Ratio
H	2
L	4

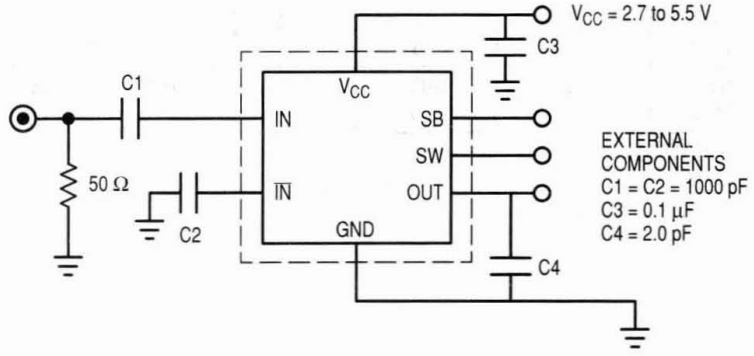
NOTES: 1. SW: H = (V_{CC} – 0.4 V) to V_{CC}; L = OPEN
2. SB: H = 2.0 V to V_{CC}; L = GND to 0.8 V

PIN CONNECTIONS



(Top View)

AC Test Circuit



ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12095D	T_A = – 40° to +85°C	SO–8
MC12095SD		SSOP–8

MAXIMUM RATINGS

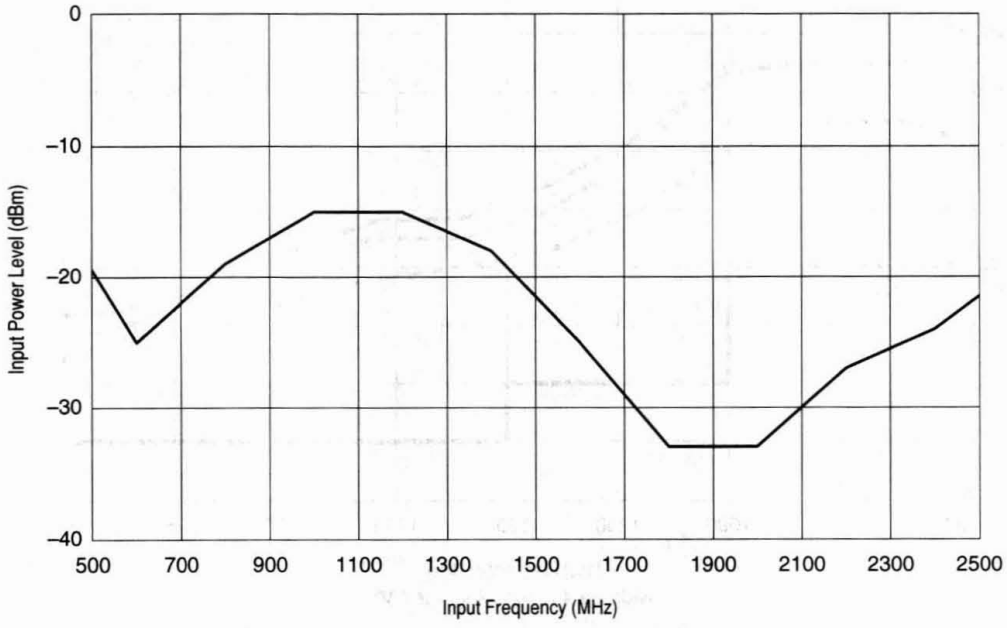
Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 6.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	Tstg	–65 to 150	°C
Maximum Output Current, Pin 4	I_O	8.0	mA

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

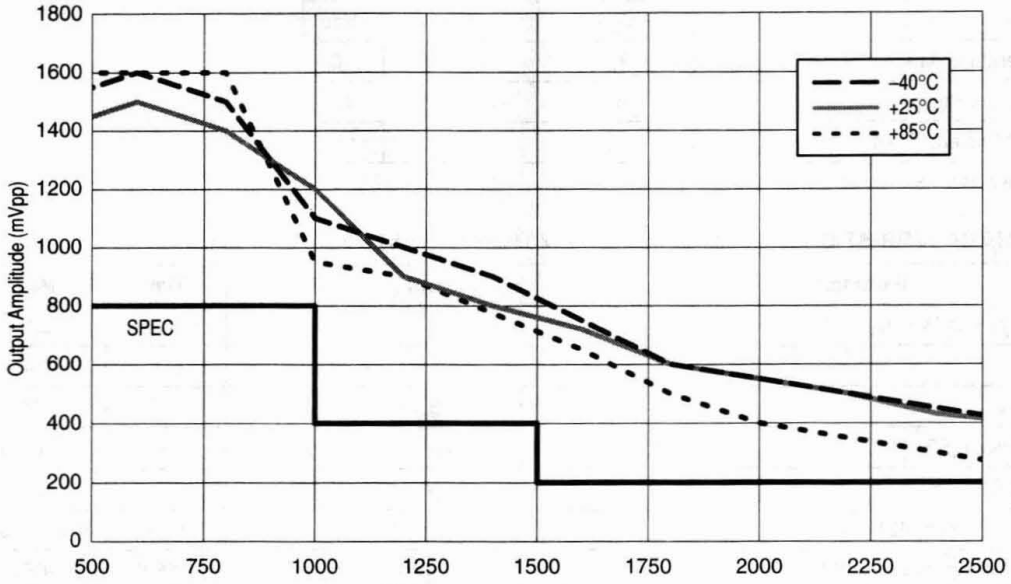
Parameter		Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)		f_t	500	3.0	2.5	GHz
Supply Current		I_{CC}	–	8.7	14	mA
Stand–By Current		ISB	–	100	200	µA
Stand–By Input HIGH (SB)		V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Stand–By Input LOW (SB)		V_{IL1}	GND	–	0.8	V
Divide Ratio Control Input HIGH (SW)		V_{IH2}	V_{CC} – 0.4	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input LOW (SW)		V_{IL2}	OPEN	OPEN	OPEN	
Output Voltage Swing (2pF Load)	500–1000 MHz Input 1000–1500 MHz Input 1500–2500 MHz Input	V_{OUT}	800 400 200	– 450 250	– – –	mVpp
Input Voltage Sensitivity		V_{IN}	200	–	1000	mVpp

Figure 1. Typical Minimum Input Sensitivity versus Input Frequency



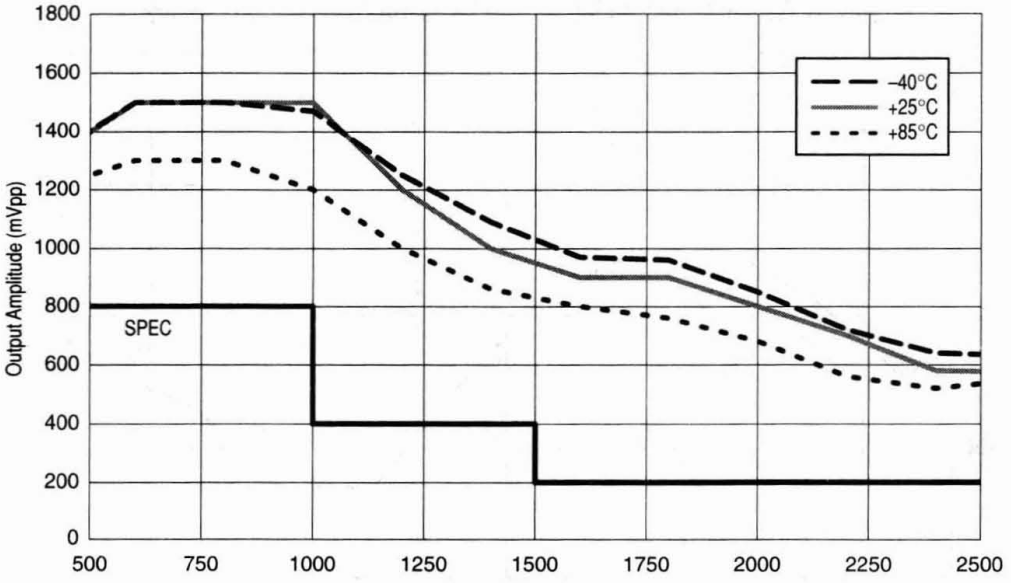
(Divide By 2 Mode, T = 25°C, V_{CC} = 2.7 V)

Figure 2. Typical Output Amplitude versus Frequency over Temperature



(Divide By 2 Mode, V_{CC} = 2.7 V)

Figure 3. Typical Output Amplitude versus Frequency over Temperature



(Divide By 4 Mode, V_{CC} = 2.7 V)

Figure 4. Input Impedance versus Frequency

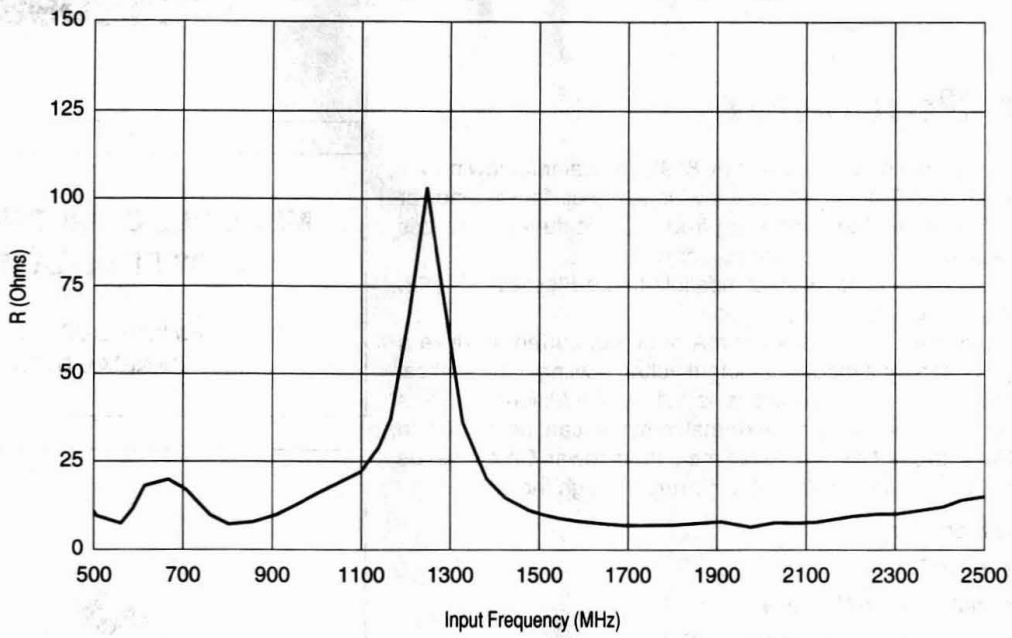
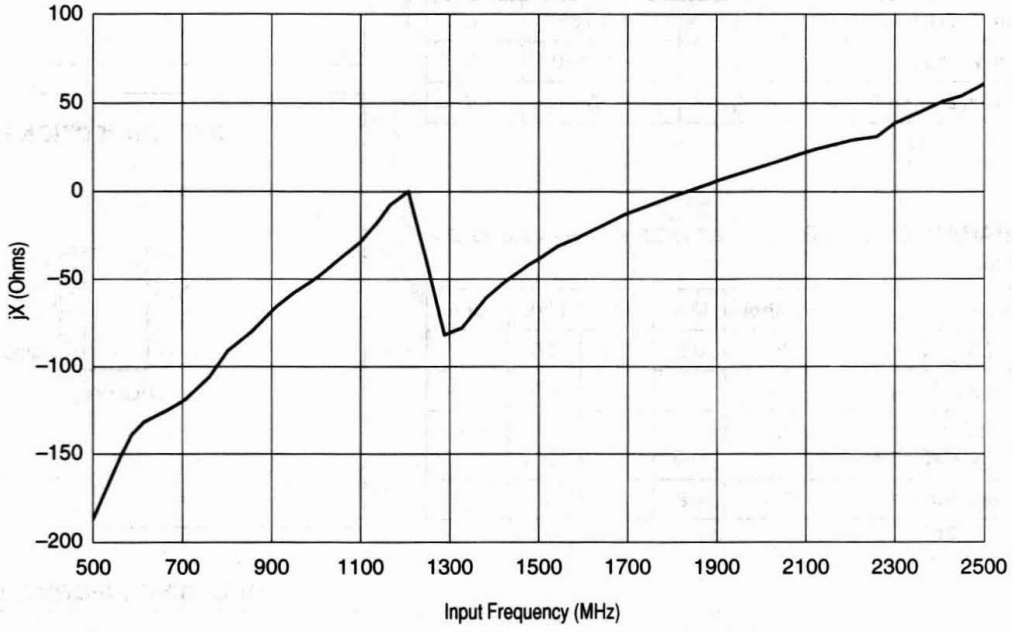


Figure 5. Input Impedance versus Frequency



MOTOROLA

MC12098

2.5 GHz Prescaler

The MC12098 is a single modulus divide by 8192 prescaler for low power frequency division of a 2.5 GHz high frequency input signal. The low power (3.6 mA typical at 5.0 V) and high operating frequency features make this prescaler ideal in satellite TV receiver applications.

The MC12098 is pin and functionally compatible to the Plessey SP4982, but with significantly lower power consumption.

On-chip output termination provides 2.0 mA of output current to drive a 12 pF (typical) high impedance load. The output voltage swing under typical supply voltage and temperature conditions is 1.1 V. If additional drive is required for the prescaler output, an external resistor can be added in parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

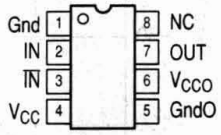
- 2.5 GHz Toggle Frequency
- Supply Voltage 2.7 to 5.5 V
- Low Power Dissipation 18 mW Typical
- Operating Temperature Range of –40 to 85°C

MECL PLL COMPONENTS
÷8192 PRESCALER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 4	V_{CC}	–0.5 to 6.0	VDC
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	Tstg	–65 to 150	°C
Maximum Output Current, Pin 7	I_O	4.0	mA

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	ft	0.5	3.0	2.5	GHz
Supply Current Output (Pin 4)	I_{CC}	-	3.6	6.5	mA
Input Voltage Sensitivity 500–2500 MHz	V_{in}	140	-	1000	mVpp
Output Voltage Swing (Note 1)	V_{out}	0.8	1.1	-	V_{pp}

NOTE: 1. Assumes C_L = 12 pF

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12098D	T_A = –40° to +85°C	SO–8

Figure 1. MC12098 Block Diagram

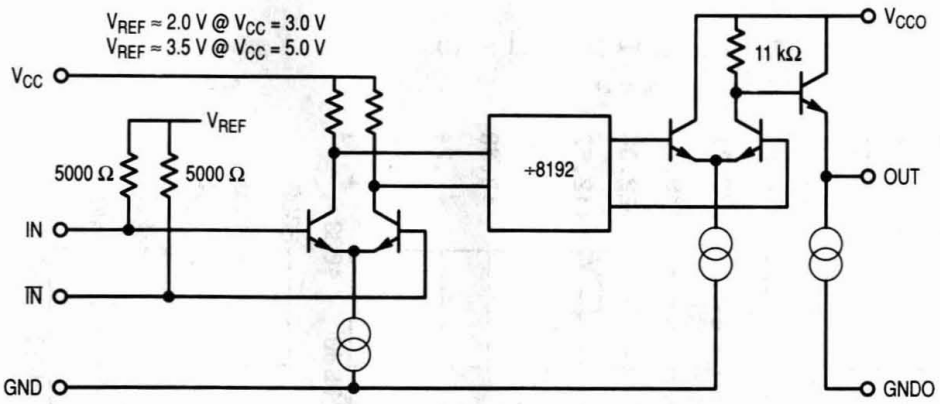
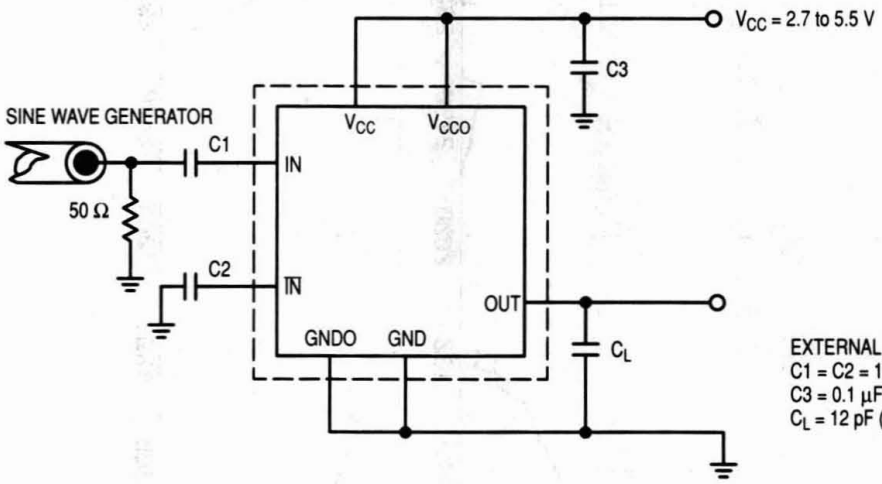
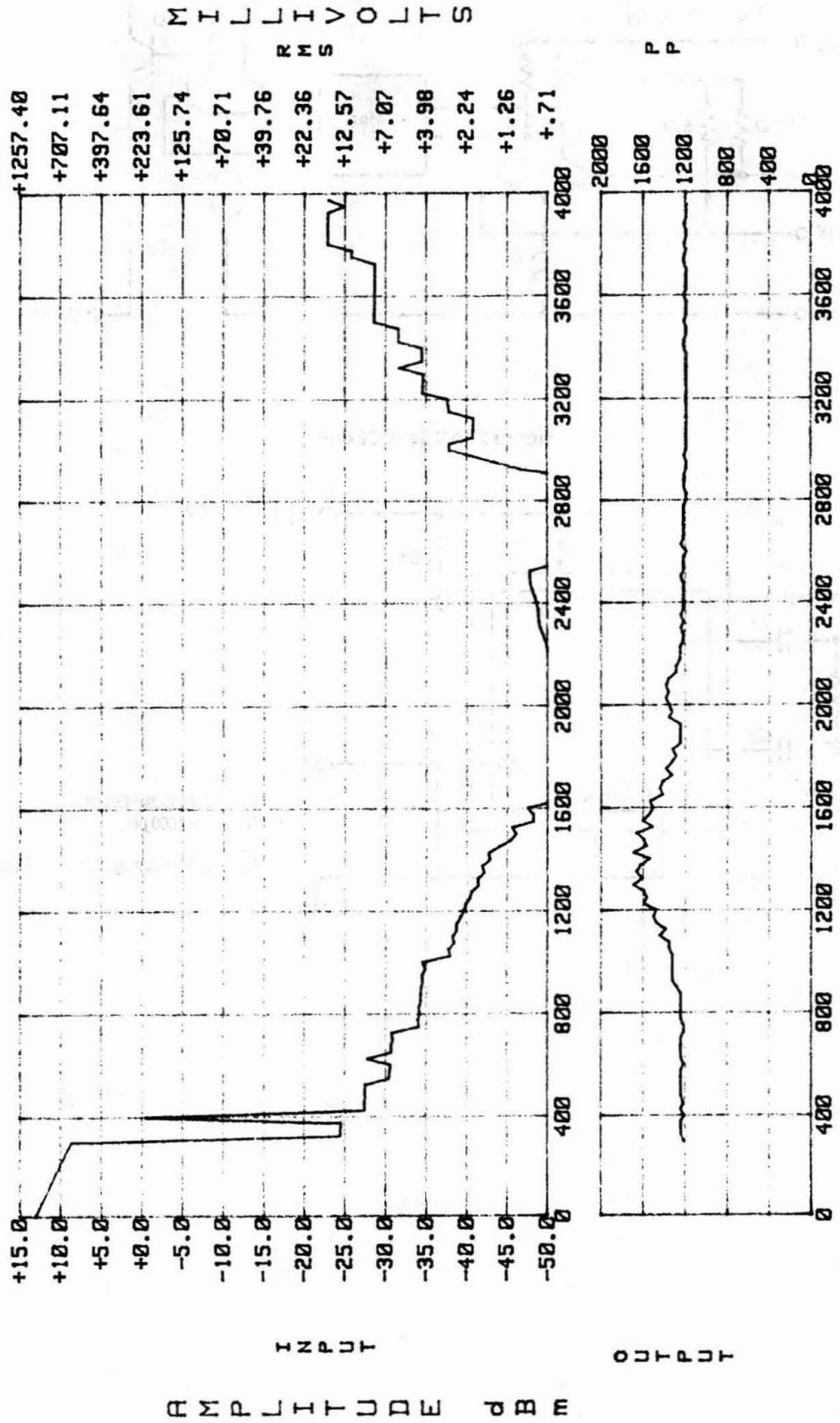


Figure 2. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 μF
C_L = 12 pF (Including Scope and Jig Capacitance)

Figure 3. MC12098 Input Signal Amplitude versus Input Frequency



(V_{CC} = 5.5 V, T_A = 25°C)

Figure 4. Input Impedance versus Frequency

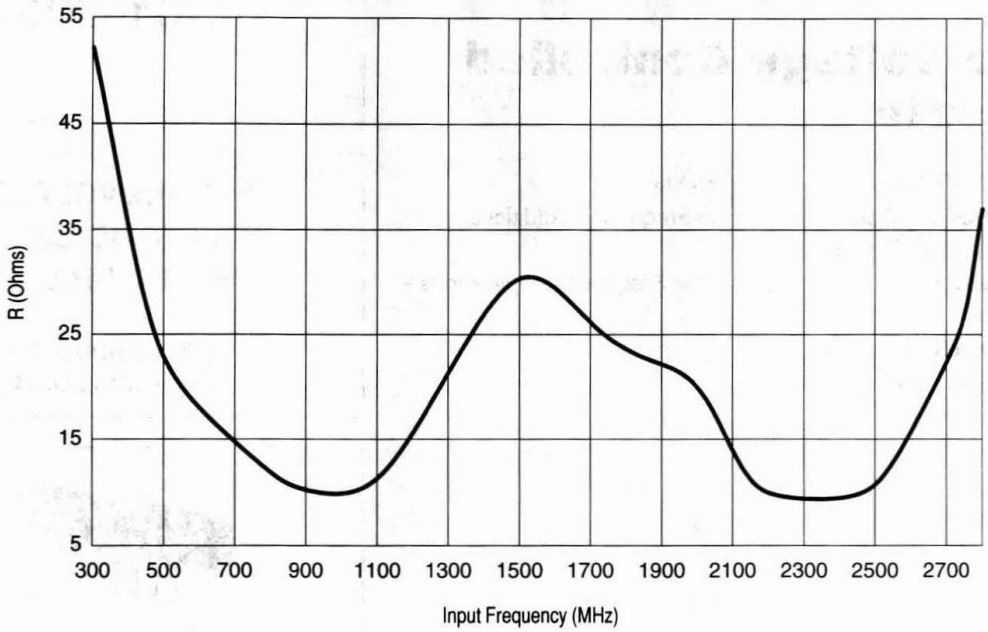
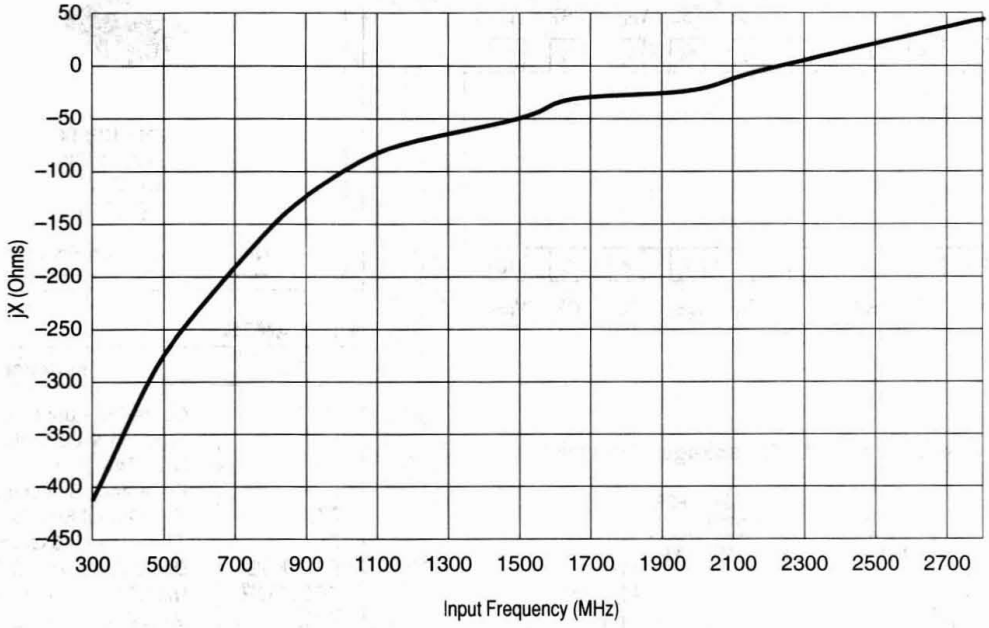


Figure 5. Input Impedance versus Frequency



MOTOROLA

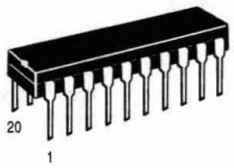
MC12100

200 MHz Voltage Controlled Multivibrator

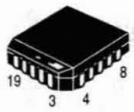
- High Frequency VCM Ideal for PLL Applications
- Single External Resistor Determines Center Frequency; Additional Resistor Determines f/V Sensitivity
- Internal Ripple Counter (1/2, 1/4, 1/8) For Low Frequency Applications – TTL/ECL Outputs
- VCO Output Enable Pins (TTL/ECL Level)
- +5.0 V Single Supply Voltage

200 MHz VOLTAGE CONTROLLED MULTIVIBRATOR

SEMICONDUCTOR TECHNICAL DATA



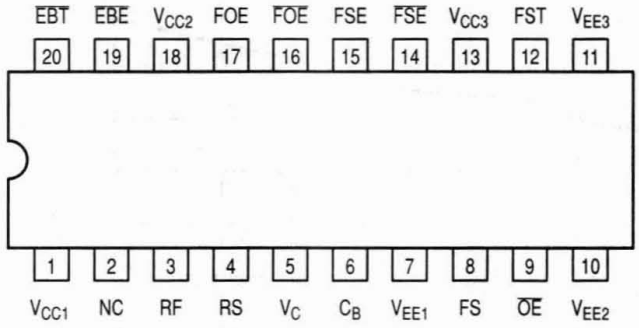
P SUFFIX
PLASTIC PACKAGE
CASE 738



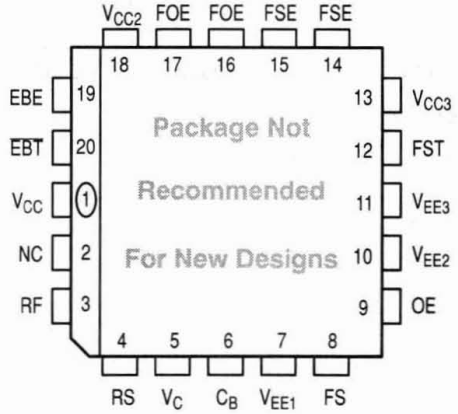
FN SUFFIX
PLASTIC PACKAGE
CASE 775
(PLCC)

Not Recommended For New Designs

Pinout: 20-Lead Plastic Package (Top View)



Pinout: 20-Lead PLCC Package (Top View)



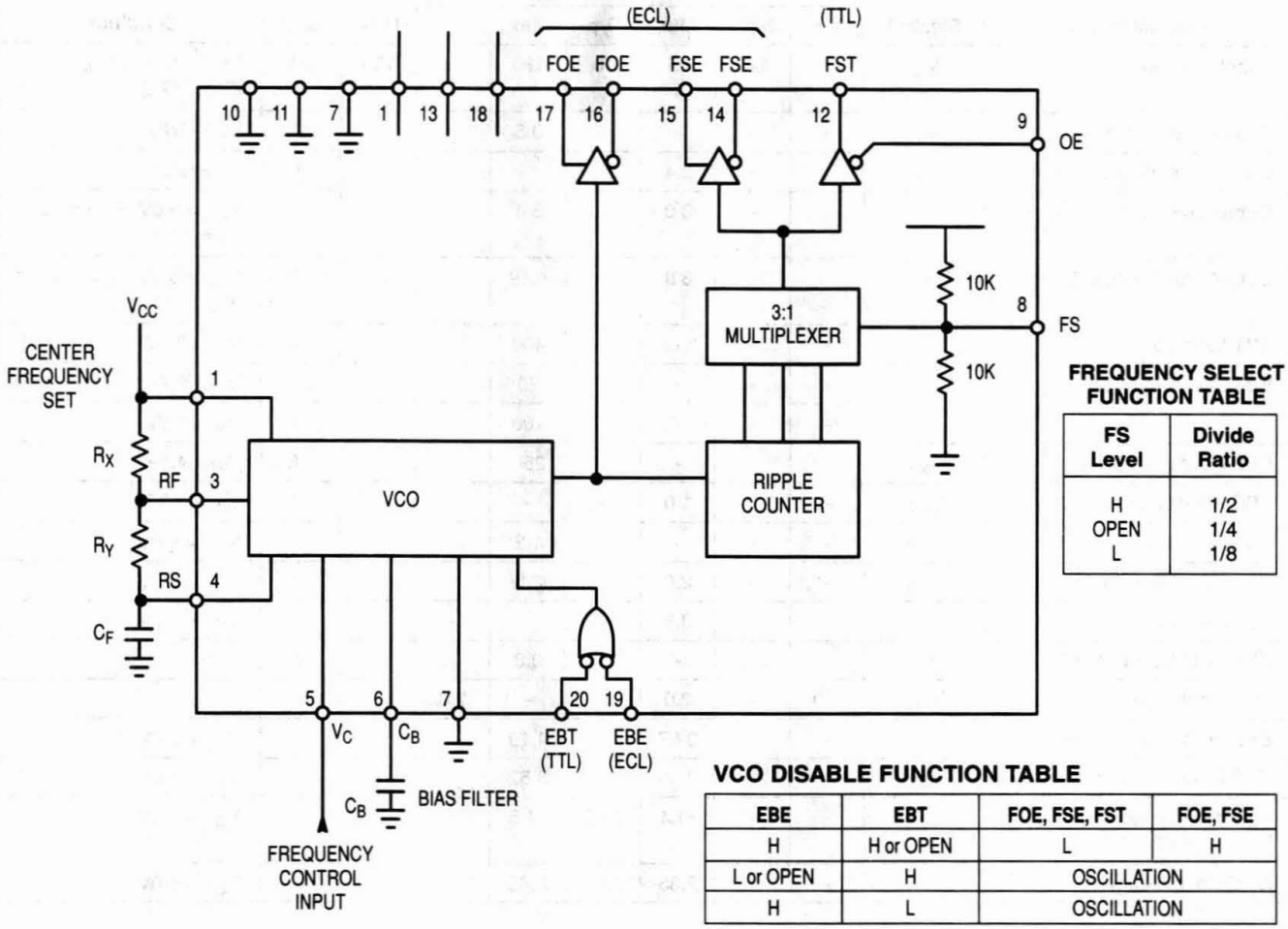
PIN NAMES

Pin	Function
RF, RS	Center Frequency Inputs
V_C	Frequency Control Input
C_B	Bias Filter Input
FS	Frequency Select Input
$\overline{OE}$	TTL Output Enable
FST	TTL ÷2, ÷4, ÷8 Output
FSE, $\overline{FSE}$	Diff ECL ÷2, ÷4, ÷8 Outputs
FOE, $\overline{FOE}$	Diff ECL ÷1 Outputs
$\overline{EBE}$	VCO Disable, ECL Level Input
$\overline{EBT}$	VCO Disable, TTL Level Input

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12100P	T_A = –40° to +75°C	Plastic

Figure 1. Block Diagram



FREQUENCY SELECT FUNCTION TABLE

FS Level	Divide Ratio
H	1/2
OPEN	1/4
L	1/8

VCO DISABLE FUNCTION TABLE

EBE	EBT	FOE, FSE, FST	FOE, FSE
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC1} V_{CC2} V_{CC3}	–0.5 to 8.0	V
Input Voltage	V_{IN} (TTL)	–0.5 to V_{CC}	V
Input Voltage	V_{IN} (ECL)	–0.5 to V_{CC}	V
Output Source Current – Surge	I_{OUT} (ECL)	100	mA
Output Source Current – Continuous		50	mA
Junction Operating Temperature	T_J	140	°C
Storage Temperature	T_{STG}	–55 to 150	°C

NOTE: ESD data available upon request.

OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Ambient Temperature	T_A	0 to 75	°C
Supply Voltage	V_{CC}	4.75 to 5.25	V
TTL High Output Current	I_{OH} (TTL)	–1.0	mA
TTL Low Output Current	I_{OL} (TTL)	20	mA

DC CHARACTERISTICS (V_{CC} = 5.0 V ±5%; R_X = 2.4 kΩ; R_Y = 1.5 kΩ; C_B = 0.001 µF, unless otherwise noted.)

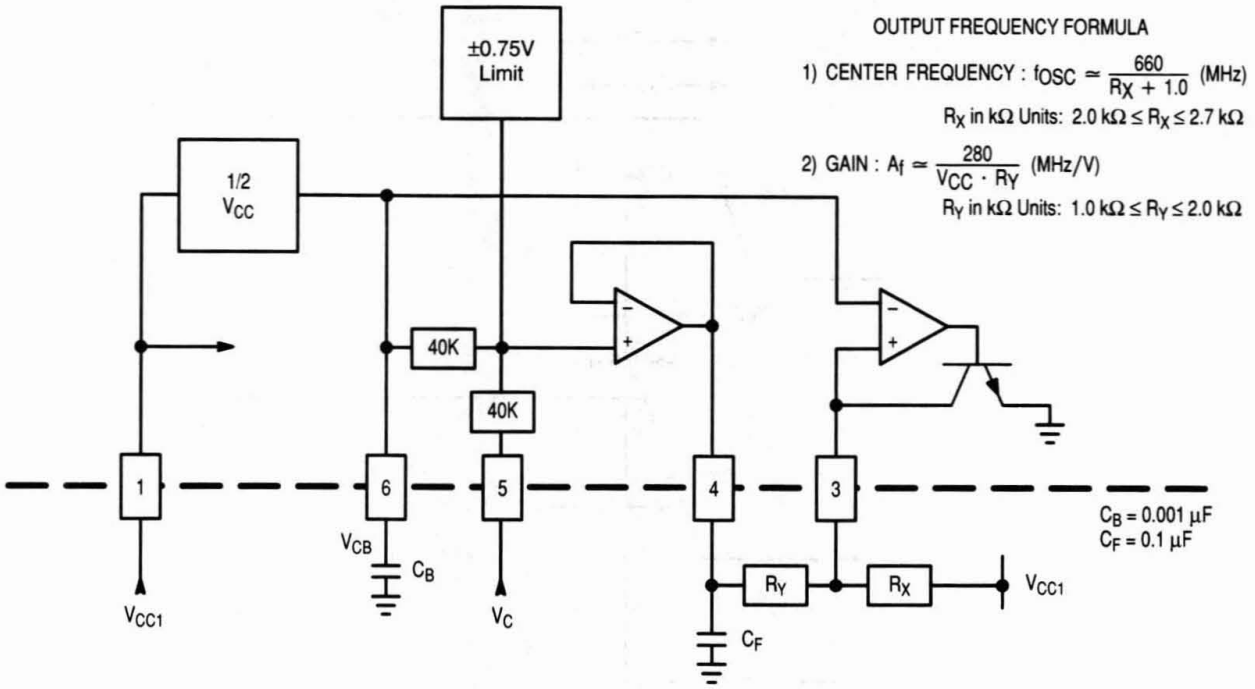
Characteristic	Symbol	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
Supply Current	I_{CC}	75	120	65	90	110	80	135	mA	$\overline{EBT}$ = $\overline{EBE}$ = V_{CC} (ECL, TTL)
Output Low Voltage, TTL	V_{OLT}	-	-	-	-	0.5	-	-	V	F_S = GND
Output High Voltage, TTL	V_{OHT}	-	-	2.4	-		-	-	V	F_S = GND
Output Low Voltage, ECL	V_{OLE}	-	-	3.0	-	3.4	-	-	V	V_{CC} = 5.0V, R_L = 50Ω, V_T = 3.0V
Output High Voltage, ECL	V_{OHE}	-	-	3.9	-	4.19	-	-	V	V_{CC} = 5.0V, R_L = 50Ω, V_T = 3.0V
$\overline{EBT}$ Input Low Current	I_{ILT}	-	-	-	-	400	-	-	µA	V_{IN} = 0.4V
$\overline{EBT}$ Input High Current	I_{IHT}	-	-	-	-	20	-	-	µA	V_{IN} = 2.7V
		-	-	-	-	100	-	-	µA	V_{IN} = 7.0V
$\overline{EBE}$ Input High Current	I_{INHE}	-	-	-	-	250	-	-	µA	V_{IN} = 4.19V
$\overline{EBE}$ Input Low Current	I_{INLE}	-	-	1.0	-	-	-	-	µA	V_{IN} = 3.05V
FS Input, Max "L" Level	V_{ILS}	-	-	-	-	1.2	-	-	V	V_{CC} = 5.0V
FS Input, "Medium" Level	V_{IMS}	-	-	2.0	-	3.0	-	-	V	V_{CC} = 5.0V
FS Input, Min "H" Level	V_{IHS}	-	-	3.8	-	-	-	-	V	V_{CC} = 5.0V
$\overline{EBT}$ Input Low Voltage	V_{ILT}	-	0.8	-	-	0.8	-	0.8	V	
$\overline{EBT}$ Input High Voltage	V_{IHT}	2.0	-	2.0	-	-	2.0	-	V	
$\overline{EBE}$ Input High Voltage	V_{IHE}	-	-	3.87	-	4.19	-	-	V	V_{CC} = 5.0V
$\overline{EBE}$ Input Low Voltage	V_{ILE}	-	-	3.05	-	3.52	-	-	V	V_{CC} = 5.0V
V_C Input Voltage, V_C = V_{CC} ÷ 2	V_{LM}	-	-	±1.1	±1.3	±1.5	-	-	V	V_{CC} = 5.0V
C_B Output Voltage	V_{CB}	-	-	2.35	2.50	2.65	-	-	V	V_{CC} = 5.0V

AC CHARACTERISTICS (V_{CC} = 5.0 V; R_X = 2.4 kΩ; R_Y = 1.5 kΩ; C_B = 0.001 µF; V_T = 3.0 V, unless otherwise noted.)

Characteristic	Symbol	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
Center Frequency (V_{VC} – V_{CB} = 0V)	FO	-	-	180	200	220	-	-	MHz	V_{CC} = +2.0V V_{EE} = –3.0V
Frequency Range (V_C = 1/2 V_{CC} ±1.5V, V_{CC} = 5.0V)	F_{MAX} – F_{MIN}	-	-	85	100	115	-	-	MHz	
FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Rise Time	t_{rE}	-	-	0.5	-	2.4	-	-	ns	
FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Fall Time	t_{fE}	-	-	0.5	-	2.4	-	-	ns	
Reset Time	TTT	-	-	-	-	35	-	-	ns	$\overline{EBT}$ ~ FST
Reset Time	TTO	-	-	-	-	25	-	-	ns	$\overline{EBT}$ ~ FOE/$\overline{FOE}$
Reset Time	TTS	-	-	-	-	30	-	-	ns	$\overline{EBT}$ ~ FSE/$\overline{FSE}$
Reset Time	TET	-	-	-	-	37	-	-	ns	$\overline{EBE}$ ~ FST
Reset Time	TEO	-	-	-	-	12	-	-	ns	$\overline{EBE}$ ~ FOE/$\overline{FOE}$
Reset Time	TES	-	-	-	-	25	-	-	ns	$\overline{EBE}$ ~ FSE/$\overline{FSE}$

NOTE: Loading: ECL = 50 Ω to V_T; TTL = 500 Ω, 50 pF

Figure 2. VCO Detail



Notes:

- For optimum VCO linearity (MHz/V), the following resistor ranges are recommended:
  2.0 kΩ ≤ R_X ≤ 2.7 kΩ (R_Y = 1.5 kΩ)
  1.0 kΩ ≤ R_Y ≤ 2.0 kΩ (R_X = 2.4 kΩ)
- TTL output maximum frequency = 50 MHz
- Simultaneous use of both ECL and TTL outputs are not recommended due to excessive power consumption for the EIAJ Type II SO package

Figure 3. AC Test Circuit (FO/t_{rE}/t_{fE} Measurement)

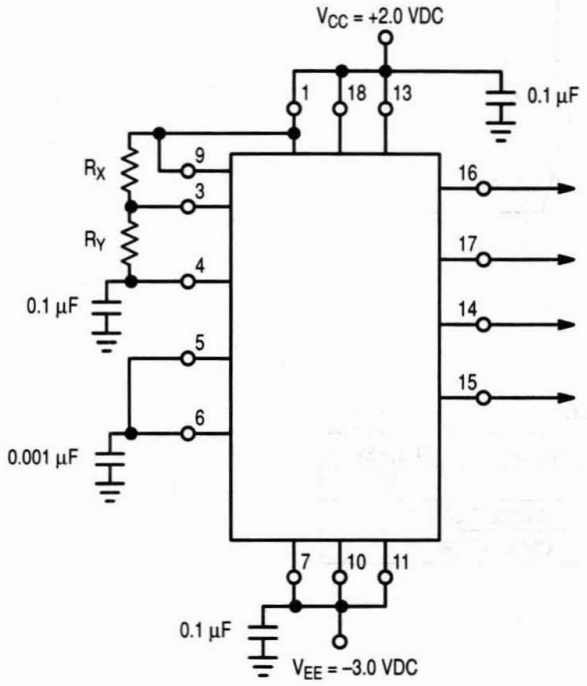


Figure 4. AC Test Circuit (Other Measurements)

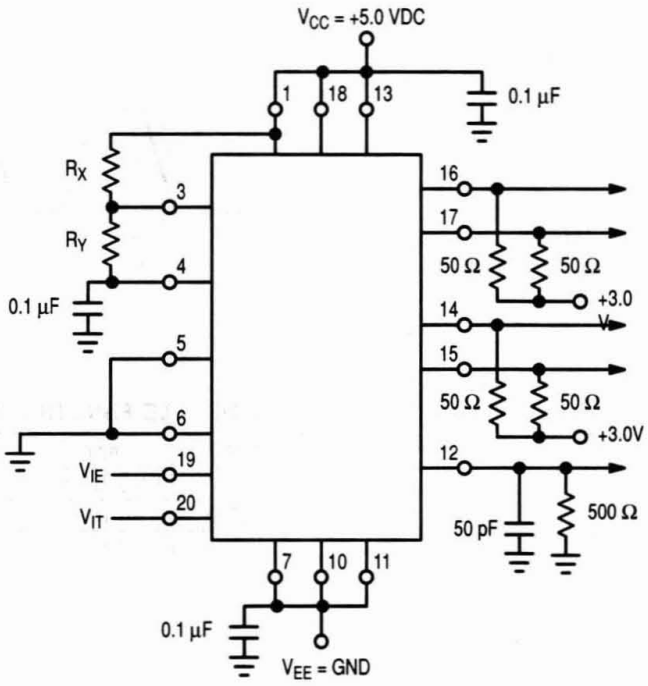
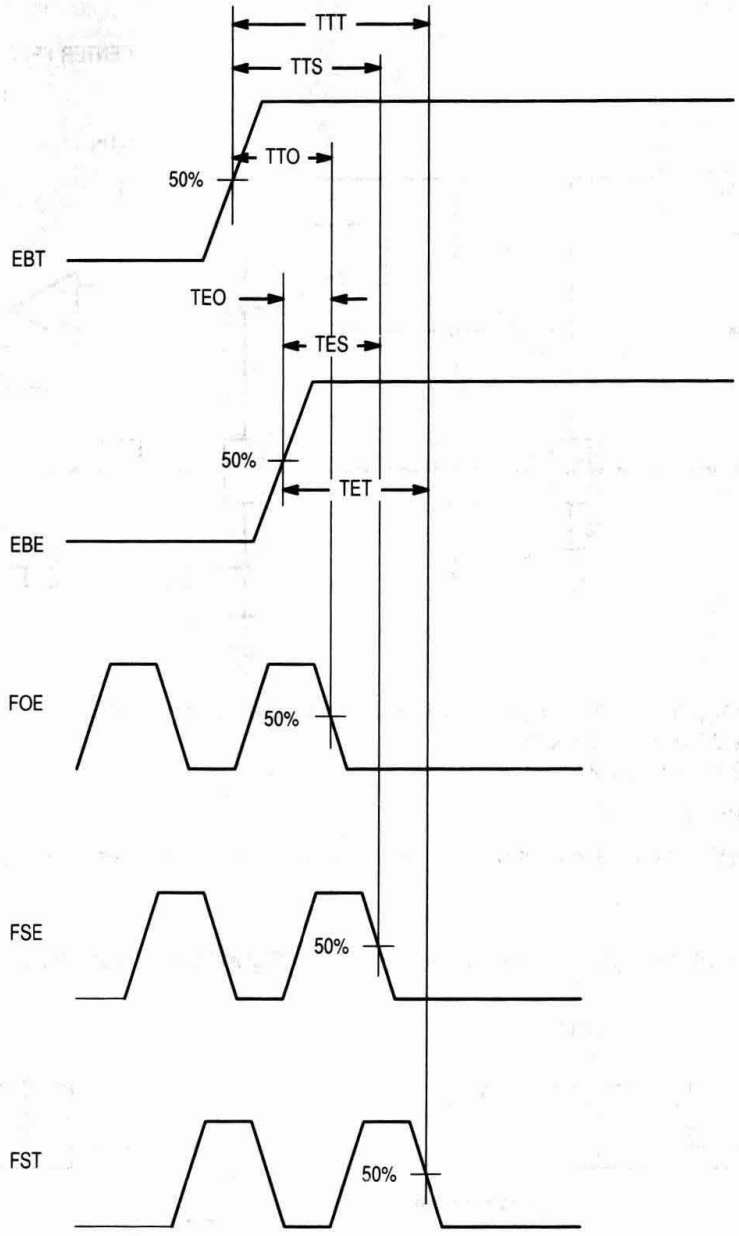


Figure 5. Switching Waveforms



VCO DISABLE FUNCTION TABLE

EBE	EBT	FOE, FSE, FST	FOE, FSE
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	

Figure 6. V_C versus Output Frequency
(Varying R_X @ V_{CC} = 5.0 V; T_A = 25°C; R_Y = 1.5 kΩ)

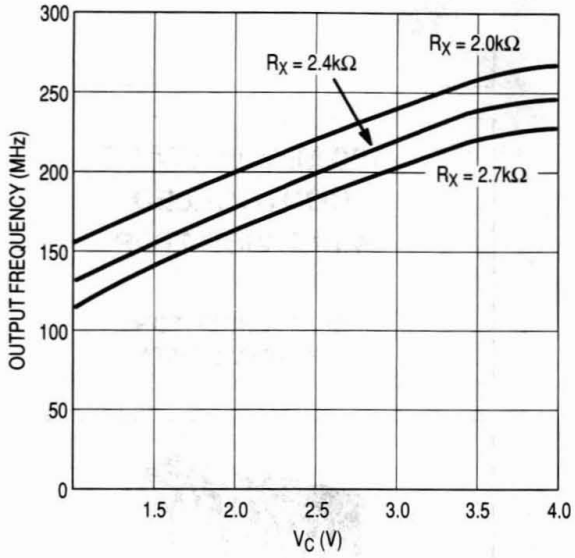


Figure 7. V_C versus Output Frequency
(Varying R_Y @ V_{CC} = 5.0 V; T_A = 25°C; R_X = 2.4 kΩ)

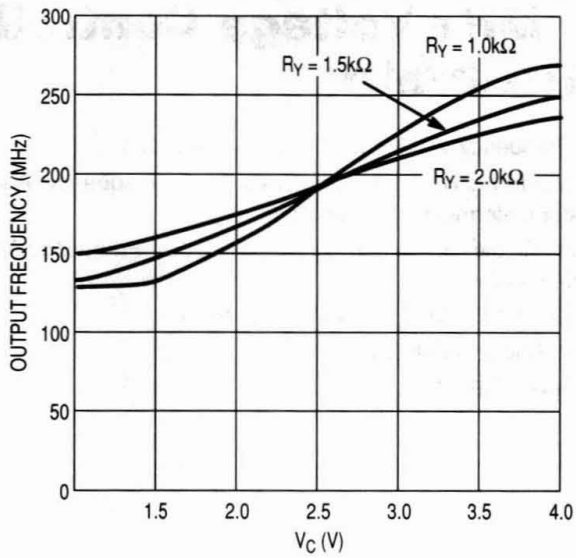


Figure 8. V_C versus Output Frequency
(Varying T_A @ V_{CC} = 5.0 V; R_X = 2.4 kΩ; R_Y = 1.5 kΩ)

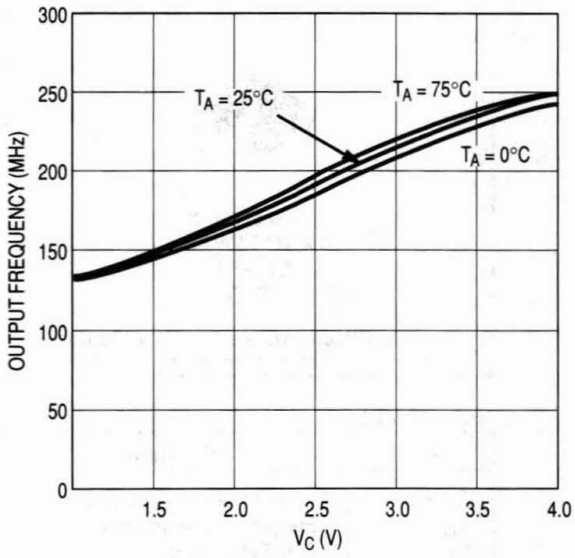
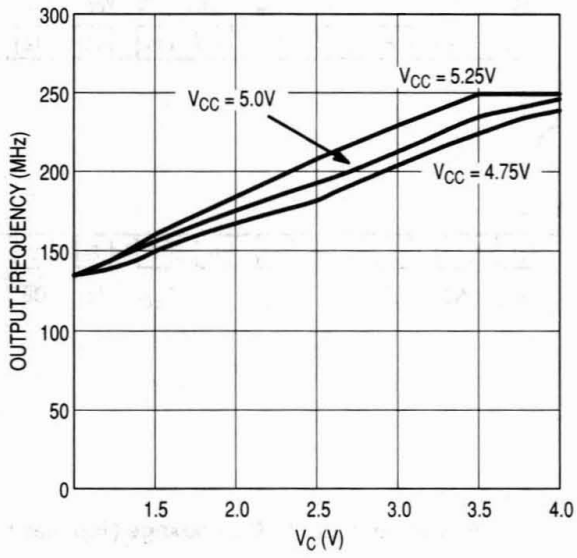


Figure 9. V_C versus Output Frequency
(Varying V_{CC} @ R_X = 2.4 kΩ; R_Y = 1.5 kΩ; T_A = 25°C)



MOTOROLA

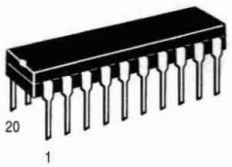
MC12101

130 MHz Voltage Controlled Multivibrator

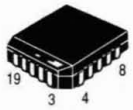
- High Frequency VCM Ideal for PLL Applications
- Single External Resistor Determines Center Frequency; Additional Resistor Determines f/V Sensitivity
- Internal Ripple Counter (1/2, 1/4, 1/8) for Low Frequency Applications, TTL/ECL Outputs
- VCO Output Enable Pins (TTL/ECL Level)
- +5.0 V Single Supply Voltage
- Packages: DIP, PLCC

130 MHz VOLTAGE CONTROLLED MULTIVIBRATOR

SEMICONDUCTOR TECHNICAL DATA



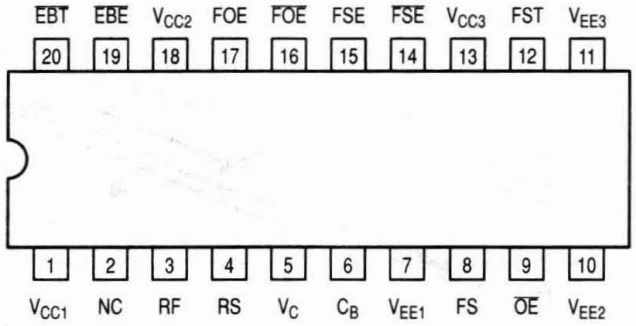
P SUFFIX
PLASTIC PACKAGE
CASE 738



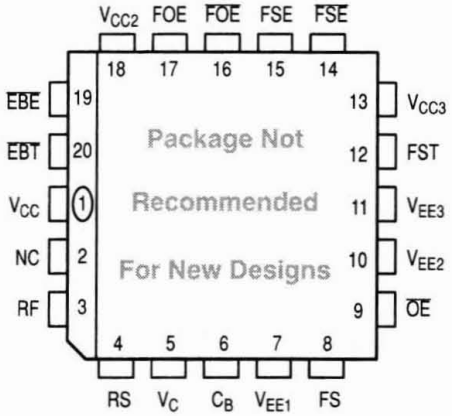
FN SUFFIX
PLASTIC PACKAGE
CASE 775
(PLCC)

Not Recommended For New Designs

Pinout: 20-Lead Plastic Package (Top View)



Pinout: 20-Lead PLCC Package (Top View)



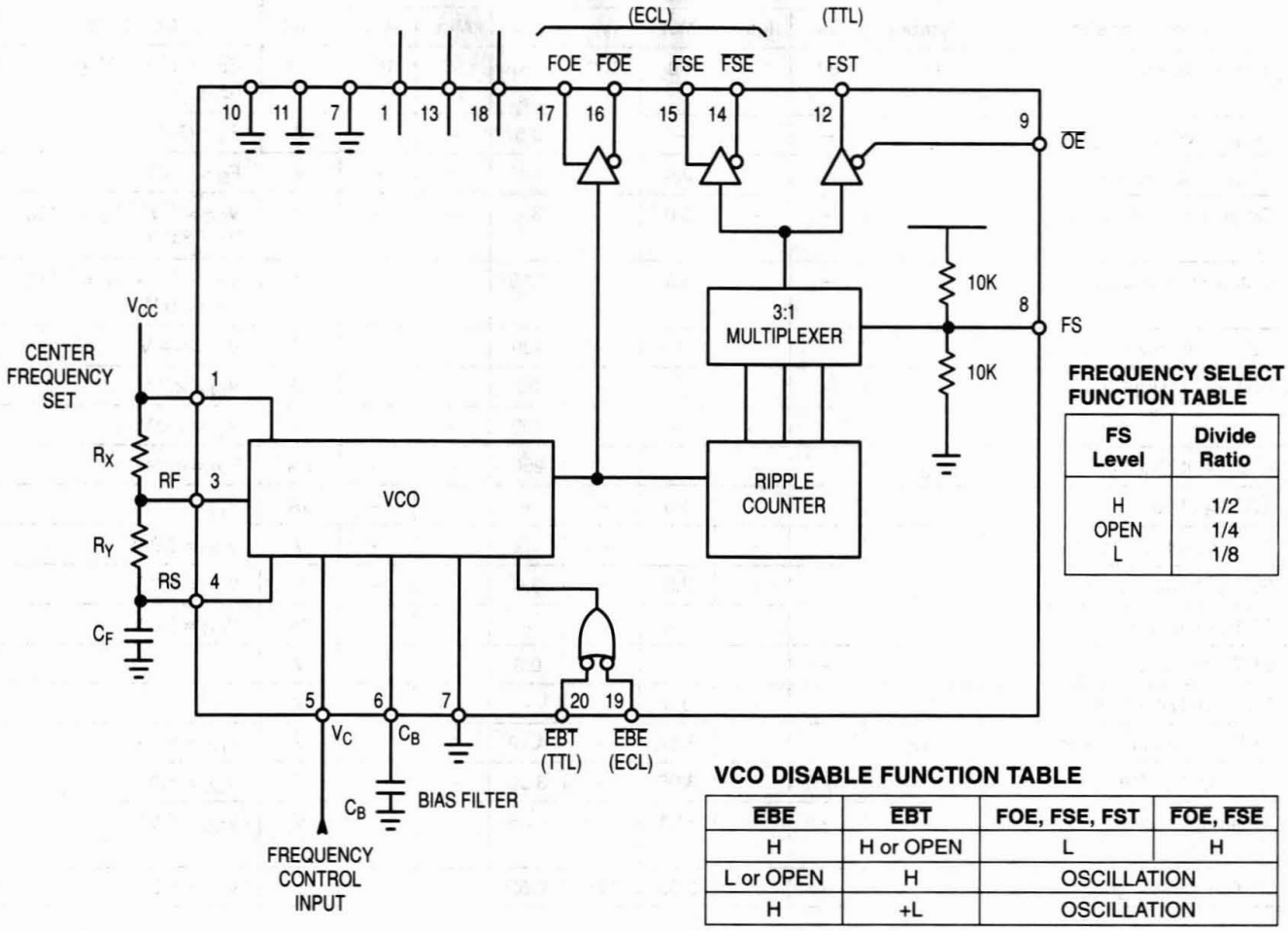
PIN NAMES

Pin	Function
RF, RS	Center Frequency Inputs
V_C	Frequency Control Input
C_B	Bias Filter Input
FS	Frequency Select Input
$\overline{OE}$	TTL Output Enable
FST	TTL ÷2, ÷4, ÷8 Output
FSE, $\overline{FSE}$	Diff ECL ÷2, ÷4, ÷8 Outputs
FOE, $\overline{FOE}$	Diff ECL ÷1 Outputs
$\overline{EBE}$	VCO Disable, ECL Level Input
$\overline{EBT}$	VCO Disable, TTL Level Input

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12101P	T_A = –40° to +75°C	Plastic

Figure 1. Block Diagram



FREQUENCY SELECT FUNCTION TABLE

FS Level	Divide Ratio
H	1/2
OPEN	1/4
L	1/8

VCO DISABLE FUNCTION TABLE

$\overline{EBE}$	$\overline{EBT}$	FOE, FSE, FST	$\overline{FOE}$, $\overline{FSE}$
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	+L	OSCILLATION	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC1} V_{CC2} V_{CC3}	–0.5 to 8.0	V
Input Voltage	V_{IN} (TTL)	–0.5 to V_{CC}	V
Input Voltage	V_{IN} (ECL)	–0.5 to V_{CC}	V
Output Source Current – Surge	I_{OUT} (ECL)	100	mA
Output Source Current – Continuous		50	mA
Junction Operating Temperature	T_J	140	°C
Storage Temperature	T_{STG}	–55 to 150	°C

NOTE: ESD data available upon request.

OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Ambient Temperature	T_A	0 to 75	°C
Supply Voltage	V_{CC}	4.75 to 5.25	V
TTL High Output Current	I_{OH} (TTL)	–1.0	mA
TTL Low Output Current	I_{OL} (TTL)	20	mA

DC CHARACTERISTICS (V_{CC} = 5.0 V ±5%; R_X = 2.4 kΩ; R_Y = 1.5 kΩ; C_B = 0.001 µF, unless otherwise noted.)

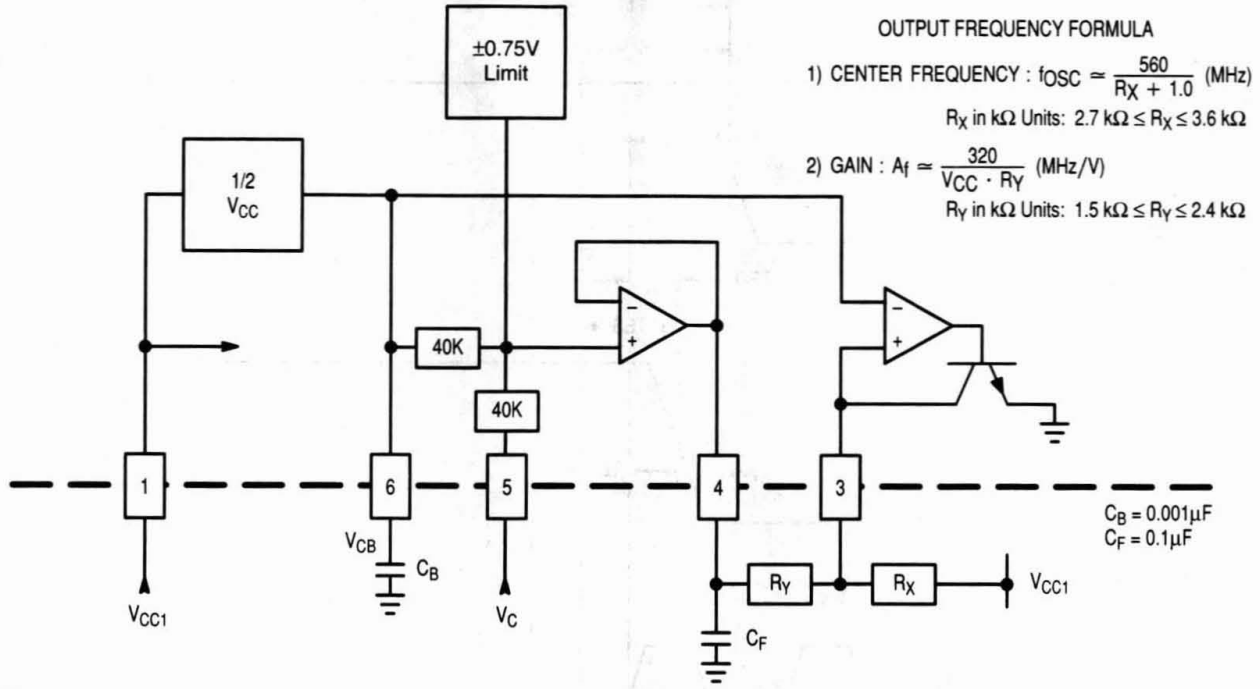
Characteristic	Symbol	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
Supply Current	I_{CC}	80	135	70	100	120	85	150	mA	$\overline{EBT}$ = $\overline{EBE}$ = V_{CC} (ECL, TTL)
Output Low Voltage, TTL	V_{OLT}	–	–	–	–	0.5	–	–	V	F_S = GND
Output High Voltage, TTL	V_{OHT}	–	–	2.4	–		–	–	V	F_S = GND
Output Low Voltage, ECL	V_{OLE}	–	–	3.0	–	3.4	–	–	V	V_{CC} = 5.0 V, R_L = 50 Ω, V_T = 3.0 V
Output High Voltage, ECL	V_{OHE}	–	–	3.9	–	4.19	–	–	V	V_{CC} = 5.0 V, R_L = 50 Ω, V_T = 3.0 V
$\overline{EBT}$ Input Low Current	I_{ILT}	–	–	–	–	400	–	–	µA	V_{IN} = 0.4 V
$\overline{EBT}$ Input High Current	I_{IHT}	–	–	–	–	20	–	–	µA	V_{IN} = 2.7 V
		–	–	–	–	100	–	–	µA	V_{IN} = 7.0 V
$\overline{EBE}$ Input High Current	I_{INHE}	–	–	–	–	250	–	–	µA	V_{IN} = 4.19 V
$\overline{EBE}$ Input Low Current	I_{INLE}	–	–	1.0	–	–	–	–	µA	V_{IN} = 3.05 V
FS Input, Max "L" Level	V_{ILS}	–	–	–	–	1.2	–	–	V	V_{CC} = 5.0 V
FS Input, "Medium" Level	V_{IMS}	–	–	2.0	–	3.0	–	–	V	V_{CC} = 5.0 V
FS Input, Min "H" Level	V_{IHS}	–	–	3.8	–	–	–	–	V	V_{CC} = 5.0 V
$\overline{EBT}$ Input Low Voltage	V_{ILT}	–	0.8	–	–	0.8	–	0.8	V	
$\overline{EBT}$ Input High Voltage	V_{IHT}	2.0	–	2.0	–	–	2.0	–	V	
$\overline{EBE}$ Input High Voltage	V_{IHE}	–	–	3.87	–	4.19	–	–	V	V_{CC} = 5.0 V
$\overline{EBE}$ Input Low Voltage	V_{ILE}	–	–	3.05	–	3.52	–	–	V	V_{CC} = 5.0 V
V_C Input Voltage, V_C = V_{CC} ÷ 2	V_{LM}	–	–	±1.1	±1.3	±1.5	–	–	V	V_{CC} = 5.0 V
C_B Output Voltage	V_{CB}	–	–	2.35	2.50	2.65	–	–	V	V_{CC} = 5.0 V

AC CHARACTERISTICS (V_{CC} = 5.0 V; R_X = 2.4 kΩ; R_Y = 1.5 kΩ; C_B = 0.001 µF; V_T = 3.0 V, unless otherwise noted.)

Characteristic	Symbol	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
Center Frequency (V_{VC} – V_{CB} = 0V)	FO	–	–	117	130	143	–	–	MHz	V_{CC} = 2.0 V V_{EE} = –3.0 V
Frequency Range (V_C = 1/2 V_{CC} ±1.5V, V_{CC} = 5.0V)	F_{MAX} – F_{MIN}	–	–	68	80	92	–	–	MHz	
FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Rise Time	t_{rE}	–	–	0.5	–	2.4	–	–	ns	
FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Fall Time	t_{fE}	–	–	0.5	–	2.4	–	–	ns	
Reset Time	TTT	–	–	–	–	40	–	–	ns	$\overline{EBT}$ ~ FST
Reset Time	TTO	–	–	–	–	25	–	–	ns	$\overline{EBT}$ ~ FOE/$\overline{FOE}$
Reset Time	TTS	–	–	–	–	35	–	–	ns	$\overline{EBT}$ ~ FSE/$\overline{FSE}$
Reset Time	TET	–	–	–	–	32	–	–	ns	$\overline{EBE}$ ~ FST
Reset Time	TEO	–	–	–	–	12	–	–	ns	$\overline{EBE}$ ~ FOE/$\overline{FOE}$
Reset Time	TES	–	–	–	–	30	–	–	ns	$\overline{EBE}$ ~ FSE/$\overline{FSE}$

NOTE: Loading: ECL = 50 Ω to V_T; TTL = 500 Ω, 50 pF

Figure 2. VCO Detail



Notes:

- For optimum VCO linearity (MHz/V), the following resistor ranges are recommended:
  3.6 kΩ ≤ R_X ≤ 4.6 kΩ (R_Y = 2.0 kΩ)
  1.5 kΩ ≤ R_Y ≤ 2.4 kΩ (R_X = 3.3 kΩ)
- TTL output maximum frequency = 50 MHz
- Simultaneous use of both ECL and TTL outputs are not recommended due to excessive power consumption for the EIAJ Type II SO package

Figure 3. AC Test Circuit (FO/t_{rE}/t_{fE} Measurement)

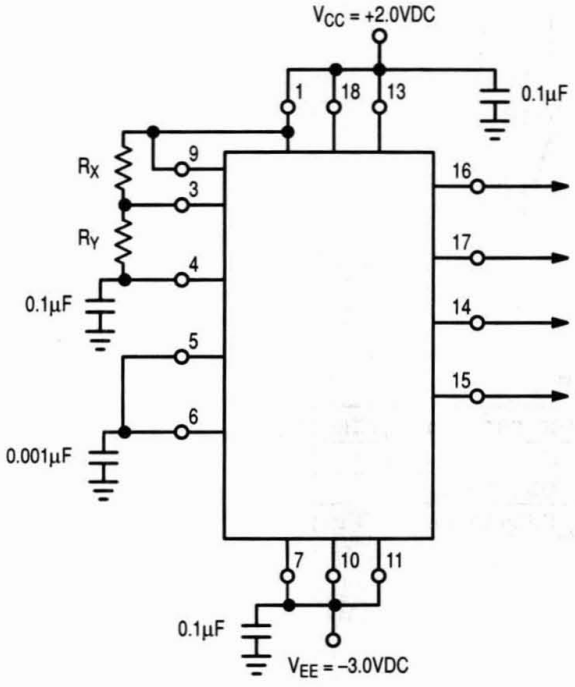


Figure 4. AC Test Circuit (Other Measurements)

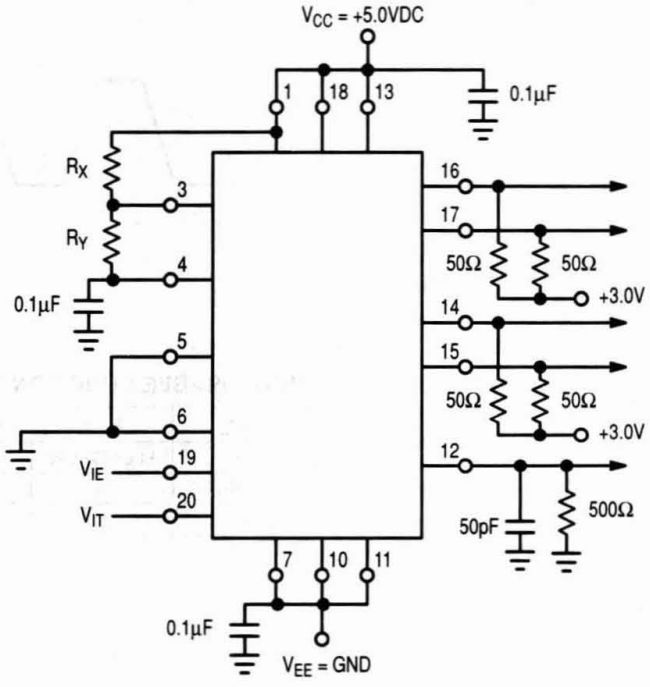
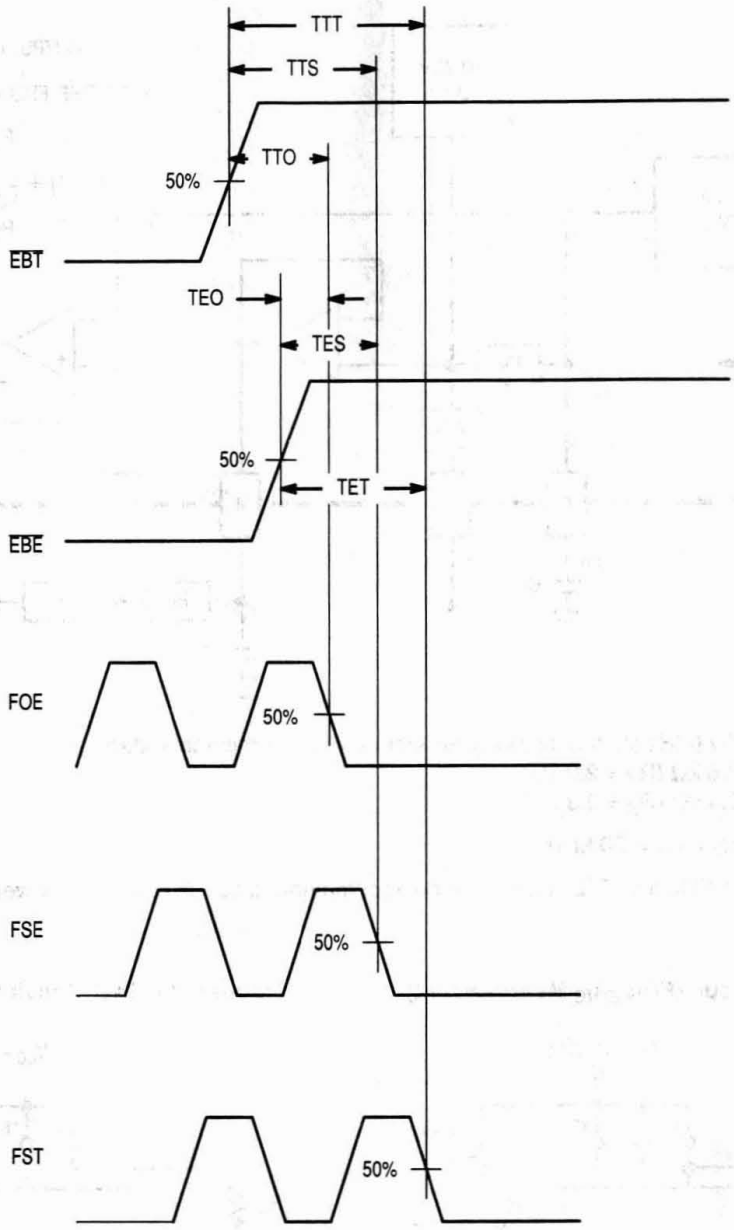


Figure 5. Switching Waveforms



VCO DISABLE FUNCTION TABLE

$\overline{\text{EBE}}$	$\overline{\text{EBT}}$	FOE, FSE, FST	$\overline{\text{FOE}}$, $\overline{\text{FSE}}$
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	

Figure 6. V_C versus Output Frequency
(Varying Rx @ V_{CC} = 5.0 V; T_A = 25°C; Ry = 2.0 kΩ)

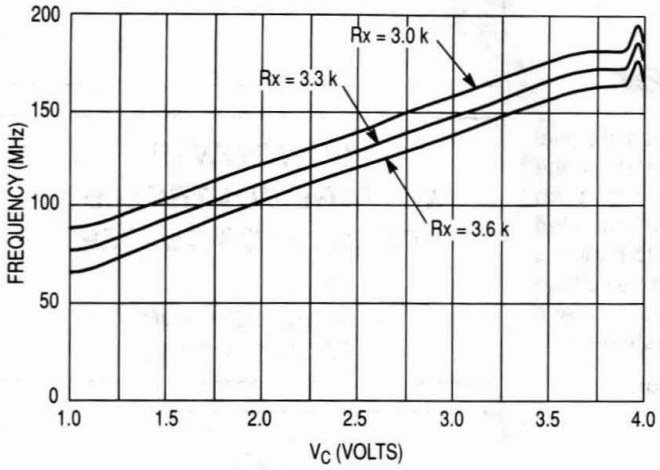


Figure 7. V_C versus Output Frequency
(Varying Ry @ V_{CC} = 5.0 V; T_A = 25°C; Ry = 3.3 kΩ)

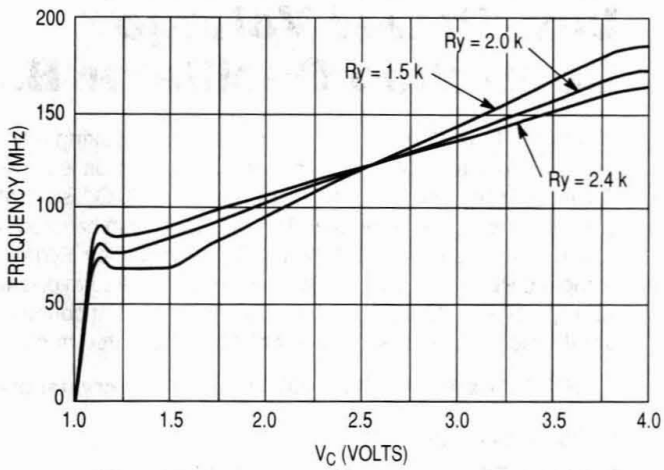


Figure 8. V_C versus Output Frequency
(Varying T_A @ V_{CC} = 5.0 V; Rx = 3.3 kΩ; Ry = 2.0 kΩ)

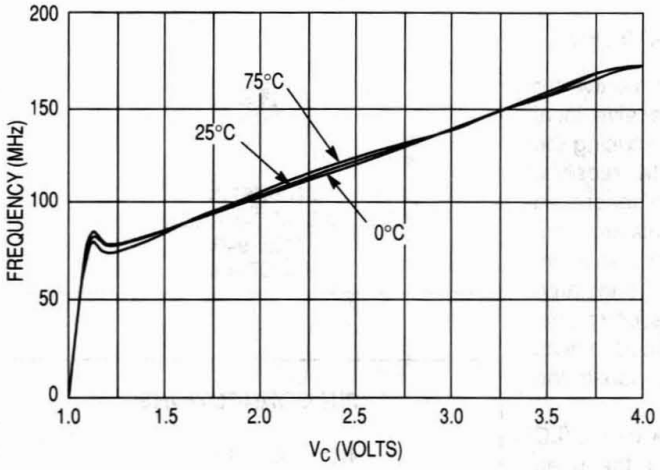
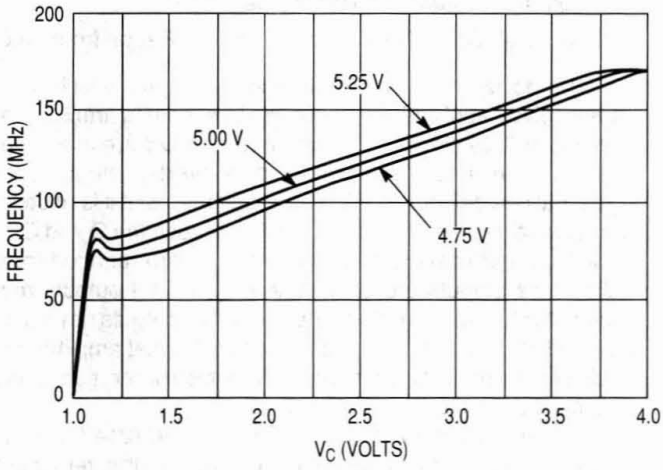


Figure 9. V_C versus Output Frequency
(Varying V_{CC} @ Rx = 3.3 kΩ; Ry = 2.0 kΩ; T_A = 25°C)



MOTOROLA

Low Power Voltage Controlled Oscillator Buffer

The MC12147 is intended for applications requiring high frequency signal generation up to 1300 MHz. An external tank circuit is used to determine the desired frequency of operation. The VCO is realized using an emitter–coupled pair topology. The MC12147 can be used with an integrated PLL IC such as the MC12202 1.1 GHz Frequency Synthesizer to realize a complete PLL sub–system. The device is specified to operate over a voltage supply range of 2.7 to 5.5 V. It has a typical current consumption of 13 mA at 3.0 V which makes it attractive for battery operated handheld systems.

NOTE: The MC12147 is NOT suitable as a crystal oscillator.

- Operates Up to 1.3 GHz
- Space–Efficient 8–Pin SOIC or SSOP Package
- Low Power 13 mA Typical @ 3.0 V Operation
- Supply Voltage of 2.7 to 5.5 V
- Typical 900MHz Performance
  - Phase Noise –105 dBc/Hz @ 100 kHz Offset
  - Tuning Voltage Sensitivity of 20 MHz/V
- Output Amplitude Adjustment Capability
- Two High Drive Outputs With a Typical Range from –8.0 to –2.0 dBm

The device has two high frequency outputs which make it attractive for transceiver applications which require both a transmit and receive local oscillator (LO) signal. The outputs Q and QB are available for servicing the receiver IF and transmitter up–converter single–ended. In receiver applications, the outputs can be used together if it is necessary to generate a differential signal for the receiver IF. Because the Q and QB outputs are open collector, terminations to the V_{CC} supply are required for proper operation. Since the outputs are complementary, BOTH outputs must be terminated even if only one is needed. The Q and QB outputs have a nominal drive level of –8dBm to conserve power. If addition signal amplitude is needed, a level adjustment pin (CNTL) is available, which when tied to ground, boosts the nominal output levels to –2.0 dBm.

External components required for the MC12147 are: (1) tank circuit (LC network); (2) Inductor/capacitor to provide the termination for the open collector outputs; and (3) adequate supply voltage bypassing. The tank circuit consists of a high–Q inductor and varactor components. The preferred tank configuration allows the user to tune the VCO across the full supply range. VCO performance such as center frequency, tuning voltage sensitivity, and noise characteristics are dependent on the particular components and configuration of the VCO tank circuit.

PIN NAMES

Pin	Function
V_{CC}	Power Supply
CNTL	Amplitude Control for Q, QB Output Pair
TANK	Tank Circuit Input
V_{REF}	Bias Voltage Output
QB	Open Collector Output
GND	Ground
Q	Open Collector Output

MC12147

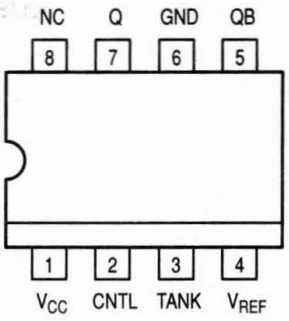
LOW POWER VOLTAGE CONTROLLED OSCILLATOR BUFFER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12147D	T_A = – 40° to +85°C	SO–8
MC12147SD		SSOP–8

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 1	V_{CC}	-0.5 to +7.0	V
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Maximum Output Current, Pin 5,7	I_O	12	mA

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = -40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (CNTL=GND) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	14.0 23.5	18 28	mA
Supply Current (CNTL=OPEN) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	8 13	13.0 22.5	mA
Output Amplitude (Pin 5 & 7) {Note 1] V_{CC} = 2.7 V 50Ω to V_{CC} V_{CC} = 2.7 V	 V_{OH}, V_{OL}	 2.6 2.1	 2.7 2.3	 – 2.4	V
Output Amplitude (Pin 5 & 7) [Note 1] V_{CC} = 5.5 V 50Ω to V_{CC} V_{CC} = 5.5 V	 V_{OH}, V_{OL}	 5.4 4.8	 5.5 5.0	 – 5.1	V
Tuning Voltage Sensitivity [Notes 2 and 3]	T_{stg}	–	20	–	MHz/V
Frequency of Operation	F_C	100	–	1300	MHz
CSR at 10 kHz Offset, 1.0 Hz BW [Notes 2 and 3]	$\mathcal{L}$(f)	–	–85	–	dBc/Hz
CSR at 100 kHz Offset, 1.0 Hz BW [Notes 2 and 3]	$\mathcal{L}$(f)	–	–105	–	dBc/Hz
Frequency Stability [Notes 2 and 3] Supply Drift Thermal Drift	 F_{sts} f_{stt}	 – –	 0.8 50	 – –	 MHz/V KHz/°C

NOTES: 1. CNTL pin tied to ground.
2. Actual performance depends on tank components selected.
3. See Figure 12, 750 MHz tank.
4. T = 25°C, V_{CC} = 5.0 V ±10%

OPERATIONAL CHARACTERISTICS

A simplified schematic of the MC12147 is found in Figure 1. The oscillator incorporates positive feedback by coupling the base of transistor Q2 to the collector of transistor Q1. In order to minimize interaction between the VCO outputs and the oscillator tank transistor pair, a buffer is incorporated into the circuit. This differential buffer is realized by the Q3 and Q4 transistor pair. The differential buffer drives the gate which contains the primary open collector outputs, Q and QB. The output is actually a current which has been set by an internal bias driver to a nominal current of 4mA. Additional circuitry is incorporated into the tail of the current source which allows the current source to be increased to approximately 10mA. This is accommodated by the addition of a resistor which is brought out to the CNTL pin. When this pin is tied to ground, the additional current is sourced through the current source thus increasing the output amplitude of the Q/QB output pair. If less than 10 mA of current is needed, a resistor can be added to ground which reduces the amount of current.

APPLICATION INFORMATION

Figure 2 illustrates the external components necessary for the proper operation of the VCO buffer. The tank circuit configuration in this figure allows the VCO to be tuned across the full operating voltage of the power supply. This is very important in 3V applications where it is desirable to utilize as much of the operating supply range as possible so as to minimize the VCO sensitivity (MHz/V). In most situations, it is desirable to keep the sensitivity low so the circuit will be less susceptible to external noise influences. An additional benefit to this configuration is that additional regulation/ filtering can be incorporated into the V_{CC} line without compromising the tuning range of the VCO. With the AC–coupled tank configuration, the V_{tune} voltage can be greater than the V_{CC} voltage supplied to the device.

There are four main areas that the user directly influences the performance of the VCO. These include Tank Design, Output Termination Selection, Power Supply Decoupling, and Circuit Board Layout/Grounding.

The design of the tank circuit is critical to the proper operation of the VCO. This tank circuit directly impacts the main VCO operating characteristics:

1) Frequency of Operation
2) Tuning Sensitivity
3) Voltage Supply Pushing
4) Phase Noise Performance

The tank circuit, in its simplest form, is realized as an LC circuit which determines the VCO operating frequency. This is described in Equation 1.

$$f_O = \frac{1}{2\pi \sqrt{LC}} \qquad \text{Equation 1}$$

In the practical case, the capacitor is replaced with a varactor diode whose capacitance changes with the voltage applied, thus changing the resonant frequency at which the VCO tank operates. The capacitive component in Equation 1 also needs to include the input capacitance of the device and other circuit and parasitic elements. Typically, the inductor is realized as a surface mount chip or a wound–coil. In addition, the lead inductance and board inductance and capacitance also have an impact on the final operating point.

Figure 1. Simplified Schematic

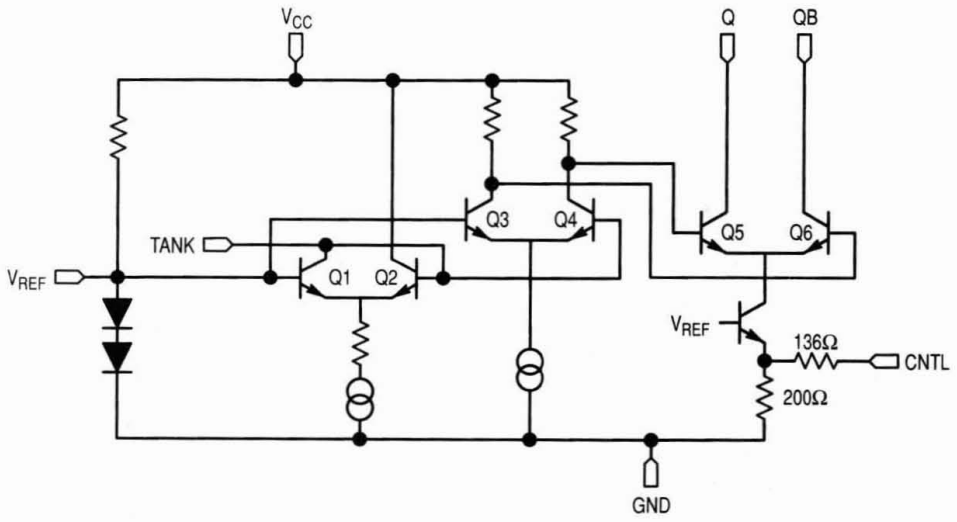
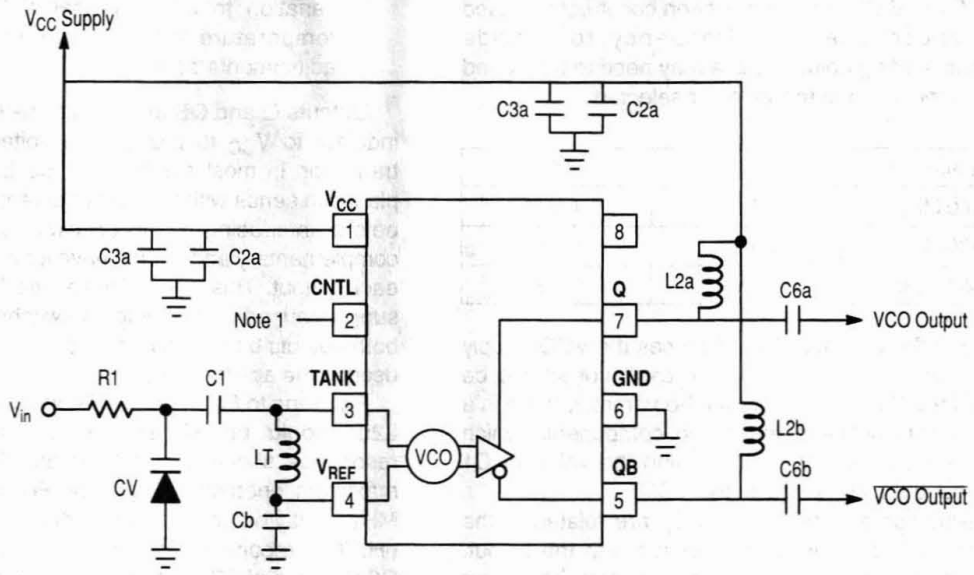


Figure 2. MC12147 Typical External Component Connections



1. This input can be left open, tied to ground, or tied with a resistor to ground, depending on the desired output amplitude needed at the Q and QB output pair.
2. Typical values for R1 range from 5.0 kΩ to 10 kΩ.

A simplified linear approximation of the device, package, and typical board parasitics has been developed to aid the designer in selecting the proper tank circuit values. All the parasitic contributions have been lumped into a parasitic capacitive component and a parasitic inductive component. While this is not entirely accurate, it gives the designer a solid starting point for selecting the tank components.

Below are the parameters used in the model.

Cp Parasitic Capacitance
Lp Parasitic Inductance
LT Inductance of Coil
C1 Coupling Capacitor Value
Cb Capacitor for decoupling the Bias Pin
CV Varactor Diode Capacitance (Variable)

The values for these components are substituted into the following equations:

$$Ci = \frac{C1 \times CV}{C1 + CV} + Cp \qquad \text{Equation 2}$$

$$C = \frac{Ci \times Cb}{Ci + Cb} \qquad \text{Equation 3}$$

$$L = Lp + LT \qquad \text{Equation 4}$$

From Figure 2, it can be seen that the varactor capacitance (CV) is in series with the coupling capacitor (C1). This is calculated in Equation 2. For analysis purposes, the parasitic capacitances (CP) are treated as a lumped element and placed in parallel with the series combination of C1 and CV. This compound capacitance (Ci) is in series with the bias capacitor (Cb) which is calculated in Equation 3. The influences of the various capacitances; C1, CP, and Cb, impact the design by reducing the variable capacitance effects of the varactor which controls the tank resonant frequency and tuning range.

Now the results calculated from Equation 2, Equation 3 and Equation 4 can be substituted into Equation 1 to calculate the actual frequency of the tank.

To aid in analysis, it is recommended that the designer use a simple spreadsheet based on Equation 1 through Equation 4 to calculate the frequency of operation for various varactor/inductor selections before determining the initial starting condition for the tank.

The two main components at the heart of the tank are the inductor (LT) and the varactor diode (CV). The capacitance of a varactor diode junction changes with the amount of reverse bias voltage applied across the two terminals. This is the element which actually "tunes" the VCO. One characteristic of the varactor is the tuning ratio which is the ratio of the capacitance at specified minimum and maximum voltage points. For characterizing the MC12147, a Matsushita (Panasonic) varactor – MA393 was selected. This device has a typical capacitance of 11 pF at 1V and 3.7 pF at 4V and the C–V characteristic is fairly linear over that range. Similar performance was also acheived with Loral varactors. A multi–layer chip inductor was used to realize the LT component. These inductors had typical Q values in the 35–50 range for frequencies between 500 and 1000MHz.

Note: There are many suppliers of high performance varactors and inductors an Motorola can not recommend one vendor over another.

The Q (quality factor) of the components in the tank circuit has a direct impact on the resulting phase noise of the oscillator. In general, the higher the Q, the lower the phase noise of the resulting oscillator. In addition to the LT and CV components, only high quality surface–mount RF chip capacitors should be used in the tank circuit. These capacitors should have very low dielectric loss (high–Q). At a minimum, the capacitors selected should be operating 100 MHz below their series resonance point. As the desired frequency of operation increases, the values of the C1 and Cb capacitors will decrease since the series resonance point

is a function of the capacitance value. To simplify the selection of C1 and Cb, a table has been constructed based on the intended operating frequency to provide recommended starting points. These may need to be altered depending on the value of the varactor selected.

Frequency	C1	Cb
200 – 500 MHz	47 pF	47 pF
500 – 900 MHz	5.1 pF	15 pF
900 – 1200 MHz	2.7 pF	15 pF

The value of the Cb capacitor influences the VCO supply pushing. To minimize pushing, the Cb capacitor should be kept small. Since C1 is in series with the varactor, there is a strong relationship between these two components which influences the VCO sensitivity. Increasing the value of C1 tends to increase the sensitivity of the VCO.

The parasitic contributions Lp and Cp are related to the MC12147 as well as parasitics associated with the layout, tank components, and board material selected. The input capacitance of the device, bond pad, the wire bond, package/lead capacitance, wire bond inductance, lead inductance, printed circuit board layout, board dielectric, and proximity to the ground plane all have an impact on these parasitics. For example, if the ground plane is located directly below the tank components, a parasitic capacitor will be formed consisting of the solder pad, metal traces, board dielectric material, and the ground plane. The test fixture used for characterizing the device consisted of a two sided copper clad board with ground plane on the back. Nominal values where determined by selecting a varactor and characterizing the device with a number of different tank/ frequency combinations and then performing a curve fit with the data to determine values for Lp and Cp. The nominal values for the parasitic effects are seen below:

Parasitic Capacitance	Cp	4.2 pF
Parasitic Inductance	Lp	2.2 nH

These values will vary based on the users unique circuit board configuration.

Basic Guidelines:

1. Select a varactor with high Q and a reasonable capacitance versus voltage slope for the desired frequency range.
2. Select the value of Cb and C1 from the table above .
3. Calculate a value of inductance (L) which will result in achieving the desired center frequency. Note that L includes both LT and Lp.
4. Adjust the value of C1 to achieve the proper VCO sensitivity.
5. Re–adjust value of L to center VCO.
6. Prototype VCO design using selected components. It is important to use similar construction techniques and materials, board thickness, layout, ground plane spacing as intended for the final product.
7. Characterize tuning curve over the voltage operation conditions.
8. Adjust, as necessary, component values – L,C1, and Cb to compensate for parasitic board effects.
9. Evaluate over temperature and voltage limits.
10. Perform worst case analysis of tank component variation to insure proper VCO operation over full temperature and voltage range and make any adjustments as needed.

Outputs Q and QB are open collector outputs and need a inductor to V_{CC} to provide the voltage bias to the output transistor. In most applications, dc–blocking capacitors are placed in series with the output to remove the dc component before interfacing to other circuitry. These outputs are complementary and should have identical inductor values for each output. This will minimize switching noise on the V_{CC} supply caused by the outputs switching. It is important that both outputs be terminated, even if only one of the outputs is used in the application.

Referring to Figure 2, the recommended value for L2a and L2b should be 47 nH and the inductor components resonance should be at least 300 MHz greater than the maximum operating frequency. For operation above 1100 MHz, it may be necessary to reduce that inductor value to 33 nH. The recommended value for the coupling capacitors C6a, C6b, and C7 is 47 pF. Figure 2 also includes decoupling capacitors for the supply line as well as decoupling for the output inductors. Good RF decoupling practices should be used with a series of capacitors starting with high quality 100 pF chip capacitors close to the device. A typical layout is shown below in Figure 3.

The output amplitude of the Q and QB can be adjusted using the CNTL pin. Refering to Figure 1, if the CNTL pin is connected to ground, additional current will flow through the current source. When the pin is left open, the nominal current flowing through the outputs is 4 mA. When the pin is grounded, the current increases to a nominal value of 10 mA. So if a 50 ohm resistor was connected between the outputs and VCC, the output amplitude would change from 200 mV pp to 500 mV pp with an additional current drain for the device of 6 mA. To select a value between 4 and 10 mA, an external resistor can be added to ground. The equation below is used to calculate the current.

$$I_{out(nom)} = \frac{(200 + 136 + R_{ext}) \times 0.8V}{200 \times (136 + R_{ext})}$$

Figure 4 through Figure 13 illustrate typical performance achieved with the MC12147. The curves illustrate the tuning curve, supply pushing characteristics, output power, current drain, output spectrum, and phase noise performance. In most cases, data is present for both a 750 MHz and 1200 MHz tank design. The table below illustrates the component values used in the designs.

Component	750MHz Tank	1200MHz Tank	Units
R1	5000	5000	Ω
C1	5.1	2.7	pF
LT	4.7	1.8	nH
CV	3.7 @ 1.0 V 11 @ 4.0 V	3.7 @ 1.0 V 11 @ 4.0 V	pF
Cb	100*	15	pF
C6, C7	47	33	pF
L2	47	47	nH

* The value of Cb should be reduced to minimize pushing.

Figure 3. MC12147 Typical Layout
(Not to Scale)

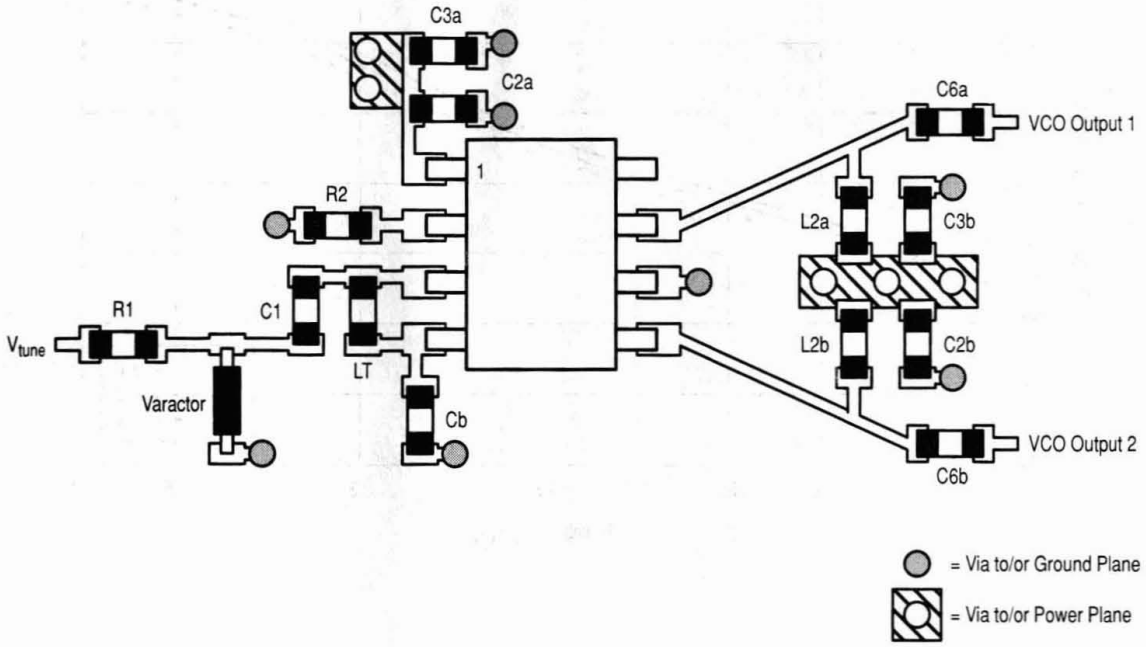


Figure 4. Typical VCO Tuning Curve, 750 MHz Tank

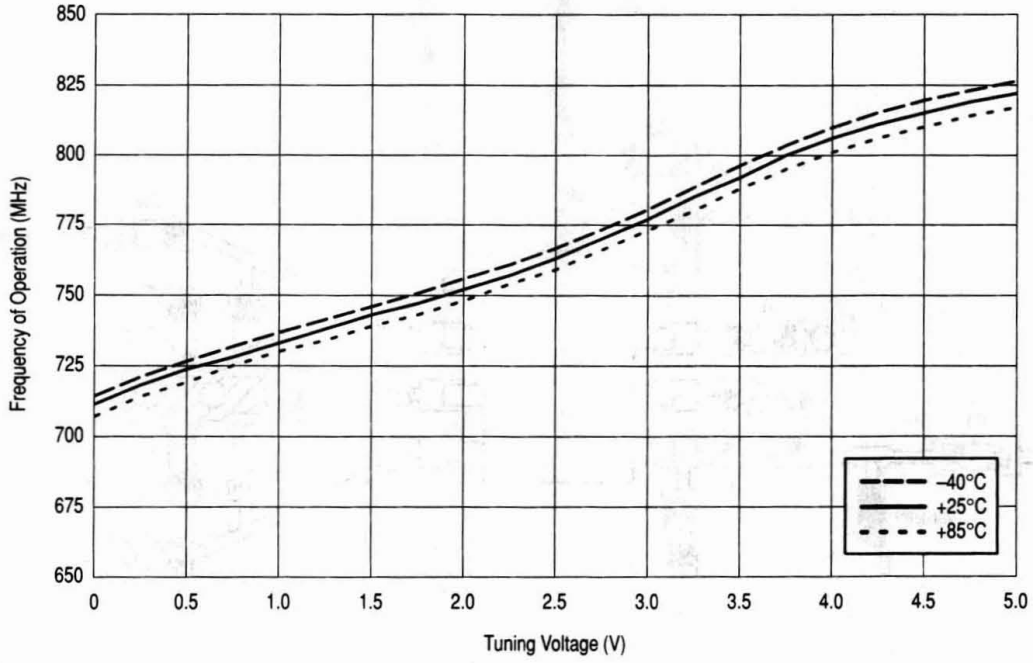


Figure 5. Typical Supply Pushing, 750MHz Tank

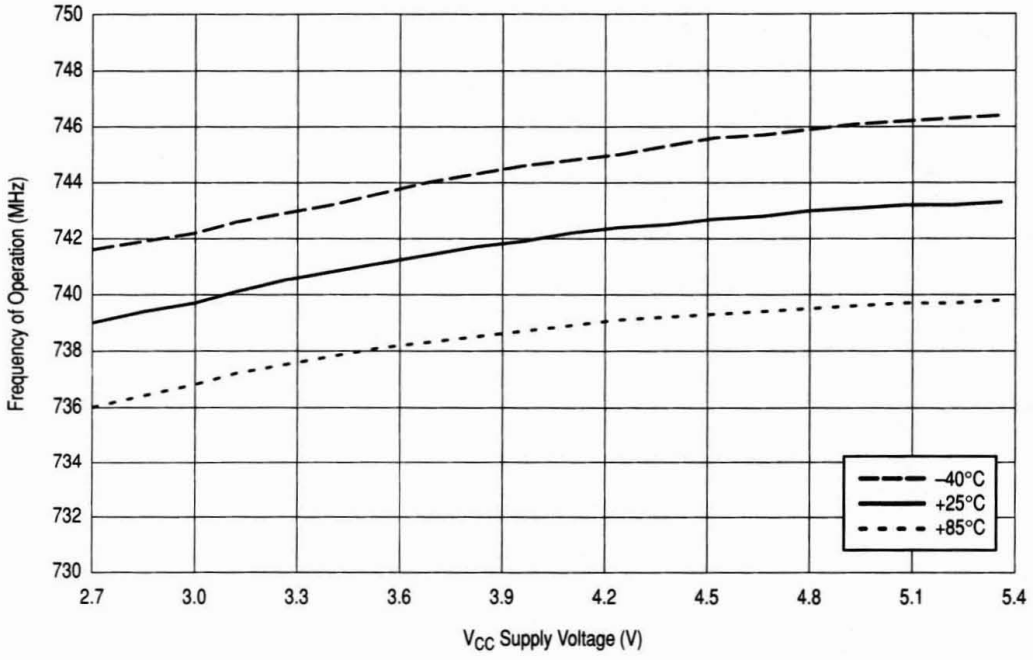


Figure 6. Typical Q/QB Output Power versus Supply, 750 MHz Tank

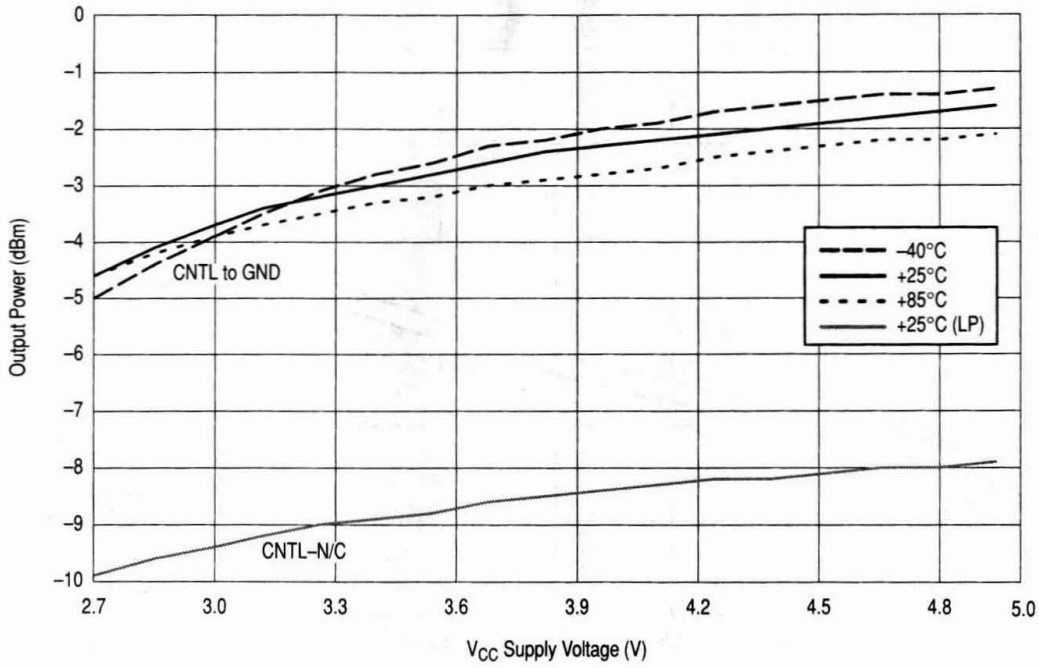


Figure 7. Typical Current Drain versus Supply, 750 MHz Tank

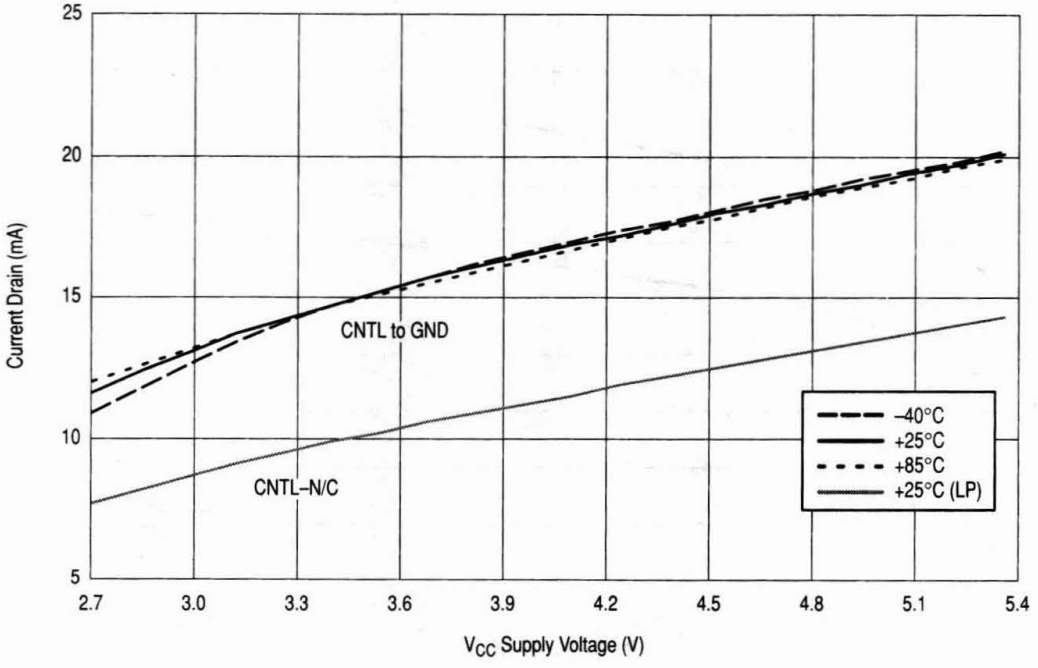


Figure 8. Typical VCO Tuning Curve, 1200 MHz Tank
(V_{CC} = 5.0 V)

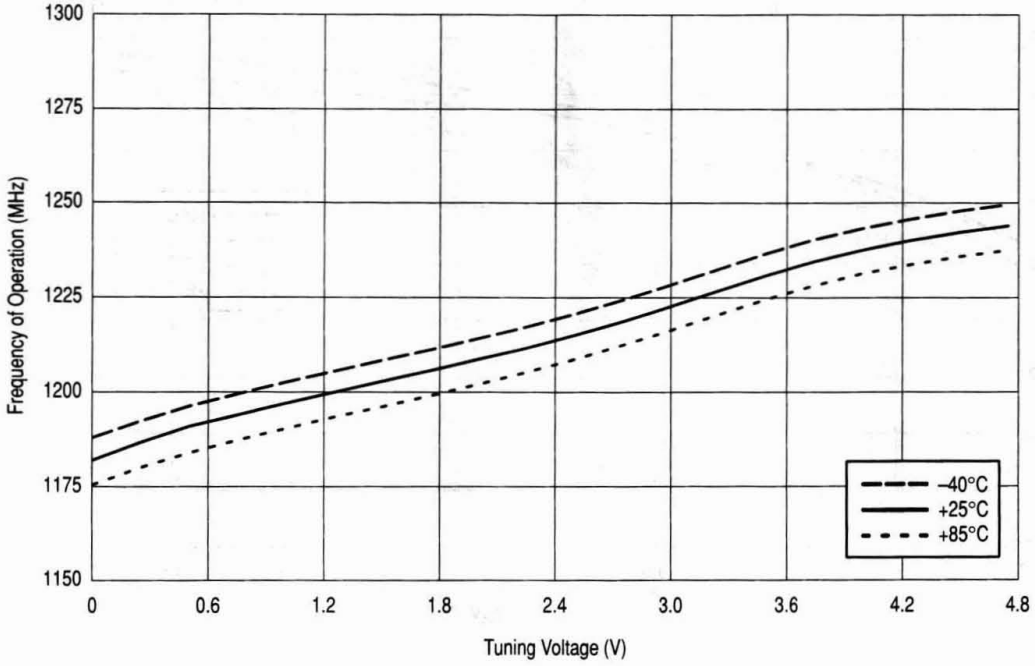


Figure 9. Typical Supply Pushing, 1200 MHz Tank

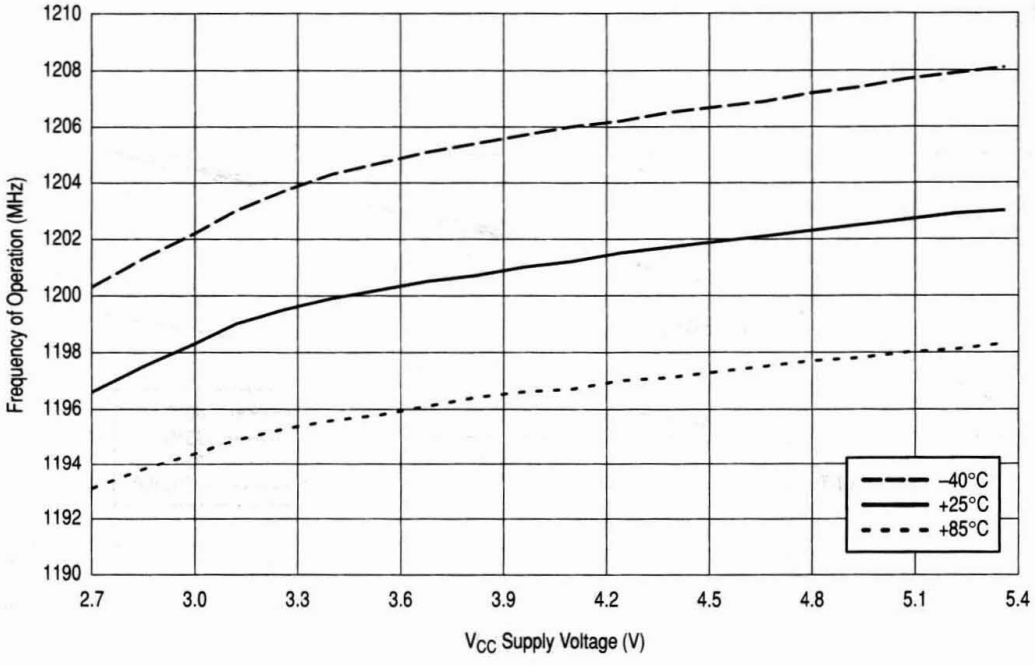


Figure 10. Q/QB Output Power versus Supply, 1200 MHz Tank

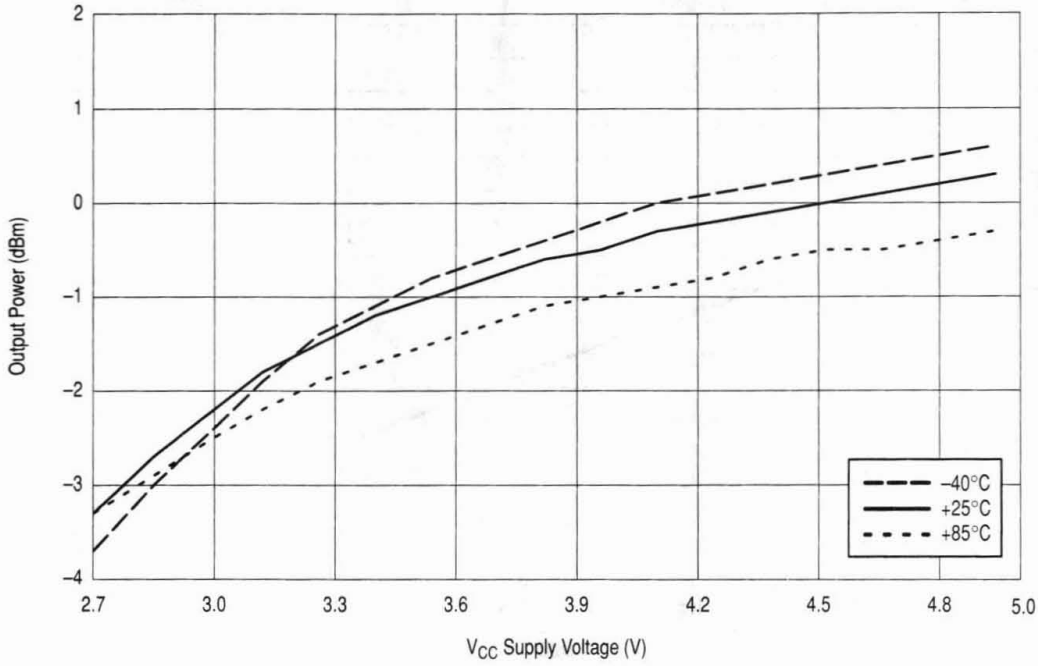


Figure 11. Typical VCO Output Spectrum

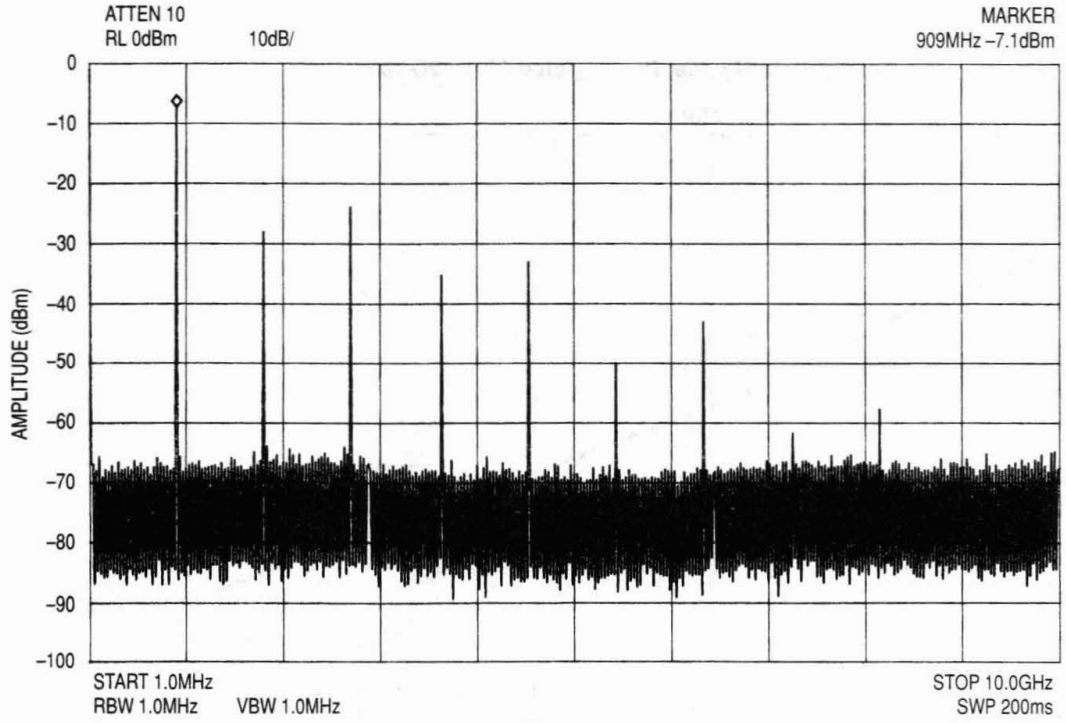


Figure 12. Typical Phase Noise Plot, 750 MHz Tank

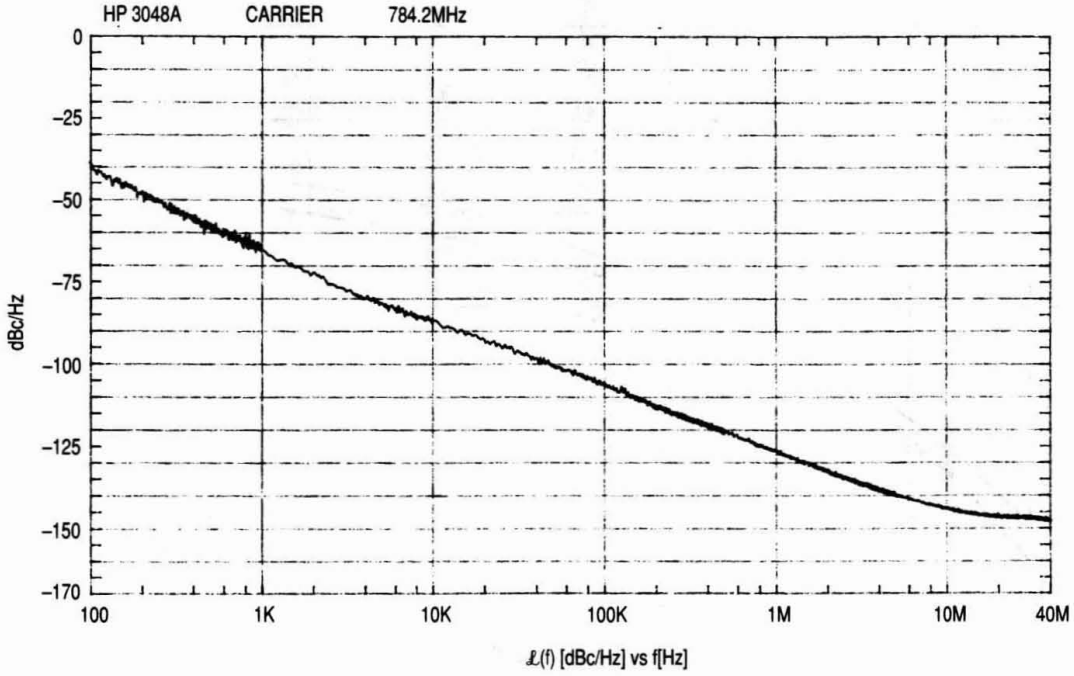
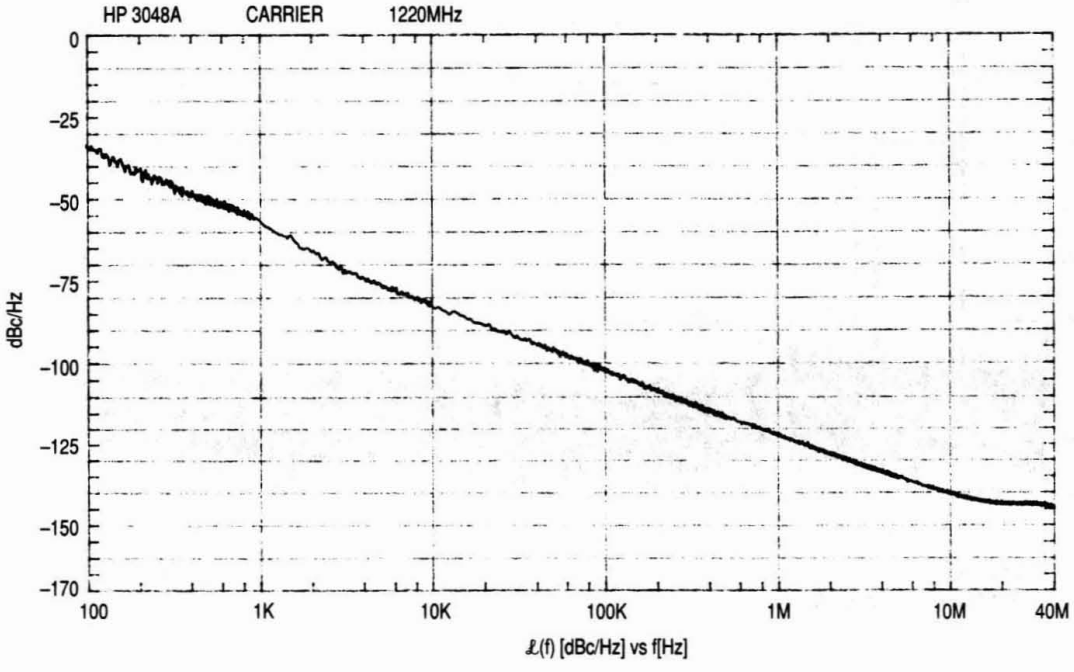


Figure 13. Typical Phase Noise Plot, 1200 MHz Tank



MOTOROLA

MC12148

Low Power Voltage Controlled Oscillator

The MC12148 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). This device may also be used in many other applications requiring a fixed frequency clock.

The MC12148 is ideal in applications requiring a local oscillator. Systems include electronic test equipment and digital high–speed telecommunications.

The MC12148 is based on the VCO circuit topology of the MC1648. The MC12148 has been realized utilizing Motorola's MOSAIC III advanced bipolar process technology which results in a design which can operate at a much higher frequency than the MC1648 while utilizing half the current. Please consult with the MC1648 data sheet for additional background information.

The ECL output circuitry of the MC12148 is not a traditional open emitter output structure and instead has an on–chip termination resistor with a nominal value of 500 ohms. This facilitates direct ac–coupling of the output signal into a transmission line. Because of this output configuration, an external pull–down resistor is not required to provide the output with a dc current path. This output is intended to drive one ECL load. If the user needs to fanout the signal, an ECL buffer such as the MC10EL16 Line Receiver/Driver should be used.

NOTE: The MC12148 is NOT useable as a crystal oscillator.

- Typical Operating Frequency Up to 1100 MHz
- Low–Power 20 mA at 5.0 Vdc Power Supply
- 8–Pin SOIC Package
- Phase Noise –90 dBc/Hz at 25 kHz Typical

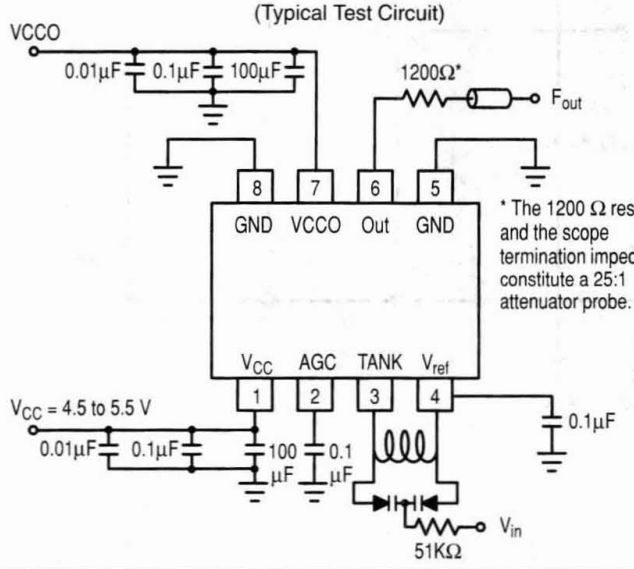
LOW POWER VOLTAGE CONTROLLED OSCILLATOR

SEMICONDUCTOR TECHNICAL DATA

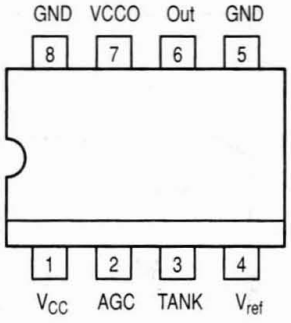
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

BLOCK DIAGRAM
(Typical Test Circuit)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12148D	$T_A = -40°$ to $+85°C$	SO–8
MC12148SD		SSOP–8

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pins 1, 7	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; T_A = –40 to 85°C, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{CC}	–	19	25	mA
Output Level HIGH (1.0 MΩ Impedance)		V_{OH}	3.95	4.17	4.61	V
Output Level LOW (1.0 MΩ Impedance)		V_{OL}	3.04	3.41	3.60	V
CSR @ 25 kHz Offset, 1.0 Hz BW		$\mathcal{L}(f)$	–	–90	–	dBc/Hz
CSR @ 1.0 MHz Offset, 1.0 Hz BW		$\mathcal{L}(f)$	–	–120	–	dBc/Hz
SNR (Signal to Noise Ratio from Carrier)		SNR	–	40	–	dB
Frequency Stability	Supply Drift	Fsts	–	3.6	–	KHz/mV
	Thermal Drift	Fstt	–	0.1	–	KHz/°C
Second Harmonic (from Carrier)		H2	–	–25	–	dBc

Figure 1. Circuit Schematic

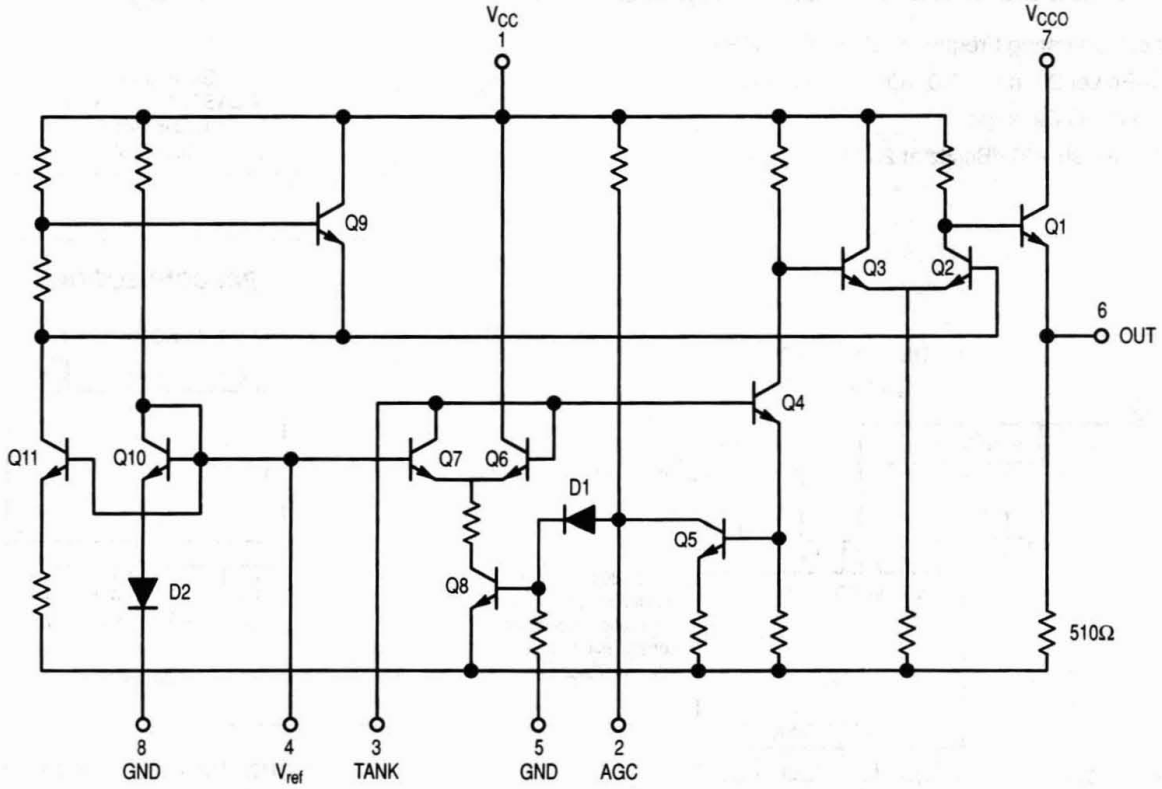
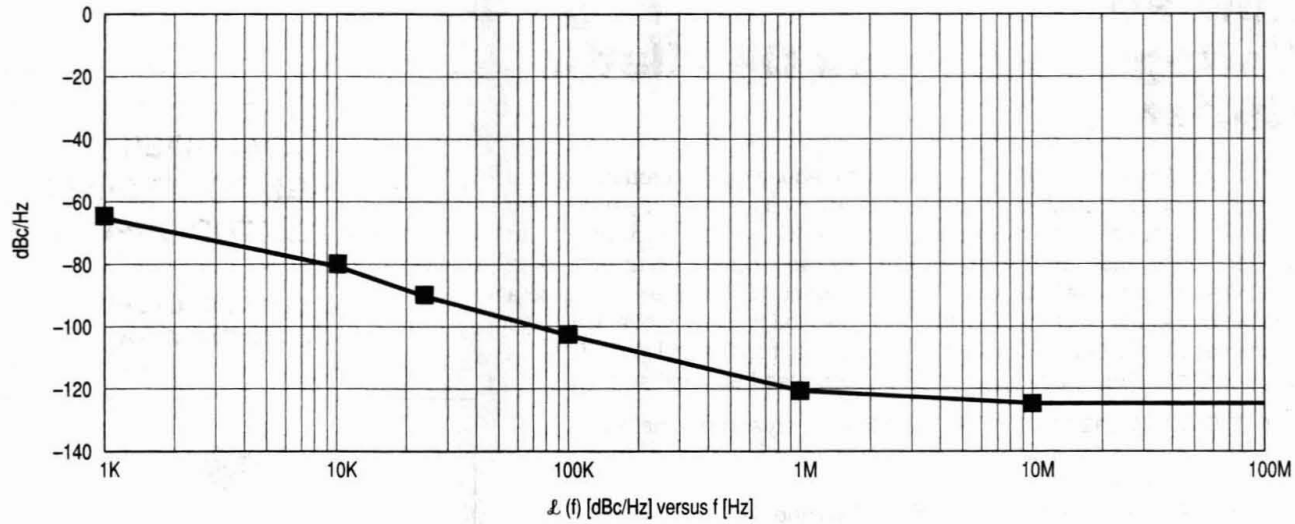


Figure 2. Typical Evaluation Results
(CSR MC12148 5.0 Vdc; V_{CC} @ 25°C; 930 MHz CW)



Tank Component Suppliers

Below are suppliers who manufacture tuning varactors and inductors which can be used to build an external tank circuit. Motorola has used these varactors and inductors for evaluation purposes, however, there are other vendors who manufacture similar products.

Coilcraft Inductors A01T thru A05T
Coilcraft–Coilcraft, Inc.
1102 Silver Lake Rd.
Gary, Illinois 60013
708–639–6400

Loral Tuning Varactors GC1500 Series
Loral
16 Maple Road
Chelmsford, Massachusetts 01824
508–256–8101 or 508–256–4113

Alpha Tuning Diodes DVH6730 Series
Alpha Semiconductor Devices Division
20 Sylvan Road
Woburn, MA 01801
617–935–5150

* At 1.1 GHz, use a Coilcraft A0IT Springair coil at 2.5 nH and a Loral Varactor 3.0 to 8.0 pF at V_{IN} = 1.0 to 5.0 V.

MOTOROLA

Low Power Voltage Controlled Oscillator Buffer

The MC12149 is intended for applications requiring high frequency signal generation up to 1300 MHz. An external tank circuit is used to determine the desired frequency of operation. The VCO is realized using an emitter–coupled pair topology. The MC12149 can be used with an integrated PLL IC such as the MC12202 1.1 GHz Frequency Synthesizer to realize a complete PLL sub–system. The device is specified to operate over a voltage supply range of 2.7 to 5.5 V. It has a typical current consumption of 15 mA at 3.0 V which makes it attractive for battery operated handheld systems.

NOTE: The MC12149 is NOT suitable as a crystal oscillator.

- Operates Up to 1.3 GHz
- Space–Efficient 8–Pin SOIC or SSOP Package
- Low Power 15 mA Typical @ 3.0 V Operation
- Supply Voltage of 2.7 to 5.5 V
- Typical 900 MHz Performance
  - Phase Noise –105 dBc/Hz @ 100 kHz Offset
  - Tuning Voltage Sensitivity of 20 MHz/V
- Output Amplitude Adjustment Capability
- Two High Drive Outputs With a Typical Range from –8.0 to –2.0 dBm
- One Low–Drive Output for Interfacing to a Prescaler

The device has three high frequency outputs which make it attractive for transceiver applications which require both a transmit and receive local oscillator (LO) signal as well as a lower amplitude signal to drive the prescaler input of the frequency synthesizer. The outputs Q and QB are available for servicing the receiver IF and transmitter up–converter single–ended. In receiver applications, the outputs can be used together if it is necessary to generate a differential signal for the receiver IF. Because the Q and QB outputs are open collector, terminations to the V_{CC} supply are required for proper operation. Since the outputs are complementary, BOTH outputs must be terminated even if only one is needed. The Q and QB outputs have a nominal drive level of –8dBm to conserve power. If addition signal amplitude is needed, a level adjustment pin (CNTL) is available, which when tied to ground, boosts the nominal output levels to –2.0 dBm. A low power VCO output (Q2) is also provided to drive the prescaler input of the PLL. The amplitude of this signal is nominally 500 mV which is suitable for most prescalers.

External components required for the MC12149 are: (1) tank circuit (LC network); (2) Inductor/capacitor to provide the termination for the open collector outputs; and (3) adequate supply voltage bypassing. The tank circuit consists of a high–Q inductor and varactor components. The preferred tank configuration allows the user to tune the VCO across the full supply range. VCO performance such as center frequency, tuning voltage sensitivity, and noise characteristics are dependent on the particular components and configuration of the VCO tank circuit.

MC12149

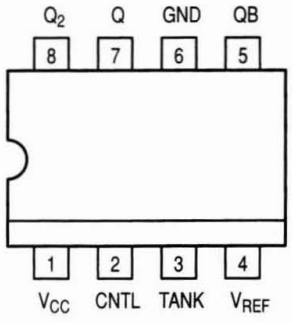
LOW POWER VOLTAGE CONTROLLED OSCILLATOR BUFFER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

SD SUFFIX
PLASTIC PACKAGE
CASE 940
(SSOP–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12149D	T_A = – 40° to +85°C	SO–8
MC12149SD		SSOP–8

PIN NAMES

Pin	Function
V_{CC}	Power Supply
CNTL	Amplitude Control for Q, QB Output Pair
TANK	Tank Circuit Input
V_{REF}	Bias Voltage Output
QB	Open Collector Output
GND	Ground
Q	Open Collector Output
Q_2	Low Power Output

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 1	V_{CC}	-0.5 to 7.0	V
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Maximum Output Current, Pin 8	I_O	7.5	mA
Maximum Output Current, Pin 5,7	I_O	12	mA

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = -40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (CNTL=GND) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	16 23.5	20 30	mA
Supply Current (CNTL=OPEN) V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	– –	10 15	15.0 24.5	mA
Output Amplitude (Pin 8) V_{CC} = 2.7 V High Impedance Load V_{CC} = 2.7 V	V_{OH}, V_{OL}	1.75 1.20	1.85 1.35	1.95 1.50	V
Output Amplitude (Pin 8) V_{CC} = 5.5 V High Impedance Load V_{CC} = 5.5 V	V_{OH}, V_{OL}	4.50 3.85	4.6 4.0	4.70 4.15	V
Output Amplitude (Pin 5 & 7) [Note 1] V_{CC} = 2.7 V 50 Ω to V_{CC} V_{CC} = 2.7 V	V_{OH}, V_{OL}	2.6 2.1	2.7 2.3	– 2.4	V
Output Amplitude (Pin 5 & 7) [Note 1] V_{CC} = 5.5 V 50Ω to V_{CC} V_{CC} = 5.5V	V_{OH}, V_{OL}	5.4 4.8	5.5 5.0	– 5.1	V
Tuning Voltage Sensitivity [Notes 2 and 3]	T_{stg}	–	20	–	MHz/V
Frequency of Operation	F_C	100	–	1300	MHz
CSR at 10 kHz Offset, 1Hz BW [Notes 2 and 3]	ℒ(f)	–	–85	–	dBc/Hz
CSR at 100 kHz Offset, 1Hz BW [Notes 2 and 3]	ℒ(f)	–	–105	–	dBc/Hz
Frequency Stability [Notes 3 and 4] Supply Drift Thermal Drift	 F_{sts} f_{stt}	 – –	 0.8 50	 – –	 MHz/V KHz/°C

NOTES: 1. CNTL pin tied to ground.
2. Actual performance depends on tank components selected.
3. See Figure 12, 750 MHz tank.
4. T = 25°C, V_{CC} = 5.0 V ±10%

OPERATIONAL CHARACTERISTICS

A simplified schematic of the MC12149 is found in Figure 1. The oscillator incorporates positive feedback by coupling the base of transistor Q2 to the collector of transistor Q1. In order to minimize interaction between the VCO outputs and the oscillator tank transistor pair, a buffer is incorporated into the circuit. This differential buffer is realized by the Q3 and Q4 transistor pair. The differential buffer drives the gate which contains the primary open collector outputs, Q and QB. The output is actually a current which has been set by an internal bias driver to a nominal current of 4mA. Additional circuitry is incorporated into the tail of the current source which allows the current source to be increased to approximately 10 mA. This is accommodated by the addition of a resistor which is brought out to the CNTL pin. When this pin is tied to ground, the additional current is sourced through the current source thus increasing the output amplitude of the Q/QB output pair. If less than 10mA of current is needed, a resistor can be added to ground which reduces the amount of current.

The Q/QB outputs drive an additional differential buffer which generate the Q2 output signal. To minimize current, the circuit is realized as an emitter–follower buffer with an on chip pull down resistor. This output is intended to drive the prescaler input of the PLL synthesizer block.

APPLICATION INFORMATION

Figure 2 illustrates the external components necessary for the proper operation of the VCO buffer. The tank circuit configuration in this figure allows the VCO to be tuned across the full operating voltage of the power supply. This is very important in 3.0 V applications where it is desirable to utilize as much of the operating supply range as possible so as to minimize the VCO sensitivity (MHz/V). In most situations, it is desirable to keep the sensitivity low so the circuit will be less susceptible to external noise influences. An additional benefit to this configuration is that additional regulation/ filtering can be incorporated into the V_{CC} line without compromising the tuning range of the VCO. With the ac–coupled tank configuration, the V_{tune} voltage can be greater than the V_{CC} voltage supplied to the device.

There are four main areas that the user directly influences the performance of the VCO. These include Tank Design, Output Termination Selection, Power Supply Decoupling, and Circuit Board Layout/Grounding.

The design of the tank circuit is critical to the proper operation of the VCO. This tank circuit directly impacts the main VCO operating characteristics:

1) Frequency of Operation
2) Tuning Sensitivity
3) Voltage Supply Pushing
4) Phase Noise Performance

The tank circuit, in its simplest form, is realized as an LC circuit which determines the VCO operating frequency. This is described in Equation 1.

$$f_o = \frac{1}{2\pi\sqrt{LC}} \qquad \text{Equation 1}$$

In the practical case, the capacitor is replaced with a varactor diode whose capacitance changes with the voltage applied, thus changing the resonant frequency at which the VCO tank operates. The capacitive component in Equation 1 also needs to include the input capacitance of the device and other circuit and parasitic elements. Typically, the inductor is realized as a surface mount chip or a wound–coil. In addition, the lead inductance and board inductance and capacitance also have an impact on the final operating point.

Figure 1. Simplified Schematic

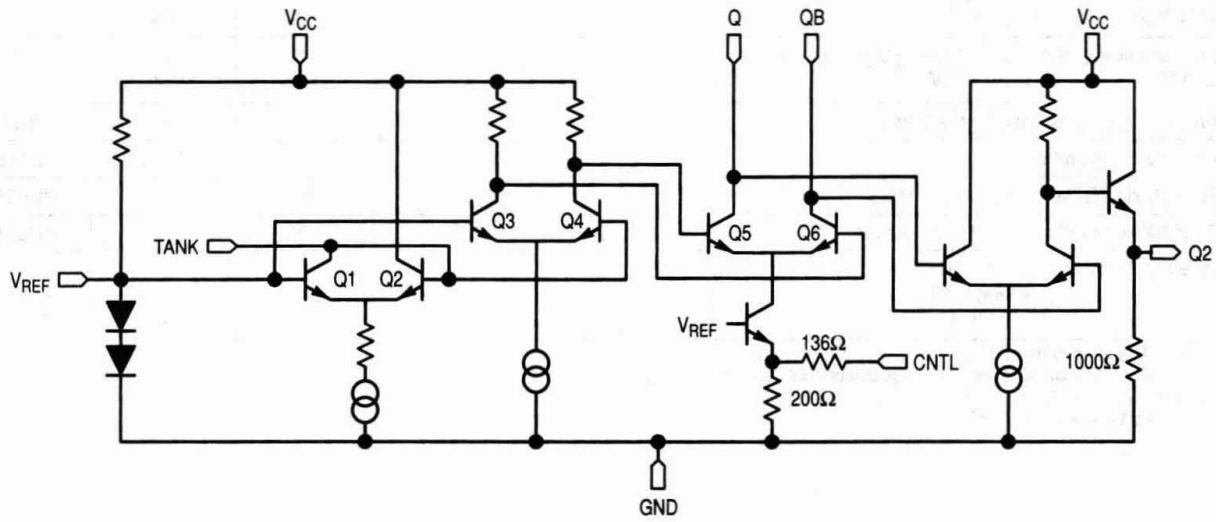
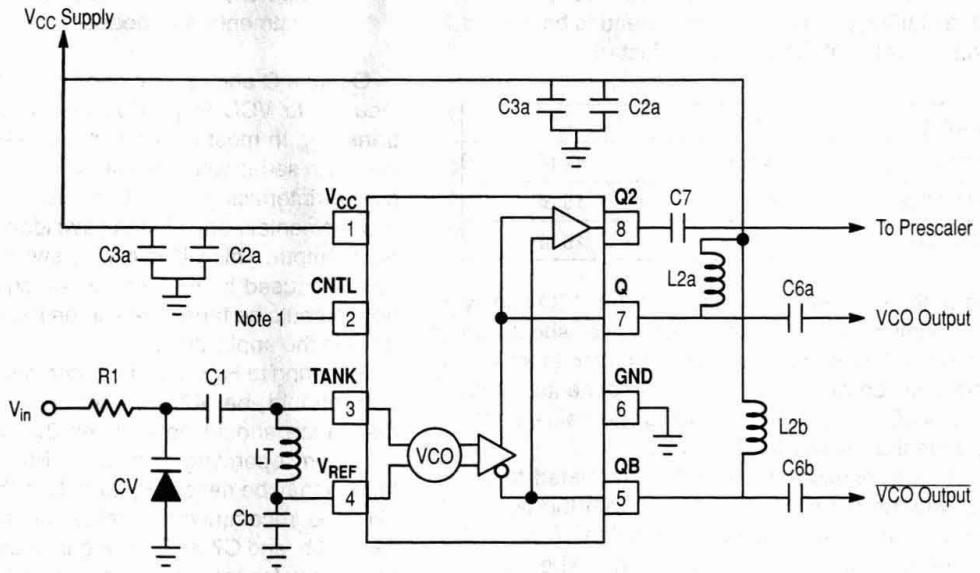


Figure 2. MC12149 Typical External Component Connections



1. This input can be left open, tied to ground, or tied with a resistor to ground, depending on the desired output amplitude needed at the Q and QB output pair.
2. Typical values for R1 range from 5.0 kΩ to 10 kΩ.

A simplified linear approximation of the device, package, and typical board parasitics has been developed to aid the designer in selecting the proper tank circuit values. All the parasitic contributions have been lumped into a parasitic capacitive component and a parasitic inductive component. While this is not entirely accurate, it gives the designer a solid starting point for selecting the tank components.

Below are the parameters used in the model.

Cp Parasitic Capacitance
Lp Parasitic Inductance
LT Inductance of Coil
C1 Coupling Capacitor Value
Cb Capacitor for decoupling the Bias Pin
CV Varactor Diode Capacitance (Variable)

The values for these components are substituted into the following equations:

$$Ci = \frac{C1 \times CV}{C1 + CV} + Cp \qquad \text{Equation 2}$$

$$C = \frac{Ci \times Cb}{Ci + Cb} \qquad \text{Equation 3}$$

$$L = Lp + LT \qquad \text{Equation 4}$$

From Figure 2, it can be seen that the varactor capacitance (CV) is in series with the coupling capacitor (C1). This is calculated in Equation 2. For analysis purposes, the parasitic capacitances (CP) are treated as a lumped element and placed in parallel with the series combination of C1 and CV. This compound capacitance (Ci) is in series with the bias capacitor (Cb) which is calculated in Equation 3. The influences of the various capacitances; C1, CP, and Cb, impact the design by reducing the variable capacitance effects of the varactor which controls the tank resonant frequency and tuning range.

Now the results calculated from Equation 2, Equation 3 and Equation 4 can be substituted into Equation 1 to calculate the actual frequency of the tank.

To aid in analysis, it is recommended that the designer use a simple spreadsheet based on Equation 1 through Equation 4 to calculate the frequency of operation for various varactor/inductor selections before determining the initial starting condition for the tank.

The two main components at the heart of the tank are the inductor (LT) and the varactor diode (CV). The capacitance of a varactor diode junction changes with the amount of reverse bias voltage applied across the two terminals. This is the element which actually "tunes" the VCO. One characteristic of the varactor is the tuning ratio which is the ratio of the capacitance at specified minimum and maximum voltage points. For characterizing the MC12149, a Matsushita (Panasonic) varactor – MA393 was selected. This device has a typical capacitance of 11 pF at 1.0 V and 3.7 pF at 4.0 V and the C–V characteristic is fairly linear over that range. Similar performance was also acheived with Loral varactors. A multi–layer chip inductor was used to realize the LT component. These inductors had typical Q values in the 35 to 50 range for frequencies between 500 and 1000 MHz.

Note: There are many suppliers of high performance varactors and inductors and Motorola can not recommend one vendor over another.

The Q (quality factor) of the components in the tank circuit has a direct impact on the resulting phase noise of the oscillator. In general, the higher the Q, the lower the phase noise of the resulting oscillator. In addition to the LT and CV components, only high quality surface–mount RF chip capacitors should be used in the tank circuit. These capacitors should have very low dielectric loss (high–Q). At a minimum, the capacitors selected should be operating 100 MHz below their series resonance point. As the desired frequency of operation increases, the values of the C1 and Cb capacitors will decrease since the series resonance point

is a function of the capacitance value. To simplify the selection of C1 and Cb, a table has been constructed based on the intended operating frequency to provide recommended starting points. These may need to be altered depending on the value of the varactor selected.

Frequency	C1	Cb
200 – 500 MHz	47 pF	47 pF
500 – 900 MHz	5.1 pF	15 pF
900 – 1200 MHz	2.7 pF	15 pF

The value of the Cb capacitor influences the VCO supply pushing. To minimize pushing, the Cb capacitor should be kept small. Since C1 is in series with the varactor, there is a strong relationship between these two components which influences the VCO sensitivity. Increasing the value of C1 tends to increase the sensitivity of the VCO.

The parasitic contributions Lp and Cp are related to the MC12149 as well as parasitics associated with the layout, tank components, and board material selected. The input capacitance of the device, bond pad, the wire bond, package/lead capacitance, wire bond inductance, lead inductance, printed circuit board layout, board dielectric, and proximity to the ground plane all have an impact on these parasitics. For example, if the ground plane is located directly below the tank components, a parasitic capacitor will be formed consisting of the solder pad, metal traces, board dielectric material, and the ground plane. The test fixture used for characterizing the device consisted of a two sided copper clad board with ground plane on the back. Nominal values where determined by selecting a varactor and characterizing the device with a number of different tank/ frequency combinations and then performing a curve fit with the data to determine values for Lp and Cp. The nominal values for the parasitic effects are seen below:

Parasitic Capacitance	Cp	4.2 pF
Parasitic Inductance	Lp	2.2 nH

These values will vary based on the users unique circuit board configuration.

Basic Guidelines:

1. Select a varactor with high Q and a reasonable capacitance versus voltage slope for the desired frequency range.
2. Select the value of Cb and C1 from the table above .
3. Calculate a value of inductance (L) which will result in achieving the desired center frequency. Note that L includes both LT and Lp.
4. Adjust the value of C1 to achieve the proper VCO sensitivity.
5. Re–adjust value of L to center VCO.
6. Prototype VCO design using selected components. It is important to use similar construction techniques and materials, board thickness, layout, ground plane spacing as intended for the final product.
7. Characterize tuning curve over the voltage operation conditions.
8. Adjust, as necessary, component values – L,C1, and Cb to compensate for parasitic board effects.
9. Evaluate over temperature and voltage limits.
10. Perform worst case analysis of tank component variation to insure proper VCO operation over full temperature and voltage range and make any adjustments as needed.

Outputs Q and QB are open collector outputs and need a inductor to VCC to provide the voltage bias to the output transistor. In most applications, DC–blocking capacitors are placed in series with the output to remove the DC component before interfacing to other circuitry. These outputs are complementary and should have identical inductor values for each output. This will minimize switching noise on the VCC supply caused by the outputs switching. It is important that both outputs be terminated, even if only one of the outputs is used in the application.

Referring to Figure 2, the recommended value for L2a and L2b should be 47 nH and the inductor components resonance should be at least 300 MHz greater than the maximum operating frequency. For operation above 1100 MHz, it may be necessary to reduce that inductor value to 33 nH. The recommended value for the coupling capacitors C6a, C6b, and C7 is 47 pF. Figure 2 also includes decoupling capacitors for the supply line as well as decoupling for the output inductors. Good RF decoupling practices should be used with a series of capacitors starting with high quality 100 pF chip capacitors close to the device. A typical layout is shown below in Figure 3.

The output amplitude of the Q and QB can be adjusted using the CNTL pin. Refering to Figure 1, if the CNTL pin is connected to ground, additional current will flow through the current source. When the pin is left open, the nominal current flowing through the outputs is 4 mA. When the pin is grounded, the current increases to a nominal value of 10 mA. So if a 50 ohm resistor was connected between the outputs and VCC, the output amplitude would change from 200 mV pp to 500 mV pp with an additional current drain for the device of 6 mA. To select a value between 4 and 10 mA, an external resistor can be added to ground. The equation below is used to calculate the current.

$$I_{out(nom)} = \frac{(200 + 136 + R_{ext}) \times 0.8V}{200 \times (136 + R_{ext})}$$

Figure 4 through Figure 13 illustrate typical performance achieved with the MC12149. The curves illustrate the tuning curve, supply pushing characteristics, output power, current drain, output spectrum, and phase noise performance. In most cases, data is present for both a 750 MHz and 1200 MHz tank design. The table below illustrates the component values used in the designs.

Component	750MHz Tank	1200MHz Tank	Units
R1	5000	5000	Ω
C1	5.1	2.7	pF
LT	4.7	1.8	nH
CV	3.7 @ 1.0 V 11 @ 4.0 V	3.7 @ 1.0 V 11 @ 4.0 V	pF
Cb	100*	15	pF
C6, C7	47	33	pF
L2	47	47	nH

NOTE: * The value of Cb should be reduced to minimize pushing.

Figure 3. MC12149 Typical Layout
(Not to Scale)

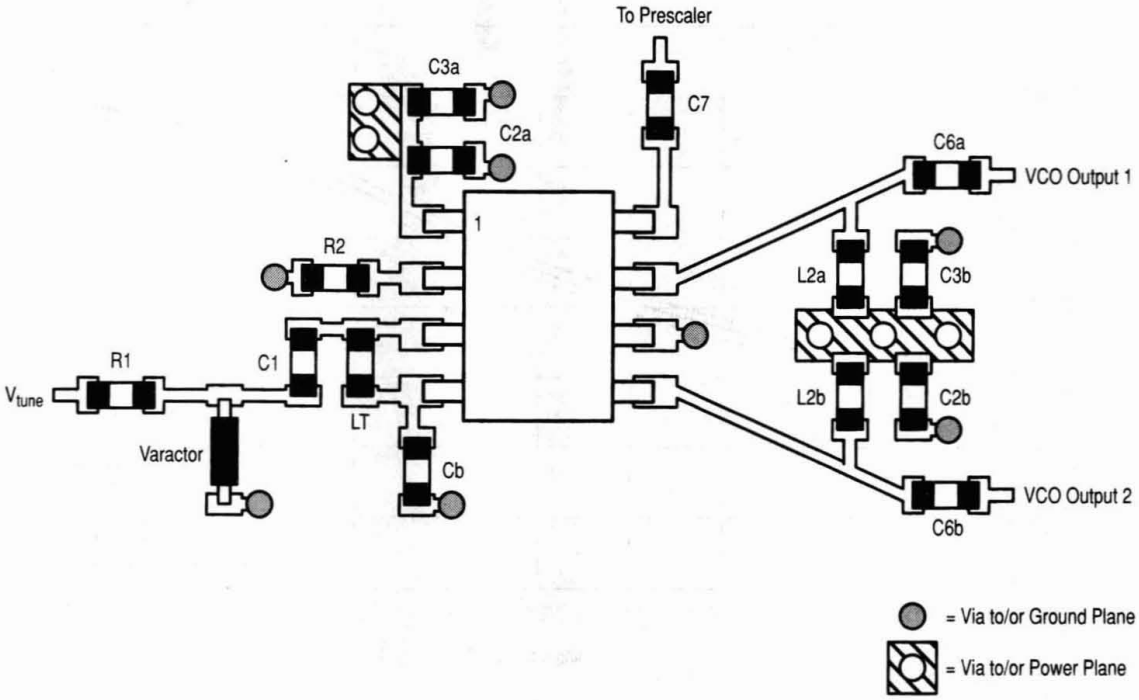


Figure 4. Typical VCO Tuning Curve, 750 MHz Tank

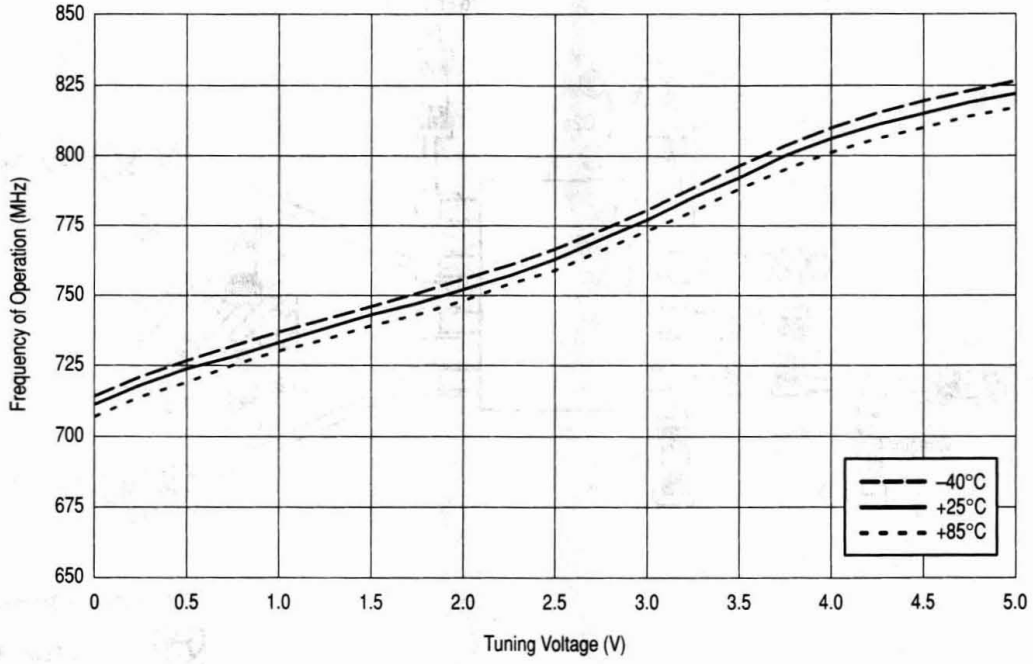


Figure 5. Typical Supply Pushing, 750 MHz Tank

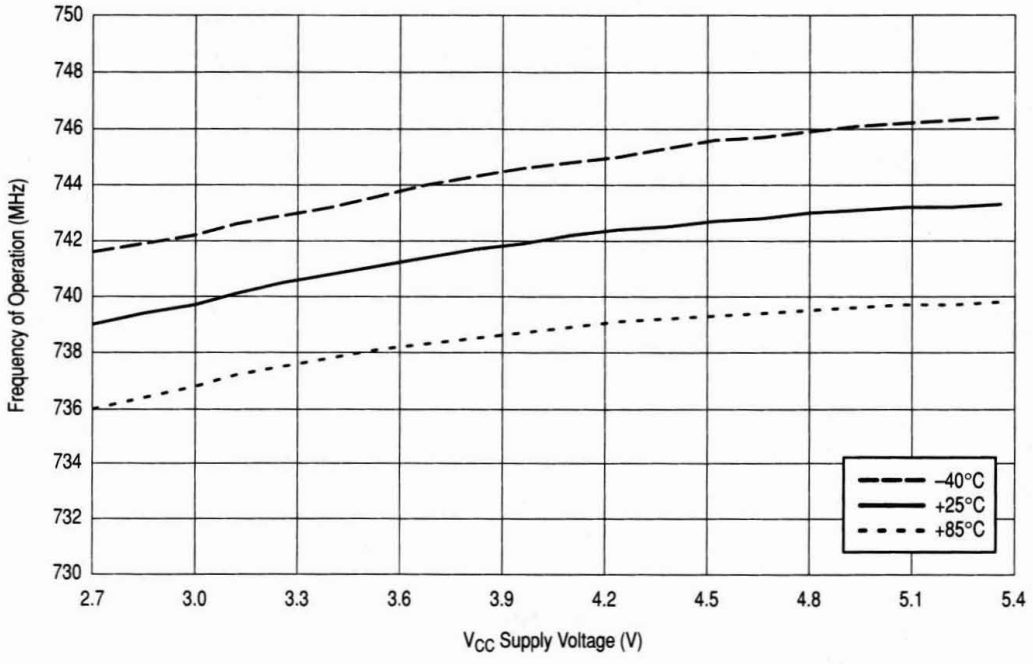


Figure 6. Typical Q/QB Output Power versus Supply, 750 MHz Tank

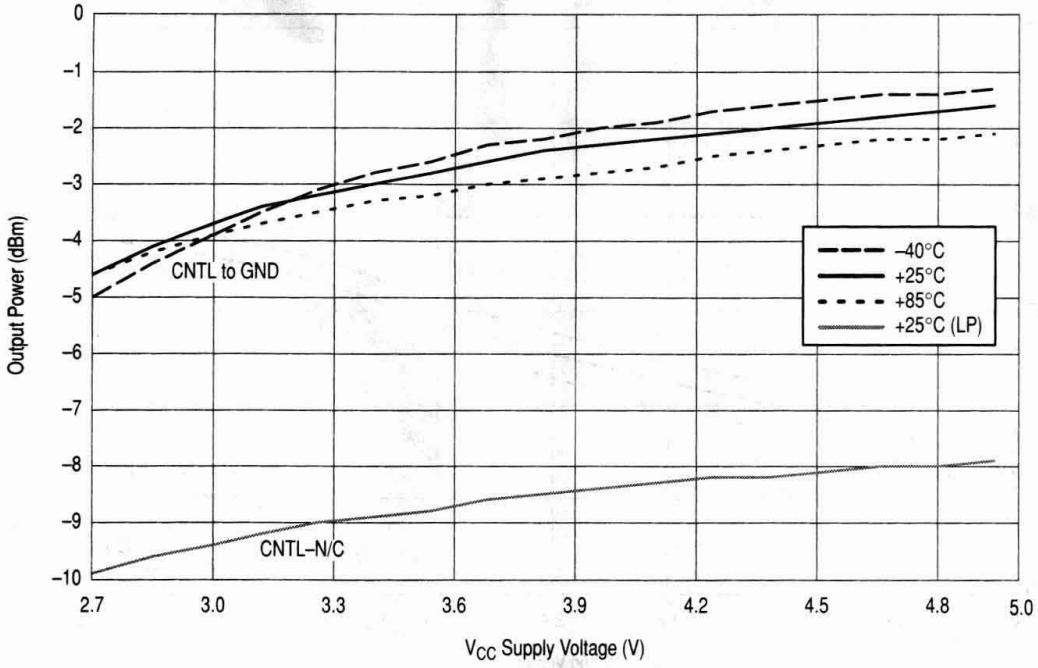


Figure 7. Typical Current Drain versus Supply, 750 MHz Tank

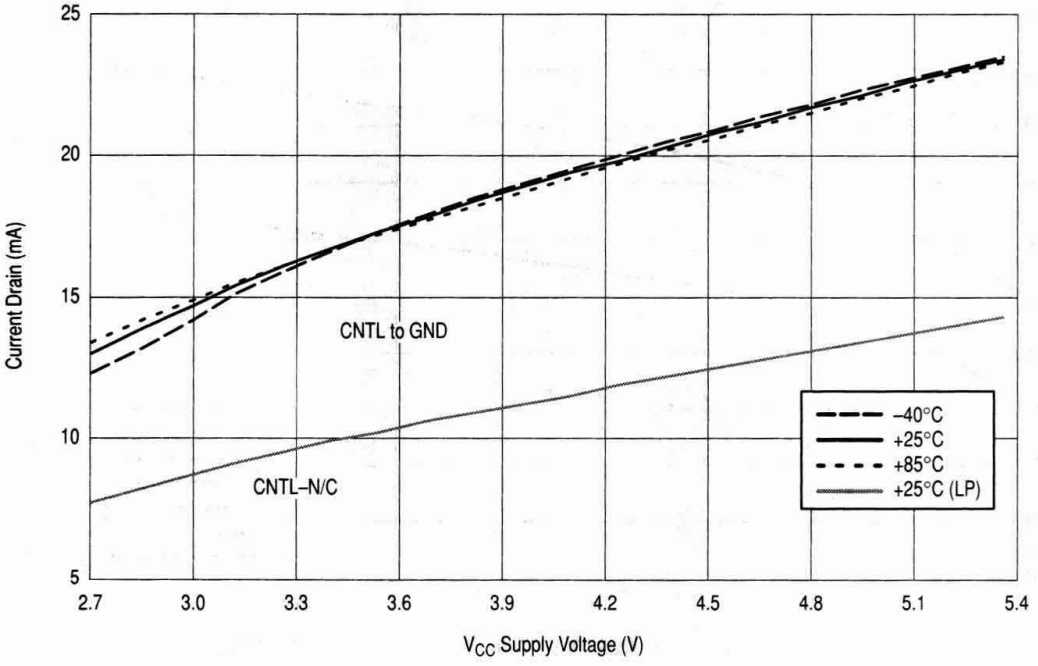


Figure 8. Typical VCO Tuning Curve, 1200 MHz Tank
(V_{CC} = 5.0 V)

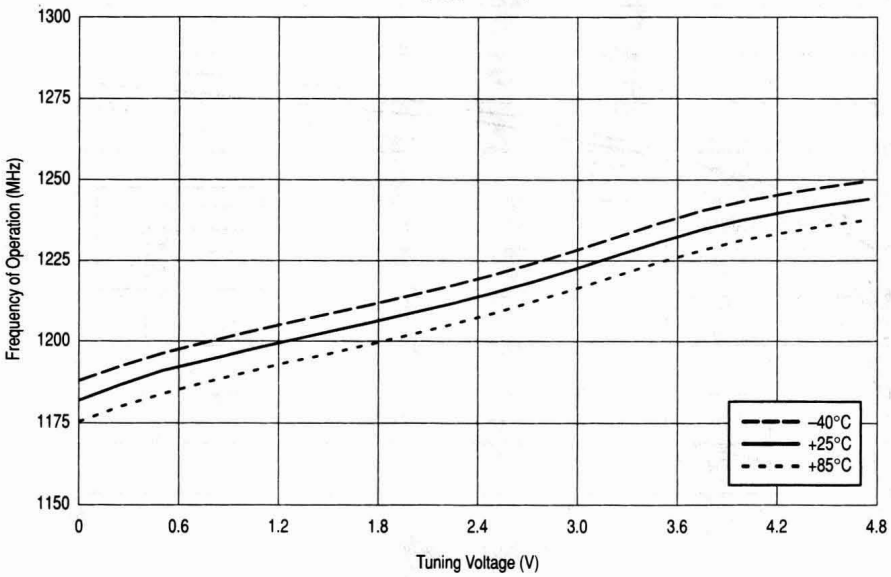


Figure 9. Typical Supply Pushing, 1200 MHz Tank

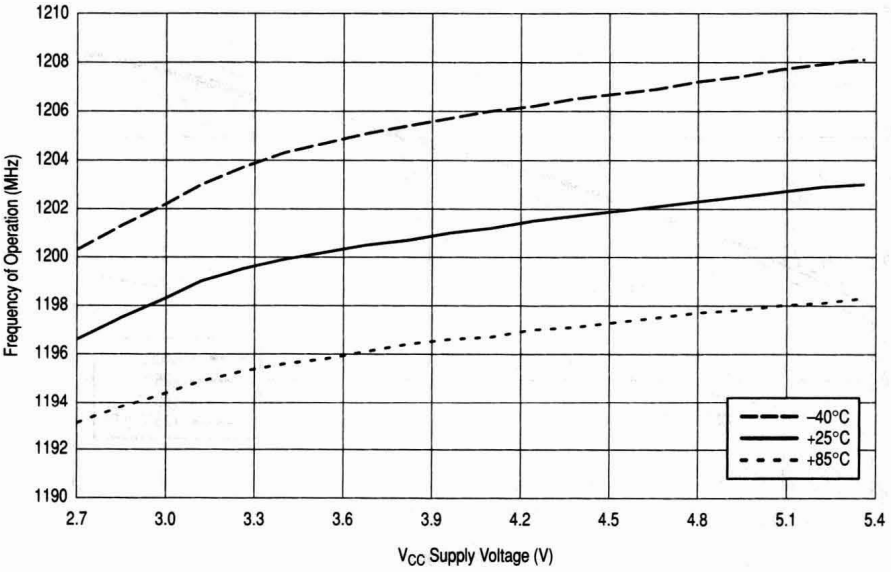


Figure 10. Q/QB Output Power versus Supply, 1200 MHz Tank

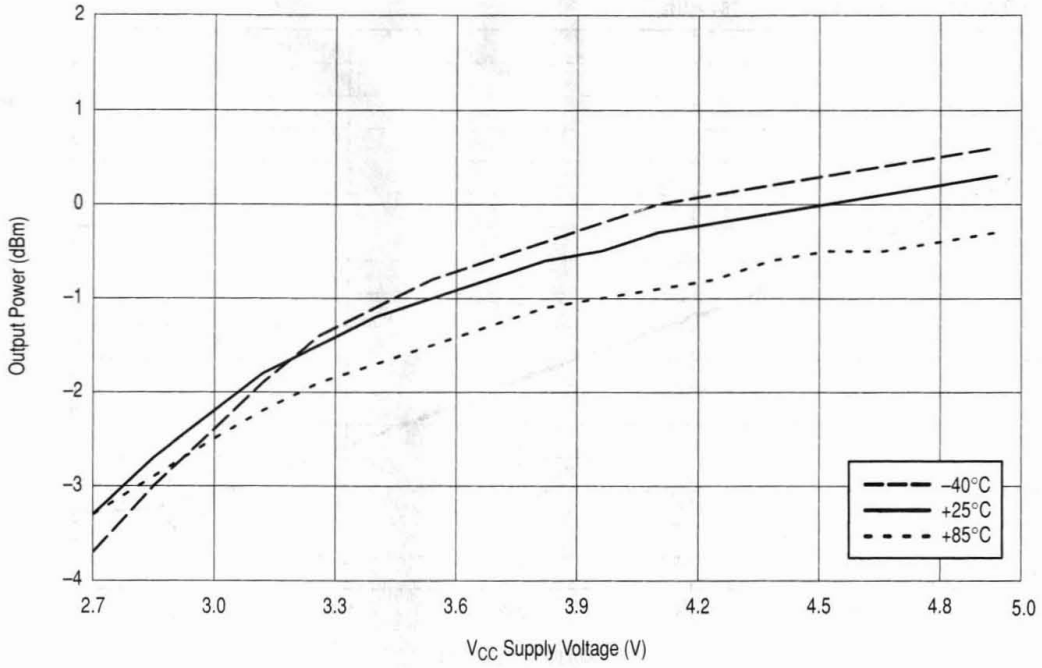


Figure 11. Typical VCO Output Spectrum

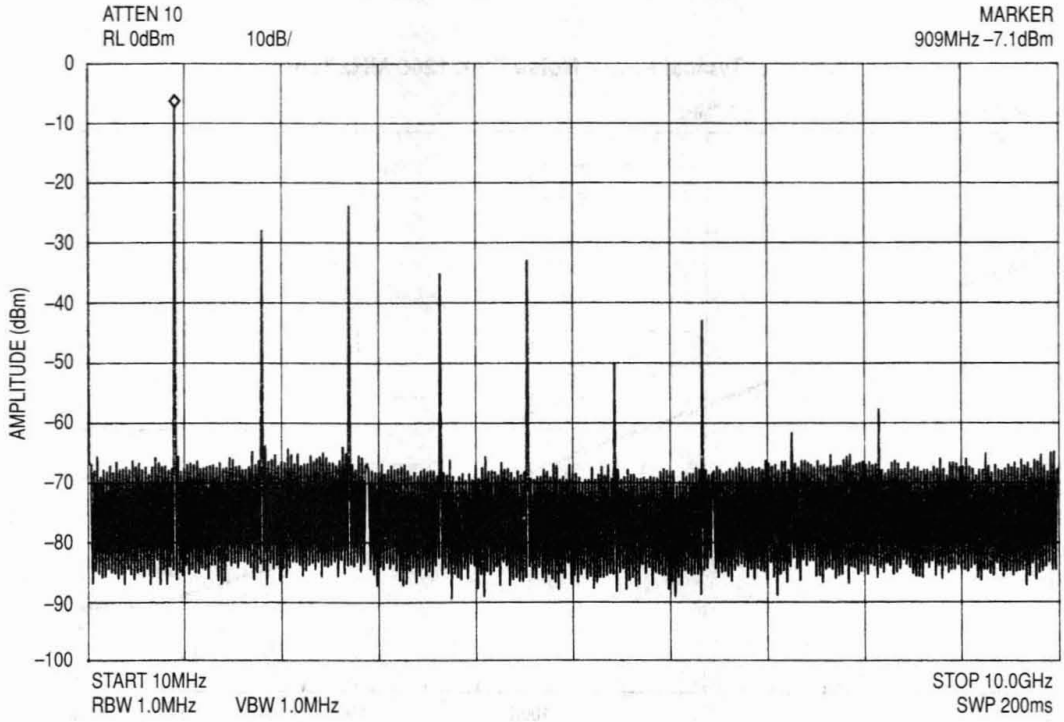


Figure 12. Typical Phase Noise Plot, 750 MHz Tank

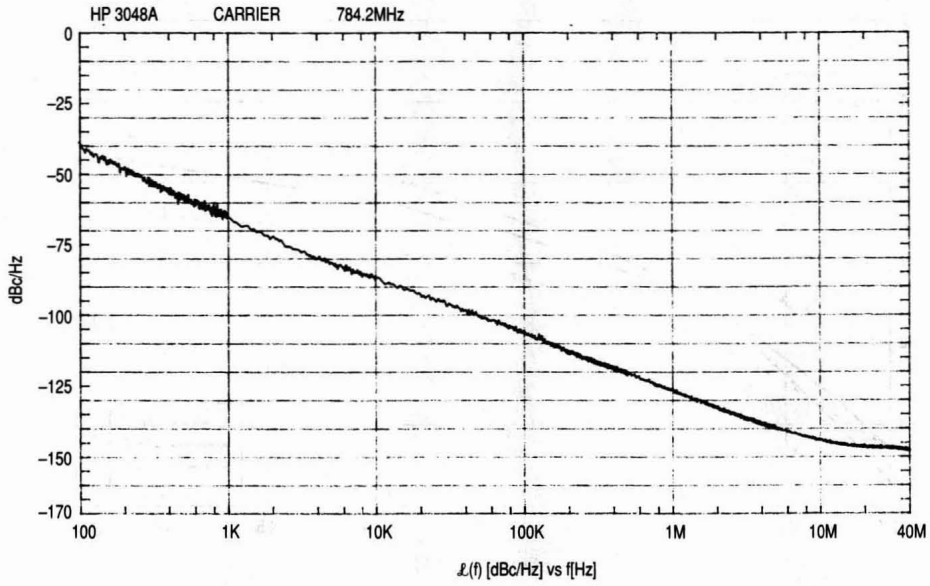
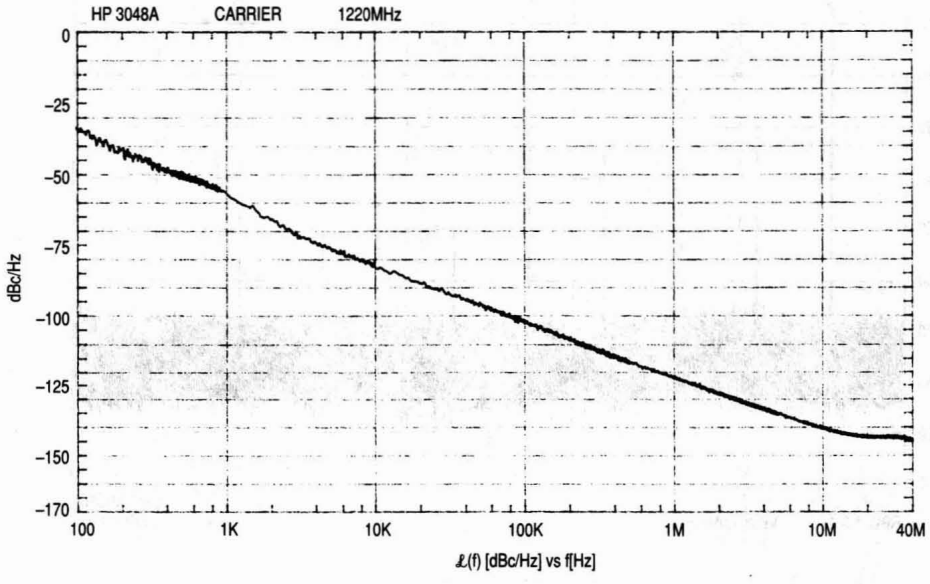


Figure 13. Typical Phase Noise Plot, 1200 MHz Tank



MOTOROLA

MC12179

500-2800 MHz Single Channel Frequency Synthesizer

500 – 2800 MHz
SINGLE CHANNEL
FREQUENCY SYNTHESIZER

SEMICONDUCTOR
TECHNICAL DATA

The MC12179 is a monolithic Bipolar synthesizer integrating the high frequency prescaler, phase/frequency detector, charge pump, and reference oscillator/buffer functions. When combined with an external loop filter and VCO, the MC12179 serves as a complete PLL subsystem. Motorola's advanced MOSAIC™ V technology is utilized for low power operation at a 5.0 V supply voltage. The device is designed for operation up to 2.8 GHz for high frequency applications such as CATV down converters and satellite receiver tuners.

- 2.8 GHz Maximum Operating Frequency
- Low Power Supply Current of 3.5 mA Typical, Including I_{CC} and I_P Currents
- Supply Voltage of 5.0 V Typical
- Integrated Divide by 256 Prescaler
- On–Chip Reference Oscillator/Buffer
  - 2.0 to 11 MHz Operation When Driven From Reference Source
  - 5.0 to 11 MHz Operation When Used With a Crystal
- Digital Phase/Frequency Detector with Linear Transfer Function
- Balanced Charge Pump Output
- Space Efficient 8–Lead SOIC
- Operating Temperature Range of –40 to 85°C

For additional information on calculating the loop filter components, an *InterActiveApNote*™ document containing software (based on a Microsoft Excel spreadsheet) and an Application Note is available. Please order DK306/D from the Motorola Literature Distribution Center.

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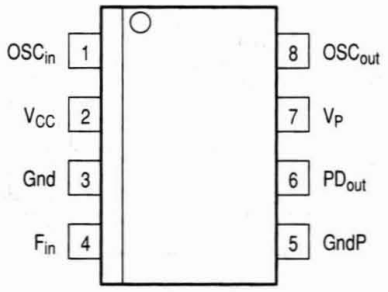
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



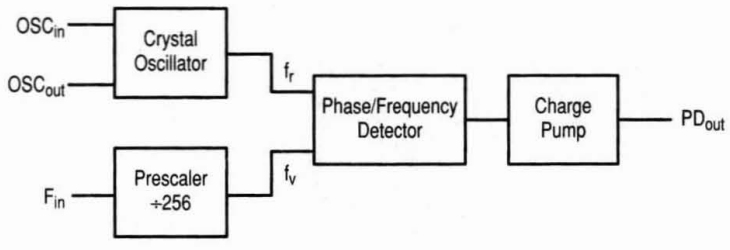
(Top View)

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 6.0	Vdc
Power Supply Voltage, Pin 7	V_P	V_{CC} to 6.0	Vdc
Storage Temperature Range	Tstg	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions as identified in the Electrical Characteristics table.
2. ESD data available upon request.

Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12179D	T_A = –40° to +85°C	SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; V_P = V_{CC} to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

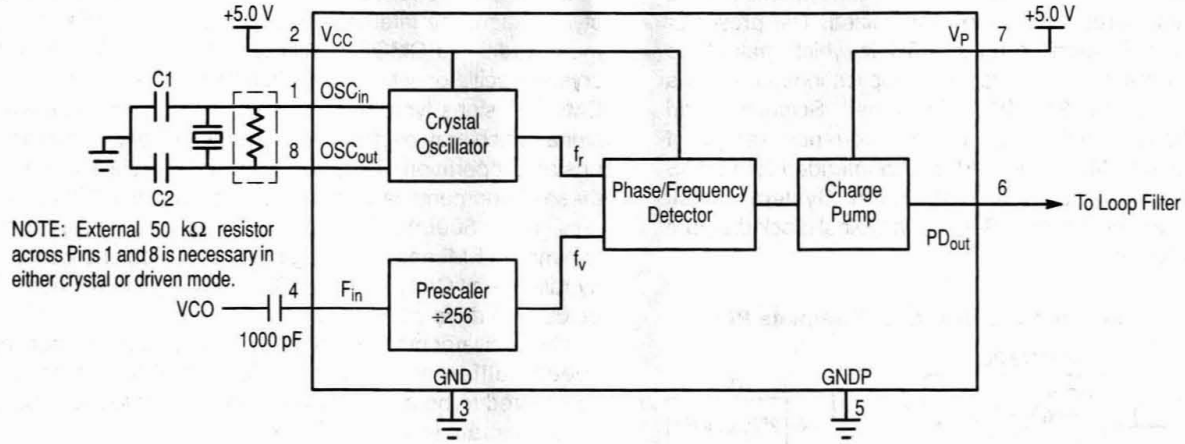
Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}	–	3.1	5.6	mA	Note 1
Supply Current for V_P	I_P	–	0.4	1.3	mA	Note 1
Operating Frequency f_{IN}max f_{IN}min	F_{IN}	2800 –	– –	– 500	MHz	Note 2
Operating Frequency Crystal Mode External Oscillator OSC_{in}	F_{OSC}	5 2	– –	11 11	MHz	Note 3 Note 4
Input Sensitivity F_{in}	V_{IN}	200	–	1000	mV_{P-P}	Note 2
Input Sensitivity External Oscillator OSC_{in}	V_{OSC}	500	–	2200	mV_{P-P}	Note 4
Output Source Current[5] (PD_{out})	I_{OH}	–2.8	–2.2	–1.6	mA	V_P = 4.5 V, V_{PDout} = V_P/2
Output Sink Current[5] (PD_{out})	I_{OL}	1.6	2.2	2.8	mA	V_P = 4.5 V, V_{PDout} = V_P/2
Output Leakage Current (PD_{out})	I_{OZ}	–	0.5	15	nA	V_P = 5.0 V, V_{PDout} = V_P/2

NOTES: 1. V_{CC} and V_P = 5.5 V; F_{IN} = 2.56 GHz; F_{OSC} = 10 MHz crystal; PD_{out} open.
2. AC coupling, F_{IN} measured with a 1000 pF capacitor.
3. Assumes C_1 and C_2 (Figure 1) limited to ≤30 pF each including stray and parasitic capacitances.
4. AC coupling to OSC_{in}.
5. Refer to Figure 15 and Figure 16 for typical performance curves over temperature and power supply voltage.

PIN FUNCTION DESCRIPTION

Pin	Symbol	I/O	Function
1	OSCin	I	Oscillator Input — An external parallel–resonant, fundamental crystal is connected between OSC_{in} and OSC_{out} to form an internal reference oscillator (crystal mode). External capacitors C1 and C2, as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. For an external reference oscillator, an external signal is AC–coupled to the OSC_{in} pin with a 1000 pF coupling capacitor, with no connection to OSC_{out}. In either mode, a resistor with a nominal value of 50 kΩ MUST be placed across the OSC_{in} and OSC_{out} pins for proper operation.
2	V_{CC}	—	Positive Power Supply. Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.
3	Gnd	—	Ground.
4	F_{in}	I	Prescaler Input — The VCO signal is AC coupled into the F_{in} pin.
5	GndP	—	Ground — For charge pump circuitry.
6	PD_{out}	O	Single ended phase/frequency detector output (charge pump output). Three–state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.
7	V_P	—	Positive power supply for charge pump. V_P MUST be equal or greater than V_{CC}. Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.
8	OSCout	O	Oscillator output, for use with an external crystal as shown in Figure 1.

Figure 1. MC12179 Expanded Block Diagram



PHASE CHARACTERISTICS

The phase comparator in the MC12179 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (f_v) signal and the reference (f_r) input. The detector can cover a range of $\pm 2\pi$ radian of f_v/f_r phase difference. The operation of the charge pump output is shown in Figure 2.

fr lags fv in phase OR fv>fr in frequency

When the phase of f_r lags that of fv or the frequency of f_v is greater than f_r, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

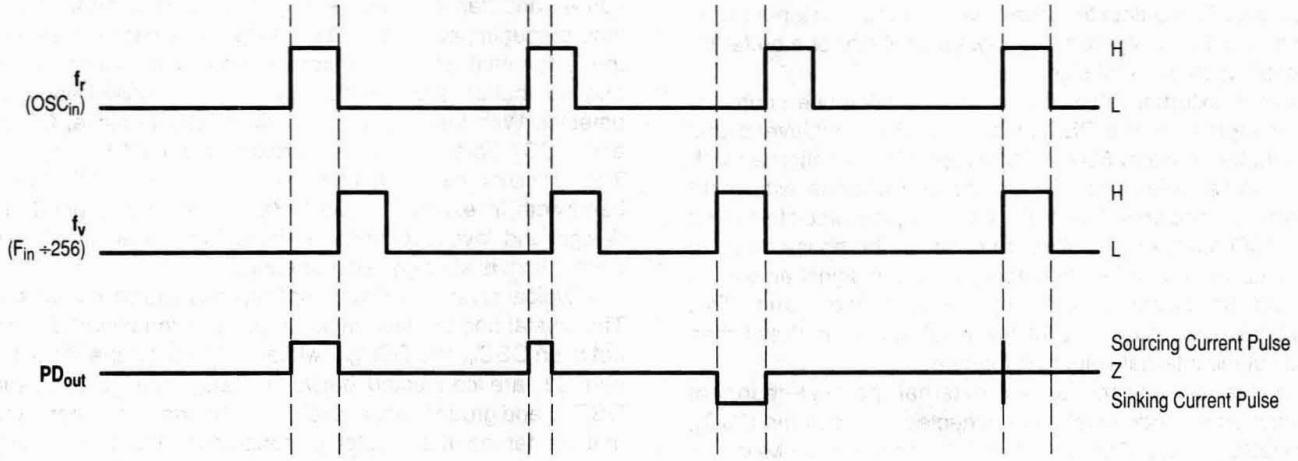
fr leads fv in phase OR fv<fr in frequency

When the phase of f_r leads that of fv or the frequency of f_v is less than f_r, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

$f_r = f_v$ in phase and frequency

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

Figure 2. Phase/Frequency Detector and Charge Pump Waveforms



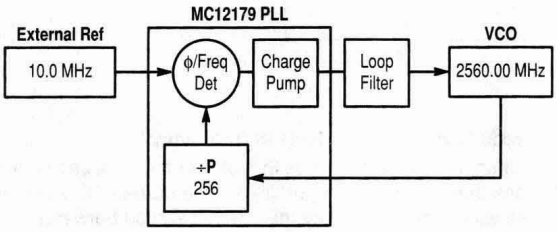
H = High voltage level; L = Low voltage level; Z = High impedance
NOTES: Phase difference detection range: ~ -2π to 2π

$$K_p\text{–Charge Pump Gain} \approx \frac{|I_{source}| + |I_{sink}|}{4\pi} = \frac{|2.2| + |-2.2|}{4\pi} = \frac{1.1\ \text{mA}}{\pi\text{radian}}$$

APPLICATIONS INFORMATION

The MC12179 is intended for applications where a fixed local oscillator is required to be synthesized. The prescaler on the MC12179 operates up to 2.8GHz which makes the part ideal for many satellite receiver applications as well as applications in the 2nd ISM (Industrial, Scientific, and Medical) band which covers the frequency range of 2400MHz to 2483MHz. The part is also intended for MMDS (Multi–channel Multi–point Distribution System) block downconverter applications. Below is a typical block diagram of the complete PLL.

Figure 3. Typical Block Diagram of Complete PLL



As can be seen from the block diagram, with the addition of a VCO, a loop filter, and either an external oscillator or crystal, a complete PLL sub–system can be realized. Since most of the PLL function is integrated into the MC12179, the user's primary focus is on the loop filter design and the crystal reference circuit. Figure 13 and Figure 14 illustrate typical VCO spectrum and phase noise characteristics. Figure 17 and Figure 18 illustrate the typical input impedance versus frequency for the prescaler input.

Crystal Oscillator Design

The MC12179 is used as a multiply–by–256 PLL circuit which transfers the high stability characteristic of a low frequency reference source to the high frequency VCO in the PLL loop. To facilitate this, the device contains an input circuit which can be configured as a crystal oscillator or a buffer for accepting an external signal source.

In the external reference mode, the reference source is AC–coupled into the OSC_{in} input pin. The input level signal should be between 500–2200 mVpp. When configured with an external reference, the device can operate with input frequencies down to 2MHz, thus allowing the circuit to control the VCO down to 512 MHz. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the input signal as it switches against the internal voltage reference.

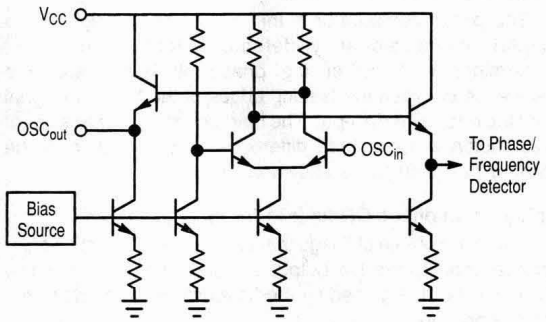
In the crystal mode, an external parallel–resonant fundamental mode crystal is connected between the OSC_{in} and OSC_{out} pins. This crystal must be between 5.0 MHz and 11 MHz. External capacitors, C1 and C2 as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen and the input capacitance of the device and any stray board capacitance.

In either mode, a 50kΩ resistor must be connected between the OSC_{in} and the OSC_{out} pins for proper device operation. The value of this resistor is not critical so a 47kΩ or 51kΩ ±10% resistor is acceptable.

Since the MC12179 is realized with an all–bipolar ECL style design, the internal oscillator circuitry is different from more traditional CMOS oscillator designs which realize the crystal oscillator with a modified inverter topology. These CMOS designs typically excite the crystal with a rail–to–rail signal which may overdrive the crystal resulting in damage or unstable operation. The MC12179 design does not exhibit these phenomena because the swing out of the OSC_{out} pin is less than 600mV. This has the added advantage of minimizing EMI and switching noise which can be generated by rail–to–rail CMOS outputs. The OSC_{out} output should not be used to drive other circuitry.

The oscillator buffer in the MC12179 is a single stage, high speed, differential input/output amplifier; it may be considered to be a form of the Pierce oscillator. A simplified circuit diagram is seen in Figure 4.

Figure 4. Simplified Crystal Oscillator/Buffer Circuit



OSC_{in} drives the base of one input of an NPN transistor differential pair. The non–inverting input of the differential pair is internally biased. OSC_{out} is the inverted input signal and is buffered by an emitter follower with a 70 μA pull–down current and has a voltage swing of about 600 mVpp. Open loop output impedance is about 425Ω. The opposite side of the differential amplifier output is used internally to drive another buffer stage which drives the phase/frequency detector. With the 50 kΩ feedback resistor in place, OSC_{in} and OSC_{out} are biased to approximately 1.1V below V_{CC}. The amplifier has a voltage gain of about 15 dB and a bandwidth in excess of 150 MHz. Adherence to good RF design and layout techniques, including power supply pin decoupling, is strongly recommended.

A typical crystal oscillator application is shown in Figure 1. The crystal and the feedback resistor are connected directly between OSC_{in} and OSC_{out}, while the loading capacitors, C1 and C2, are connected between OSC_{in} and ground, and OSC_{out} and ground respectively. It is important to understand that as far as the crystal is concerned, the two loading capacitors are in series (albeit through ground). So when the crystal specification defines a specific loading capacitance, this refers to the total external (to the crystal) capacitance seen across its two pins.

This capacitance consists of the capacitance contributed by the amplifier (IC and packaging), layout capacitance, and the series combination of the two loading capacitors. This is illustrated in the equation below:

$$C_I = C_{AMP} + C_{STRAY} + \frac{C1 \times C2}{C1 + C2}$$

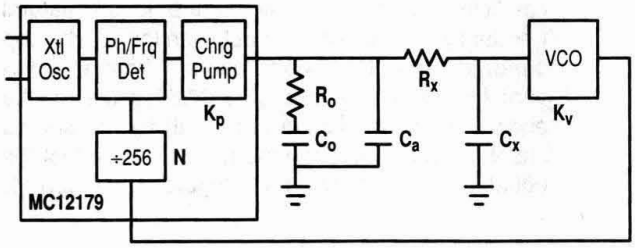
Provided the crystal and associated components are located immediately next to the IC, thus minimizing the stray capacitance, the combined value of C_{AMP} and C_{STRAY} is approximately 5pF. Note that the location of the OSC_{in} and OSC_{out} pins at the end of the package, facilitates placing the crystal, resistor and the C1 and C2 capacitors very close to the device. Usually, one of the capacitors is in parallel with an adjustable capacitor used to trim the frequency of oscillation. It is important that the total external (to the IC) capacitance seen by either OSC_{in} or OSC_{out}, be no greater than 30pF.

In operation, the crystal oscillator will start up with the application of power. If the crystal is in a can that is not grounded it is often possible to monitor the frequency of oscillation by connecting an oscilloscope probe to the can; this technique minimizes any disturbance to the circuit. If a malfunction is indicated, a high impedance, low capacitance, FET probe may be connected to either OSC_{in} or OSC_{out}. Signals typically seen at those points will be very nearly sinusoidal with amplitudes of roughly 300 to 600 mVpp. Some distortion is inevitable and has little bearing on the accuracy of the signal going to the phase detector.

Loop Filter Design

Because the device is designed for a non–frequency agile synthesizer (i.e., how fast it tunes is not critical) the loop filter design is very straight forward. The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated below in Figure 5.

Figure 5. Loop Filter



The R_o/C_o components realize the primary loop filter. C_a is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R_x/C_x realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a 4th order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a 2nd order loop (R_o/C_o) and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools can be used.

Component	Guideline
C_a	$<0.1 \times C_o$
R_x	$>10 \times R_o$
C_x	$<0.1 \times C_o$

The focus of the design effort is to determine what the loop's natural frequency, ω_o, should be. This is determined by R_o, C_o, K_p, K_v, and N. Because K_p, K_v, and N are given, it is only necessary to calculate values for R_o and C_o. There are 3 considerations in selecting the loop bandwidth:

1) Maximum loop bandwidth for minimum tuning speed
2) Optimum loop bandwidth for best phase noise performance
3) Minimum loop bandwidth for greatest reference sideband suppression

Usually a compromise is struck between these 3 cases, however, for the fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are 3 major sources of phase noise in the phase–locked loop – the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution equal to the total divide–by–N ratio. This is mathematically described in Figure 10. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. This is described in Figure 11. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15 dB has been selected, which corresponds to data in Figure 14.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturer. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the Crystal Reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 6.

The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. In the example of Figure 6, the optimum bandwidth is approximately 15 KHz.

Figure 6. Graphical Analysis of Optimum Bandwidth

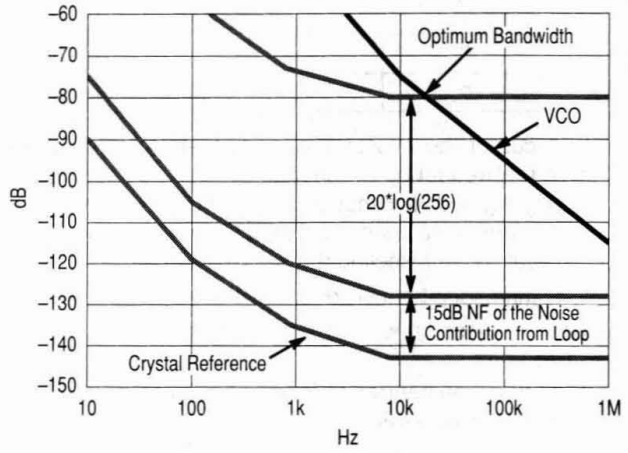
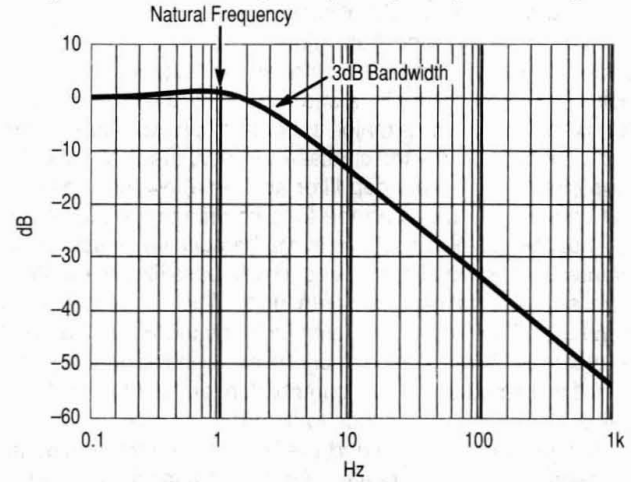


Figure 7. Closed Loop Frequency Response for $\zeta = 1$



To simplify analysis further a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 7 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore the optimum loop bandwidth is 15kHz/2.5 or 6kHz (37.7krads) with a damping coefficient, $\zeta \approx 1$. T(s) is the transfer function of the loop filter.

Figure 8. Design Equations for the 2nd Order System

$$T(s) = \frac{R_oC_os + 1}{\left(\frac{NC_o}{K_pK_v}\right)s^2 + R_oC_os + 1} = \frac{\left(\frac{2\zeta}{\omega_o}\right)s + 1}{\left(\frac{1}{\omega_o{}^2}\right)s^2 + \left(\frac{2\zeta}{\omega_o}\right)s + 1}$$

$$\left(\frac{NC_o}{K_pK_v}\right) = \left(\frac{1}{\omega_o{}^2}\right) \rightarrow \omega_o = \sqrt{\frac{K_pK_v}{NC_o}} \rightarrow \boxed{C_o \approx \left(\frac{K_pK_v}{N\omega_o{}^2}\right)}$$

$$R_oC_o = \left(\frac{2\zeta}{\omega_o}\right) \rightarrow \zeta = \left(\frac{\omega_oR_oC_o}{2}\right) \rightarrow \boxed{R_o = \left(\frac{2\zeta}{\omega_oC_o}\right)}$$

In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 256 – 48 dB) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 6.

Step 5: Correlate this loop bandwidth to the loop natural frequency and select components per Figure 8. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined above in a math tool or spread sheet is useful. To aid in the use of such a tool the equations are summarized in Figures 9 through 11.

Figure 9. Loop Parameter Relations

Let: $\frac{NC_o}{K_pK_v} = \frac{1}{\omega_o{}^2}$, $R_oC_o = \frac{2\zeta}{\omega_o}$

Let: $C_a = aC_o$, $C_x = bC_o$, $A = 1 + a$, and $B = 1 + a + b$

Let: $R_oC_o = \frac{1}{\omega_3}$, $R_xC_x = \frac{1}{\omega_4}$, $R_o(C_a + C_x) = \frac{1}{\omega_5}$

Let: $K_3\omega_3 = \omega_o$, $K_4\omega_4 = \omega_o$, $K_5\omega_5 = \omega_o$

Figure 10. Transfer Function for the Crystal Noise in the Frequency Plane

$$T(j\omega) = N \cdot \frac{1 + j\left(2\zeta\frac{\omega}{\omega_o}\right)}{\left(1 + K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) + j\left(2\zeta\frac{\omega}{\omega_o} - (AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}$$

Figure 11. Transfer Function for the VCO Noise in the Frequency Plane

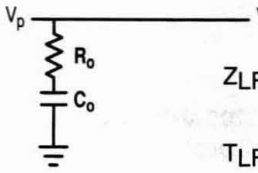
$$T(j\omega) = \frac{\left(K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) - j\left((AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}{\left(1 + K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) + j\left(2\zeta\frac{\omega}{\omega_o} - (AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}$$

Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps. Step 1 is to find the voltage generated by the impedance of the loop filter. Step 2 is to find the transfer function from the input of the loop filter to its output. The "voltage" times the "transfer function" is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL multiply the filter's impedance by the gain constant of the phase detector then multiply that by the filter's transfer function (which is unity in the 2nd and 3rd order cases below).

Figure 12. Overall Transfer Function of the PLL

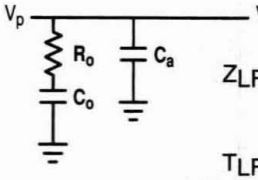
For the 2nd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_os}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

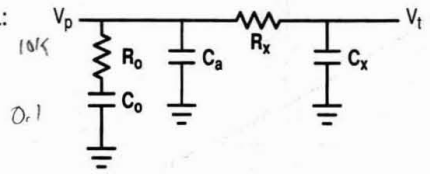
For the 3rd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_oR_oC_as^2 + (C_o + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

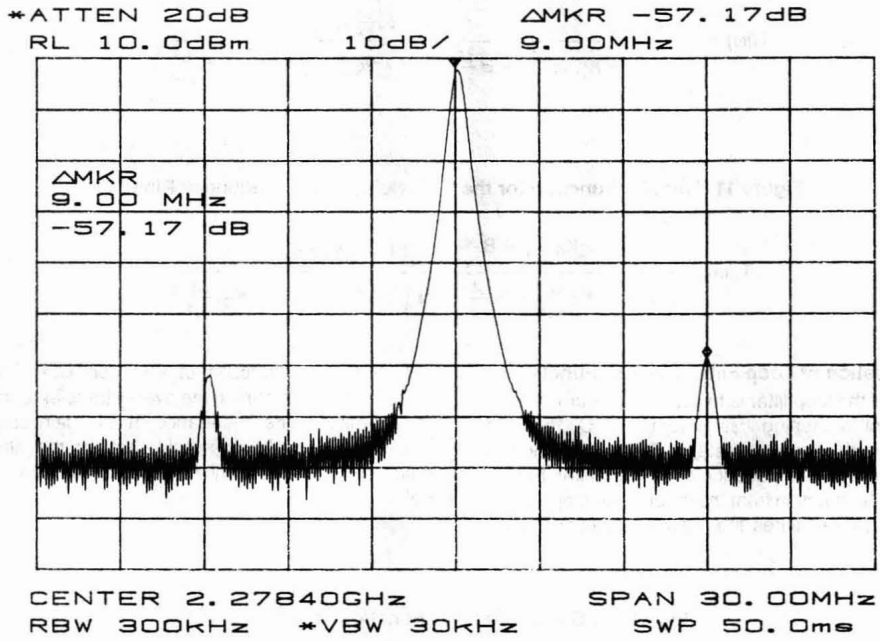
For the 4th Order PLL:



$$Z_{LF}(s) = \frac{(R_oC_os + 1)\ (R_xC_xs + 1)}{C_oR_oC_aR_xC_xs^3 + [\ (C_o + C_a)R_xC_x + C_oR_o(C_x + C_a)\ ]\ s^2 + (C_o + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)}\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

Figure 13. VCO Output Spectrum with MC12179, V_{CC} = 5.0 V
(ECLiPTEK 8.9 MHz Crystal and ZCOM 2500 VCO)



NOTE: Spurs can be reduced further by narrowing the loop bandwidth of the PLL loop filter and/or adding an extra filter (R_x/C_x)

Figure 14. Typical Phase Noise Plot, 2200 MHz VCO
(With the MC12179 in a Closed Loop)

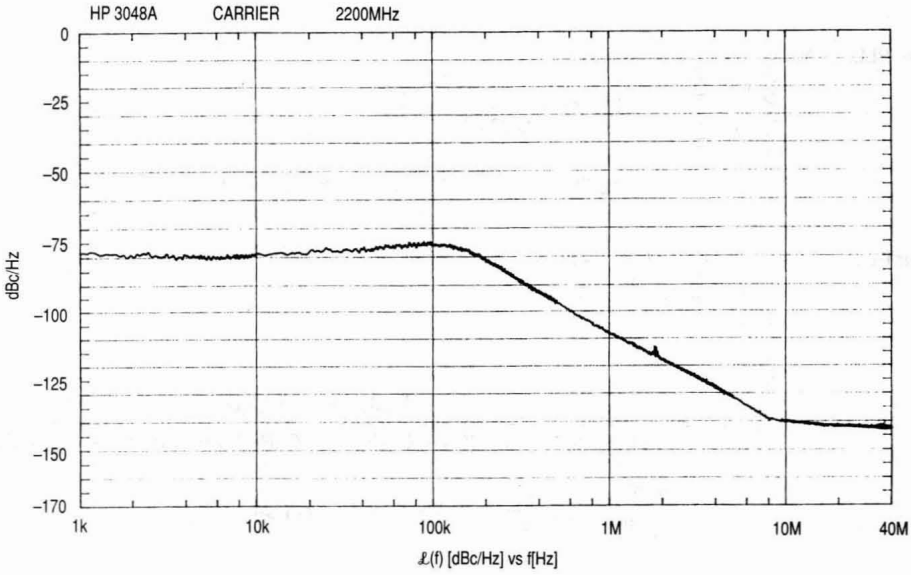


Figure 15. Typical Charge Pump Current versus Temperature
(V_{CC} = V_{pp} = 5.0 V)

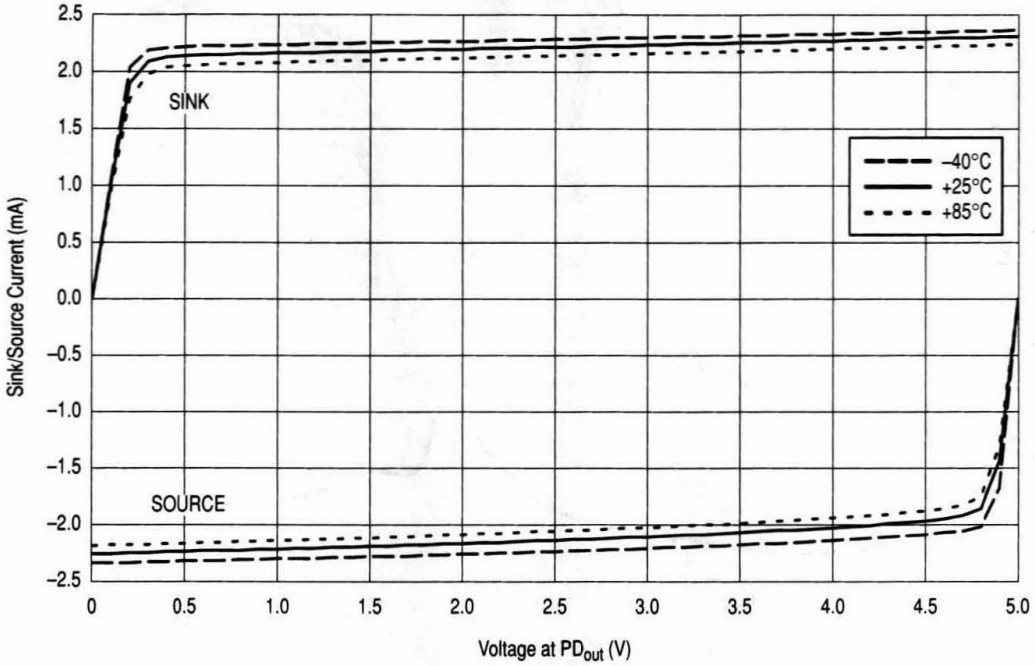


Figure 16. Typical Charge Pump Current versus Voltage
(T = 25°C)

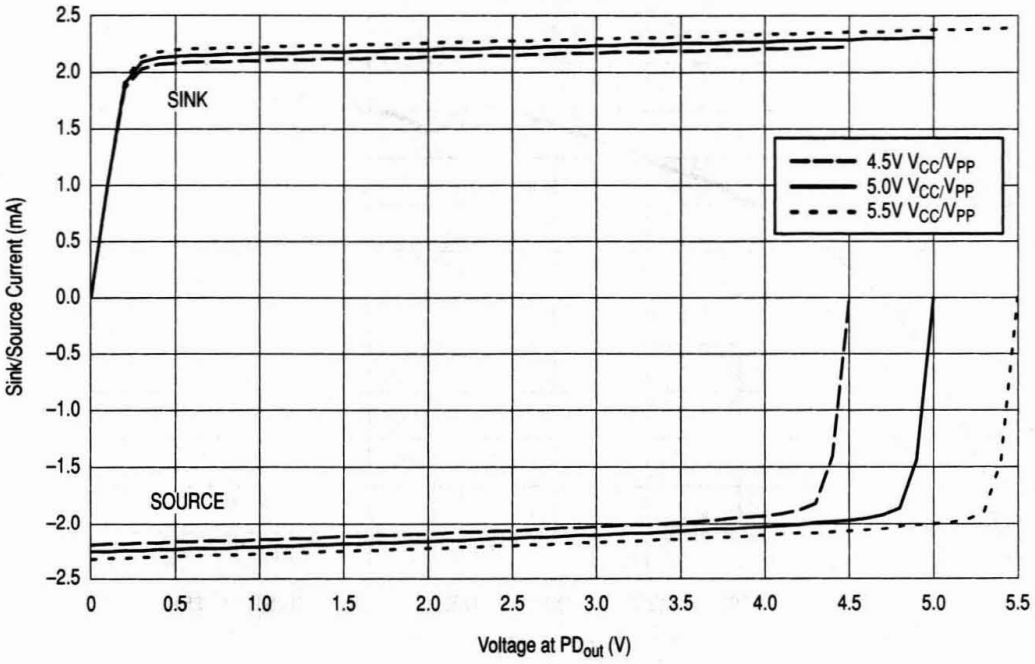


Figure 17. Typical Real Input Impedance versus Input Frequency
(For the F_{in} Input)

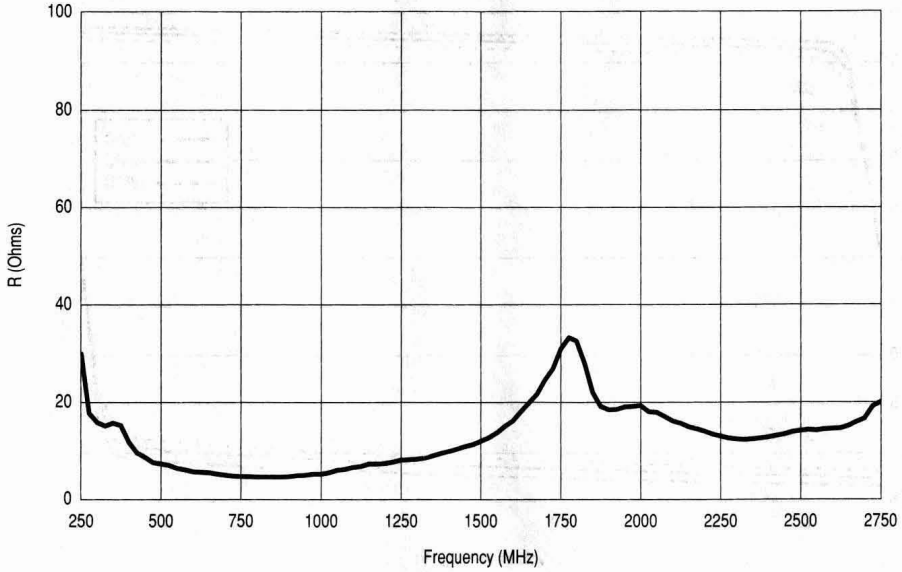
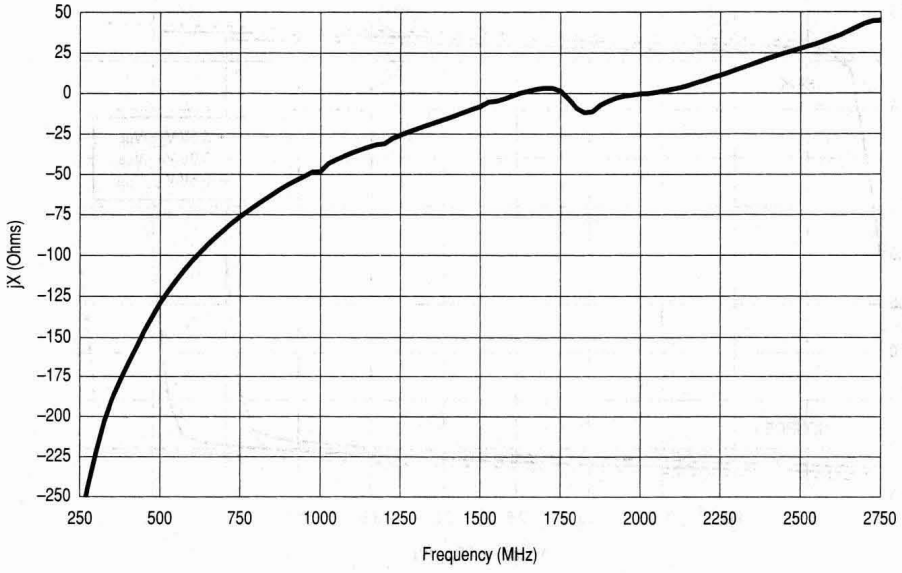


Figure 18. Typical Imaginary Input Impedance versus Input Frequency
(For the F_{in} Input)



MOTOROLA

MC12181

125-1000 MHz Frequency Synthesizer

The MC12181 is a monolithic bipolar synthesizer integrating a high performance prescaler, programmable divider, phase/frequency detector, charge pump, and reference oscillator/buffer functions. The device is capable of synthesizing a signal which is 25 to 40 times the input reference signal. The device has a 4–bit parallel interface to set the proper total multiplication which can range from 25 to 40. When combined with an external passive loop filter and VCO, the MC12181 serves as a complete PLL subsystem.

- 2.7 to 5.5 V Operation
- Low power supply current of 4.25 mA typical
- On chip reference oscillator/buffer supporting wide frequency operating range from 5 to 25 MHz
- 4–bit parallel interface for programming divider (N = 25 .... 40)
- Wide 125 – 1000 MHz frequency of operation
- Digital phase/frequency detector with linear transfer function
- Balanced Charge Pump Output
- Space efficient 16 lead SOIC package
- Operating Temperature Range of –40 to 85°C
- > 1000 V ESD Protection (I/O to Ground, I/O to V_{CC})

The device is suitable for applications where a fixed local oscillator (LO) needs to be synthesized or where a limited number of LO frequencies need to be generated. The device also has auxiliary open emitter outputs (Pout and Rout) for observing the inputs to the phase detector for verification purposes. In normal use the pins should be left open. The Reset input is normally LOW. When this input is placed in the HIGH state the reference prescaler is reset and the charge pump output (Do) is placed in the OFF state.

The 4–bit programming interface maps into divider states ranging from 25 to 40. A is the LSB and D is the MSB. The data inputs (A,B,C, and D) are CMOS compatible and have pull–up resistors. The inputs can be tied directly to Vcc or Ground for programming or can be interfaced to an external data latch/register. Table 1 below has a mapping of the programming states.

Table 1. Programming States

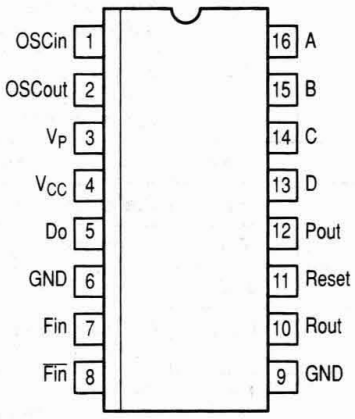
D	C	B	A	Divider
L	L	L	L	25
L	L	L	H	26
L	L	H	L	27
L	L	H	H	28
L	H	L	L	29
L	H	L	H	30
L	H	H	L	31
L	H	H	H	32
H	L	L	L	33
H	L	L	H	34
H	L	H	L	35
H	L	H	H	36
H	H	L	L	37
H	H	L	H	38
H	H	H	L	39
H	H	H	H	40

125 – 1000 MHZ FREQUENCY SYNTHESIZER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS

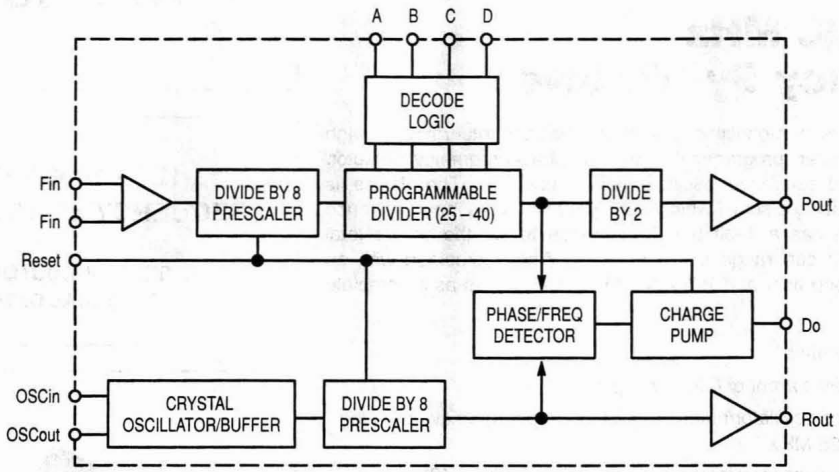


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12181D	T_A = –40° to +85°C	SO–16

Figure 1. MC12181 Programmable Synthesizer



PIN NAMES

Pin No.	Pin	Function
1	OSCin	An external parallel resonant, fundamental crystal is connected between OSCin and OSCout to form an internal reference crystal oscillator. External capacitors C1 and C2 are required to set the proper crystal load capacitance and oscillator frequency (Figure 2). For an external reference oscillator, a signal is ac–coupled into the OSCin pin. In either mode a 50 kΩ resistor MUST be connected between OSCin and OSCout.
2	OSCout	Oscillator output, for use with an external crystal as shown in Figure 2.
3	V_P	Positive power supply for charge pump. V_P MUST be greater than or equal to V_{CC}. Bypassing should be placed as close as possible to this pin and be connected directly to the ground plane.
4	V_{CC}	Positive power supply. Bypassing should be placed as close as possible to this pin and be connected directly to the ground plane.
5	Do	Single ended phase/frequency detector output. Three–state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.
6	GND	Ground. This pin should be directly tied to the ground plane.
7	Fin	Prescaler input – The VCO signal is ac–coupled into the Fin Pin.
8	Fin	Complementary prescaler input – This pin should be capacitively coupled to ground.
9	GND	Ground. This pin should be directly tied to the ground plane.
10	Rout	Open emitter test point used to verify proper operation of the reference divider chain. In normal operation this pin should be left OPEN.
11	Reset	Test pin used to clear the prescalers (Reset = H). When the Reset is in the HIGH state, the charge pump output is disabled. The Reset input has an internal pulldown. In normal operation it can be left open or tied to ground.
12	Pout	Open emitter test point used to verify proper operation of the programmable divider chain. The output is a divide–by–2 version of the programmable input to the phase/frequency detector. In normal operation this pin should be left OPEN.
13 14 15 16	D C B A	Digital control inputs for setting the value of the programmable divider. A is the LSB and D is the MSB. In normal operation these pins can be tied to V_{CC} and/or ground to program a fixed divide or they can be driven by a CMOS logic level when used in a programmable mode. There is an internal pull–up resistor to V_{CC} on each input.

Figure 2. Typical Applications Example

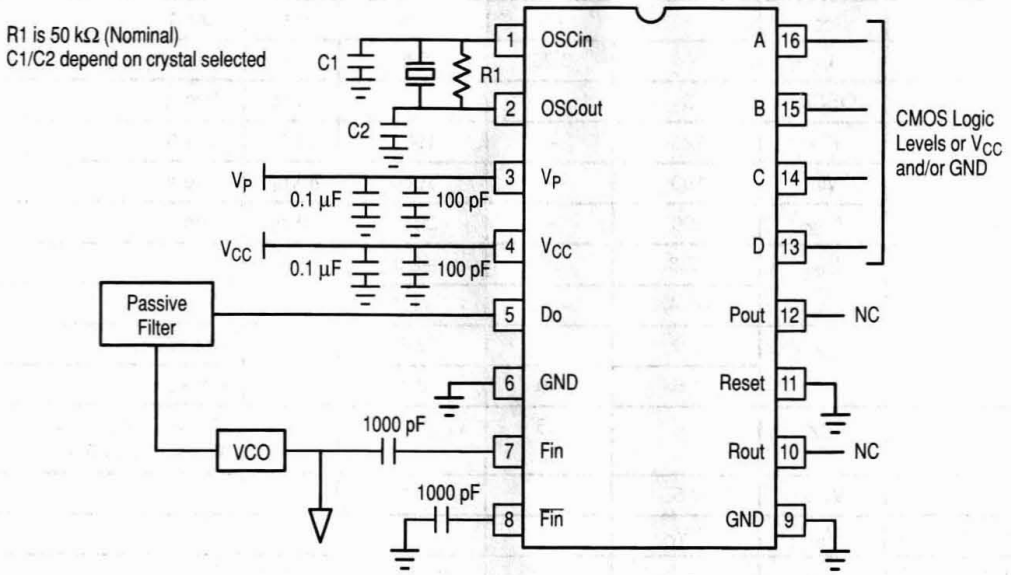
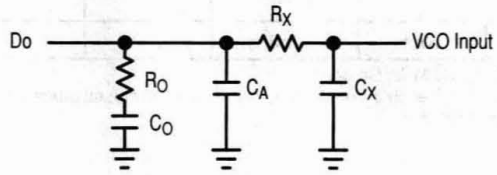


Figure 3. Typical Passive Loop Filter Topology



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Range	V_{CC}	2.7	5.5	VDC
Maximum Supply Range	V_{CC}max	–	–6.0	VDC
Maximum Charge Pump Voltage	$V_P$max	–	V_{CC} to +6.0	VDC
Temperature Ambient	T_A	–40	85	°C
Storage Temperature	T_{STG}	–65	150	°C
Maximum Input Signal (Any Pin)	V_{in}max	–	V_{CC}+0.5 V	VDC

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; V_P = V_{CC} to 6.0 V; T_A = –40 to +85°C, unless otherwise noted.)

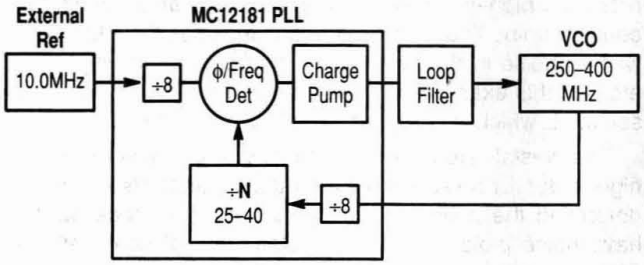
Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}	–	4.0	5.5	mA	Note 1
Supply Current for V_P	I_P	–	0.25	0.5	mA	Note 1
Input Frequency Range	OSCin	5	–	25	MHz	Note 2
RF Input Frequency Range	Fin	125	–	1000	MHz	Note 3
Fin Input Sensitivity	Vin	100	–	1000	mVpp	Note 4
OSCin Input Sensitivity	V_{OSC}	500	–	2200	mVpp	Note 4
Output Source Current (Do)	I_{OH}	–2.8	–2.2	–2.0	mA	Note 5
		–2.4	–2.0	–1.6		Note 6
Output Sink Current (Do)	I_{OL}	2.0	2.4	2.8	mA	Note 5
		1.6	2.0	2.4		Note 6
Output Leakage Current (Do)	I_{OZ}	–	0.5	10	nA	V_{CC}=5.5; V_P = 6.0 V; VDo=0.5 to 5.5 V
Charge Pump Operating Volt	VDo	0.5	–	V_P–0.5	V	
Input HIGH Voltage Reset, A, B, C, D	V_{IH}	0.7 V_{CC}	–	–	V	
Input LOW Voltage Reset, A, B, C, D	V_{IL}	–	–	0.3 V_{CC}	V	
Input HIGH Current A, B, C, D	I_{IH}	–	–	+1	µA	
Reset		–	–	+100		
Input LOW Current A, B, C, D	I_{IL}	–100	–	–	µA	
Reset		–1	–	+1		
Output Amplitude (Pout, Rout)	Vout	250	400	–	mVpp	Note 7

NOTES: 1. V_{CC} and V_P = 5.5 V; Fin = 1.0 GHz; OSCin = 25 MHz; Do open.
2. Assumes C_1 and C_2 (Figure 2) limited to ≤30 pF each including stray capacitance in crystal mode, ac coupled input for external reference mode.
3. AC coupling, Fin measured with a 1000pF capacitor.
4. Signal ac coupling in input.
5. V_{CC} = 5.5 V; V_P = 6.0 V; V_{DO} = 3.0 V.
6. V_P = V_{CC} = 3.0 V; V_{DO} = 1.5 V.
7. Minimum resistor value of 25 kΩ to ground.

APPLICATIONS INFORMATION

The MC12181 is intended for applications where a fixed LO, or a limited number of local oscillator frequencies is required to be synthesized. The device acts as a x25 – 40 PLL. The 4–bit parallel interface allows 1 of 16 divide ratios to be selected. Internally there are fixed divide by 8 prescalers in the reference and programmable paths of the PLL. The MC12181 operates from 125 MHz to 1000 MHz which makes the part ideal for FCC Title 47; Part 15 applications in the 260 MHz to 470 MHz band and the 902 to 928 MHz Band. Figure 4 shows a typical block diagram of the application.

Figure 4. Typical Block Diagram of Complete PLL



As can be seen from the block diagram, with the addition of a VCO, a loop filter, and either an external oscillator or crystal, a complete PLL sub–system can be realized. Since most of the PLL functions are integrated into the 12181, the users focus is on the loop filter design and the crystal reference oscillator circuit.

Crystal Oscillator Design

The PLL is used to transfer the high stability characteristic of a low frequency reference source to the high frequency VCO within the PLL loop. To facilitate this, the device contains an input circuit which can be configured as a crystal oscillator or a buffer for accepting an external signal source.

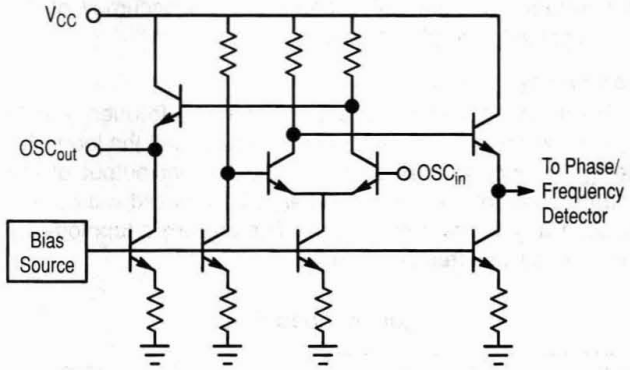
In the external reference mode, the reference source is ac–coupling into the OSCin input pin. The level of this signal should be between 500 – 2200 mVp–p. An external low noise reference should be used when it is desired to obtain the best close–in phase noise performance for the PLL. In addition the input reference amplitude should be close to the upper amplitude specification. This maximizes the slew rate of the input signal as it switches against the internal voltage reference.

In the crystal mode, an external parallel–resonant fundamental mode crystal should be connected between the OSCin and OSCout pins. This crystal must be between 5 and 25 MHz. External capacitors C1 and C2, as shown in Figure 2, are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal choosen and the input capacitance of the device as well as stray board capacitance.

Since the MC12181 is realized with an all–bipolar ECL style design, the internal oscillator circuitry is different from more traditional CMOS oscillator designs which realize the crystal oscillator with a modified inverter topology. These CMOS designs typically excite the crystal with a rail–to–rail signal which may overdrive the crystal resulting in damage or unstable operation. The MC12181 design does not exhibit this phenomena because the swing out of the OSCout pin is less than 600 mVp–p. This has the added advantage of minimizing EMI and switching noise which can be generated by rail–to–rail CMOS outputs. The OSCout output should not be used to drive other circuitry.

The oscillator buffer in the MC12181 is a single stage, high speed, differential input/output amplifier; it may be considered to be a form of the Pierce oscillator. A simplified circuit diagram is seen in Figure 5.

Figure 5. Simplified Crystal Oscillator/Buffer Circuit



OSC_{in} drives the base of one input of an NPN transistor differential pair. The non–inverting input of the differential pair is internally biased. OSC_{out} is the inverted input signal and is buffered by an emitter follower with a 70 μA pull–down current and has a voltage swing of about 600mVp–p. Open loop output impedance is approximately 425 Ω. The opposite side of the differential amplifier output is used internally to drive another buffer stage which drives the phase/frequency detector. With the 50 kΩ feedback resistor in place, OSC_{in} and OSC_{out} are biased to approximately 1.1 V below V_{CC}. The amplifier has a voltage gain of about 15dB and a bandwidth in excess of 150 MHz. Adherence to good RF design and layout techniques, including power supply pin decoupling, is strongly recommended.

A typical crystal oscillator application is shown in Figure 2. The crystal and the feedback resistor are connected directly between OSC_{in} and OSC_{out}, while the loading capacitors, C1 and C2, are connected between OSC_{in} and ground, and OSC_{out} and ground respectively. It is important to understand that as far as the crystal is concerned, the two loading capacitors are in series (albeit through ground). So when the crystal specification defines a specific loading capacitance, this refers to the total external (to the crystal) capacitance seen across its two pins.

This capacitance consists of the capacitance contributed by the amplifier (IC and packaging), layout capacitance, and the series combination of the two loading capacitors. This is illustrated in the equation below:

$$C_I = C_{AMP} + C_{STRAY} + \frac{C1 \times C2}{C1 + C2}$$

Provided the crystal and associated components are located immediately next to the IC, thus minimizing the stray capacitance, the combined value of C_{AMP} and C_{STRAY} is approximately 5pF. Note that the location of the OSC_{in} and OSC_{out} pins at the end of the package, facilitates placing the crystal, resistor and the C1 and C2 capacitors very close to the device. Usually, one of the capacitors is in parallel with an adjustable capacitor used to trim the frequency of oscillation.

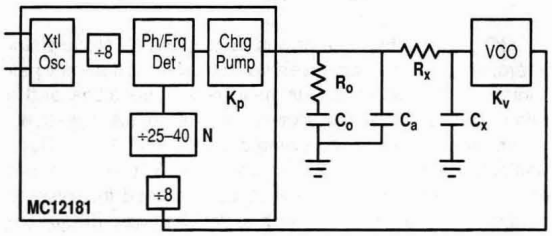
It is important that the total external (to the IC) capacitance seen by either OSC_{in} or OSC_{out}, be no greater than 30pF.

In operation, the crystal oscillator will start up with the application of power. If the crystal is in a can that is not grounded it is often possible to monitor the frequency of oscillation by connecting an oscilloscope probe to the can; this technique minimizes any disturbance to the circuit. If this is not possible, a high impedance, low capacitance, FET probe can be connected to either OSC_{in} or OSC_{out}. Signals typically seen at those points will be very nearly sinusoidal with amplitudes of roughly 300–600mVp–p. Some distortion is inevitable and has little bearing on the accuracy of the signal going to the phase detector.

Loop Filter Design

Because the device is designed for a non–frequency agile synthesizer (i.e., how fast it tunes is not critical) the loop filter design is very straight forward. The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated in Figure 6.

Figure 6. Loop Filter



The R_o/C_o components realize the primary loop filter. C_a is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R_x/C_x realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a 4th order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a 2nd order loop (R_o/C_o) and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools should be used.

Component	Guideline
C_a	$<0.1 \times C_o$
R_x	$>10 \times R_o$
C_x	$<0.1 \times C_o$

The focus of the design effort is to determine what the loop's natural frequency, ω_o, should be. This is determined by R_o, C_o, K_p, K_v, and N_t. Because K_p, K_v, and N_t are given, it is only necessary to calculate values for R_o and C_o. There are 3 considerations in selecting the loop bandwidth:

4) Maximum loop bandwidth for minimum tuning speed
5) Optimum loop bandwidth for best phase noise performance
6) Minimum loop bandwidth for greatest reference sideband suppression

Usually a compromise is struck between these 3 cases, however, for a fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are 3 major sources of phase noise in the phase–locked loop – the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15dB has been selected, which corresponds to data in Figure 17.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturers of both devices. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the Crystal Reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 7.

The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. In the example of Figure 7, the optimum bandwidth is approximately 15 KHz.

Figure 7. Graphical Analysis of Optimum Bandwidth

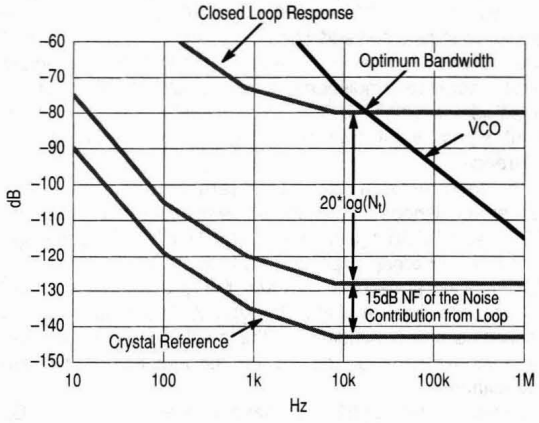
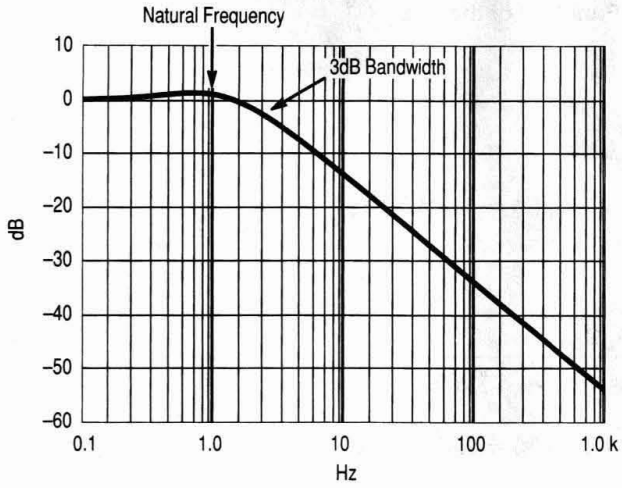


Figure 8. Closed Loop Frequency Response for ζ = 1



To simplify analysis further a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 8 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore the optimum loop bandwidth is 15 kHz/2.5 or 6.0 kHz (37.7 krads) with a damping coefficient, $\zeta \approx 1$. T(s) is the transfer function of the loop filter.

$$T(s) = \frac{R_o C_o s + 1}{\left(\frac{NC_o}{K_p K_v}\right)s^2 + R_o C_o s + 1} = \frac{\left(\frac{2\zeta}{\omega_o}\right)s + 1}{\left(\frac{1}{\omega_o^2}\right)s^2 + \left(\frac{2\zeta}{\omega_o}\right)s + 1}$$

$$\left(\frac{NC_o}{K_p K_v}\right) = \left(\frac{1}{\omega_o^2}\right) \rightarrow \omega_o = \sqrt{\frac{K_p K_v}{NC_o}} \rightarrow \boxed{C_o = \left(\frac{K_p K_v}{N\omega_o^2}\right)}$$

$$R_o C_o = \left(\frac{2\zeta}{\omega_o}\right) \rightarrow \zeta = \left(\frac{\omega_o R_o C_o}{2}\right) \rightarrow \boxed{R_o = \left(\frac{2\zeta}{\omega_o C_o}\right)}$$

where N_t = Total PLL Divide Ratio — 8×N where (N = 25...40)
K_v = VCO Gain — Hz/V
K_p = Phase Detector/Charge Pump Gain — A
= ($|I_{OH}| + |I_{OL}|$) / 2

Technically, K_v and K_p should be expressed in Radian units [K_v (RAD/V), K_p (A/RAD)]. Since the component design equation contains the $K_v \times K_p$ term. the 2π cancels and the values can be epressed as above.

Figure 9. Design Equations for the 2nd Order System

In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 8 × N) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 7.

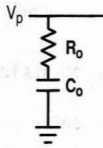
Step 5: Correlate this loop bandwidth to the loop natural frequency per Figure 8. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined in Figure 9, a math tool or spread sheet is useful to select the values for R_o and C_o.

Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps. Step 1 is to find the voltage generated by the impedance of the loop filter. Step 2 is to find the transfer function from the input of the loop filter to its output. The "voltage" times the "transfer function" is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL multiply the filter's impedance by the gain constant of the phase detector then multiply that by the filter's transfer function (Figure 10 contains the transfer function equations for 2nd, 3rd and 4th order PLL filters.)

Figure 10. Overall Transfer Function of the PLL

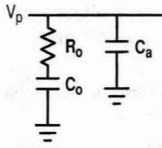
For the 2nd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_os}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \ , \ V_p(s) = K_p(s)Z_{LF}(s)$$

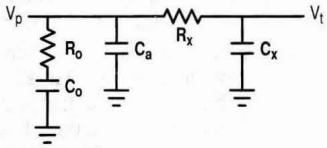
For the 3rd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_oR_oC_as^2 + (C_o + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \ , \ V_p(s) = K_p(s)Z_{LF}(s)$$

For the 4th Order PLL:



$$Z_{LF}(s) = \frac{(R_oC_os + 1)\ (R_xC_xs + 1)}{C_oR_oC_aR_xC_xs^3 + [\ (C_o + C_a)R_xC_x + C_oR_o(C_x + C_a)\ ]\ s^2 + (C_o + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)} \ , \ V_p(s) = K_p(s)Z_{LF}(s)$$

Figure 11. Typical Charge Pump Current versus Temperature
(V_{CC} = 5.5 V; V_P = 6.0 V)

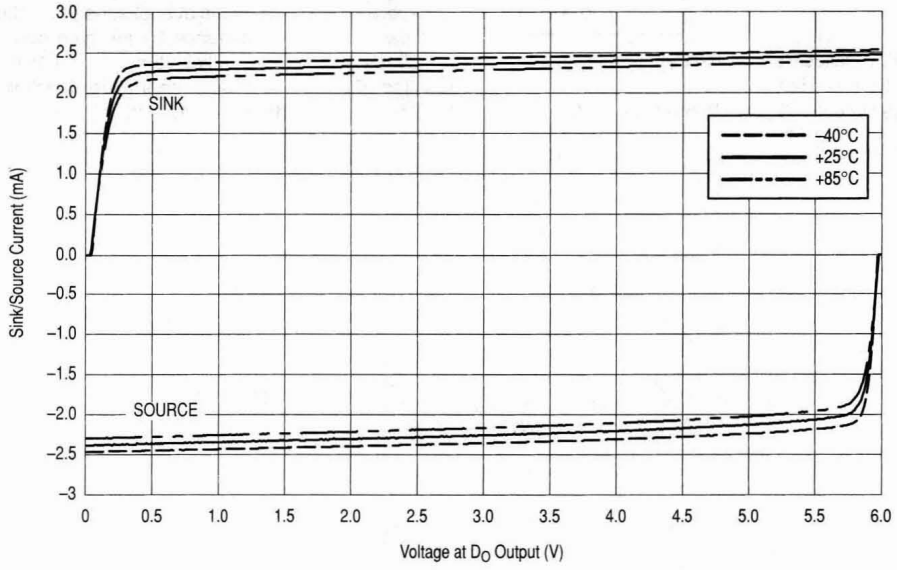


Figure 12. Typical Leakage Current at D_O Over V_{DO} Range
(V_{CC} = 5.5 V; V_P = 6.0 V; T = 25°C)

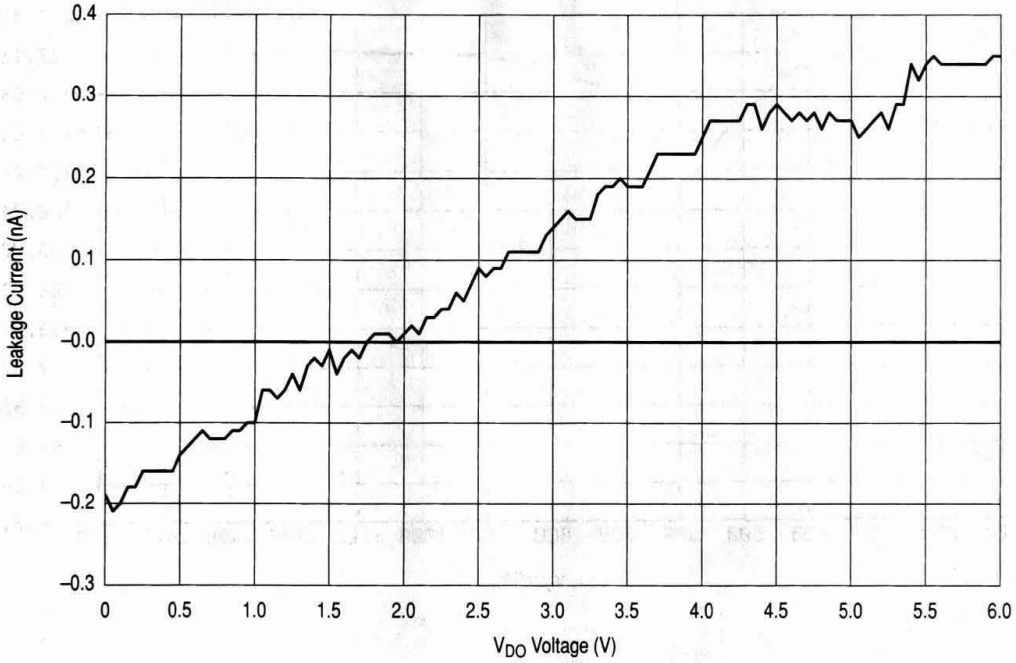


Figure 13. Typical F_{in} Input Impedance versus Input Frequency

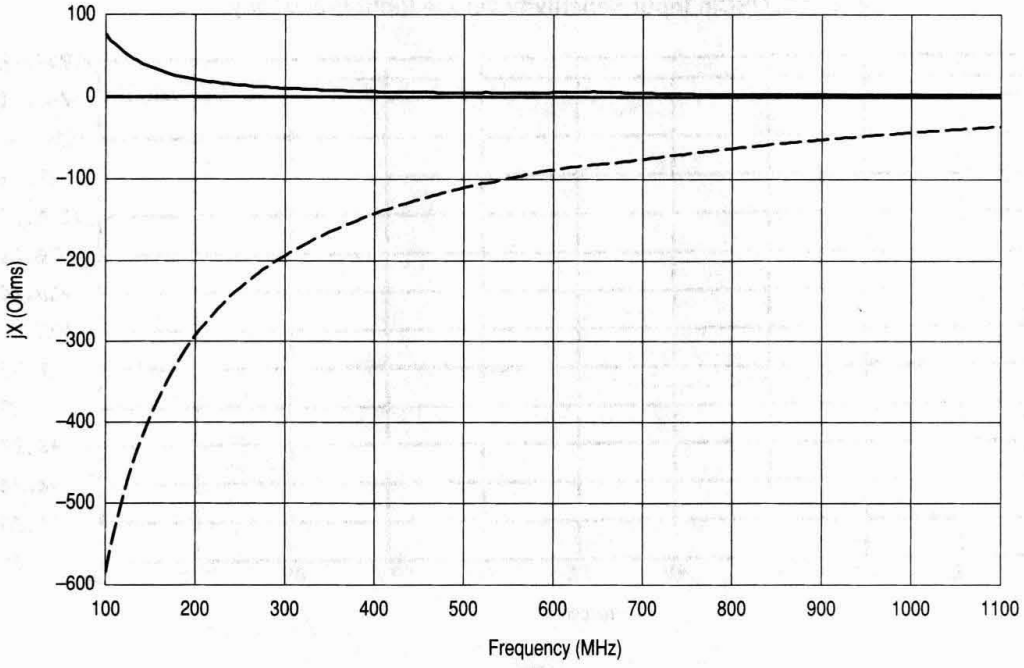


Figure 14. F_{in} Input Signal Sensitivity versus Input Frequency

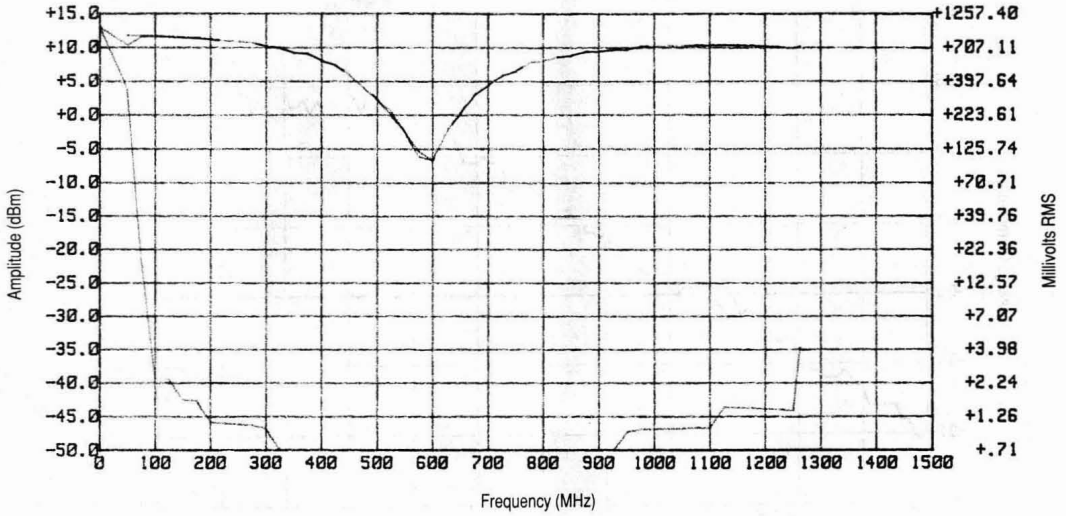


Figure 15. OSCin Input Sensitivity versus Input Frequency

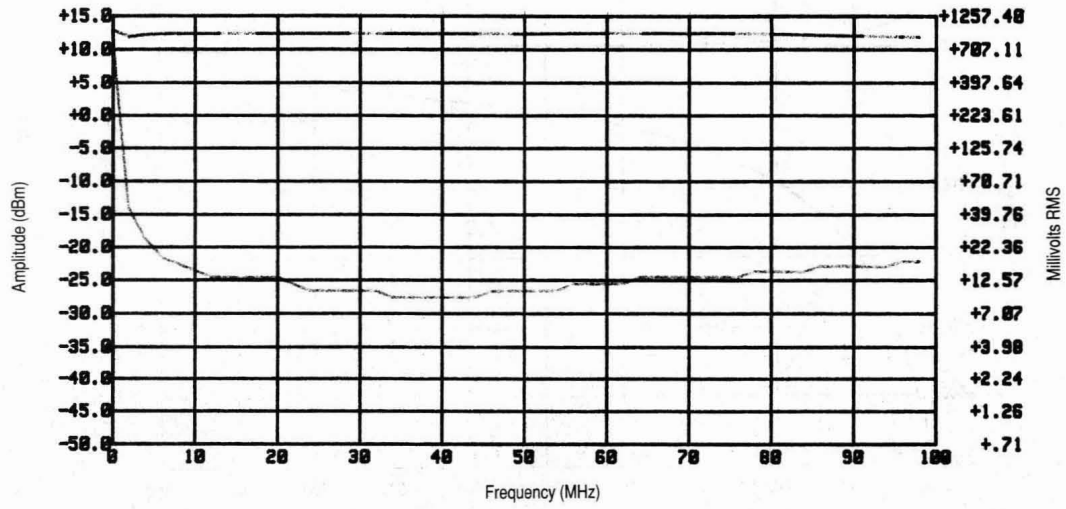


Figure 16. VCO Output Spectrum
(P=30, 8.0 MHz ECLiPTEK Crystal)

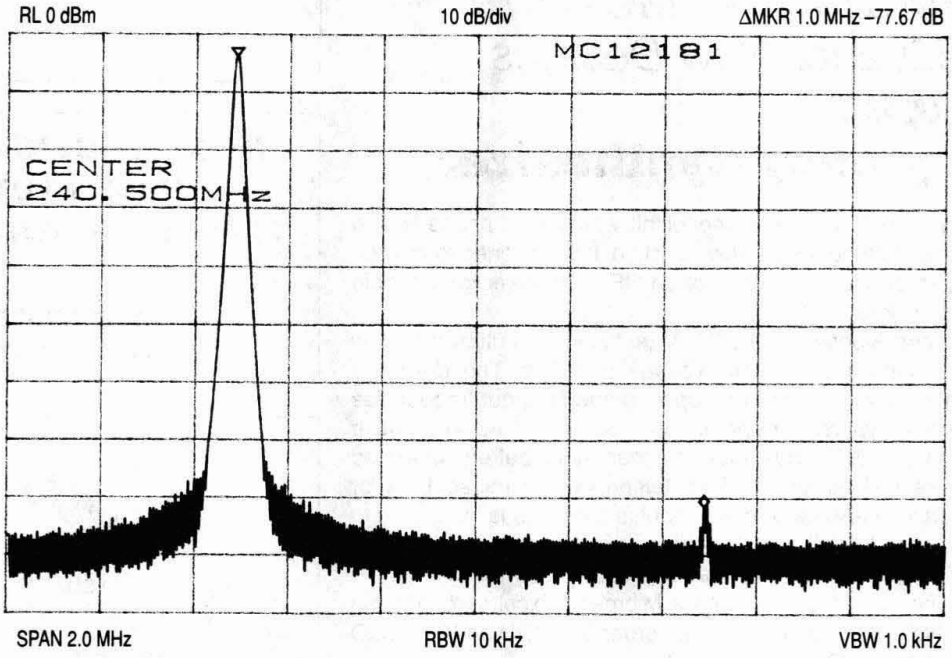
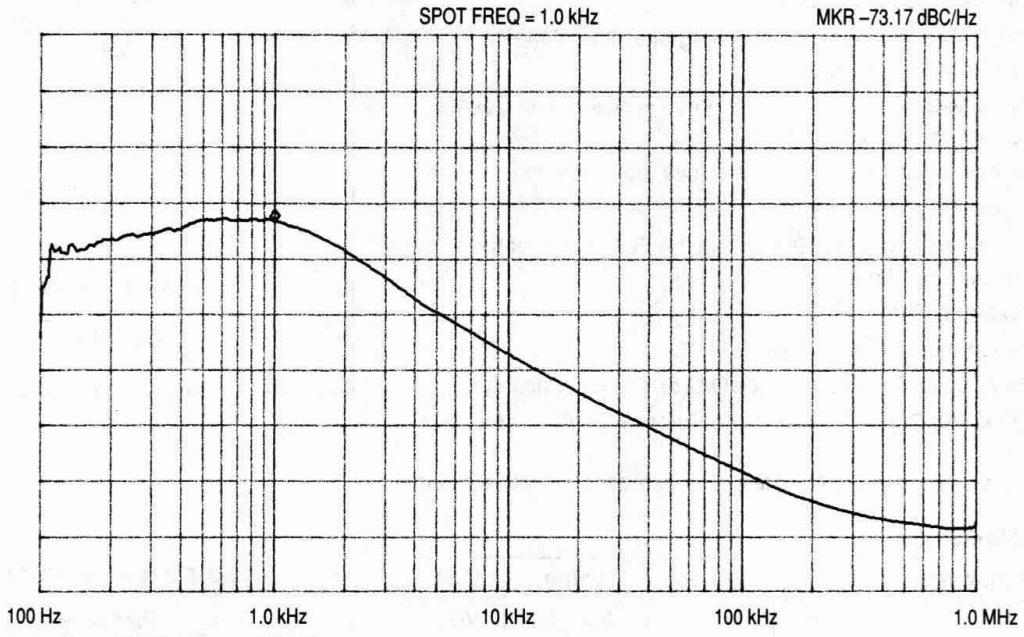


Figure 17. Typical Phase Noise Plot, 240MHz
(Low Noise 10 MHz Reference Input)



MOTOROLA

Consider MC145190, MC145191 or MC145202 for New Designs

Serial Input PLL Frequency Synthesizer

MC12202

MECL PLL COMPONENTS
SERIAL INPUT PLL
FREQUENCY SYNTHESIZER

SEMICONDUCTOR
TECHNICAL DATA

The MC12202 is a 1.1 GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse–swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

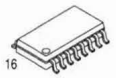
Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7 V. The device is designed for operation over 2.7 to 5.5 V supply range for input frequencies up to 1.1 GHz with a typical current drain of 6.5 mA. The low power consumption makes the MC12202 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 64/65 or 128/129 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 5.8 mA Typical for I_{CC} and 0.7 mA Typical for I_P
- Supply Voltage of 2.7 to 5.5 V
- Dual Modulus Prescaler With Selectable Divide Ratios of 64/65 or 128/129
- On–Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14–Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7–Bit Swallow Counter and an 11–Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of –40 to 85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages
- The MC12202 Is Pin Compatible With the Fujitsu MB1502 or MB1511

Not Recommended For New Designs

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



M SUFFIX
PLASTIC PACKAGE
CASE 966
(SO–16)

DT SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

MOSAIC V, Mfax and *InterActiveApNote* are trademarks of Motorola, Inc.

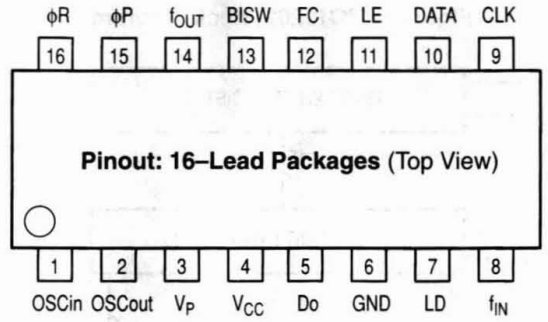
MAXIMUM RATINGS (Note 1)

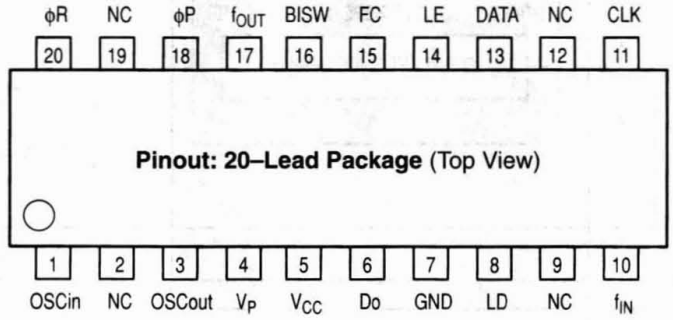
Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 4 (Pin 5 in 20–lead package)	V_{CC}	–0.5 to 6.0	VDC
Power Supply Voltage, Pin 3 (Pin 4 in 20–lead package)	V_p	V_{CC} to 6.0	VDC
Storage Temperature Range	Tstg	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12202D	$T_A = -40°$ to +85°C	SO–16
MC12022M		SO–16
MC12022DT		TSSOP–20

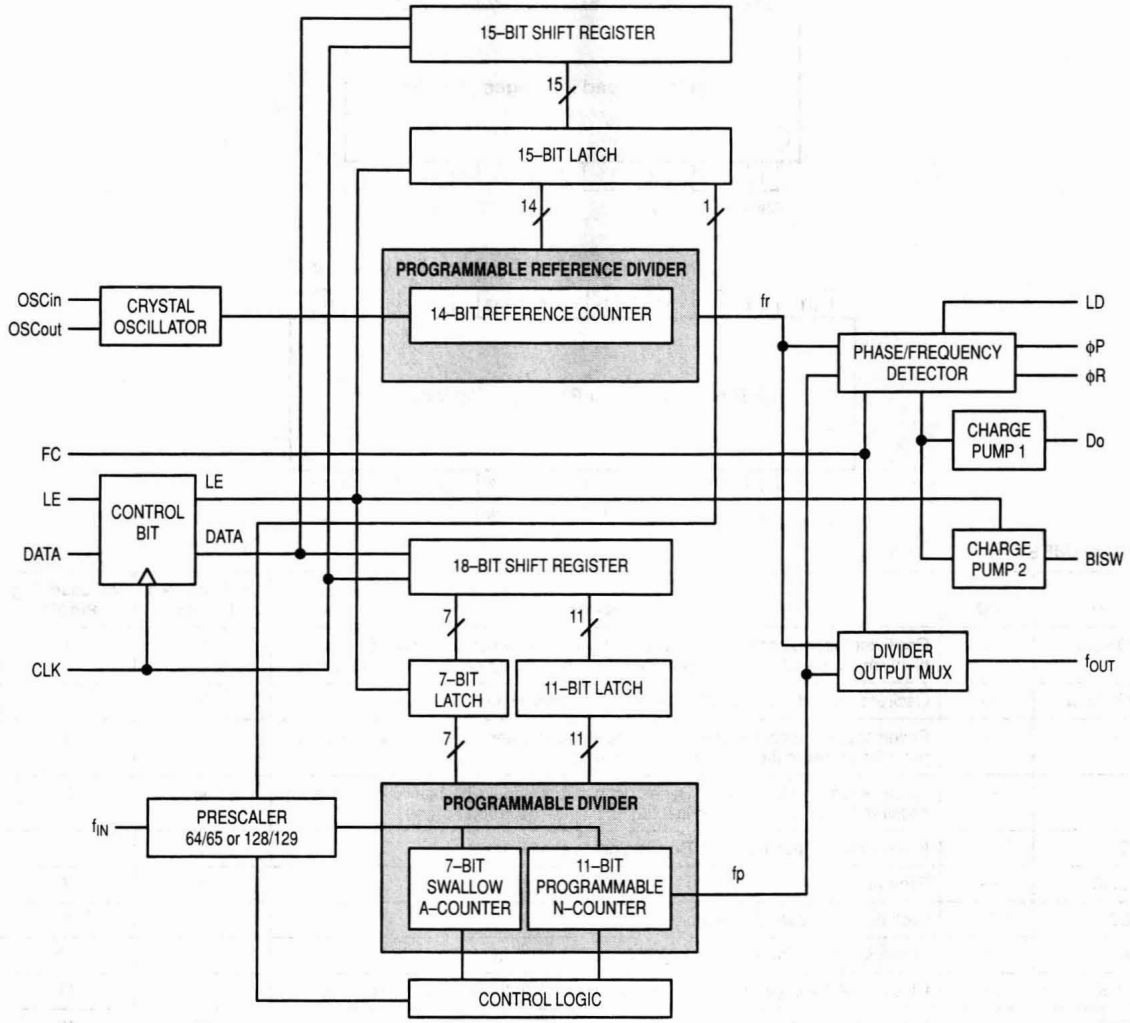



ϕR NC ϕP fOUT BISW FC LE DATA NC CLK
20 19 18 17 16 15 14 13 12 11
Pinout: 20–Lead Package (Top View)
1 2 3 4 5 6 7 8 9 10
OSCin NC OSCout VP VCC Do GND LD NC fIN

PIN NAMES

Pin	I/O	Function	16–Lead Pkg Pin No.	20–Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal may be connected between OSCin and OSCout. It is highly recommended that an external source be ac coupled into this pin (see text).	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V_P	—	Power supply for charge pumps (V_P should be greater than or equal to V_{CC}) V_p provides power to the Do, BISW and ϕP outputs	3	4
V_{CC}	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f_{IN}	I	Prescaler input. The VCO signal is AC–coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects fp or fr on the f_{OUT} pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN ("analog switch is ON") the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f_{OUT}	O	Phase comparator input signal. When FC is HIGH, f_{OUT}=fr, programmable reference divider output; when FC is LOW, f_{OUT}=fp, programmable divider output	14	17
ϕP	O	Output for external charge pump. Standard CMOS output level	15	18
ϕR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

Figure 1. MC12202 Block Diagram



DATA ENTRY FORMAT

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14–bit programmable reference divider plus the prescaler setting bit, and the 18–bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

Control bit: "H" = data is transferred into 15–bit latch of programmable reference divider

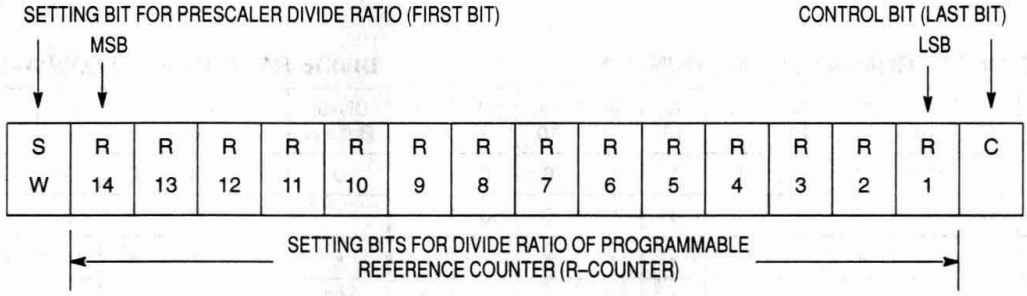
"L" = data is transferred into 18–bit latch of programmable divider

WARNING: Switching CLK or DATA after the device is programmed may generate noise on the charge pump outputs which will affect the VCO.

PROGRAMMABLE REFERENCE DIVIDER

16–bit serial data format for the programmable reference counter, "R–counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15–bit shift register into the 15–bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for ÷128/129, SW=1 for ÷64/65). An R divide ratio less than 8 is prohibited.

For Control bit (C) = HIGH:



DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

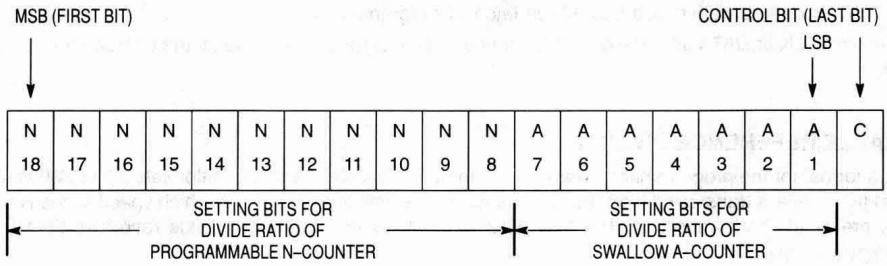
PRESCALER SELECT BIT

Prescaler Divide Ratio P	SW
128/129	0
64/65	1

PROGRAMMABLE DIVIDER

19–bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18–bit shift register into the 18–bit latch which specifies the swallow A–counter divide ratio (0 to 127) and the programmable N–counter divide ratio (16 to 2047). An N–counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



DIVIDE RATIO OF PROGRAMMABLE N–COUNTER **DIVIDE RATIO OF SWALLOW A–COUNTER**

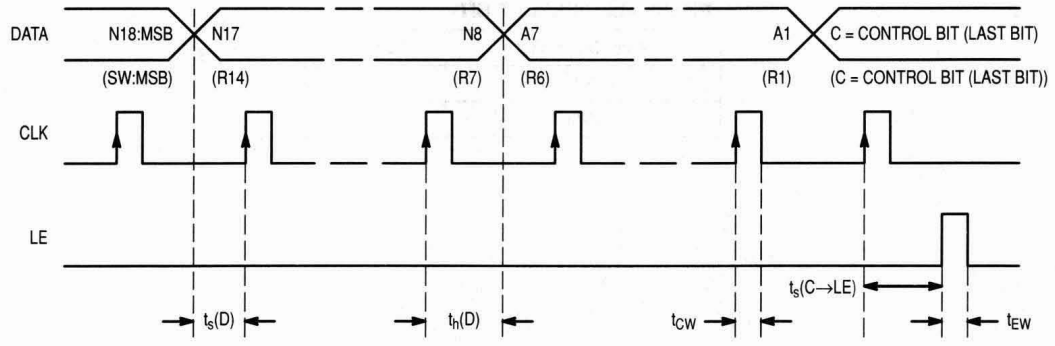
Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	127	1	1	1	1	1	1	1

DIVIDE RATIO SETTING

fvco = [(P•N)+A]•fosc ÷ R with A<N

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11–bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7–bit swallow counter (0 to 127, A<N)
- fosc: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14–bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (64 or 128)

Figure 2. Serial Data Input Timing



NOTES:Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

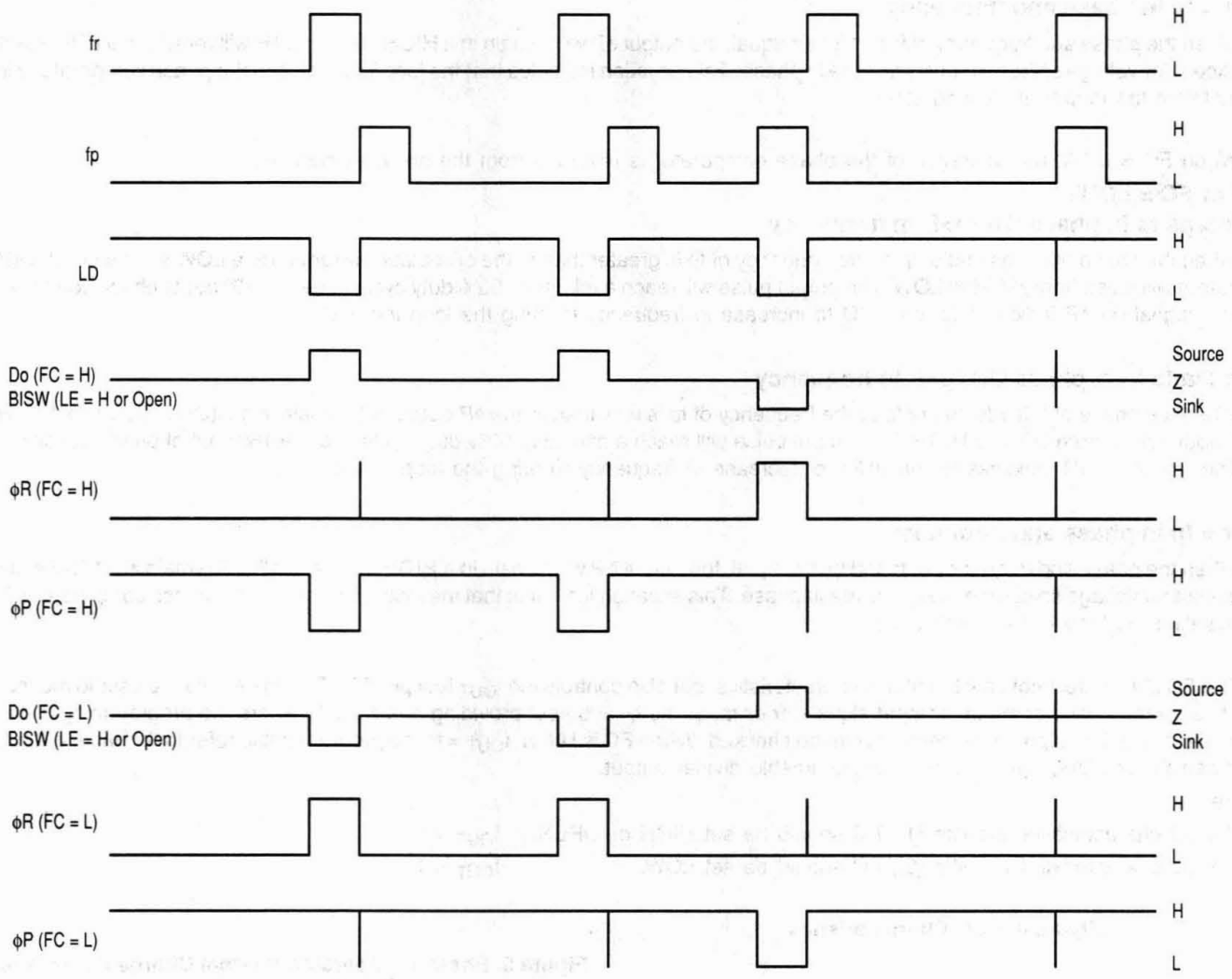
$t_s(D)$ = Setup Time DATA to CLK	$t_s(D) \geq 10ns$
$t_h(D)$ = Hold Time DATA to CLK	$t_h(D) \geq 20ns$
t_{CW} = CLK Pulse Width	$t_{CW} \geq 30ns$
t_{EW} = LE Pulse Width	$t_{EW} \geq 20ns$
$t_s(C \rightarrow LE)$ = Setup Time CLK to LE	$t_s(C \rightarrow LE) \geq 30ns$

PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12202 is a high speed digital phase frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians. The phase comparator outputs are standard CMOS rail–to–rail levels (V_P to GND for ϕP and V_{CC} to GND for ϕR), designed for up to 20MHz operation into a 15pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures 3 and 5. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs, ϕR and ϕP, as well as the charge pump output Do can be reversed by switching the FC pin.

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms



NOTES: Do and BISW are current outputs.
Phase difference detection range: -2π to $+2\pi$
Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When fr > fp or fr < fp, spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{source} + I_{sink}}{4\pi} \right| = \frac{4mA}{4\pi}$$

For FC = HIGH:

fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕP output will remain in a HIGH state while the ϕR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕR output will remain in a LOW state while the ϕP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

For FC = LOW:

fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕR output will remain in a LOW state while the ϕP output will pulse from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕP output will remain in a HIGH state while the ϕR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the f_{OUT} test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the f_{OUT} output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, f_{OUT} = fr, the programmable reference divider output. When FC is LOW, f_{OUT} = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. f_{OUT} = fr

If VCO characteristics are like (2), FC should be set LOW. f_{OUT} = fp

Figure 4. VCO Characteristics

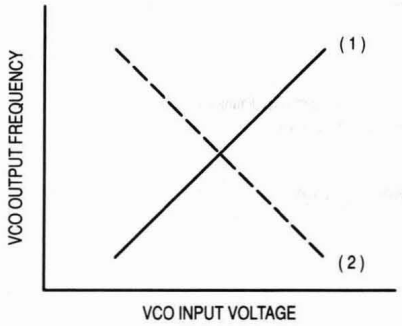
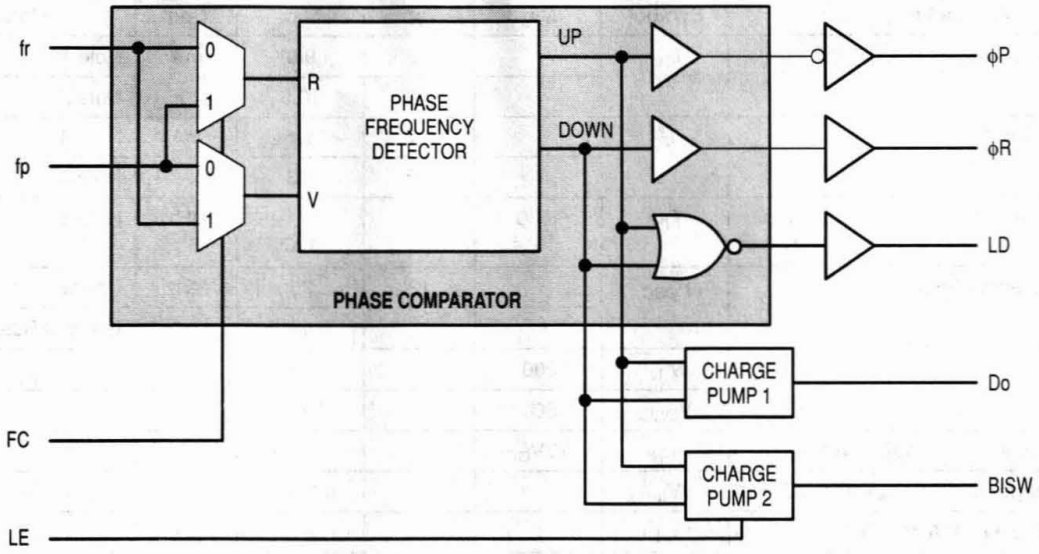


Figure 5. Phase Comparator, Internal Charge Pump, and f_{OUT} Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	ϕR	ϕP	f_{OUT}	Do	ϕR	ϕP	f_{OUT}
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTE: Z = High impedance
When LE is HIGH or Open, BISW has the same characteristics as Do.

Figure 6. Detailed Phase Comparator Block Diagram



LOCK DETECT

The Lock Detect (LD) output pin provides a LOW pulse when fr and fp are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See Figure 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See Figure 9.

OSCILLATOR INPUT

For best operation, an external reference oscillator is recommended. The signal should be AC–coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC–coupled signal must be between 500 and 2200 mV peak–to–peak. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the signal as it switches against the internal voltage reference.

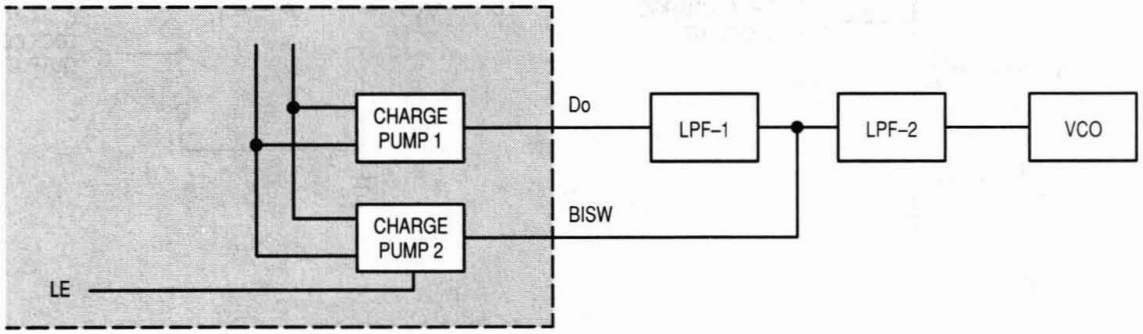
The device incorporates an on–chip reference oscillator/buffer so that an external parallel–resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure 10 are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance). However, using the on–chip reference oscillator, greatly increases the synthesized phase noise.

DUAL INTERNAL CHARGE PUMPS ("ANALOG SWITCH")

Due to the pure Bipolar nature of the MC12202 design, the "analog switch" function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure 7 below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN ("analog switch is ON"), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

Figure 7. "Analog Switch" Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}		5.8	9.0	mA	Note 1
			7.2	10.5		Note 2
Supply Current for V_P	I_P		0.7	1.1	mA	Note 3
			0.8	1.3		Note 4
Operating Frequency f_{IN}max f_{IN}min	F_{IN}	1100		100	MHz	Note 5
Operating Frequency (OSCin)	F_{OSC}		12	20	MHz	Crystal Mode
				40	MHz	External Reference Mode
Input Sensitivity f_{IN}	V_{IN}	200		1000	mVpp	
OSCin	V_{OSC}	500		2200	mVpp	
Input HIGH Voltage CLK, DATA, LE, FC	V_{IH}	0.7V_{CC}			V	
Input LOW Voltage CLK, DATA, LE, FC	V_{IL}			0.3V_{CC}	V	V_{CC} = 5.5V
Input HIGH Current (DATA and CLK)	I_{IH}		1.0	2.0	µA	V_{CC} = 5.5V
Input LOW Current (DATA and CLK)	I_{IL}	–10	–5.0		µA	V_{CC} = 5.5V
Input Current (OSCin)	I_{OSC}		130 –310		µA	OSCin = V_{CC} OSCin = V_{CC} – 2.2V
Input HIGH Current (LE and FC)	I_{IH}		1.0	2.0	µA	
Input LOW Current (LE and FC)	I_{IL}	–75	–60		µA	
Charge Pump Output Current	I_{Source}[6]	–2.6	–2.0	–1.4	mA	V_{Do} = V_P/2; V_P = 2.7V
Do and BISW	I_{Sink}[6]	+1.4	+2.0	+2.6		V_{BISW} = V_P/2; V_P = 2.7V
	I_{Hi-Z}	–15		+15	nA	0.5 < V_{DO} < V_P–0.5 0.5 < V_{BISW} < V_P–0.5
Output HIGH Voltage (LD, ϕR, ϕP, f_{OUT})	V_{OH}	4.4			V	V_{CC} = 5.0V
		2.4			V	V_{CC} = 3.0V
Output LOW Voltage (LD, ϕR, ϕP, f_{OUT})	V_{OL}			0.4	V	V_{CC} = 5.0V
				0.4	V	V_{CC} = 3.0V
Output HIGH Current (LD, ϕR, ϕP, f_{OUT})	I_{OH}	–1.0			mA	
Output LOW Current (LD, ϕR, ϕP, f_{OUT})	I_{OL}	1.0			mA	

1. V_{CC} = 3.3V, all outputs open.
2. V_{CC} = 5.5V, all outputs open.
3. V_P = 3.3V, all outputs open.
4. V_P = 6.0V, all outputs open.
5. AC coupling, F_{IN} measured with a 1000pF capacitor.
6. Source current flows out of the pin and sink current flows into the pin.

Figure 8. Typical External Charge Pump Circuit

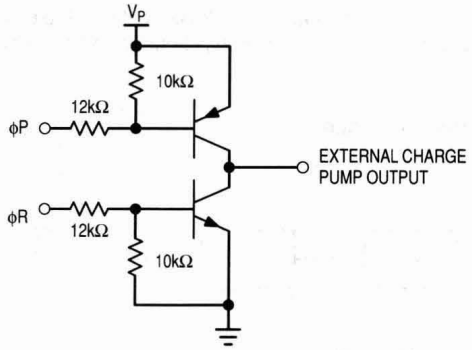


Figure 9. Typical Lock Detect Circuit

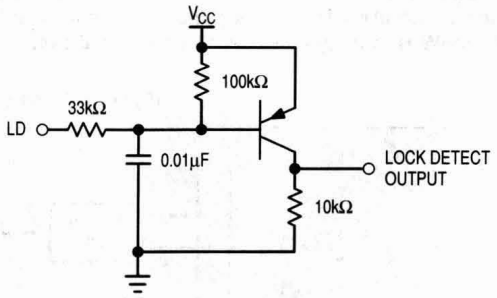
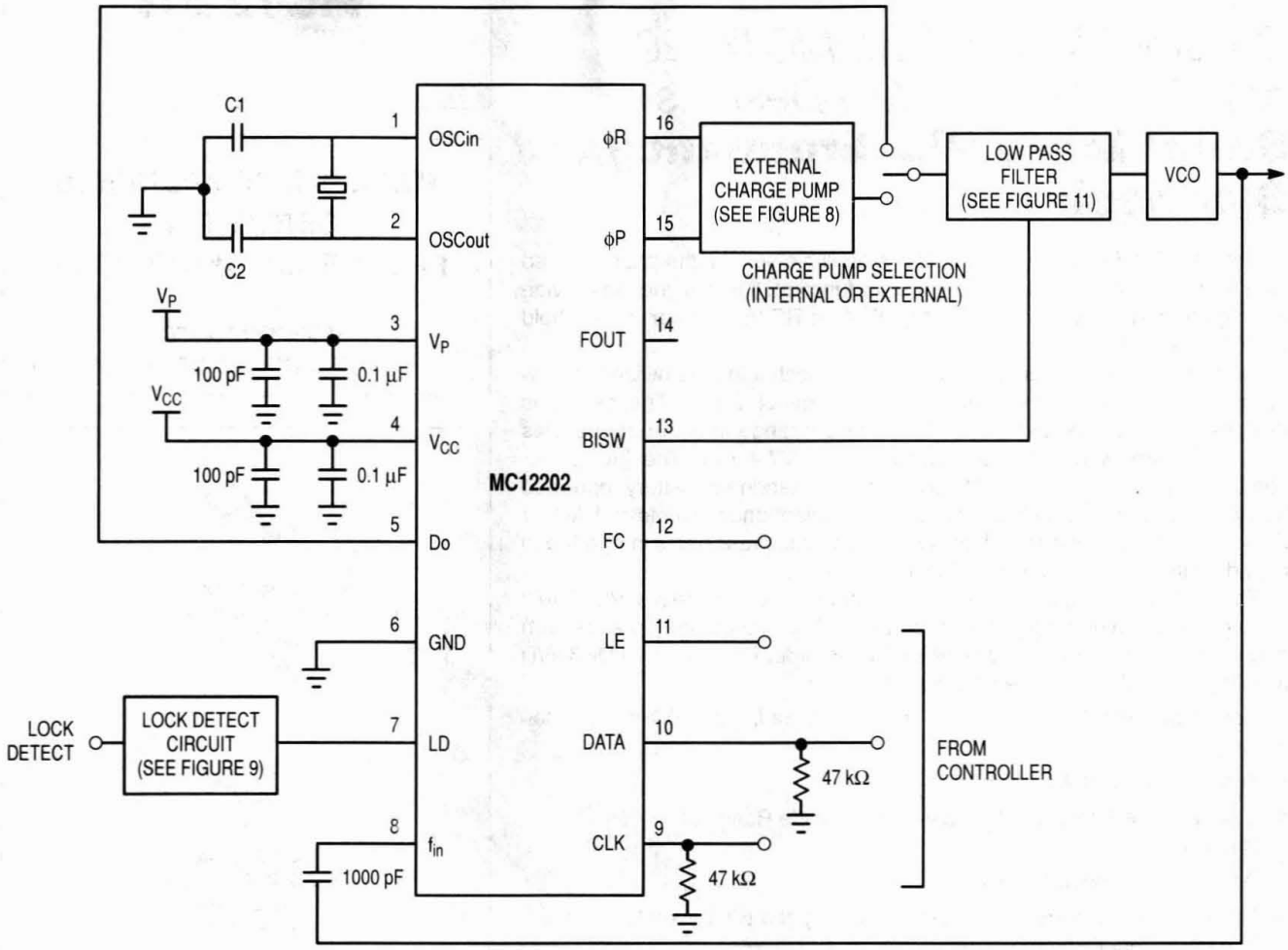
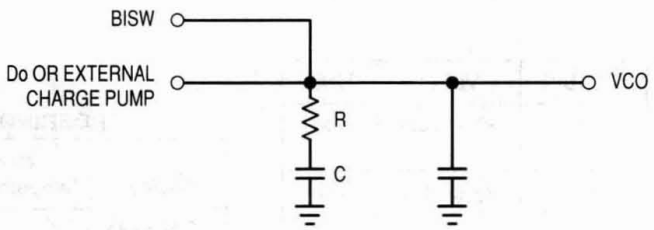


Figure 10. Typical Applications Example (16–Pin Package)



C1, C2: Dependent on Crystal Oscillator

Figure 11. Typical Loop Filter



MOTOROLA

MC12206

Consider MC145200, MC145201 or MC145202 for New Designs

Serial Input PLL Frequency Synthesizer

MECL PLL COMPONENTS
SERIAL PLL
FREQUENCY SYNTIESIZER

SEMICONDUCTOR
TECHNICAL DATA

The MC12206 is a 2.0 GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse–swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7 V. The device is designed for operation over 2.7 to 5.5 V supply range for input frequencies up to 2.0 GHz with a typical current drain of 7.4 mA. The low power consumption makes the MC12206 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 64/65 or 128/129 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 6.7 mA Typical for I_{CC} and 0.7 mA Typical for I_P
- Supply Voltage of 2.7 to 5.5 V
- Dual Modulus Prescaler With Selectable Divide Ratios of 64/65 or 128/129
- On–Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14–Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7–Bit Swallow Counter and an 11–Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of –40 to 85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

DT SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

Not Recommended For New Designs

MOSAIC V, Mfax and *InterActiveApNote* are trademarks of Motorola, Inc.

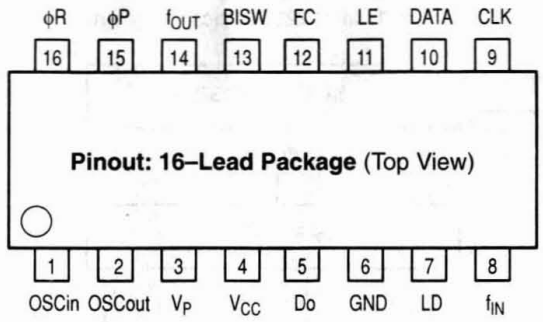
MAXIMUM RATINGS (Note 1)

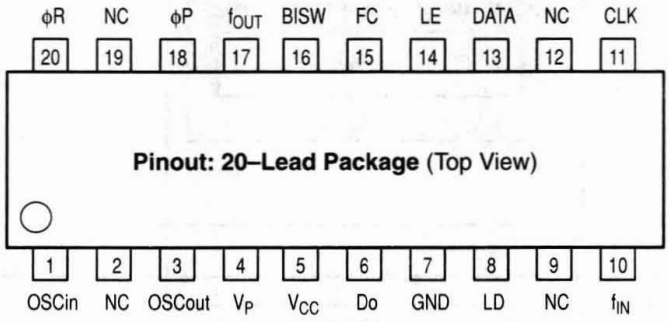
Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 4 (Pin 5 in 20–lead package)	V_{CC}	–0.5 to 6.0	Vdc
Power Supply Voltage, Pin 3 (Pin 4 in 20–lead package)	V_P	V_{CC} to 6.0	Vdc
Storage Temperature Range	Tstg	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12206D	T_A = – 40° to +85°C	SO–16
MC12026DT		TSSOP–20

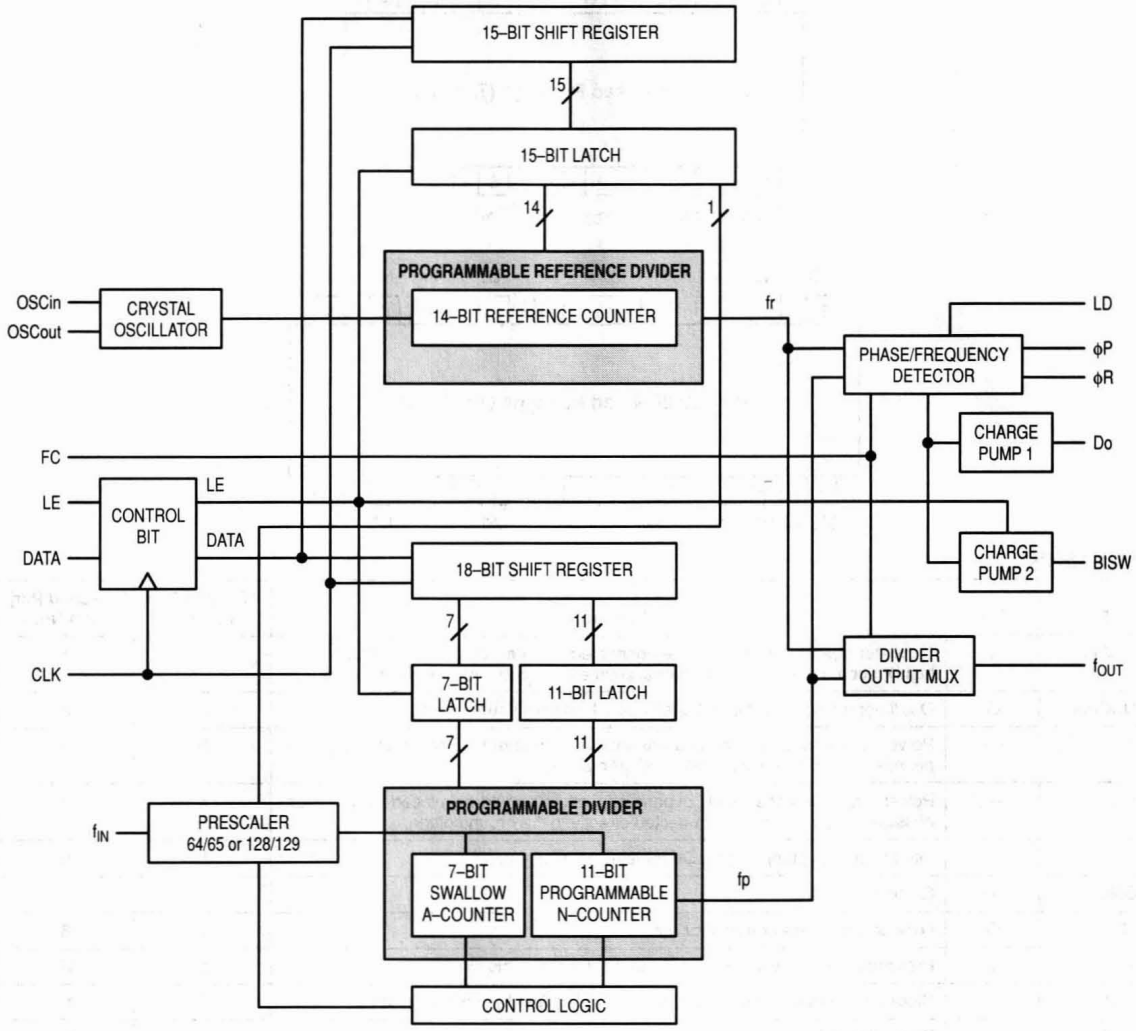



φR NC φP fOUT BISW FC LE DATA NC CLK
20 19 18 17 16 15 14 13 12 11
Pinout: 20–Lead Package (Top View)
1 2 3 4 5 6 7 8 9 10
OSCin NC OSCout VP VCC Do GND LD NC fIN

PIN NAMES

Pin	I/O	Function	16–Lead Pkg Pin No.	20–Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal may be connected between OSCin and OSCout. It is highly recommended that an external source be ac coupled into this pin (see text).	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V_P	—	Power supply for charge pumps (V_P should be greater than or equal to V_{CC}) V_p provides power to the Do, BISW and φP outputs	3	4
V_{CC}	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f_{IN}	I	Prescaler input. The VCO signal is ac–coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects fp or fr on the f_{OUT} pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN ("analog switch is ON") the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f_{OUT}	O	Phase comparator input signal. When FC is HIGH, f_{OUT}=fr, programmable reference divider output; when FC is LOW, f_{OUT}=fp, programmable divider output	14	17
φP	O	Output for external charge pump. Standard CMOS output level	15	18
φR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

Figure 1. MC12206 Block Diagram



DATA ENTRY FORMAT

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14–bit programmable reference divider plus the prescaler setting bit, and the 18–bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

Control bit: "H" = data is transferred into 15–bit latch of programmable reference divider

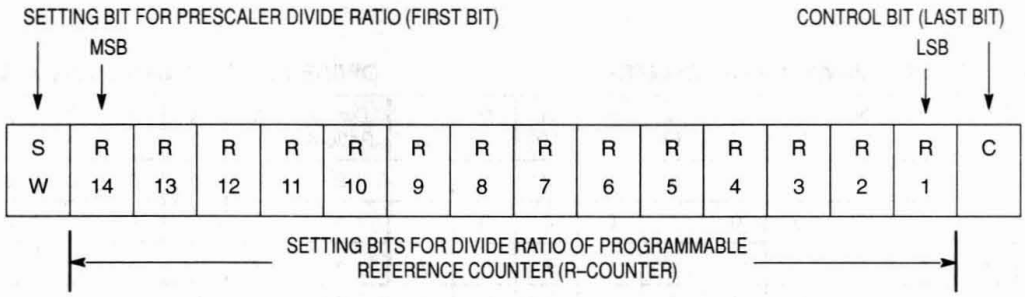
"L" = data is transferred into 18–bit latch of programmable divider

WARNING: Switching CLK or DATA after the device is programmed may generate noise on the charge pump outputs which will affect the VCO.

PROGRAMMABLE REFERENCE DIVIDER

16–bit serial data format for the programmable reference counter, "R–counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15–bit shift register into the 15–bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for ÷128/129, SW=1 for ÷64/65). An R divide ratio less than 8 is prohibited.

For Control bit (C) = HIGH:



DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

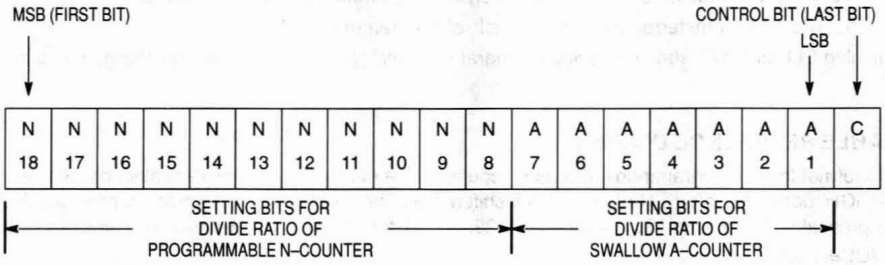
PRESCALER SELECT BIT

Prescaler Divide Ratio P	SW
128/129	0
64/65	1

PROGRAMMABLE DIVIDER

19–bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18–bit shift register into the 18–bit latch which specifies the swallow A–counter divide ratio (0 to 127) and the programmable N–counter divide ratio (16 to 2047). An N–counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



DIVIDE RATIO OF PROGRAMMABLE N–COUNTER **DIVIDE RATIO OF SWALLOW A–COUNTER**

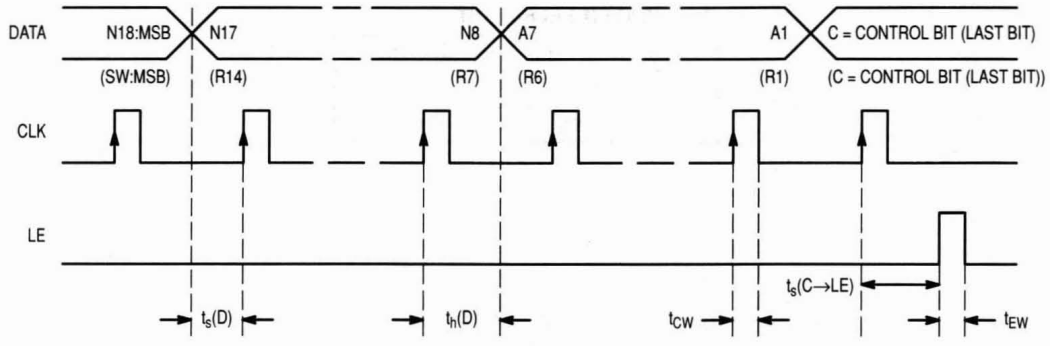
Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	127	1	1	1	1	1	1	1

DIVIDE RATIO SETTING

fvco = [(P•N)+A]•fosc ÷ R with A<N

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11–bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7–bit swallow counter (0 to 127, A<N)
- fosc: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14–bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (64 or 128)

Figure 2. Serial Data Input Timing



NOTES:Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

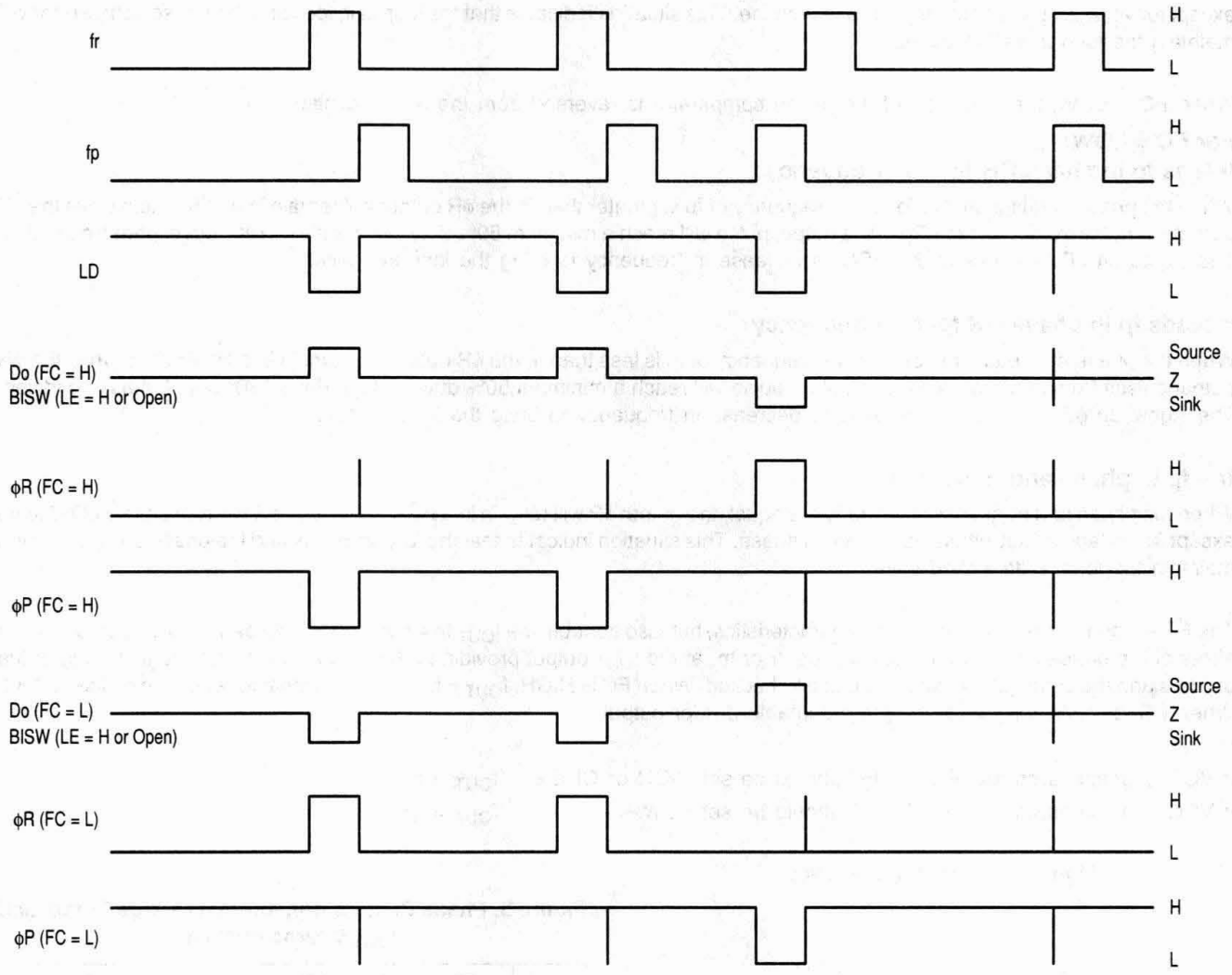
t_s(D) = Setup Time DATA to CLK	t_s(D) ≥ 10 ns
t_h(D) = Hold Time DATA to CLK	t_h(D) ≥ 20 ns
t_{CW} = CLK Pulse Width	t_{CW} ≥ 30 ns
t_{EW} = LE Pulse Width	t_{EW} ≥ 20 ns
t_s(C→LE) = Setup Time CLK to LE	t_s(C→LE) ≥ 30 ns

PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12206 is a high speed digital phase frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians. The phase comparator outputs are standard CMOS rail–to–rail levels (V_P to GND for ϕP and V_{CC} to GND for ϕR), designed for up to 20 MHz operation into a 15 pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures 3 and 5. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs, ϕR and ϕP, as well as the charge pump output Do can be reversed by switching the FC pin.

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms



NOTES: Do and BISW are current outputs.
Phase difference detection range: -2π to $+2\pi$
Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When fr > fp or fr < fp, spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{source} + I_{sink}}{4\pi} \right| = \frac{4mA}{4\pi}$$

For FC = HIGH:
fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕP output will remain in a HIGH state while the ϕR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕR output will remain in a LOW state while the ϕP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

For FC = LOW:
fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕR output will remain in a LOW state while the ϕP output will pulse from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕP output will remain in a HIGH state while the ϕR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop to lock.

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When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the f_{OUT} test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the f_{OUT} output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, f_{OUT} = fr, the programmable reference divider output. When FC is LOW, f_{OUT} = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. f_{OUT} = fr

If VCO characteristics are like (2), FC should be set LOW. f_{OUT} = fp

Figure 4. VCO Characteristics

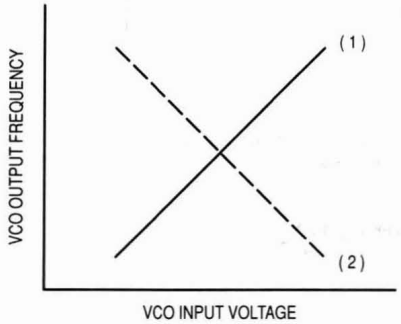
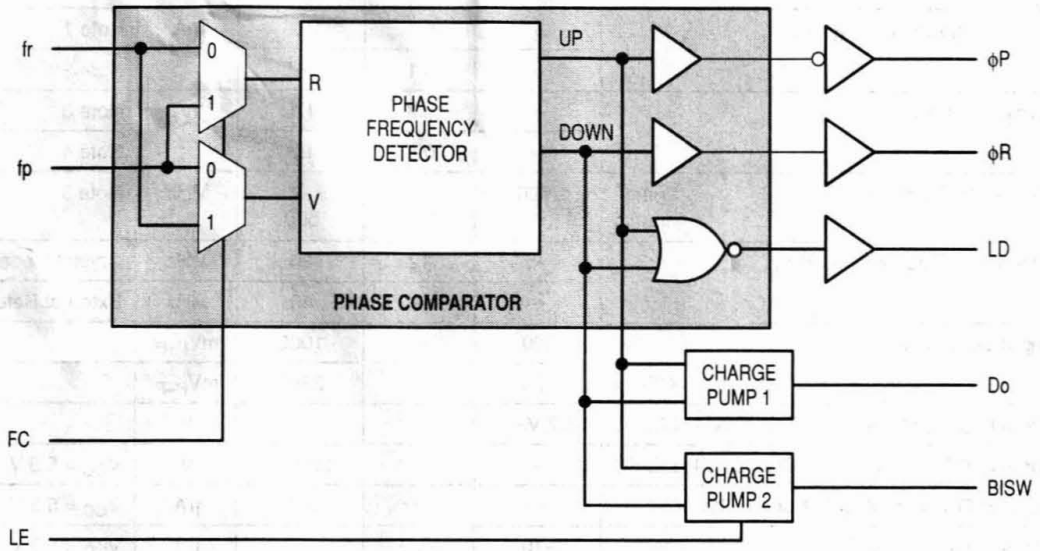


Figure 5. Phase Comparator, Internal Charge Pump, and f_{OUT} Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	ϕR	ϕP	f_{OUT}	Do	ϕR	ϕP	f_{OUT}
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTES: Z = High impedance
When LE is HIGH or Open, BISW has the same characteristics as Do.

Figure 6. Detailed Phase Comparator Block Diagram



LOCK DETECT

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OSCILLATOR INPUT

For best operation, an external reference oscillator is recommended. The signal should be AC–coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC–coupled signal must be between 500 and 2200 mV peak–to–peak. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the signal as it switches against the internal voltage reference.

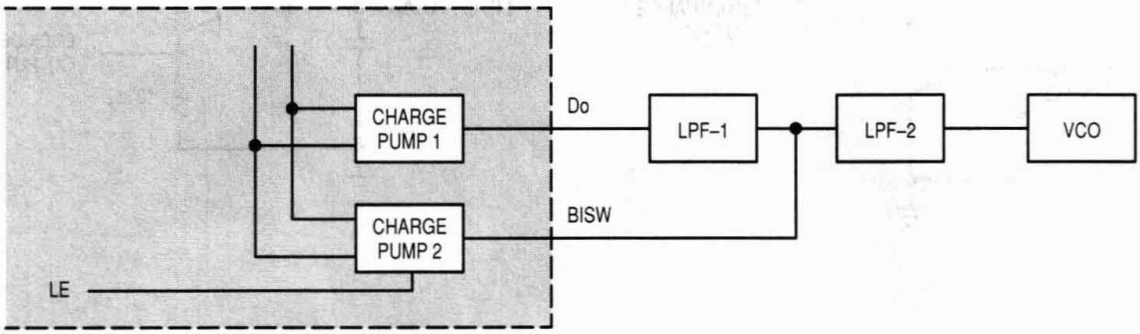
The device incorporates an on–chip reference oscillator/buffer so that an external parallel–resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure 10 are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance). However, using the on–chip reference oscillator greatly increases the synthesized phase noise.

DUAL INTERNAL CHARGE PUMPS ("ANALOG SWITCH")

Due to the pure Bipolar nature of the MC12206 design, the "analog switch" function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure 7 below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN ("analog switch is ON"), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

Figure 7. "Analog Switch" Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to 85°C, unless otherwise noted.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current for V_{CC}	–	6.7	10.5	mA	Note 1
		–	8.1	12.5		Note 2
I_P	Supply Current for V_p	–	0.7	1.1	mA	Note 3
		–	0.8	1.3		Note 4
F_{IN}	Operating Frequency f_{IN}max f_{IN}min	2000 –	– –	– 500	MHz	Note 5
F_{OSC}	Operating Frequency (OSCin)	–	12	20	MHz	Crystal Mode
		–	–	40	MHz	External Reference Mode
V_{IN}	Input Sensitivity f_{IN}	200	–	1000	mV_{P-P}	
V_{OSC}	OSCin	500	–	2200	mV_{P-P}	
V_{IH}	Input HIGH Voltage CLK, DATA, LE, FC	0.7 V_{CC}	–	–	V	
V_{IL}	Input LOW Voltage CLK, DATA, LE, FC	–	–	0.3 V_{CC}	V	V_{CC} = 5.5 V
I_{IH}	Input HIGH Current (DATA and CLK)	–	1.0	2.0	µA	V_{CC} = 5.5 V
I_{IL}	Input LOW Current (DATA and CLK)	–10	–5.0		µA	V_{CC} = 5.5 V
I_{OSC}	Input Current (OSCin)	– –	130 –310	– –	µA	OSCin = V_{CC} OSCin = V_{CC} – 2.2 V
I_{IH}	Input HIGH Current (LE and FC)	–	1.0	2.0	µA	
I_{IL}	Input LOW Current (LE and FC)	–75	–60	–	µA	
I_{Source}[6]	Charge Pump Output Current	–2.6	–2.0	–1.4	mA	V_{Do} = V_P/2; V_P = 2.7 V
I_{Sink}[6]	Do and BISW	+1.4	+2.0	+2.6		V_{BISW} = V_P/2; V_P = 2.7 V
I_{Hi-Z}		–15	–	+15	nA	0.5 < V_{DO} < V_P – 0.5 0.5 < V_{BISW} < V_P – 0.5
V_{OH}	Output HIGH Voltage (LD, ϕR, ϕP, f_{OUT})	4.4	–	–	V	V_{CC} = 5.0 V
		2.4	–	–	V	V_{CC} = 3.0 V
V_{OL}	Output LOW Voltage (LD, ϕR, ϕP, f_{OUT})	–	–	0.4	V	V_{CC} = 5.0 V
		–	–	0.4	V	V_{CC} = 3.0 V
I_{OH}	Output HIGH Current (LD, ϕR, ϕP, f_{OUT})	–1.0	–	–	mA	
I_{OL}	Output LOW Current (LD, ϕR, ϕP, f_{OUT})	1.0	–	–	mA	

1. V_{CC} = 3.3 V, all outputs open.
2. V_{CC} = 5.5 V, all outputs open.
3. V_p = 3.3 V, all outputs open.
4. V_p = 6.0 V, all outputs open.
5. AC coupling, F_{IN} measured with a 1000 pF capacitor.
6. Source current flows out of the pin and sink current flows into the pin.

Figure 8. Typical External Charge Pump Circuit

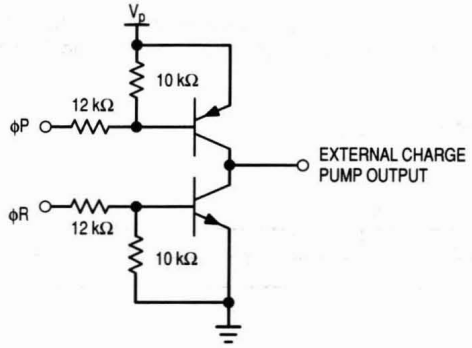


Figure 9. Typical Lock Detect Circuit

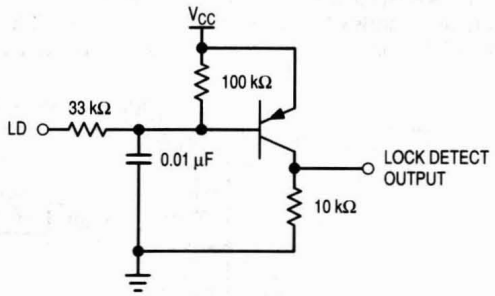
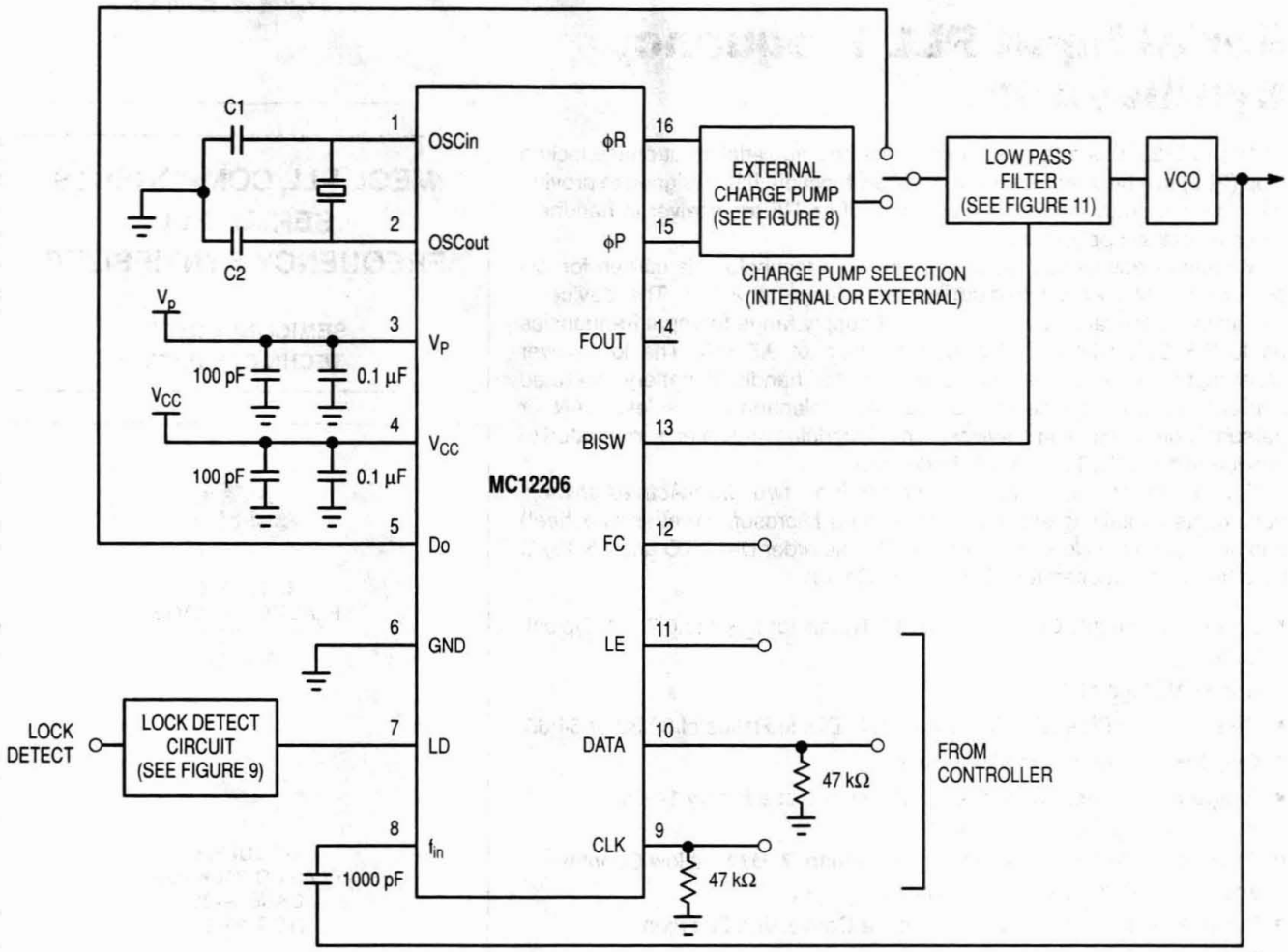
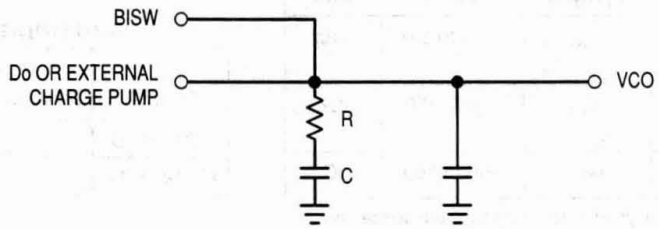


Figure 10. Typical Applications Example (16–Pin Package)



C1, C2: Dependent on Crystal Oscillator

Figure 11. Typical Loop Filter



MOTOROLA

MC12210

Serial Input PLL Frequency Synthesizer

MECL PLL COMPONENTS
SERIAL PLL
FREQUENCY SYNTIESIZER

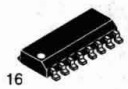
SEMICONDUCTOR
TECHNICAL DATA

The MC12210 is a 2.5 GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse–swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7 V. The device is designed for operation over 2.7 to 5.5 V supply range for input frequencies up to 2.5 GHz with a typical current drain of 9.5 mA. The low power consumption makes the MC12210 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 32/33 or 64/65 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 8.8 mA Typical for I_{CC} and 0.7 mA Typical for I_P
- Supply Voltage of 2.7 to 5.5 V
- Dual Modulus Prescaler With Selectable Divide Ratios of 32/33 or 64/65
- On–Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14–Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7–Bit Swallow Counter and an 11–Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of –40 to 85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

DT SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

MOSAIC V, Mfax and *InterActiveApNote* are trademarks of Motorola, Inc.

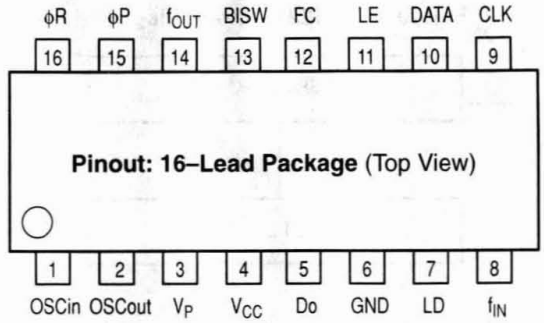
MAXIMUM RATINGS (Note 1)

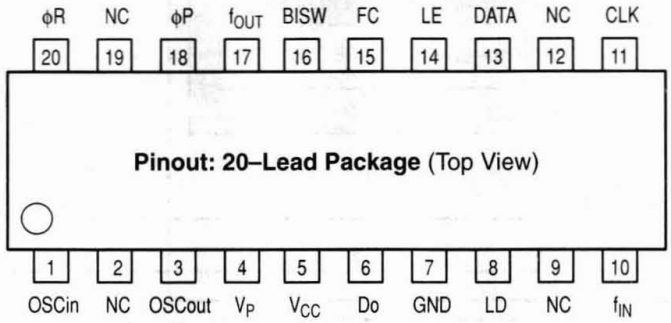
Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 4 (Pin 5 in 20–lead package)	V_{CC}	–0.5 to 6.0	Vdc
Power Supply Voltage, Pin 3 (Pin 4 in 20–lead package)	V_p	V_{CC} to 6.0	Vdc
Storage Temperature Range	Tstg	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12210D	T_A = – 40° to +85°C	SO–16
MC12210DT		TSSOP–20

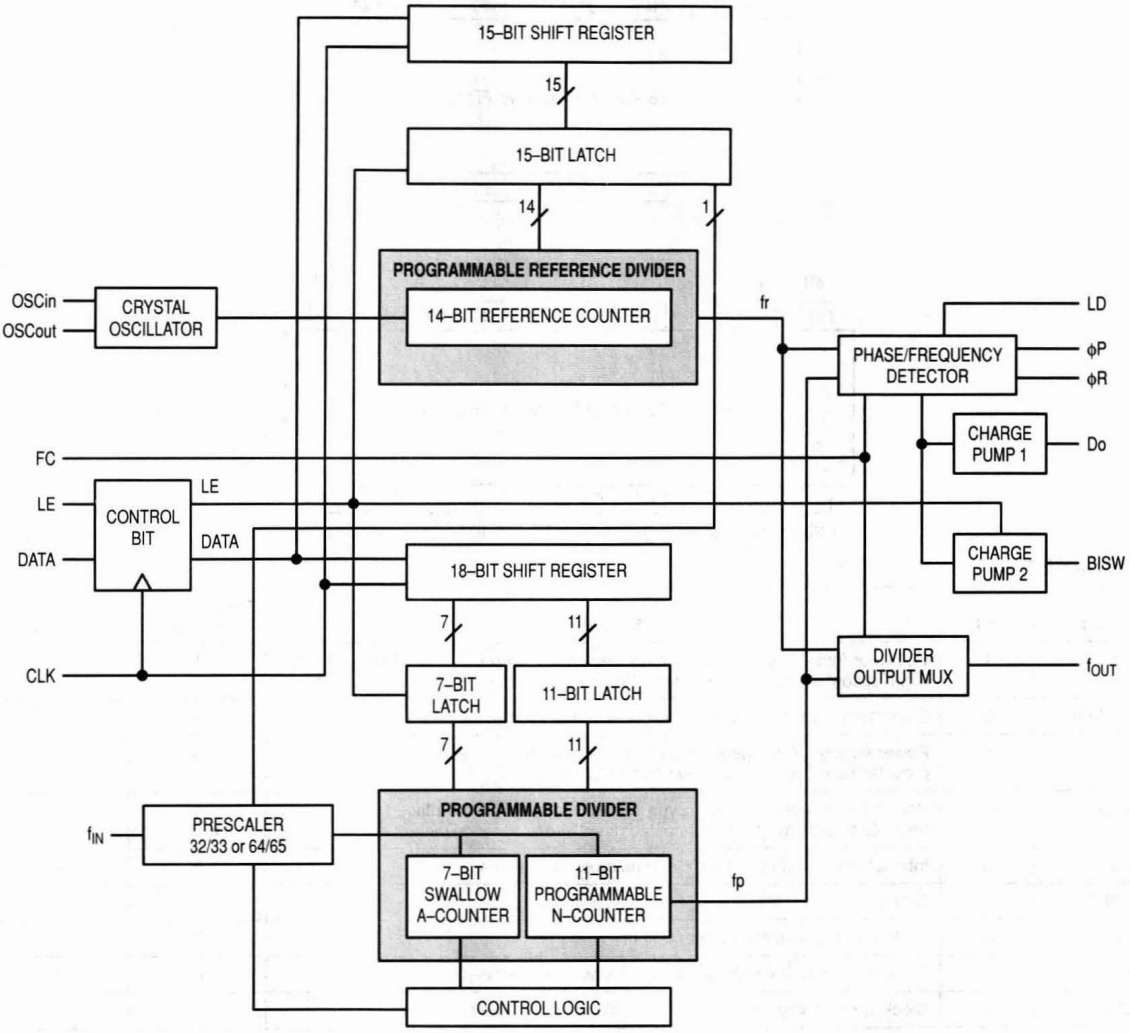



ϕR NC ϕP fOUT BISW FC LE DATA NC CLK
20 19 18 17 16 15 14 13 12 11
Pinout: 20–Lead Package (Top View)
1 2 3 4 5 6 7 8 9 10
OSCin NC OSCout VP VCC Do GND LD NC fIN

PIN NAMES

Pin	I/O	Function	16–Lead Pkg Pin No.	20–Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal may be connected between OSCin and OSCout. It is highly recommended that an external source be ac coupled into this pin (see text).	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V_P	—	Power supply for charge pumps (V_P should be greater than or equal to V_{CC}) V_P provides power to the Do, BISW and ϕP outputs	3	4
V_{CC}	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f_{IN}	I	Prescaler input. The VCO signal is AC–coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects fp or fr on the f_{OUT} pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN ("analog switch is ON") the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f_{OUT}	O	Phase comparator input signal. When FC is HIGH, f_{OUT}=fr, programmable reference divider output; when FC is LOW, f_{OUT}=fp, programmable divider output	14	17
ϕP	O	Output for external charge pump. Standard CMOS output level	15	18
ϕR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

Figure 1. MC12210 Block Diagram



DATA ENTRY FORMAT

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14–bit programmable reference divider plus the prescaler setting bit, and the 18–bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

Control bit: "H" = data is transferred into 15–bit latch of programmable reference divider

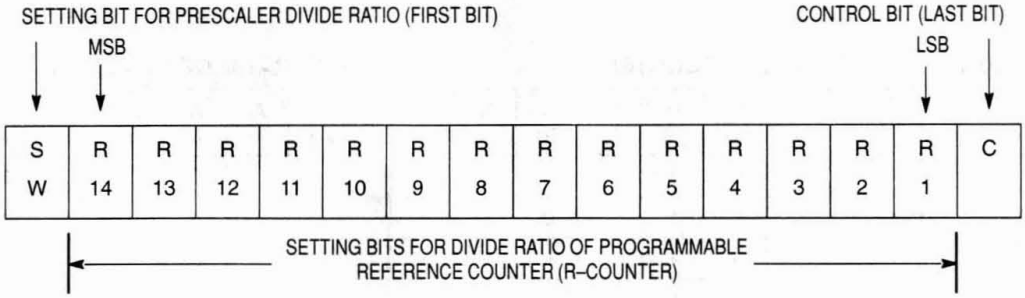
"L" = data is transferred into 18–bit latch of programmable divider

WARNING: Switching CLK or DATA after the device is programmed may generate noise on the charge pump outputs which will affect the VCO.

PROGRAMMABLE REFERENCE DIVIDER

16–bit serial data format for the programmable reference counter, "R–counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15–bit shift register into the 15–bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for ÷64/65, SW=1 for ÷32/33). An R divide ratio less than 8 is prohibited.

For Control bit (C) = HIGH:



DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

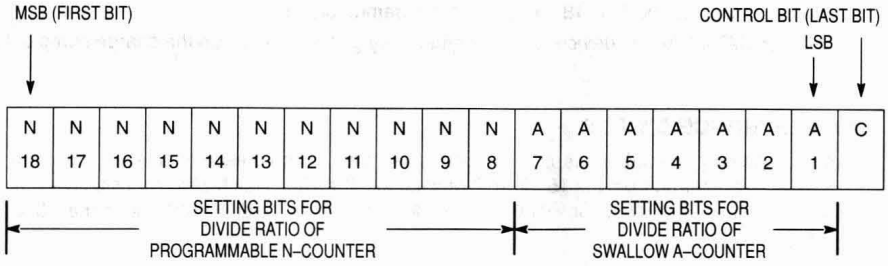
PRESCALER SELECT BIT

Prescaler Divide Ratio P	SW
64/65	0
32/33	1

PROGRAMMABLE DIVIDER

19–bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18–bit shift register into the 18–bit latch which specifies the swallow A–counter divide ratio (0 to 127) and the programmable N–counter divide ratio (16 to 2047). An N–counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



DIVIDE RATIO OF PROGRAMMABLE N–COUNTER

Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

DIVIDE RATIO OF SWALLOW A–COUNTER

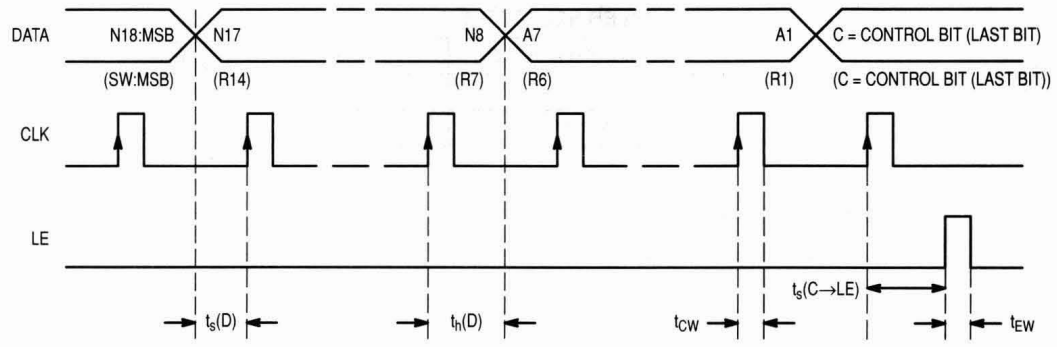
Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

DIVIDE RATIO SETTING

fvco = [(P•N)+A]•fosc ÷ R with A<N

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11–bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7–bit swallow counter (0 to 127, A<N)
- fosc: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14–bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (32 or 64)

Figure 2. Serial Data Input Timing



NOTES:Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

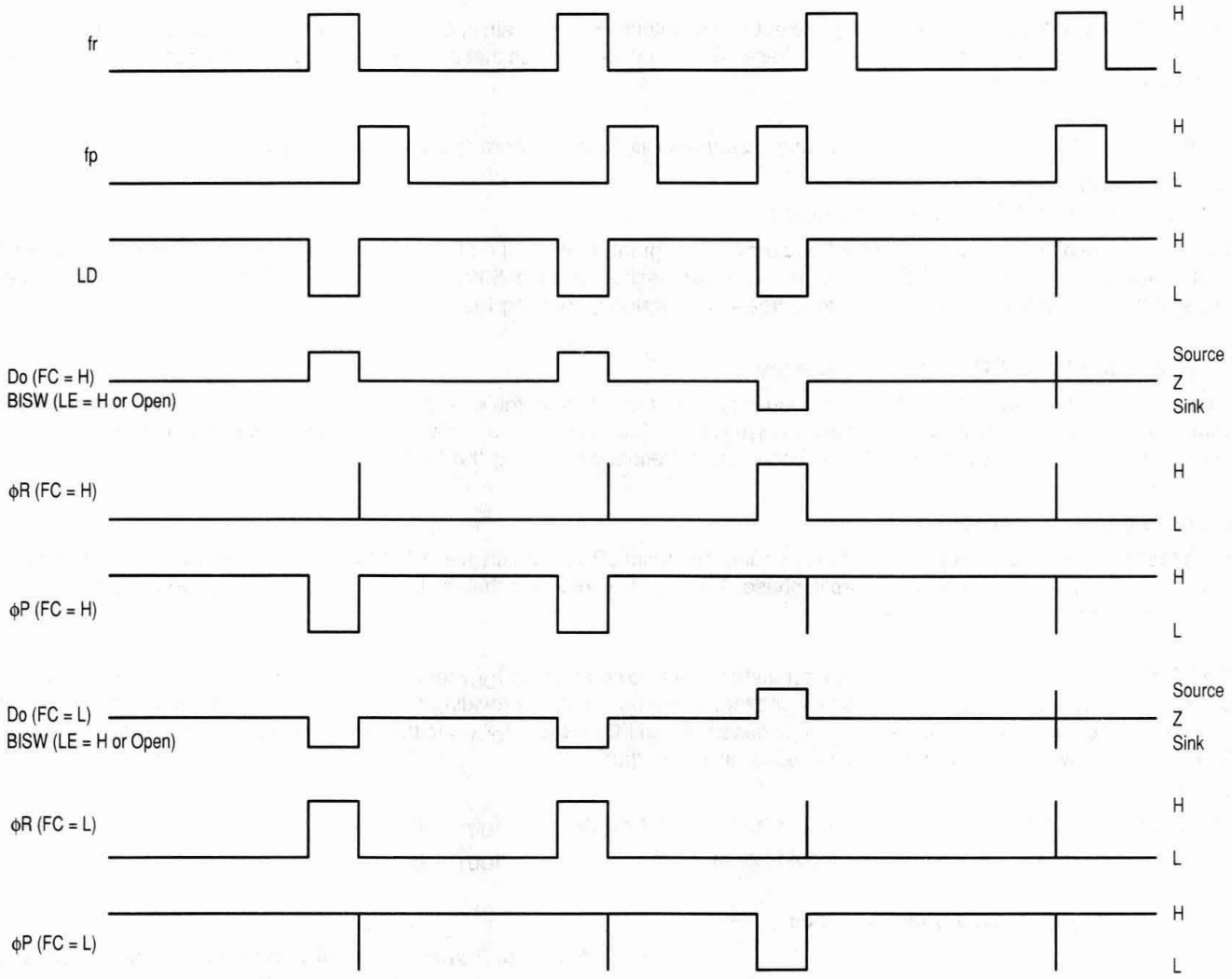
$t_s(D)$ = Setup Time DATA to CLK	$t_s(D) \geq 10$ ns
$t_h(D)$ = Hold Time DATA to CLK	$t_h(D) \geq 20$ ns
t_{CW} = CLK Pulse Width	$t_{CW} \geq 30$ ns
t_{EW} = LE Pulse Width	$t_{EW} \geq 20$ ns
$t_s(C \rightarrow LE)$ = Setup Time CLK to LE	$t_s(C \rightarrow LE) \geq 30$ ns

PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12210 is a high speed digital phase frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians. The phase comparator outputs are standard CMOS rail–to–rail levels (V_P to GND for ϕP and V_{CC} to GND for ϕR), designed for up to 20MHz operation into a 15pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures 3 and 5. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs, ϕR and ϕP, as well as the charge pump output Do can be reversed by switching the FC pin.

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms



NOTES: Do and BISW are current outputs.
Phase difference detection range: -2π to $+2\pi$
Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When fr > fp or fr < fp, spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{source} + I_{sink}}{4\pi} \right| = \frac{4mA}{4\pi}$$

For FC = HIGH:

fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕP output will remain in a HIGH state while the ϕR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕR output will remain in a LOW state while the ϕP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

For FC = LOW:

fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕR output will remain in a LOW state while the ϕP output will pulse from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕP output will remain in a HIGH state while the ϕR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the f_{OUT} test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the f_{OUT} output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, f_{OUT} = fr, the programmable reference divider output. When FC is LOW, f_{OUT} = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. f_{OUT} = fr

If VCO characteristics are like (2), FC should be set LOW. f_{OUT} = fp

Figure 4. VCO Characteristics

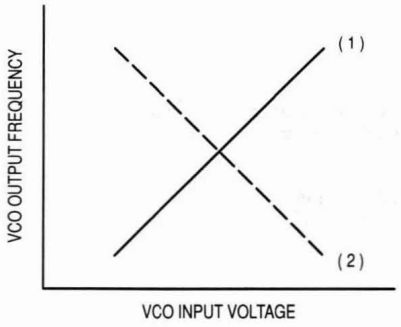


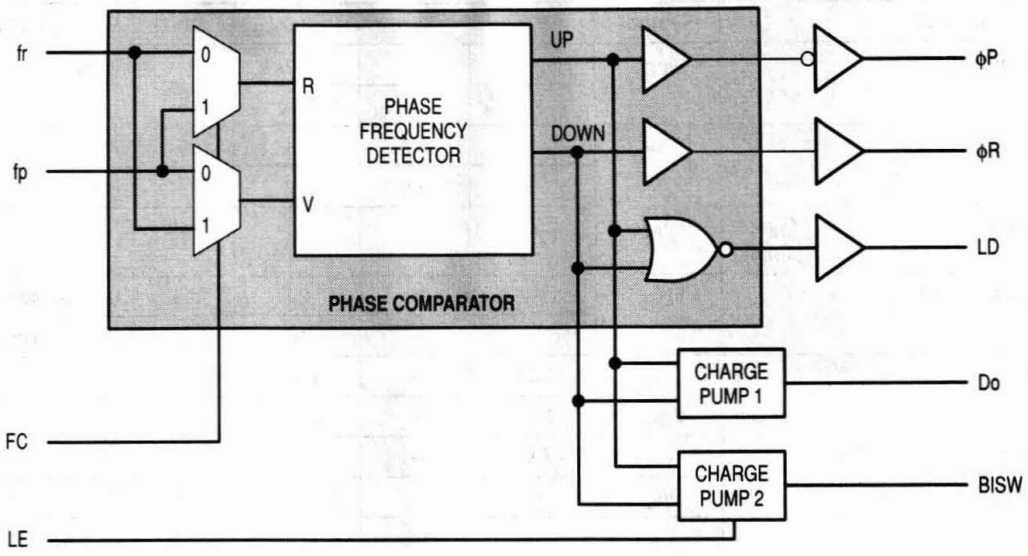
Figure 5. Phase Comparator, Internal Charge Pump, and f_{OUT} Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	ϕR	ϕP	f_{OUT}	Do	ϕR	ϕP	f_{OUT}
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTES: Z = High impedance

When LE is HIGH or Open, BISW has the same characteristics as Do.

Figure 6. Detailed Phase Comparator Block Diagram



LOCK DETECT

The Lock Detect (LD) output pin provides a LOW pulse when fr and fp are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See Figure 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See Figure 9.

OSCILLATOR INPUT

For best operation, an external reference oscillator is recommended. The signal should be AC–coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC–coupled signal must be between 500 and 2200 mV peak–to–peak. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the signal as it switches against the internal voltage reference.

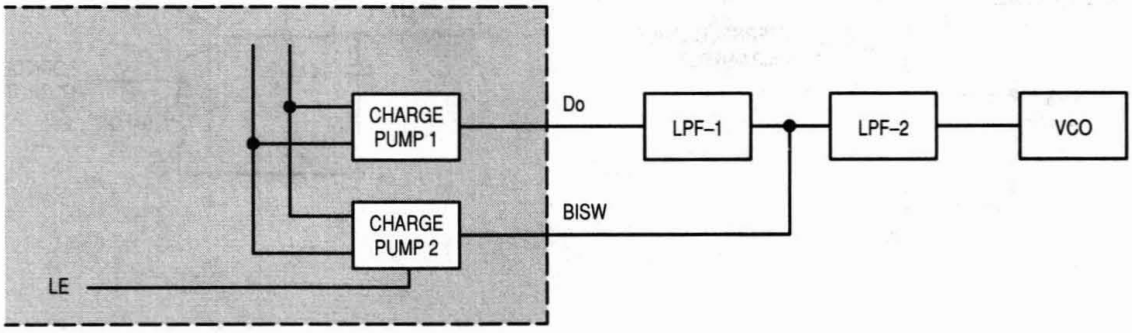
The device incorporates an on–chip reference oscillator/buffer so that an external parallel–resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure 10 are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance). However, using the on–chip reference oscillator greatly increases the synthesized phase noise.

DUAL INTERNAL CHARGE PUMPS ("ANALOG SWITCH")

Due to the pure Bipolar nature of the MC12210 design, the "analog switch" function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure 7 below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN ("analog switch is ON"), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

Figure 7. "Analog Switch" Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V; T_A = –40 to +85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}	–	8.8	13.0	mA	Note 1
		–	10.2	16.0		Note 2
Supply Current for V_P	I_P	–	0.7	1.1	mA	Note 3
		–	0.8	1.3		Note 4
Operating Frequency f_{IN}max f_{IN}min	F_{IN}	2500 –	– –	– 500	MHz	Note 5
Operating Frequency (OSCin)	F_{OSC}	–	12	20	MHz	Crystal Mode
		–	–	40	MHz	External Reference Mode
Input Sensitivity f_{IN}	V_{IN}	200	–	1000	mVpp	
OSCin	V_{OSC}	500	–	2200	mVpp	
Input HIGH Voltage CLK, DATA, LE, FC	V_{IH}	0.7 V_{CC}	–	–	V	
Input LOW Voltage CLK, DATA, LE, FC	V_{IL}	–	–	0.3 V_{CC}	V	V_{CC} = 5.5 V
Input HIGH Current (DATA and CLK)	I_{IH}	–	1.0	2.0	µA	V_{CC} = 5.5 V
Input LOW Current (DATA and CLK)	I_{IL}	–10	–5.0	–	µA	V_{CC} = 5.5 V
Input Current (OSCin)	I_{OSC}	– –	130 –310	– –	µA	OSCin = V_{CC} OSCin = V_{CC} – 2.2 V
Input HIGH Current (LE and FC)	I_{IH}	–	1.0	2.0	µA	
Input LOW Current (LE and FC)	I_{IL}	–75	–60	–	µA	
Charge Pump Output Current	I_{Source}[6]	–2.6	–2.0	–1.4	mA	V_{Do} = V_p/2; V_p = 2.7 V
Do and BISW	I_{Sink}[6]	+1.4	+2.0	+2.6		V_{BISW} = V_p/2; V_p = 2.7 V
	I_{Hi-Z}	–15	–	+15	nA	0.5< V_{DO} < V_p – 0.5 0.5 < V_{BISW} < V_p – 0.5
Output HIGH Voltage (LD, ϕR, ϕP, f_{OUT})	V_{OH}	4.4	–	–	V	V_{CC} = 5.0 V
		2.4	–	–	V	V_{CC} = 3.0 V
Output LOW Voltage (LD, ϕR, ϕP, f_{OUT})	V_{OL}	–	–	0.4	V	V_{CC} = 5.0 V
		–	–	0.4	V	V_{CC} = 3.0 V
Output HIGH Current (LD, ϕR, ϕP, f_{OUT})	I_{OH}	–1.0	–	–	mA	
Output LOW Current (LD, ϕR, ϕP, f_{OUT})	I_{OL}	1.0	–	–	mA	

1. V_{CC} = 3.3 V, all outputs open.
2. V_{CC} = 5.5 V, all outputs open.
3. V_P = 3.3 V, all outputs open.
4. V_p = 6.0 V, all outputs open.
5. AC coupling, F_{IN} measured with a 1000 pF capacitor.
6. Source current flows out of the pin and sink current flows into the pin.

Figure 8. Typical External Charge Pump Circuit

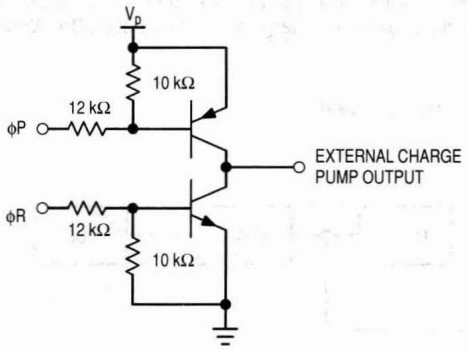


Figure 9. Typical Lock Detect Circuit

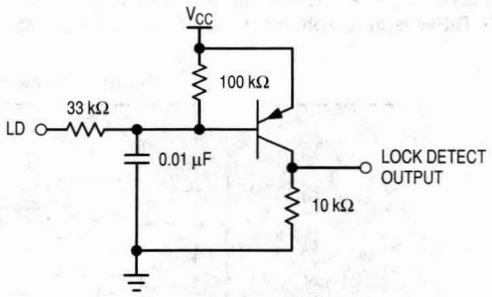
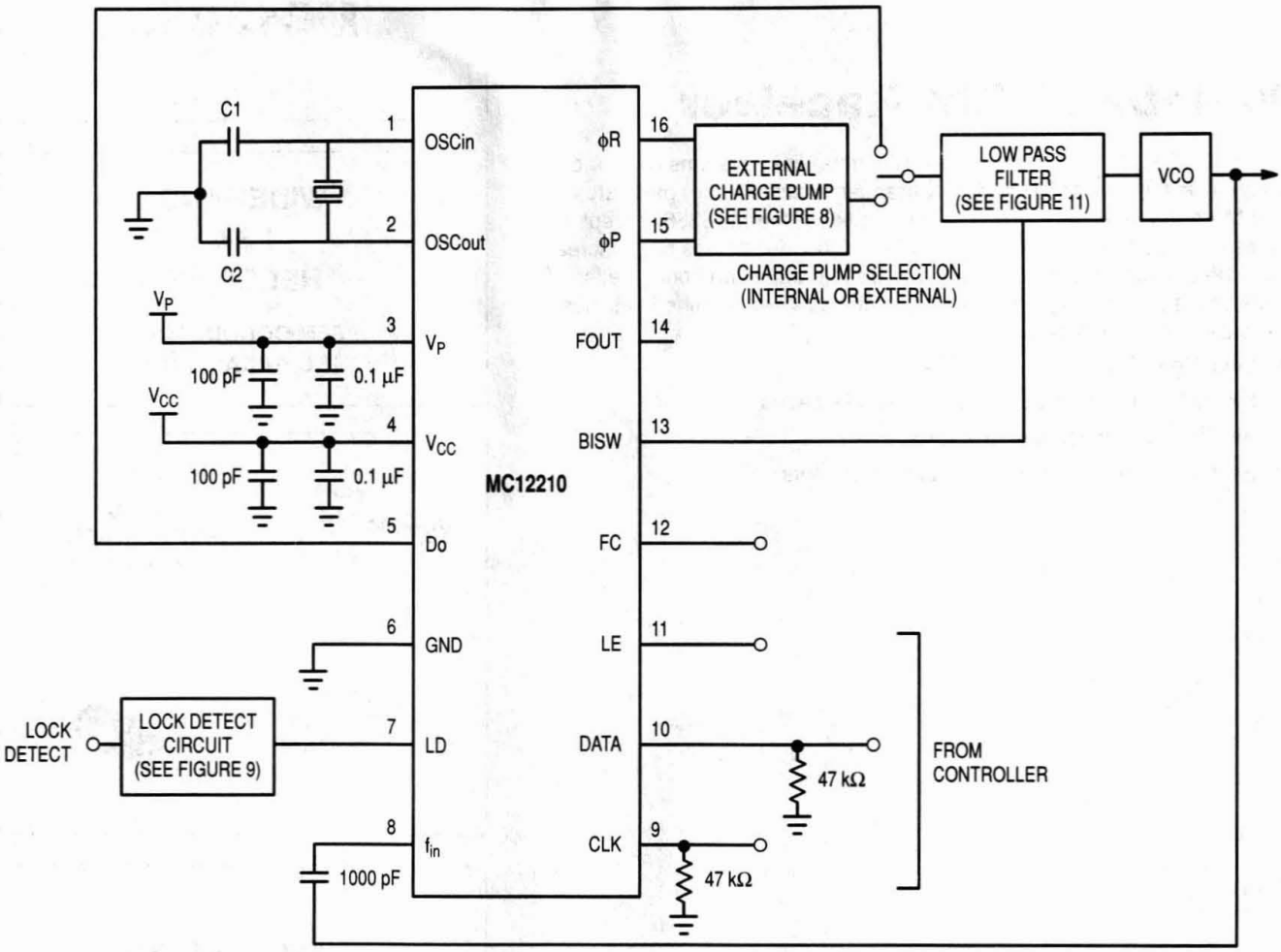
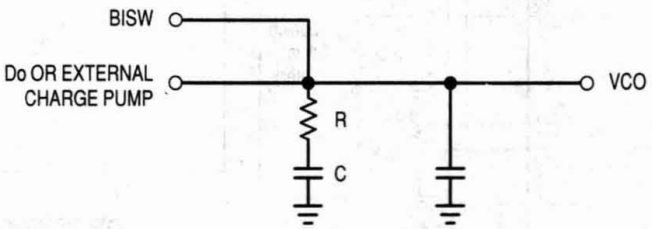


Figure 10. Typical Applications Example (16–Pin Package)



C1, C2: Dependent on Crystal Oscillator

Figure 11. Typical Loop Filter



MOTOROLA

MC13055

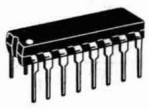
Wideband FSK Receiver

The MC13055 is intended fo RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0 M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

- Input Sensitivity 20 μV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

WIDEBAND FSK RECEIVER

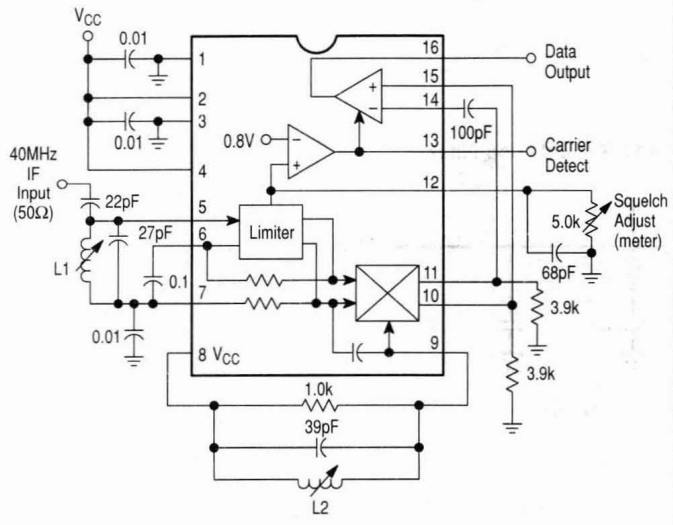
SEMICONDUCTOR TECHNICAL DATA



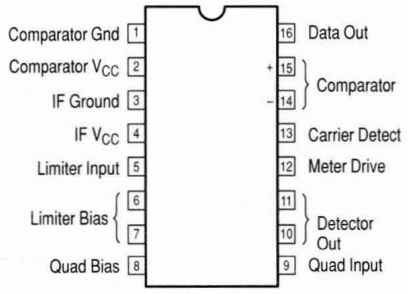
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Figure 1. Block Diagram and Application Circuit



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13055D	T_A = – 40 to +85°C	SO–16
MC13055P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, test circuit of Figure 2.)

Characteristic		Conditions	Min	Typ	Max	Unit
Total Drain Current		12 + 14	–	20	25	mA
Data Comparator Pull–Down Current		I16	–	10	–	mA
Meter Drive Slope versus Input		I12	4.5	7.0	9.0	μA/dB
Carrier Detect Pull–Down Current		I13	–	1.3	–	mA
Carrier Detect Pull–Up Current		I13	–	500	–	μA
Carrier Detect Threshold Voltage		V12	690	800	1010	mV
DC Output Current		I10, I11	–	430	–	μA
Recovered Signal		V10 – V11	–	350	–	mVrms
Sensitivity for 20 dB S + N/N, BW = 5.0 MHz		VIN	–	20	–	μVrms
S + N/N at V_{in} = 50 μV		V10 – V11	–	30	–	dB
Input Impedance @ 40 MHz	R_{in} C_{in}	Pin 5, Ground	– –	4.2 4.5	– –	kΩ pF
Quadrature Coil Loading	R_{in} C_{in}	Pin 9 to 8	– –	7.6 5.2	– –	kΩ pF

Figure 2. Test Circuit

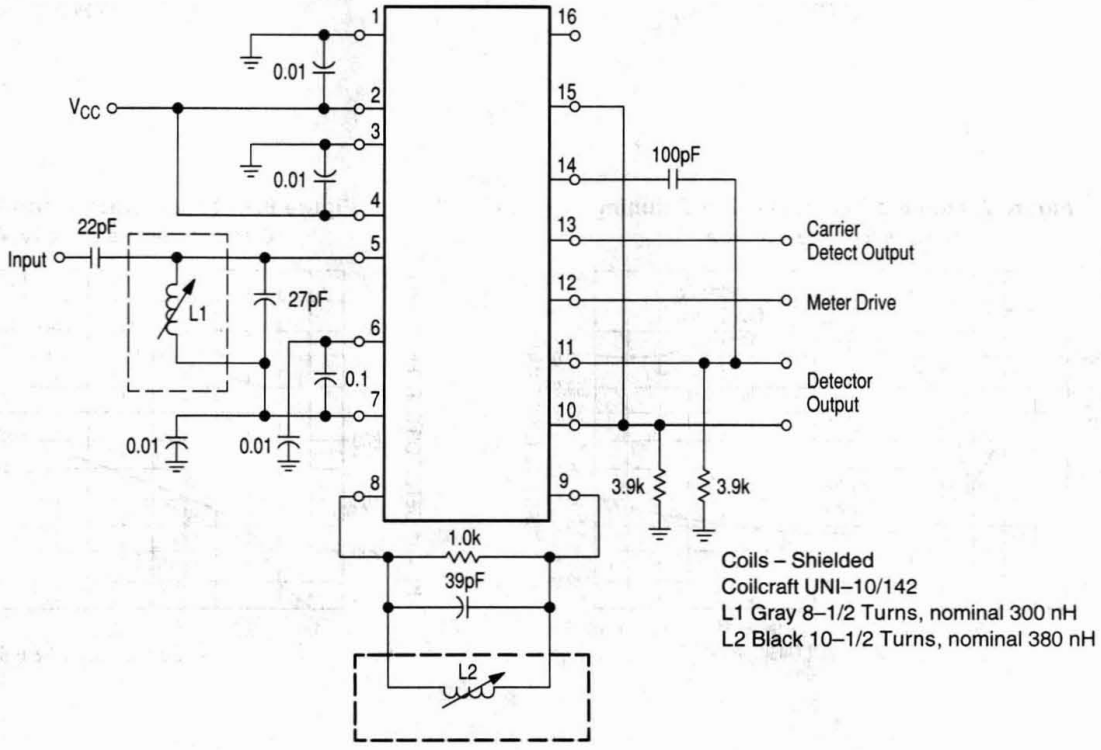


Figure 3. Overall Gain, Noise, AM Rejection

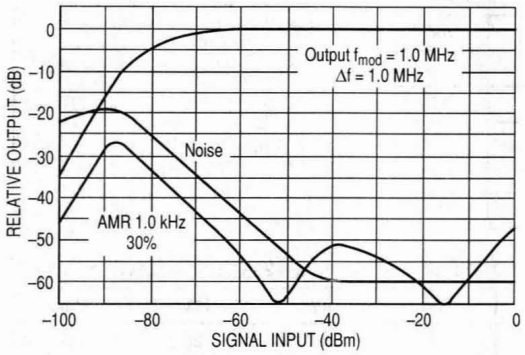


Figure 4. Meter Current versus Signal

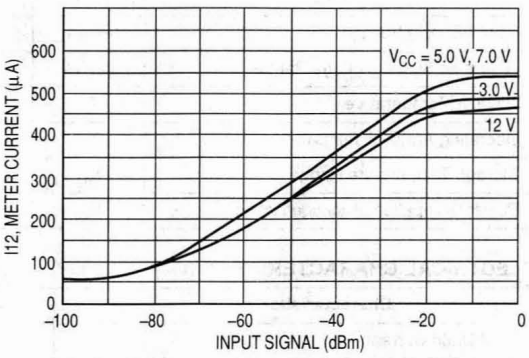


Figure 5. Untuned Input: Limiting Sensitivity versus Frequency

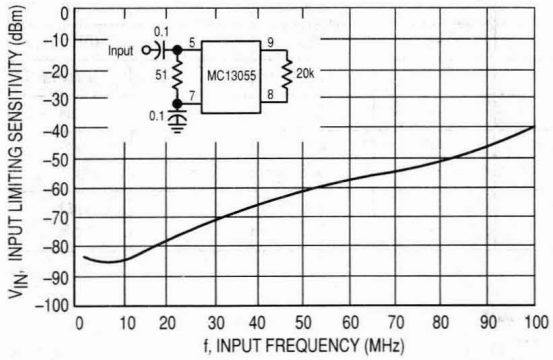


Figure 6. Untuned Input: Meter Current versus Frequency

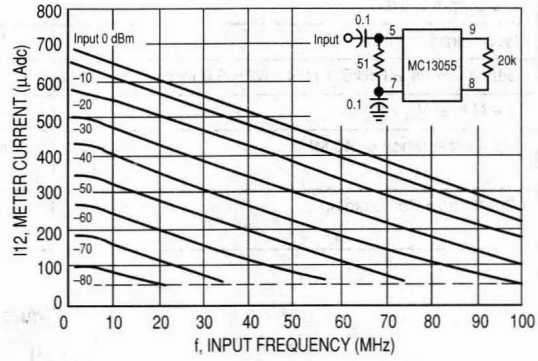


Figure 7. Limiting Sensitivity and Detuning versus Supply Voltage

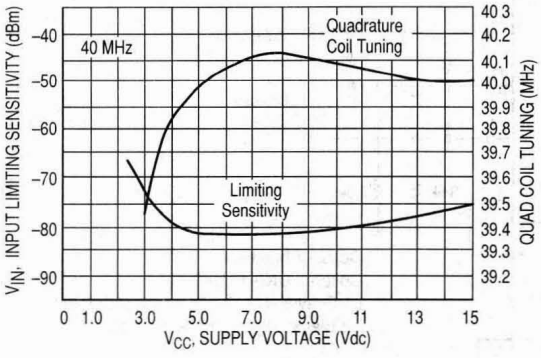


Figure 8. Detector Current and Power Supply Current versus Supply Voltage

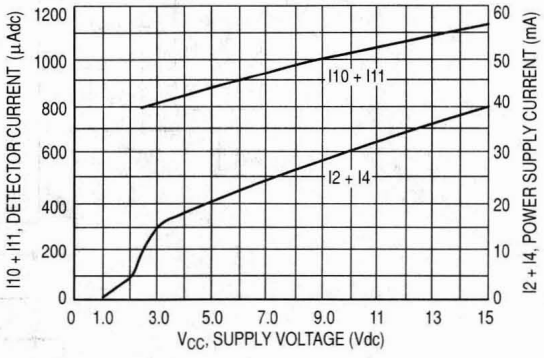


Figure 9. Recovered Audio versus Temperature

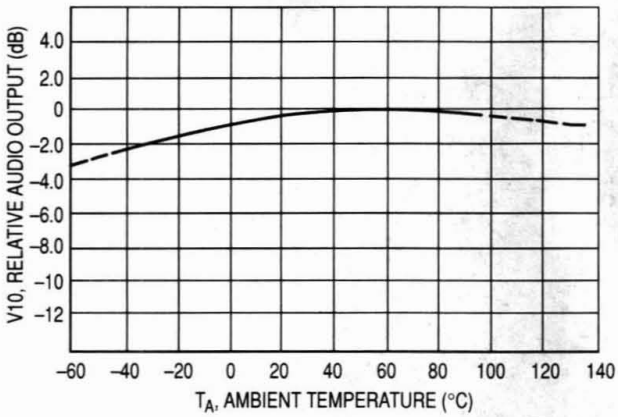


Figure 10. Carrier Detect Threshold versus Temperature

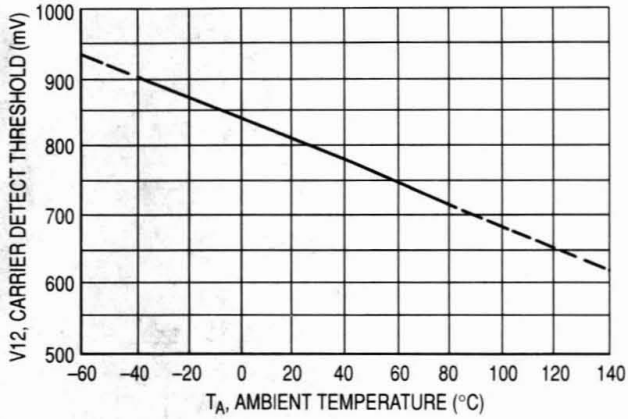


Figure 11. Meter Current versus Temperature

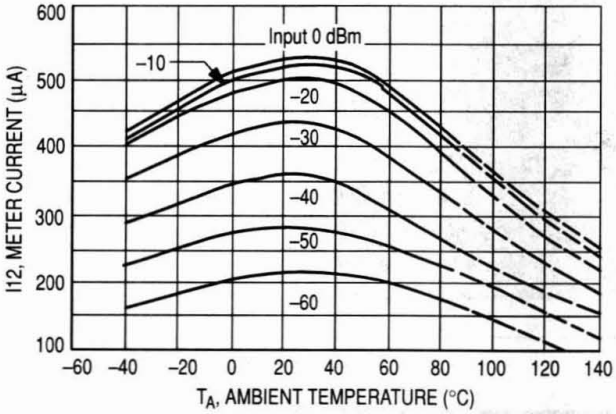


Figure 12. Input Limiting versus Temperature

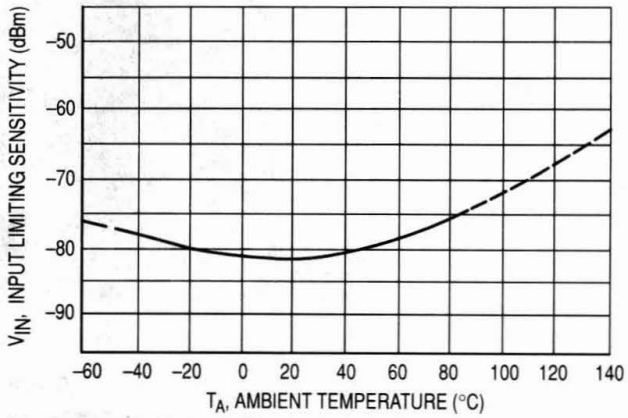


Figure 13. Input Impedance, Pin 5

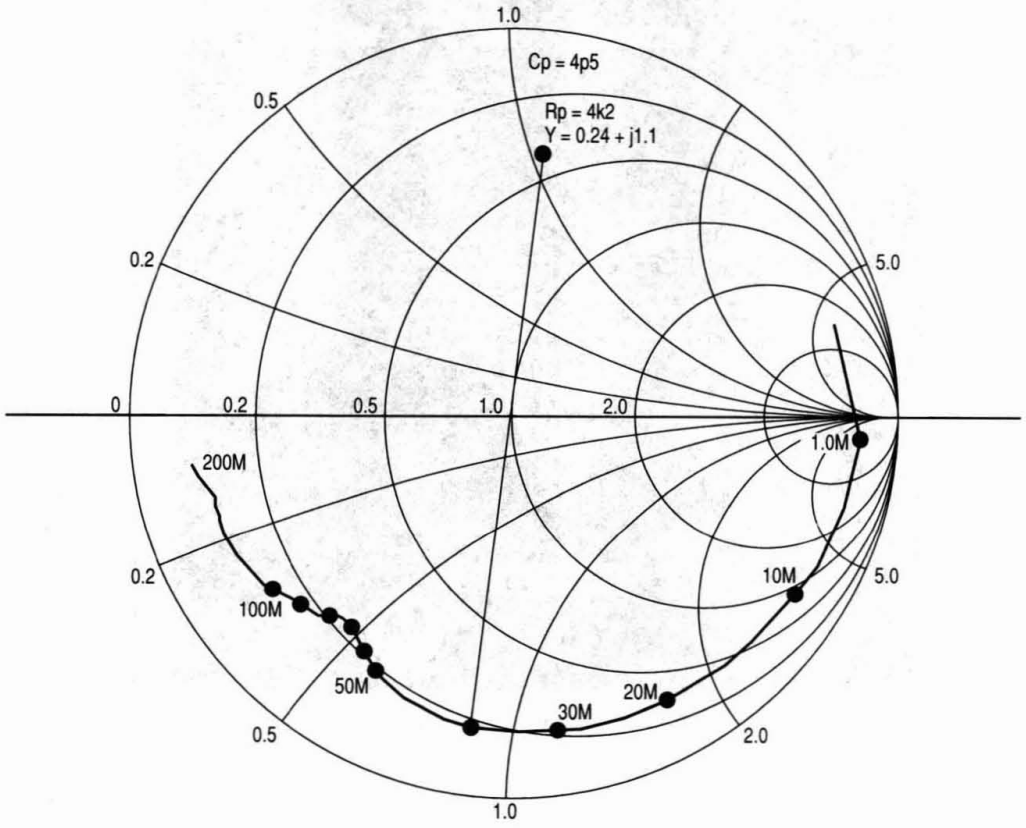
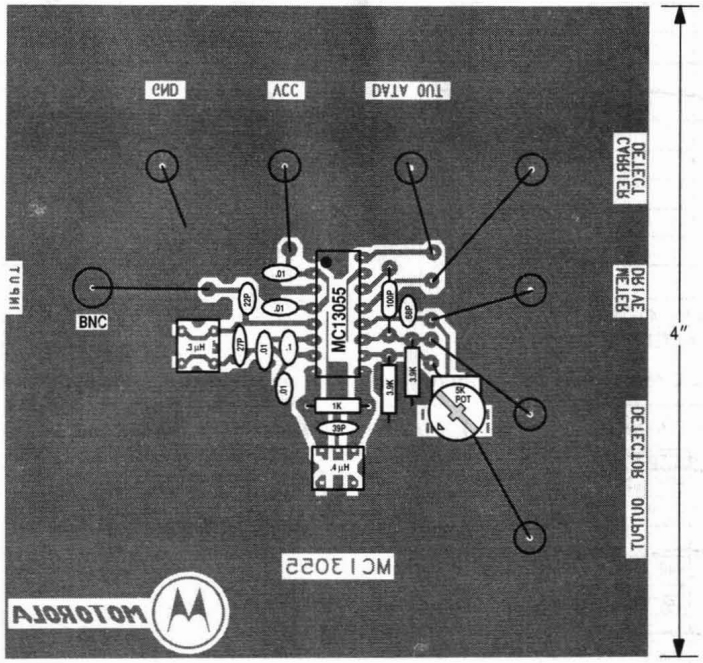
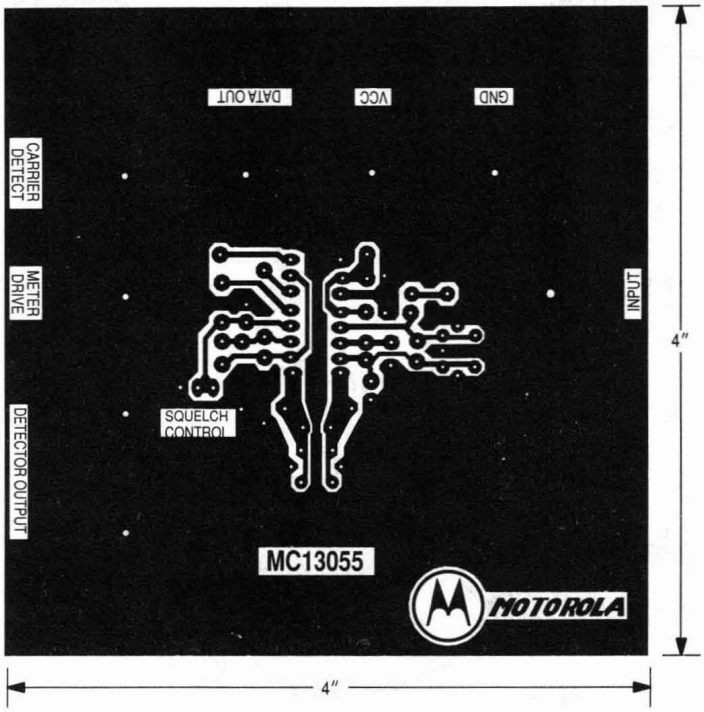


Figure 14. Test Fixture
(Component Layout)



(Circuit Side View)



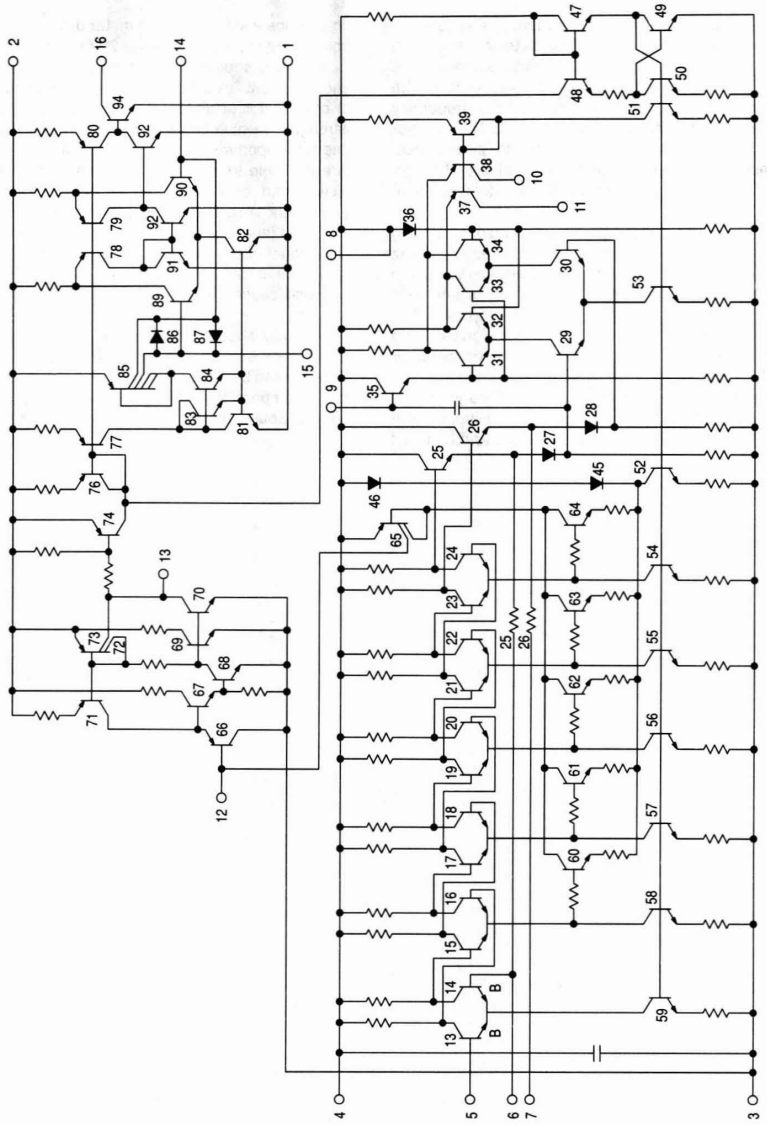


Figure 15. Internal Schematic

GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open–collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent DC level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor (R) from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or noninverted form.

MOTOROLA

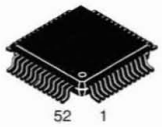
MC13109

Universal Cordless Telephone Subsystem IC

UNIVERSAL CT–1 SUBSYSTEM INTEGRATED CIRCUIT

The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices
- AN1575: Refer to Application Note for a List of "Worldwide Cordless Telephone Frequencies" (Chapter 8 Addendum of DL128 Data Book)



FB SUFFIX
PLASTIC PACKAGE
CASE 848B
(QFP–52)

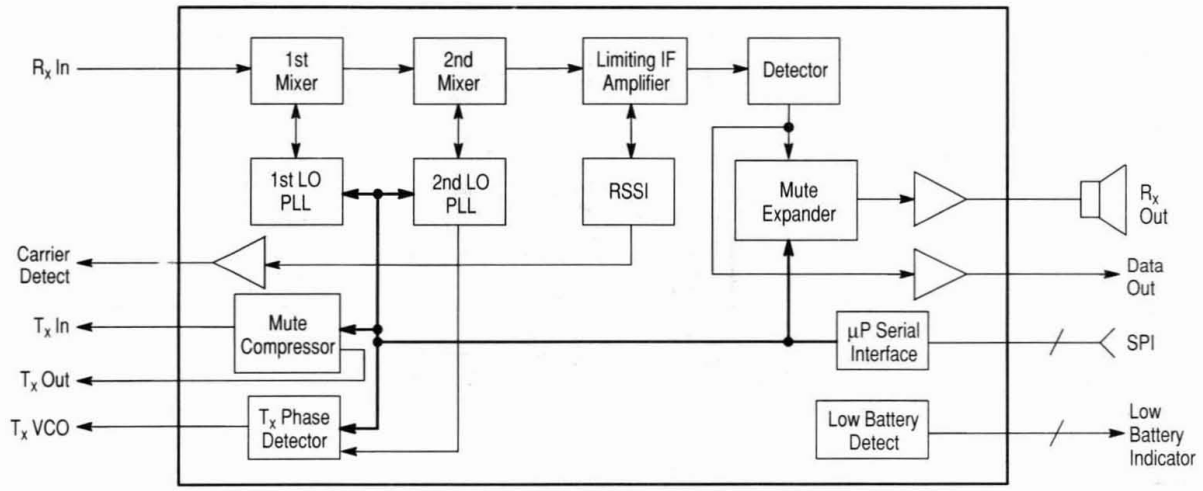
FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(Thin QFP)

Not Recommended For New Designs "A" Version Upcoming

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13109FB	T_A = –20° to +85°C	QFP–52
MC13109FTA		TQFP–48

Simplified Block Diagram



This device contains 6,609 active transistors.

Figure 1. MC13109FB Test Circuit

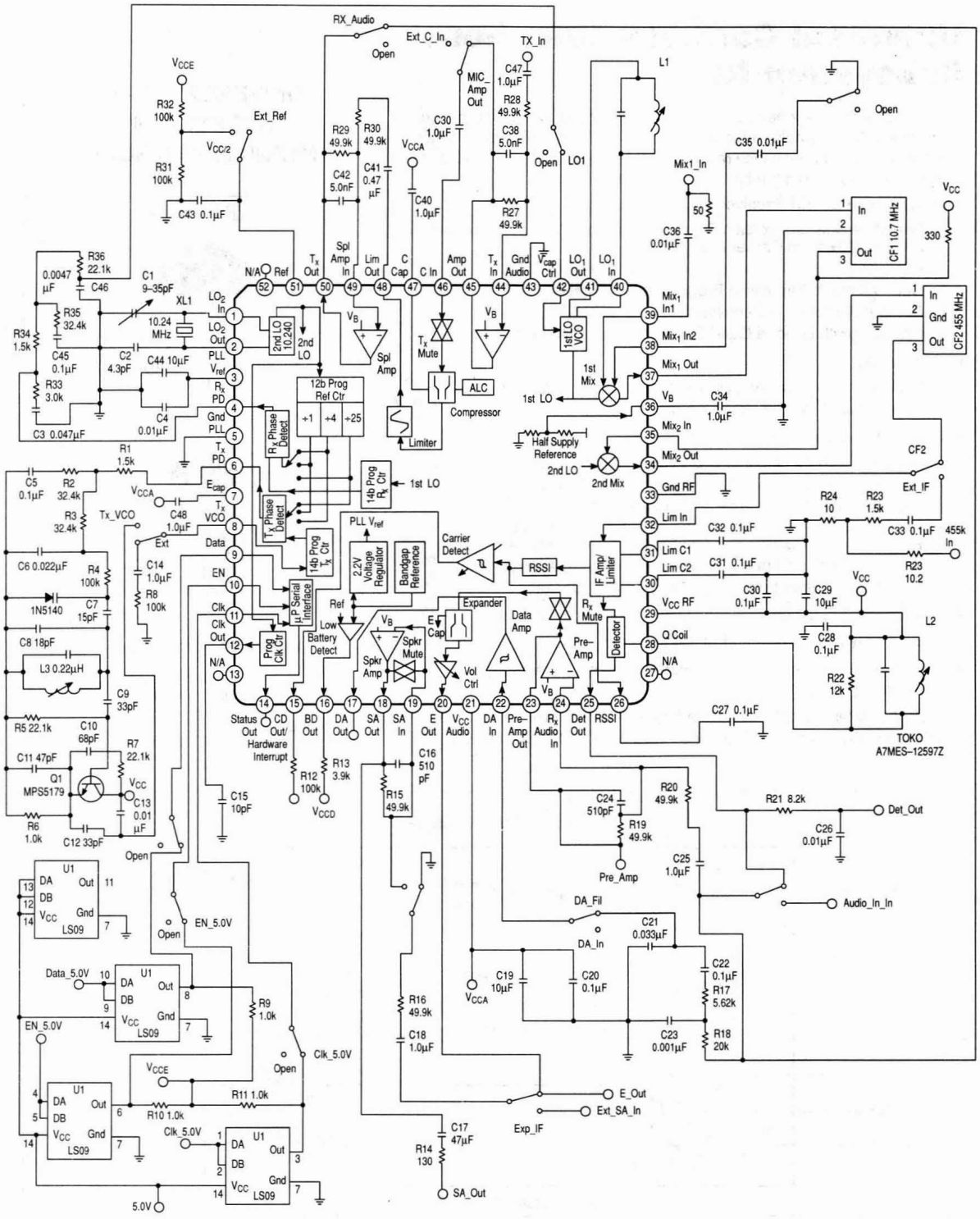
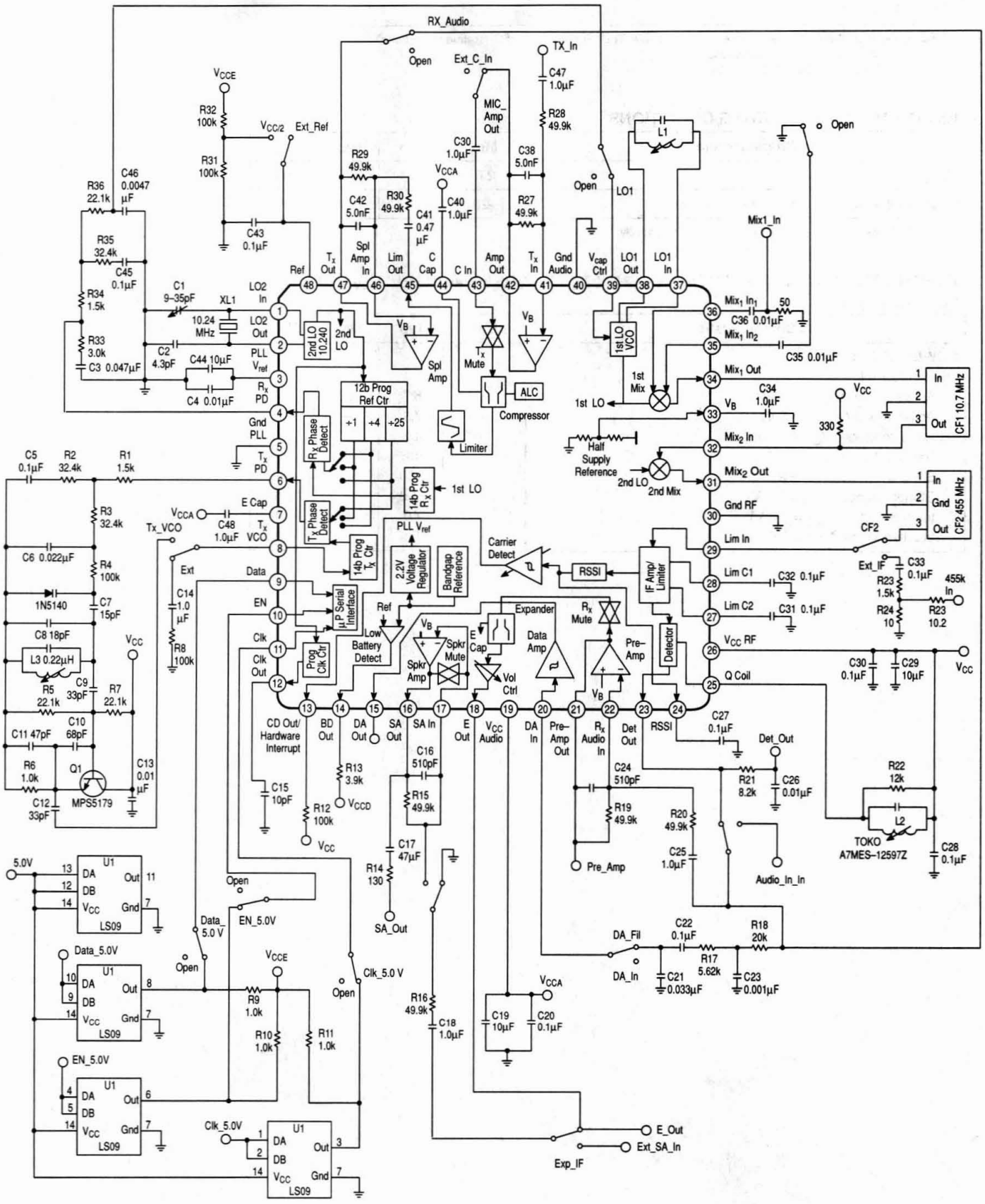


Figure 2. MC13109FTA Test Circuit



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +5.5	Vdc
Junction Temperature	T_J	−65 to +150	°C

NOTE: 1. Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Min	Typ	Max	Unit
V_{CC}	2.0	–	5.5	Vdc
Operating Ambient Temperature	–20	–	85	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C, RF In = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz; Test Circuit Figure 1.)

Characteristic	Min	Typ	Max	Unit
POWER SUPPLY				
Static Current				
Active Mode (V_{CC} = 2.6 V)	–	6.7	12	mA
Active Mode (V_{CC} = 3.6 V)	–	7.1	–	mA
Receive Mode (V_{CC} = 2.6 V)	–	4.3	7.0	mA
Receive Mode (V_{CC} = 3.6 V)	–	4.5	–	mA
Standby Mode (V_{CC} = 2.6 V)	–	300	600	µA
Standby Mode (V_{CC} = 3.6 V)	–	600	–	µA
Inactive Mode (V_{CC} = 2.6 V)	–	40	80	µA
Inactive Mode (V_{CC} = 3.6 V)	–	56	–	µA

ELECTRICAL CHARACTERISTICS (continued)

FM Receiver

The FM receivers can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25 channel U.S., without the need for any external switching circuitry (see Figure 29).

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_O = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Sensitivity (Input for 12 dB SINAD)	Matched Impedance Differential Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	–	0.7	–	µVrms
1st Mixer Conversion Gain	V_{in} = 1.0 mVrms, with CF_1 Load	Mix_1 $In_{1/2}$	CF_1	MX_{gain1}	–	10	–	dB
2nd Mixer Conversion Gain	V_{in} = 3.0 mVrms, with CF_2 Load	Mix_2 In	CF_2	MX_{gain2}	–	20	–	dB
1st and 2nd Mixer Gain Total	V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load	Mix_1 $In_{1/2}$	CF_2	MX_{gainT}	24	30	–	dB
1st Mixer Input Impedance	–	–	Mix_1 In_1 Mix_1 In_2	Z_{in1}	–	1.0	–	kΩ
2nd Mixer Input Impedance	–	–	Mix_2 In	Z_{in2}	–	3.0	–	kΩ
1st Mixer Output Impedance	–	–	Mix_1 Out	Z_{out1}	–	330	–	Ω
2nd Mixer Output Impedance	–	–	Mix_2 Out	Z_{out2}	–	1.5	–	kΩ
IF –3.0 dB Limiting Sensitivity	f_{in} = 455 kHz	Lim In	Det Out	IF Sens	–	55	–	µVrms
Total Harmonic Distortion (CCITT Filter)	With R_C = 8.2 kΩ/ 0.01 µF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	THD	–	0.7	–	%
Recovered Audio	With R_C = 8.2 kΩ/ 0.01 µF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	AFO	80	100	154	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.01 µF	Mix_1 $In_{1/2}$	Det Out	SN	–	49	–	dB
AM Rejection Ratio	30% AM, V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.001 µF	Mix_1 $In_{1/2}$	Det Out	AMR	–	37	–	dB
First Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_1 $In_{1/2}$	Mix_1 Out	TOI_{mix1}	–	–10	–	dBm
Second Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_2 In	Mix_2 Out	TOI_{mix2}	–	–27	–	dBm
Detector Output Impedance	–	–	Det Out	Z_O	–	870	–	Ω

ELECTRICAL CHARACTERISTICS (continued)

RSSI/Carrier Detect

Connect 0.01 µF to Gnd from "RSSI" output pin to form the carrier detect filter. "CD Out" is an open collector output which requires an external 100 kΩ pull–up resistor to V_{CC}. The carrier detect threshold is programmable through the MPU interface.

(R_L = 100 kΩ, V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI Output Current Dynamic Range	–	Mix_1 In	RSSI	RSSI	–	65	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix_1 In	CD Out	V_T	–	22.5	–	µVrms
Hysteresis	–	Mix1 In	CD Out	Hys	–	2.0	–	dB
Output High Voltage	V_{in} = 0 µVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{in} = 100 µVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OL}	–	0.01	0.4	V
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	V_{Trange}	–20	–	11	dB
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	V_{Tn}	–	32	–	–

Data Amp Comparator (see Figure 4)

Inverting hysteresis comparator. Open collector output with internal 100 kΩ pull–up resistor. A band pass filter is connected between the "Det Out" pin and the "DA In" pin with component values as shown in the attached block diagram. The "DA In" input signal is ac coupled.

(V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	V_{CC} – 0.9	V_{CC} – 0.7	V_{CC} – 0.5	V
Input Impedance	–	–	DA In	Z_I	–	11	–	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage	V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	DA In	DA Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	DA In	DA Out	V_{OL}	–	0.03	0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Pre–Amplifier/Expander/R_x Mute/Volume Control (See Figure 4)

The Pre–Amplifier is an inverting rail–to–rail output swing operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The expander analog ground is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The volume control can be adjusted through the MPU interface. The "R_x Audio In" input signal is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, Set External Pre–Amplifier R's for Gain of 1, Volume Control = (0111).)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Pre–Amp Open Loop Gain	–	R_x Audio In	Pre–Amp	A_{VOL}	–	60	–	dB
Pre–Amp Gain Bandwidth	–	R_x Audio In	Pre–Amp	GBW	–	100	–	kHz
Pre–Amp Maximum Output Swing	R_L = 10 kΩ	R_x Audio In	Pre–Amp	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}
Expander 0 dB Gain Level	V_{in} = –10 dBV	R_x Audio In	E Out	G	–3.0	–0.11	3.0	dB
Expander Gain Tracking	V_{in} = –20 dBV, Output Relative to G V_{in} = –30 dBV, Output Relative to G	R_x Audio In	E Out	G_t	–21 –42	–19.65 –39.42	–19 –37	dB
Total Harmonic Distortion	V_{in} = –10 dBV	R_x Audio In	E Out	THD	–	0.5	–	%
Maximum Output Voltage	Increase input voltage until output voltage THD = 5%, then measure output voltage. R_L = 10 kΩ	R_x Audio In	E Out	V_{Omax}	–	–5.0	–	dBV
Attack Time	E_{cap} = 1.0 µF, R_{filt} = 20 kΩ (See Appendix B)	R_x Audio In	E Out	t_a	–	3.0	–	ms
Release Time	E_{cap} = 1.0 µF, R_{filt} = 20 kΩ (See Appendix B)	R_x Audio In	E Out	t_r	–	13.5	–	ms
Compressor to Expander Crosstalk	V (R_x Audio In) = 0 Vrms, V_{in} = –10 dBV	C In	E Out	C_T	–	–	–70	dB
R_x Mute	V_{in} = –10 dBV No popping detectable during R_x Mute transitions	R_x Audio In	E Out	M_e	–	–70	–	dB
Volume Control Range	Programmable through MPU Interface	–	–	V_{Crange}	–14	–	16	dB
Volume Control Steps	Programmable through MPU Interface	–	–	V_{Cn}	–	16	–	–

ELECTRICAL CHARACTERISTICS (continued)

Speaker Amplifier/SP Mute

The Speaker Amplifier is an inverting rail–to–rail operational amplifier. The non–inverting input terminal is connected to the internal V_B half supply reference. External resistors and capacitors are used to set the gain and frequency response. The "SA In" input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Maximum Output Swing	V_{CC} = 2.3 V, R_L = 130 Ω V_{CC} = 2.3 V, R_L = 600 Ω V_{CC} = 3.4 V, R_L = 600 Ω	SA In	SA Out	V_{Omax}	– – –	0.8 2.0 3.0	– – –	V_{pp}
SP Mute	V_{in} = –20 dBV R_L = 130 Ω No popping detectable during SP Mute transitions	SA In	SA Out	M_{sp}	–	–70	–	dB

Mic Amplifier (See Figure 6)

The Mic Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors are connected to set the gain and frequency response. The "T_x In" input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	T_x In	Amp Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	T_x In	Amp Out	G_{BW}	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	T_x In	Amp Out	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}

ELECTRICAL CHARACTERISTICS (continued)

Compressor/ALC/T_x Mute/Limiter (See Figure 5)

The compressor analog gound is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The "C In" input is ac coupled. The ALC (Automatic Level Control) provides a soft limit to the output signal swing as the input voltage increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface.

(Test Conditions: V_{CC} = 2.6 V, f_{in} = 1.0 kHz, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Compressor 0 dB Gain Level	V_{in} = –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	G	–3.0	–0.17	3.0	dB
Compressor Gain Tracking	V_{in} = –30 dBV, Output Relative to G V_{in} = –50 dBV, Output Relative to G	C In	Lim Out	G_t	–11 –23	–10.23 –20.23	–9.0 –17	dB
Maximum Compressor Gain	V_{in} –70 dBV	C In	Lim Out	A_{Vmax}	–	30	–	dB
Total Harmonic Distortion	V_{in} –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	THD	–	0.5	–	%
Input Impedance	–	C In	Lim Out	Z_{in}	–	16	–	kΩ
Attack Time	C_{cap} = 1.0 µF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_a	–	3.0	–	ms
Release Time	C_{cap} = 1.0 µF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_r	–	13.5	–	ms
Expander to Compressor Crosstalk	V (C In) = 0 Vrms, V_{in} = –10 dBV	R_x Audio In	Lim Out	C_T	–	–	–40	dB
T_x Data Mute	V_{in} = –10 dBV, ALC disabled No popping detectable during R_x Mute transitions	C In	Lim Out	M_e	–	–70	–	dB
ALC Dynamic Range	–	C In	Lim Out	DR	–24	–	–2.5	dBV
ALC Output Level	V_{in} = –18 dBV V_{in} = –2.5 dBV	C In	Lim Out	ALC_{out}	– –	–16 –12	– –	dBV
Limiter Output Level	ALC disabled	C In	T_x Out	V_{lim}	–	0.8	–	V_{pp}

ELECTRICAL CHARACTERISTICS (continued)

Splatter Amplifier (see Figure 7)

The Splatter Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The "Spl Amp In" input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	Spl Amp In	T_x Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	Spl Amp In	T_x Out	GBW	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	Spl Amp In	T_x Out	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}

T_x Audio Path Recommendation

The recommended configuration for the T_x Audio path includes setting the Microphone Amplifier gain to 16 dB using the external gain setting resistors and setting the Splatter Amplifier gain to 9.0 dB using the external gain setting resistors. With these gain values, the total T_x Path transfer characteristic is shown in Figure 7.

PLL Voltage Regulator

The PLL supply voltage is regulated to a nominal of 2.2 V. The "V_{CC} Audio" pin is the supply voltage for the internal voltage regulator. The "PLL V_{ref}" pin is the 2.2 V regulated output voltage. Two capacitors with 10 µF and 0.01 µF values must be connected to the "PLL V_{ref}" pin to filter and stabilize this regulated voltage. The voltage regulator provides power for the 2nd LO, R_x and T_x PLL's, and MPU Interface. The voltage regulator can also be used to provide a regulated supply voltage for external IC's. R_x and T_x PLL loop performance are independent of the power supply voltage when the voltage regulator is used. The voltage regulator requires about 200 mV of "headroom". When the power supply decreases to within about 200 mV of the output voltage, the regulator will go out of regulation but the output voltage will not turn off. Instead, the output voltage will maintain about a 200 mV delta to the power supply voltage as the power supply voltage continues to decrease. The "PLL V_{ref}" pin can be connected to "V_{CC} Audio" by the external wiring if voltage higher than 2.2 V is required. But it should not be connected to other supply except "V_{CC} Audio". The voltage regulator is "on" in the Active and R_x modes. In the Standby and Inactive modes, the voltage regulator is turned off to reduce current drain and the "PLL V_{ref}" pin is internally connected to "V_{CC} Audio" (i.e., the supply voltage is maintained but is now unregulated).

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Output Voltge Level	V_{CC} = 2.6 V, O_L = 0 mA	–	V_{CC} PLL	V_{out}	1.9	2.2	2.5	V
Line Regulation	I_L = 0 mA, V_{CC} = 2.6 to 5.5 V	V_{CC}	V_{CC} PLL	Reg_{line}	–	1.43	40	mV
Load Regulation	V_{CC} = 2.6 V, I_L = 0 to 1.0 mA	V_{CC}	V_{CC} PLL	Reg_{load}	–	–1.86	40	mV
Drop–Out Voltage	I_L = 0 mA	–	–	DO	–	–	V_{out} + 200	mV

ELECTRICAL CHARACTERISTICS (continued)

Low Battery Detect

An external resistor divider is connected to the "Ref" input pin to set the threshold for the low battery detect. The voltage at the "Ref" input pin is compared to an internal 1.23 V Bandgap reference voltage. The "BD Out" pin is open collector and requires and external pull–up resistor to V_{CC}.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Average Threshold Voltage	Take average of rising and falling threshold	Ref	Ref/ BD Out	Threshold	–	1.23	–	V
Hysteresis	–	Ref	Ref/ BD Out	Hys	–	4.0	–	mV
Input Current	V_{in} = 1.6 V	–	Ref	I_{in}	–50	5.71	+50	nA
Output High Voltage	V_{ref} = 1.6, R_L = 3.9 kΩ	Ref	BD Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{ref} = 0.9, R_L = 3.9 kΩ	Ref	BD Out	V_{OL}	–	0.12	0.4	V

Figure 3. Data Amp Operation

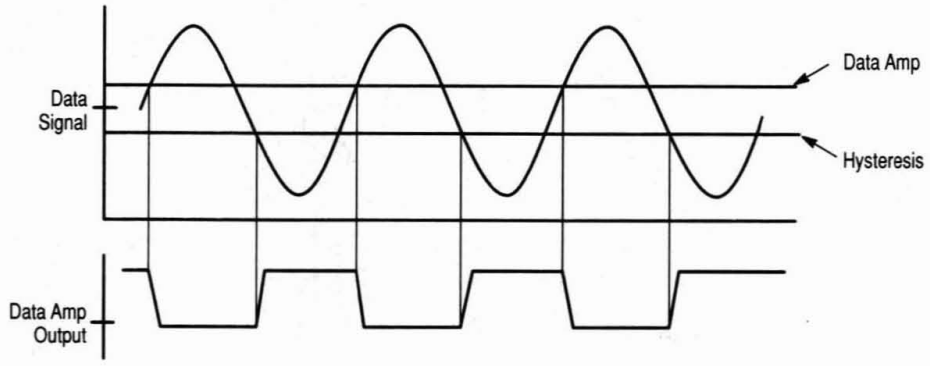


Figure 4. Typical Expander Response

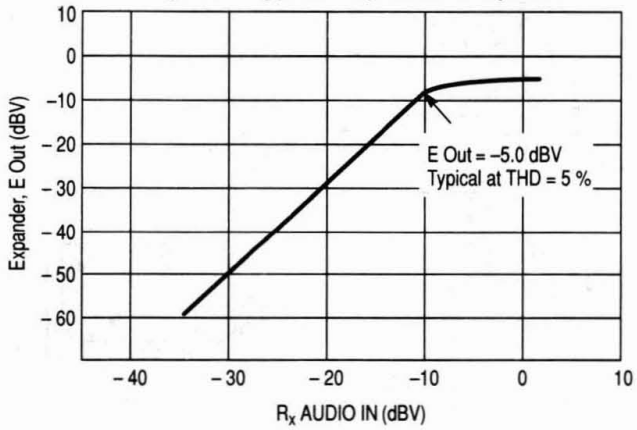


Figure 5. Typical Compressor/ALC/Limiter Response

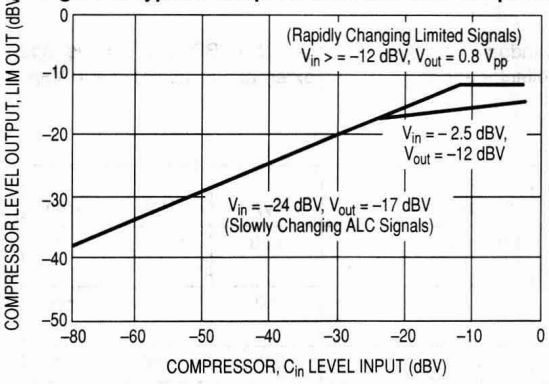


Figure 6. Total T_x Path, Mic Amp Gain = 16 dB, Splatter Amp Gain = 9.0 dB

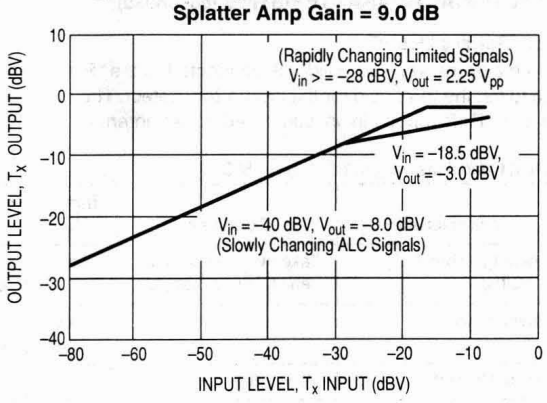
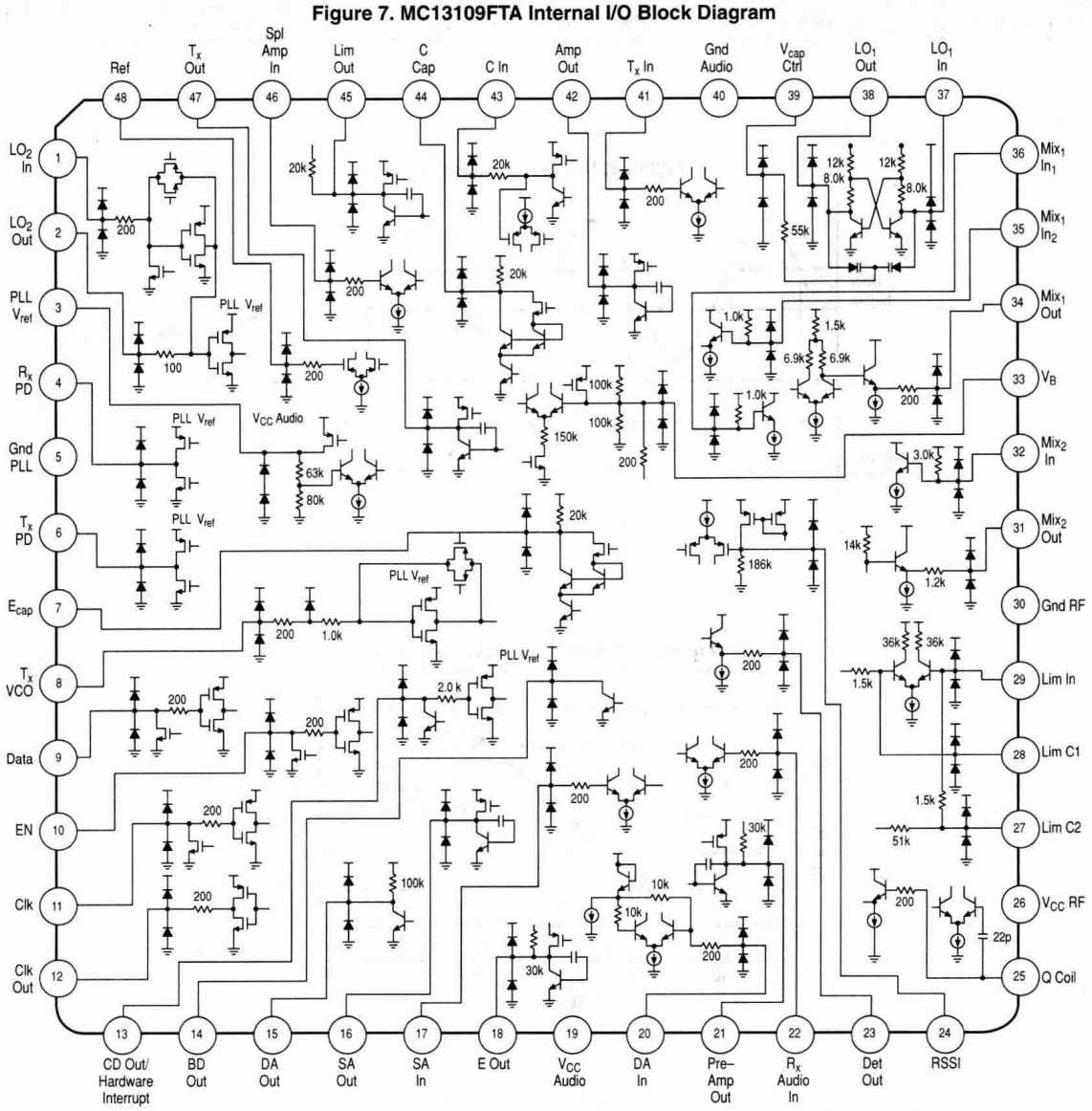


Figure 7. MC13109FTA Internal I/O Block Diagram



PIN FUNCTION DESCRIPTION

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
1 2	1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver.
3	3	PLL V_{ref}	Supply	Voltage Regulator output pin. The internal voltage regulator provides a stable power supply voltage for the R_x and T_x PLL's and can also be used as a regulated supply voltage for the other IC's.
4	4	R_x PD	Output	Three state voltage output of the R_x Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_x PLL loop filter. It is important to minimize the line length and capacitance of this pin.
5	5	Gnd PLL	Gnd	Ground pin for PLL section of IC.
6	6	T_x PD	Output	Three state voltage output of the T_x Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T_x PLL loop filter. It is important to minimize the line length and capacitance on this pin.
7	7	E Cap	–	Expander rectifier filter capacitor pin. Connect capacitor to V_{CC}.
8	8	T_x VCO	Input	Transmit divide counter input which is driven by an ac coupled external transmit loop VCO. The minimum signal level is 200 mV_{pp} @ 80.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	12	Clk Out	Output	Microprocesor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output whch can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
N/A	14	Status Out	Output	This pin indicates when the internal latches may have lost memory due to a power glitch.
13	15	CD Out/ Hardware Interrupt	Output/ Input	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from Inactive Mode.
14	16	BD Out	Output	Low battery detect output (open collector with external pull–up resistor).
15	17	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
16	18	SA Out	Output	Speaker amplifier output.
17	19	SA In	Input	Speaker amplifier input (ac coupled).
18	20	E Out	Output	Expander output.
19	21	V_{CC} Audio	Supply	V_{CC} supply for audio section.
20	22	DA In	Input	Data amplifier input (ac coupled).
21	23	Pre–Amp Out	Output	Pre–amplifier output for connection of pre–amplifier feedback resistor.
22	24	R_x Audio In	Input	R_x audio input to pre–amplifier (ac coupled).
23	25	Det Out	Output	Audio output from FM detector.
24	26	RSSI	–	Receive signal strength indicator filter capacitor.
N/A	27	N/A	–	Note used.
25	28	Q Coil	–	A quad coil or ceramic discriminator are connected to this pin.
26	29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
27 28	30 31	Lim C2 Lim C1	–	IF amplifier/limiter capacitor pins.

PIN FUNCTION DESCRIPTION (continued)

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
29	32	Lim In	Input	Signal input for IF amplifier/limiter.
30	33	Gnd RF	Gnd	Ground pin for RF section of the IC.
31	34	Mix_2 Out	Output	Second mixer output.
32	35	Mix_2 In	Input	Second mixer input.
33	36	V_B	–	Internal half supply analog ground reference.
34	37	Mix_1 Out	Output	First mixer output.
35	38	Mix_1 In_2	Input	Negative polarity first mixer input.
36	39	Mix_1 In_1	Input	Positive polarity first mixer input.
37 38	40 41	LO_1 In LO_1 Out	–	Tank elements for 1st LO multivibrator oscillator are connected to these pins.
39	42	V_{cap} Ctrl	–	1st LO varactor control pin.
40	43	Gnd Audio	Gnd	Ground for audio section of the IC.
41	44	T_x In	Input	T_x path input to Microphone Amplifier (ac coupled).
42	45	Amp Out	Output	Microphone amplifier output.
43	46	C In	Input	Compressor input (ac coupled).
44	47	C Cap	–	Compressor rectifier filter capacitor pin. Connect capacitor to V_{CC}.
45	48	Lim Out	Output	T_x path limiter output.
46	49	Spl Amp In	Input	Splatter amplifier input (ac coupled).
47	50	T_x Out	Output	T_x path audio output.
48	51	Ref	Input	Reference voltage input for low battery detect.
N/A	52	N/A	–	Not used.

Power Supply Voltage

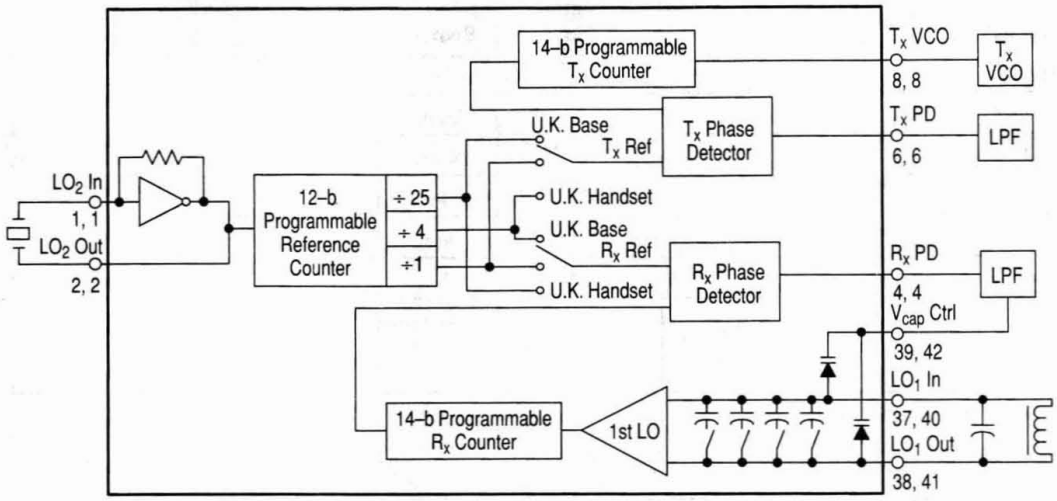
This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on two ro three NiCad cells or on 5.0 V power.

PLL Frequency Synthesizer General Description

Figure 8 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable thorugh the MCU serial interface and supports most country channel frequencies including USA (25 ch), France, Spain, Australia, Korea, New Zealand, U.K., Netherlands and China (see channel frequency tables in Appendix A).

The 2nd local oscillator and reference divider provide the reference frequency for the R_x and T_x PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_x and T_x reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U.K. The 14–bit T_x counter is programmed for the desired transmit channel frequency. The 14–bit R_x counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #6 and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

Figure 8. Dual PLL Simplified Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
PLL PIN DC						
Input Voltage Low	–	Data Clk EN Hardware Int.	V_{IL}	–	0.3	V
Input Voltage High	–	Data Clk EN	V_{IH}	"PLL V_{ref}" – 0.3	"V_{CC} Audio"	V
Input Current Low	V_{in} = 0.3 V	Data Clk EN	I_{IL}	–5.0	–	μA
Input Current High	V_{in} = (V_{CC} Audio) – 0.3	Data Clk EN	I_{IH}	–	5.0	μA
Hysteresis Voltage	–	Data Clk EN	V_{hys}	1.0	–	V
Output Current High	–	R_x PD T_x PD	I_{OH}	–	–0.7	mA
Output Current Low	–	R_x PD T_x PD	I_{OL}	0.7	–	mA
Output Voltage Low	I_{IL} = 0.7 mA	R_x PD T_x PD	V_{OL}	–	(PLL V_{ref})* 0.2	V
Output Voltage High	I_{IH} = –0. 7mA	R_x PD T_x PD	V_{OH}	(PLL V_{ref})* 0.8	–	V
Tri–State Leakage Current	V = 1.2 V	R_x PD T_x PD	I_{OZ}	–50	50	nA
Input Capacitance	–	Data Clk EN	C_{in}	–	8.0	pF
Output Capacitance	–	R_x PD T_x PD	C_{out}	–	8.0	pF

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
PLL PIN INTERFACE						
EN to Clk Setup Time	–	EN, Clk	t_{suEC}	200	–	ns
Data to Clk Setup Time	–	Data, Clk	t_{suDC}	100	–	ns
Hold Time	–	Data, Clk	t_h	90	–	ns
Recovery Time	–	EN, Clk	t_{rec}	90	–	ns
Input Pulse Width	–	EN, Clk	t_w	100	–	ns
Input Rise and Fall Time	–	Data Clk EN	t_r, t_f	– – –	9.0 – –	µs
MPU Interface Power–Up Delay	90% of PLL V_{ref} to Data, Clk, EN	–	t_{puMPU}	–	100	µs

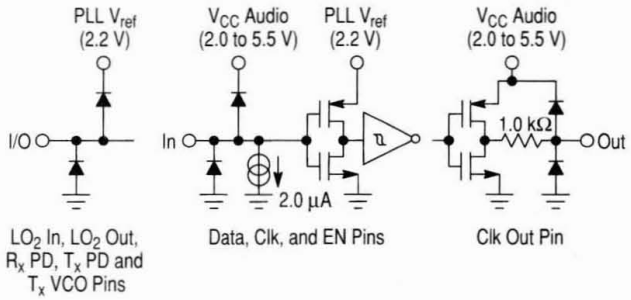
PLL LOOP

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
2nd LO Frequency	–	LO_2 In LO_2 Out	f_{LO}	–	12	MHz
"T_x VCO" Input Frequency	V_{in} = 200 mV_{pp}	T_x VCO	f_{txmax}	–	80	MHz

PLL I/O Pin Specifications

The 2nd LO, R_x and T_x PLL's and MPU serial interface are normally powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, R_x PD, T_x PD, T_x VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}". Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 9 shows a simplified schematic of the PLL I/O pins.

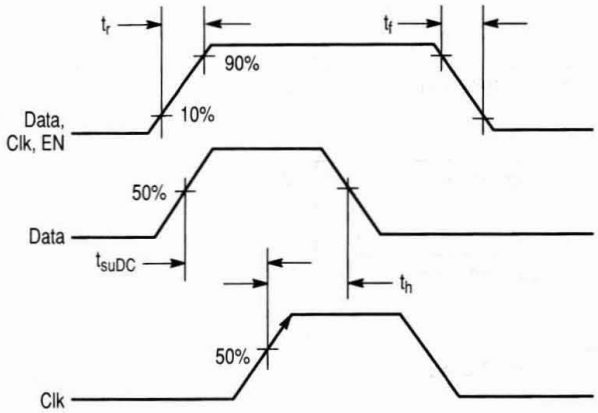
Figure 9. PLL I/O Pin Simplified Schematics



Microprocessor Serial Interface

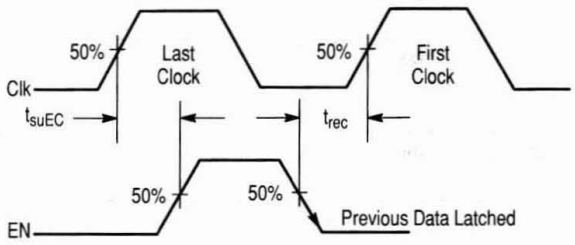
The "Data", "Clk", and "EN" pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counter and various control functions. The "Data" and "Clk" pins are used to load data into the shift register. Figure 10 shows "Data" and "Clk" pin timing. Data is clocked on positive clock transitions.

Figure 10. Data and Clock Timing Requirement



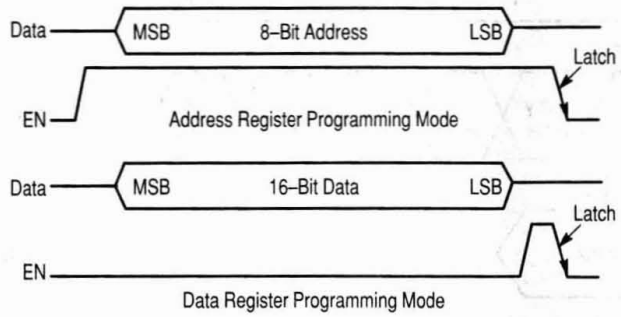
After data is loaded into the shift register, the data is latched into the appropriate latch register using the "EN" pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 11 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 11. Enable Timing Requirement



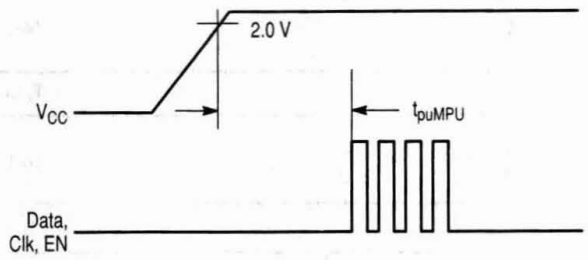
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 12 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when "EN" is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the "EN" high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 12. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 μs after the power supply has reached its minimum level during power–up (See Figure 13). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_x, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 13. Microprocessor Serial Interface Power–Up Delay



Status Out

This is a digital output which indicates whether the latch registers have been reset to their power–up default values. Latch power–up default values are given in Figure 32. If there is a power glitch or ESD event which causes the latch registers to be reset to their default values, the "Status Out" pin will indicate this to the MPU so it can reload the correct information into the latch registers.

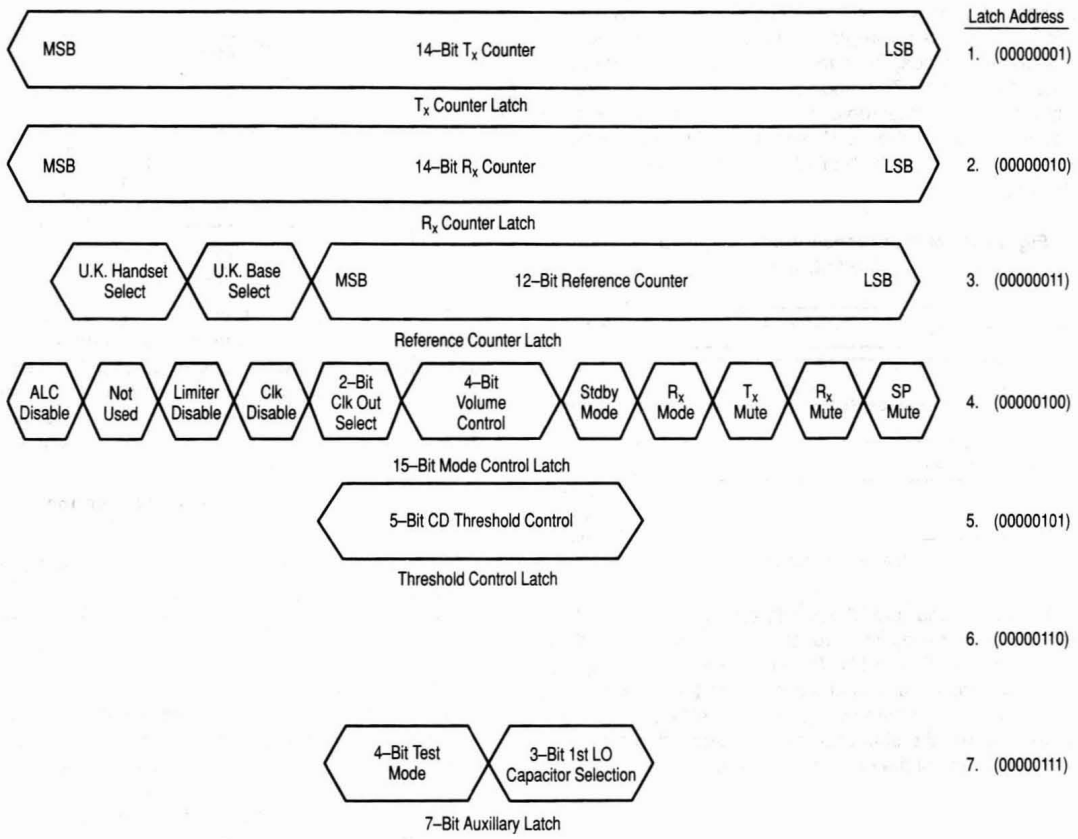
Figure 14. Status Out Operation

Status Latch Register Bits	Status Out Logic Level
Latch bits not at power–up default value	0
Latch bits at power–up default value	1

Data Registers

Figure 15 shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. "Don't care" bits can be loaded into the shift register first if 8–bit bytes of data are loaded.

Figure 15. Microprocessor Interface Data Latch Registers



Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 16 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries.

Figure 16. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency
10.24 MHz	2048	1	5.0 kHz
10.24 MHz	1024	4	2.5 kHz
11.15 MHz	2230	1	5.0 kHz
12.00 MHz	2400	1	5.0 kHz
11.15 MHz	1784	1	6.25 kHz
11.15 MHz	446	4	6.25 kHz
11.15 MHz	446	25	1.0 kHz

Reference Counter

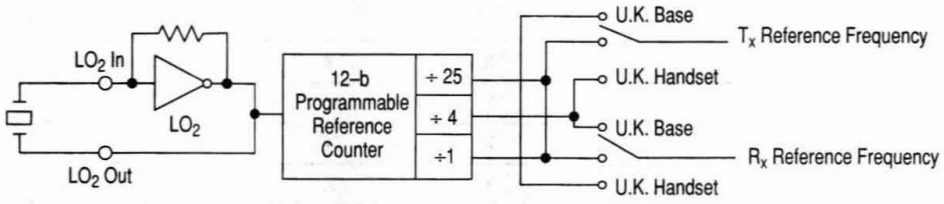
Figure 17 shows how the reference frequencies for the R_x and T_x loops are generated. All countries except U.K. require that the T_x and R_x reference frequencies be identical. In this case, set "U.K. Base Select" and "U.K. Handset Select" bits to "0". Then the fixed divider is set to "1" and the T_x and R_x reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value fo T_x and R_x.

For U.K. base operation, set "U.K. Base Select" to "1". For U.K. handset operation, set "U.K. Handset Select" to "1". The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T_x and R_x reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set "U.K. Base Select" to "1" and set "U.K. Handset Select" to "1". This will give a fixed divide by 4 for both the T_x and R_x reference. Then set the reference divider to 1024 to get a total divider of 4096.

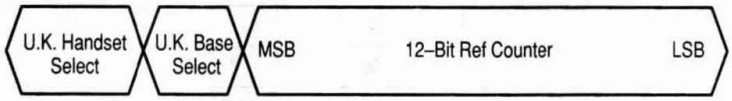
Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Control Register. Operation of the Control Register is explained in Figures 18 through 25.

Figure 17. Reference Register Programming Mode



U.K. Handset Select	U.K. Base Select	T_x Divider Value	R_x Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Base Set
1	0	4	25	U.K. Hand Set
1	1	4	4	Netherlands Base and Hand Set



14–Bit Reference Counter Latch

Figure 18. Control Register Bits

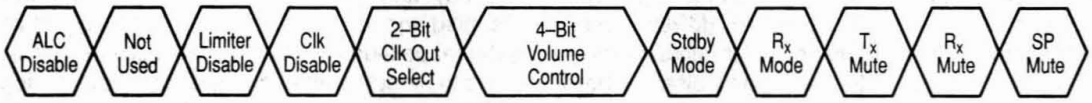


Figure 19. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T_x Mute	1 0	Transmit Channel Muted Normal Operation
R_x Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13109 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R_x, Standby, Interrupt and Inactive. In Active Mode, all circuit blocks are powered. In R_x mode, all circuitry is powered down exept for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 20 shows the control register bit values for selection of each power saving mode and Figure 21 show the circuit blocks which are powered in each of these operating mode.

Figure 20. Power Saving Mode Selection

Stdby Mode Bit	R_x Mode Bit	"CD Out/Hardware Interrupt" Pin	Power Saving Mode
0	0	X	Active
0	1	X	R_x
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Inactive

Figure 21. Circuit Blocks Powered During Power Saving Modes

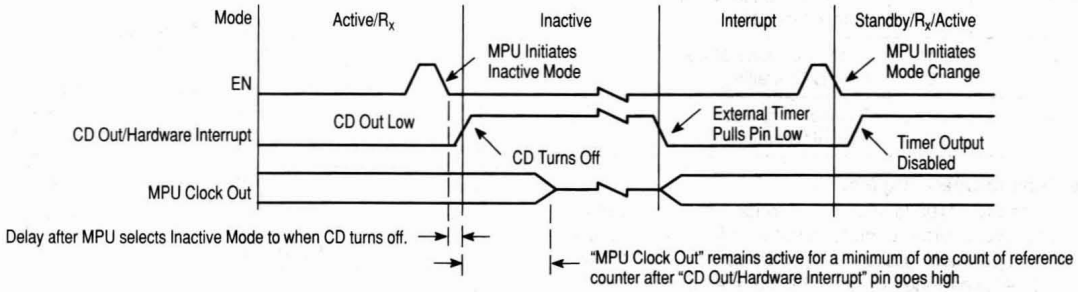
Circuit Blocks	Active	R_x	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver	X	X		
1st LO VCO	X	X		
R_x PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_x PLL	X			
R_x Audio Path	X			
T_x Audio Path	X			

NOTE: 1. In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13109 into the Inactive mode, which turns off the MPU Clock Output (see Figure 22), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 µs) after the command is given to switch into the "Inactive" mode. An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_x modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state due to the external pull–up resistor. In the Inactive mode the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low" by the external timing circuit, the MC13109 swtiches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R_x modes.

Figure 22. Hardware Interrupt Operation


Mode
Active/Rx
Inactive
Interrupt
Standby/Rx/Active
MPU Initiates Inactive Mode
MPU Initiates Mode Change
EN
CD Out Low
External Timer Pulls Pin Low
CD Out/Hardware Interrupt
CD Turns Off
Timer Output Disabled
MPU Clock Out
Delay after MPU selects Inactive Mode to when CD turns off.
"MPU Clock Out" remains active for a minimum of one count of reference counter after "CD Out/Hardware Interrupt" pin goes high

"Clk Out" Divider Programming

The "Clk Out" pin is derived from the 2nd local oscillator and can be used to drive a microprocessor, thereby reducing the number of crystals required. Figure 23 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 24 shows the "Clk Out" register bit values.

Figure 23. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	3	5	10
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

Figure 24. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	5
1	1	10

MPU "Clk Out" Power–Up Default Divider Value

The power–up default divider value is "divide by 10". This provides an MPU clock of about 1.0 MHz after initial power–up. The reason for choosing this relatively low clock frequency after intial power–up is that some microprocessors that operate down to a 2.0 V power supply have a maximum clock frequency fo 1.0 MHz. After initial power–up, the MPU can change the clock divider value to set the clock to the desired operating frequency. Special care has been taken in the design of the clock divider to ensure that the transition between one clock divider value and another is "smooth" (i.e., there will be no narrow clock pulses to disturb the MPU).

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13109 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in–series with the "Clk Out" output driver. A small capacitor can be connected to the "Clk Out" line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the "Clk Out" line.

Volume Control

The volume control can be programmed in 2.0 dB gain steps from –14 dB to +16 dB. The power–up default value is 0 dB.

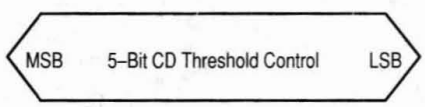
Figure 25. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the Carrier Detect threshold. Operation of these latch bits are explained in Figures 26 and 27.

Figure 26. Gain Control Latch Bits



Carrier Detect Threshold Programming

Th "CD Out" pin will give an indication to the microprocessor if a carier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be set through the MPU interface as shown in Figure 27 below.

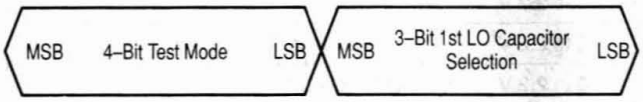
Figure 27. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9.0 dB
0	1	1	0	0	12	–8.0 dB
0	1	1	0	1	13	–7.0 dB
0	1	1	1	0	14	–6.0 dB
0	1	1	1	1	15	–5.0 dB
1	0	0	0	0	16	–4.0 dB
1	0	0	0	1	17	–3.0 dB
1	0	0	1	0	18	–2.0 dB
1	0	0	1	1	19	–1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Auxiliary Register

The auxiliary register contains a 3–bit 1st LO Capacitor Selection latch and a 4–bit Test Mode latch. Operation of these latch bits are explained in Figures 28, 29 and 30.

Figure 28. Auxiliary Register Latch Bits



First Local Oscillator Capacitor Selection for 25 Channel U.S. Operation

There is a very large frequency difference between the minimum and maximum channel frequencies in the proposed 25 Channel U.S. standard. The sensitivity of the 1st LO is not large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figure 29 shows the schematic of the 1st LO tank circuit. Figure 30 shows the latch control bit values.

The internal varactor temperature coefficient is 1800 ppm/°C (C_O = 8.9 pF at 25°C, V_{cap} control voltage = 1.2 V, F_{req} = 36 MHz). Customer is suggested to use a negative temperature coefficient capacitor in 1st LO tank circuit when the whole operating temperature range of –40 to +85°C is considered.

Figure 29. 1st LO Schematic

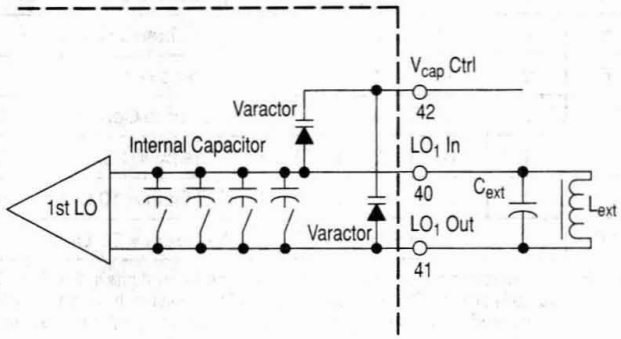


Figure 30. 1st LO Capacitor Select for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap Bit 0	1st LO Cap. Select	U.S. Base Channels	U.S. Handset Channels	Internal Cap. Value (Excluding Varactor)	Varactor Value over 0.5 to 2.2 V Range	External Capacitor Value	External Inductor Value
0	0	0	0	16 – 25	–	0.92 pF	10 – 6.4 pF	27 pF	0.47 µH
0	0	0	0	–	16 – 25	0.92 pF	10 – 6.4 pF	33 pF	0.47 µH
0	0	1	1	1 – 6	–	2.61 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	0	2	7 – 15	–	1.82 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	1	3	–	1 – 6	8.69 pF	10 – 6.4 pF	33 pF	0.47 µH
1	0	0	4	–	7 – 15	7.19 pF	10 – 6.4 pF	33 pF	0.47 µH

Figure 31. Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_x V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mV_{pp}	–
1	0	0	0	1	R_x Counter, upper 6	0 to 2.2 V	Input Frequency/64
2	0	0	1	0	R_x Counter, lower 8	0 to 2.2 V	See Note Below
3	0	0	1	1	R_x Prescaler	0 to 2.2 V	Input Frequency/4
4	0	1	0	0	T_x Counter, upper 6	0 to 2.2 V	Input Frequency/64
5	0	1	0	1	T_x Counter, lower 8	0 to 2.2 V	See Note Below
6	0	1	1	0	T_x Prescaler	>200 mV_{pp}	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.2 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.2 V	Input Frequency/100
9	1	0	0	1	AGC Gain = 10 Option	N/A	–
10	1	0	1	0	AGC Gain = 25 Option	N/A	–

NOTE: To determine the correct output, look at the lower 8 bits in the R_x or T_x register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6 bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Test Modes

Test Mode Control latch bits enable independent testing of internal counters and set AGC Gain Options. In test mode, the "T_x VCO" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0" for normal operation. Test mode operation is described in Figure 31. During normal operation and when testing the T_x Prescaler, the "T_x VCO" input can be a minimum of 200 mV_{pp} at 80 MHz and should be ac coupled. For other test modes, input signals should be standard logic levels of 0 to 2.2 V and a maximum frequency of 16 MHz.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The MC13109 is initially placed in the Rx mode with all mutes active and nothing disabled. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The MPU clock output divider is set to 10 to give the minimum clock output frequency. The T_x and R_x latch registers are set for USA Channel Frequency #21. Figure 32 shows the initial power–up states for all latch registers.

Figure 32. Latch Register Power–Up Defaults

		MSB								LSB							
Register	Count	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_x	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_x	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	–	–	–	–	–	–	–	–	–	–	1	0	1	0	0
TM	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

Figure 33. I_{CC} versus V_{CC} at Active Mode

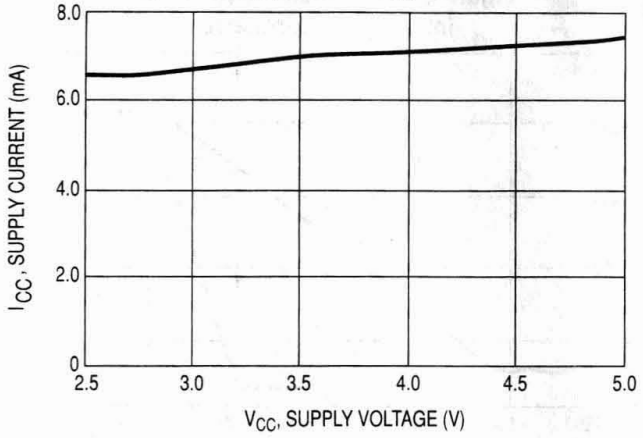


Figure 34. I_{CC} versus V_{CC} at Receive Mode

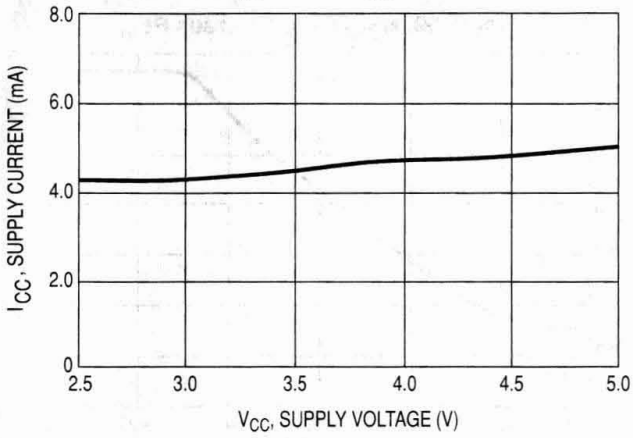


Figure 35. I_{CC} versus V_{CC} at Standby Mode

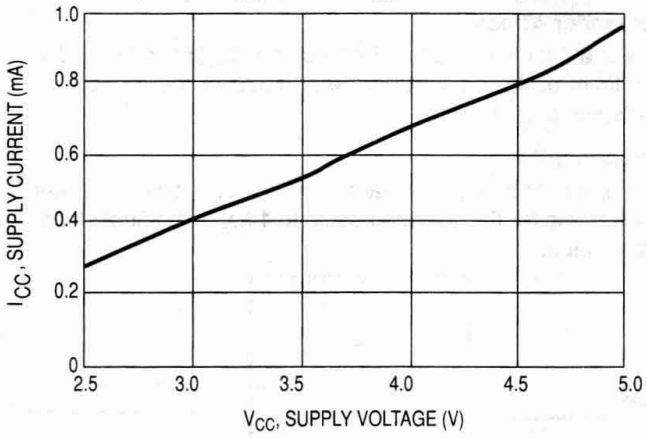


Figure 36. I_{CC} versus V_{CC} at Inactive Mode

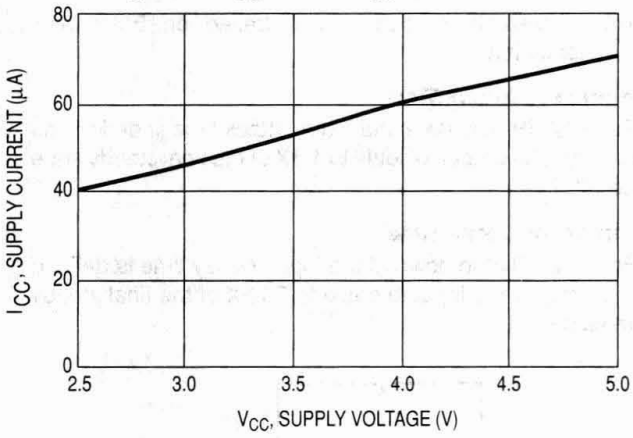


Figure 37. RF_{in} versus AF_{out}, N+D, N, AMR

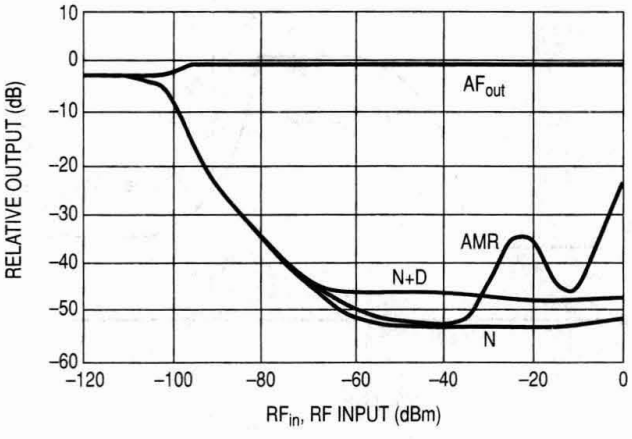


Figure 38. Recovered Audio/THD versus f_{DEV}

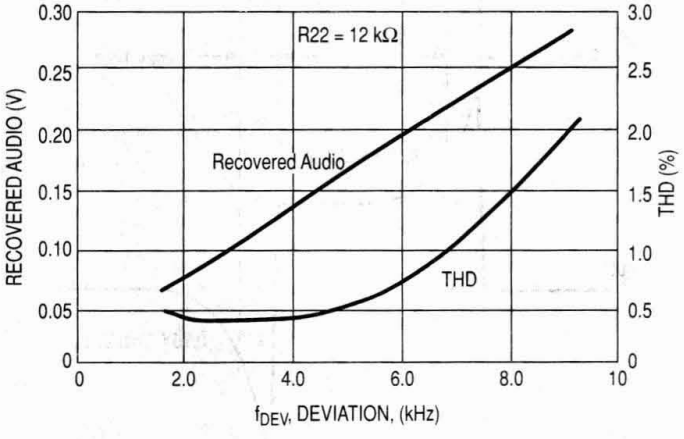


Figure 39. RSSI Output versus RF_{in}

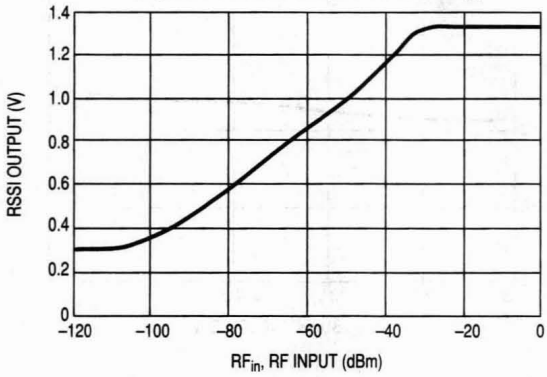
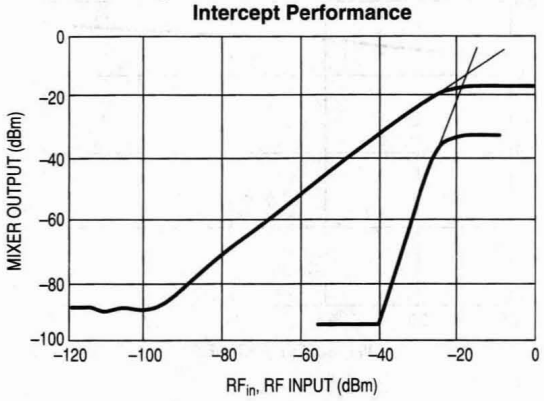


Figure 40. First Mixer Third Order Intercept Performance



APPENDIX A – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME

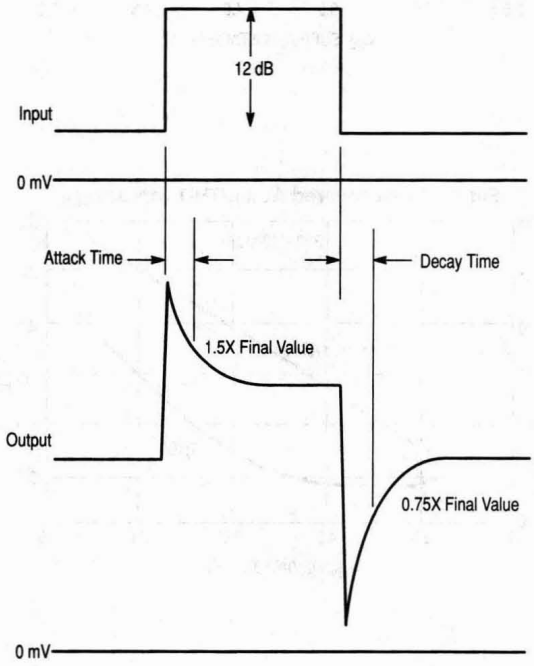
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

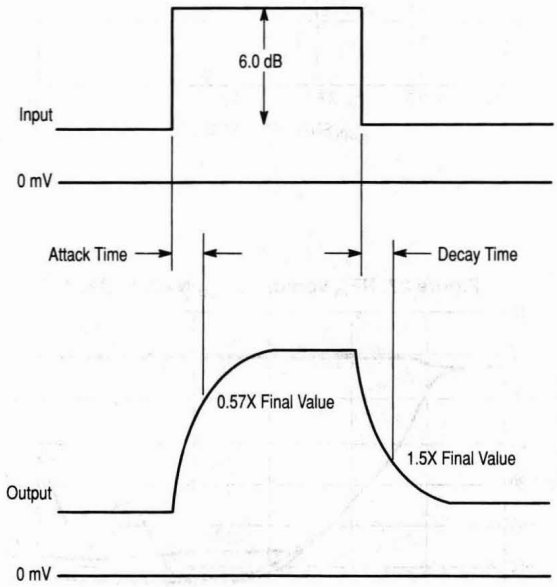


Expander Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expander Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

Advance Information

Universal Cordless Telephone Subsystem IC

MC13110A/B
MC13111A/B

UNIVERSAL NARROWBAND FM RECEIVER INTEGRATED CIRCUIT

The MC13110A/B and MC13111A/B integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, external adjustments, and lowers overall costs. It is designed for use in both the handset and the base.

- MC13110A and MC13111A: Fully Programmable in all Power Modes
- MC13110B and MC13111B: MPU Clk Out and Second Local Oscillator are "Always On". There is No Inactive Mode
- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expander Includes Mute, Digital Volume Control, Speaker Driver, Programmable Low Pass Filter, and Gain Block
  - Compressor Includes Mute, Programmable Low Pass Filter, Limiter, and Gain Block
- MC13110A/B only: Frequency Inversion Scrambler
  - Function Controlled via MPU Interface
  - Programmable Carrier Modulation Frequency
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign Cordless Telephone Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Low Battery Detect
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- 2.7 to 5.5 V Operation (15 µA Current Consumption in Inactive Mode)
- AN1575: Refer to this Application Note for a List of the "Worldwide Cordless Telephone Frequencies

52 1

FB SUFFIX
PLASTIC PACKAGE
CASE 848B
(QFP–52)

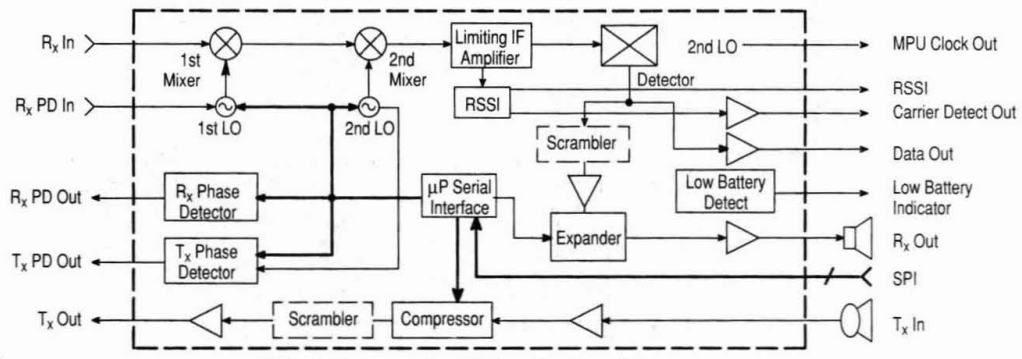
48 1

FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13110AFB	$T_A = -40°$ to $+85°C$	QFP–52
MC13110AFTA		LQFP–48
MC13110BFB		QFP–52
MC13110BFTA		LQFP–48
MC13111AFB		QFP–52
MC13111AFTA		LQFP–48
MC13111BFB		QFP–52
MC13111BFTA		LQFP–48

Simplified Block Diagram

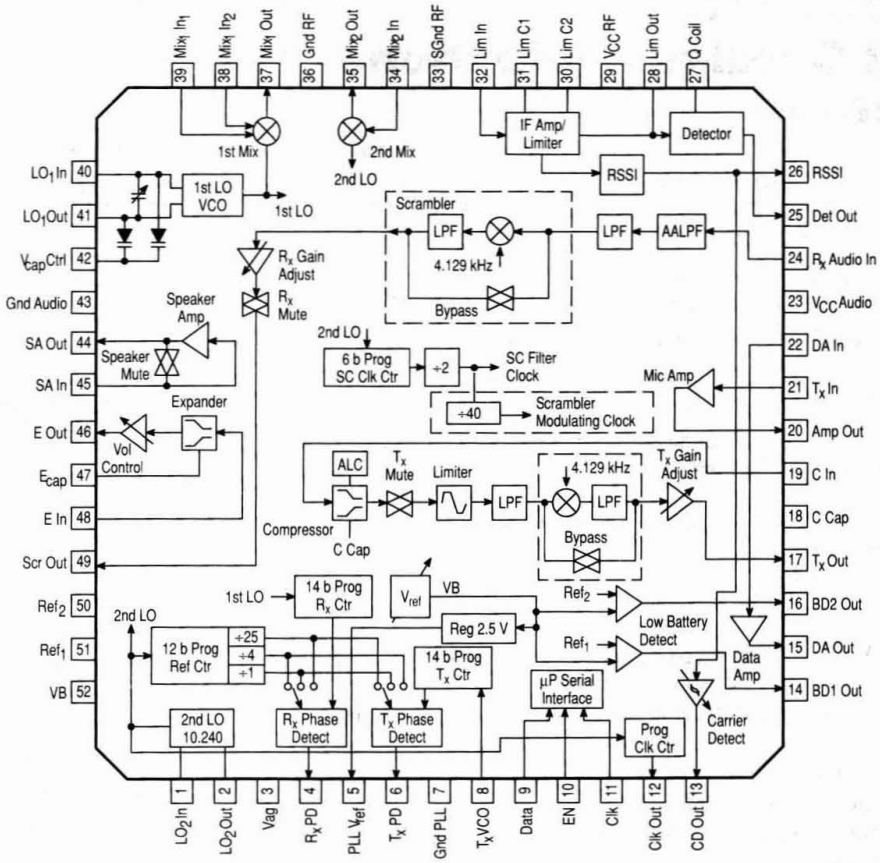


NOTE:
[ ] = MC13110A/B Only

This device contains 8262 active transistors.

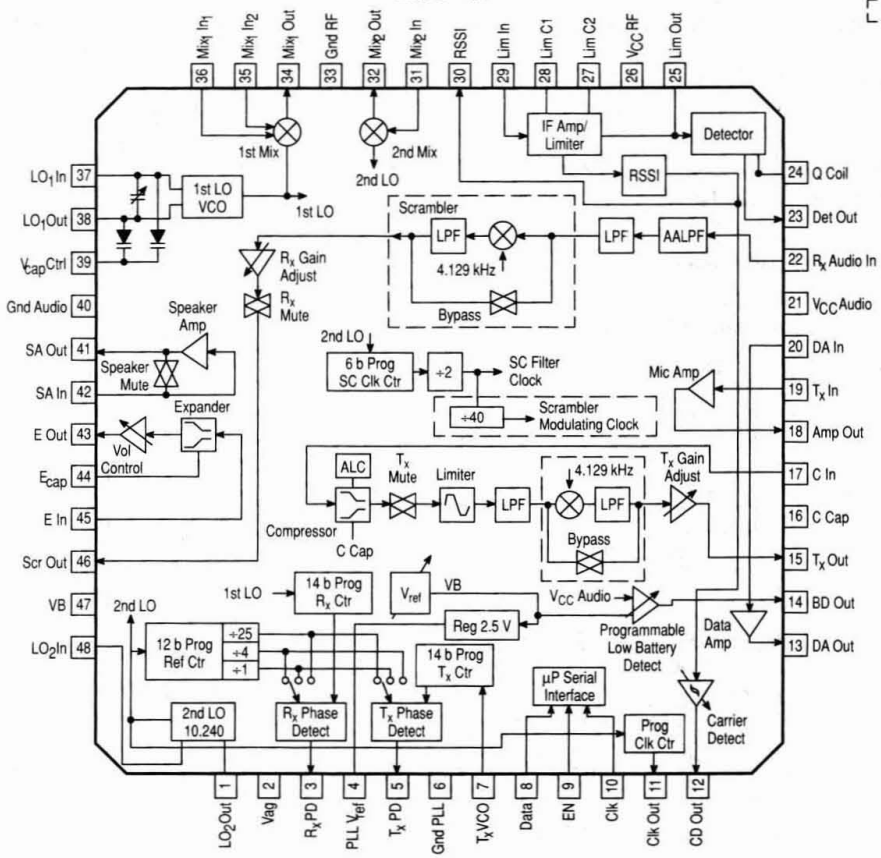
PIN CONNECTIONS

QFP–52



LQFP–48

NOTE:
[ ] = MC13110A/B Only



MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +6.0	Vdc
Junction Temperature	T_J	−65 to +150	°C
Maximum Power Dissipation, T_A = 25°C	P_D	70	mW

NOTES: 1. Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.5	Vdc
Operating Ambient Temperature	T_A	–40	–	85	°C
Input Voltage Low (Data, Clk, EN)	V_{IL}	–	–	0.3	V
Input Voltage High (Data, Clk, EN)	V_{IH}	PLL V_{ref} – 0.3	–	–	V
Bandgap Reference Voltage	V_B	–	1.5	–	V

NOTE: 3. All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise specified, IP3 = 0; Test Circuit Figure 1.)

Characteristic	Symbol	Figure	Min	Typ	Max	Unit
Static Current		1				
Active Mode	ACT I_{CC}		5.5	8.5	10.5	mA
Receive Mode	R_x I_{CC}		3.1	4.1	5.3	mA
Standby Mode	STD I_{CC}		–	465	560	µA
Inactive Mode [Note 4]	INACT I_{CC}		–	15	30	µA
Current Increase When IP3 = 1 (Active and Receive Modes)	I_{IP3}	1	–	1.4	1.8	mA

NOTE: 4. MC13110B/MC13111B versions have no inactive mode.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz, $V_{cap\ ctrl}$ = 1.2 V)								
Input Sensitivity (for 12 dB SINAD at Det Out Using C–Message Weighting Filter)	68, 69	Mix_1 In_1/In_2	Det Out	V_{SIN}	–	2.2	–	µVrms
50 Ω Termination, Generator Referred					–	–100	–	dBm
Single–Ended, Matched Input, Generator Referred					–	0.4	–	
					–	–115	–	
Differential, Matched Input, Generator Referred					–	0.4	–	
					–	–115	–	
First and Second Mixer Voltage Gain Total (V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load)	1	Mix_1 In_1 or In_2	Mix_2 Out	MX_{gainT}	24	29	–	dB
Isolation of First Mixer Output and Second Mixer Input (V_{in} = 1.0 mVrms, with CFI Removed)	–	Mix_1 In_1 or In_2	Mix_2 In	Mix–Iso	–	60	–	dB
Total Harmonic Distortion (V_{in} = 3.16 mVrms)	1	Mix_1 In_1 or In_2	Det Out	THD	–	1.4	2.0	%
Recovered Audio (V_{in} = 3.16 mVrms)	1	Mix_1 In_1 or In_2	Det Out	AFO	80	112	150	mVrms
AM Rejection Ratio (V_{in} = 3.16 mVrms, 30% AM, @ 1.0 kHz)	1	Mix_1 In_1 or In_2	Det Out	AMR	30	48	–	dB
Signal to Noise Ratio (V_{in} = 3.16 mVrms, No Modulation)	–	Mix_1 In_1 or In_2	Det Out	SNR	–	48	–	dB
FIRST MIXER (No Modulation, f_{in} = USA Ch21, 46.77 MHz, 50 Ω Termination at Inputs)								
Input Impedance		–	Mix_1					kΩ
Single–Ended	16		In_1 or In_2	R_{PS1}	–	1.6	–	pF
				C_{PS1}	–	3.7	–	
Differential	16		Mix_1 In_1/In_2	R_{PD1}	–	1.6	–	
				C_{PD1}	–	1.8	–	
Output Impedance	14	–	Mix_1 Out	R_{P1} Out	–	300	–	Ω
				C_{P1} Out	–	3.7	–	pF
Voltage Conversion Gain (V_{in} = 1.0 mVrms, with CF_1 Filter as Load)	17, 18	Mix_1 In_1 or In_2	Mix_1 Out	MX_{gain1}	–	12	–	dB
1.0 dB Voltage Compression Level (Input Referred)		Mix_1	Mix_1 Out	V_O Mix_1				mVrms
IP3 Bit Set to 0	19, 21	In_1 or In_2		1 dB	–	20	–	dBm
					–	–21	–	
IP3 Bit Set to 1	20, 21				–	56	–	
					–	–12	–	
Third Order Intercept (Input Referred) [Note 5]		Mix_1	Mix_1 Out	TOI_{mix1}				mVrms
IP3 Bit Set to 0	19, 21	In_1 or In_2			–	64	–	dBm
					–	–11	–	
IP3 Bit Set to 1	20, 21				–	178	–	
					–	–2.0	–	
–3.0 dB IF Bandwidth	22	Mix_1 In_1 or In_2	Mix_1 Out	Mix_1 BW	–	13	–	MHz

NOTE: 5. Third order intercept calculated for input levels 10 dB below 1.0 dB compression point.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
SECOND MIXER (No Modulation, f_{in} = 10.7 MHz, 50 Ω Termination at Inputs)								
Input Impedance	24	Mix_2 In	Mix_2 In	R_{P2} In C_{P2} In	– –	2.8 3.6	– –	kΩ pF
Output Impedance	24	–	Mix_2 Out	R_{P2} Out C_{P2} Out	– –	1.5 6.1	– –	kΩ pF
Voltage Conversion Gain (V_{in} = 1.0 mVrms, with CF_2 Filter as Load)	26, 27	Mix_2 In	Mix_2 Out	MX_{gain2}	–	20	–	dB
1.0 dB Voltage Compression Level (Input Referred) IP3 Bit Set 0	28, 30	Mix_2 In	Mix_2 Out	V_O Mix_2 1 dB	 – –	 32 –17	 – –	mVrms dBm
IP3 Bit Set 1	29, 30				– –	45 –14	– –	
Third Order Intercept (Input Referred) [Note 6] IP3 Bit Set 0	28, 30	Mix_2 In	Mix_2 Out	TOI_{mix2}	 – –	 136 –4.3	 – –	mVrms dBm
IP3 Bit Set 1	29, 30				– –	158 –3.0	– –	
–3.0 dB IF Bandwidth	31	Mix_2 In	Mix_2 Out	Mix_2 BW	–	2.5	–	MHz
LIMITER/DEMODULATOR (f_{in} = 455 kHz, f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
Input Impedance	49	Lim In	Lim In	R_{PLim} C_{PLim}	– –	1.5 16	– –	kΩ pF
Detector Output Impedance	–	–	Det Out	R_O	–	1.1	–	kΩ
IF –3.0 dB Limiting Sensitivity	1	Lim In	Det Out	IF Sens	–	71	100	μVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
RSSI/CARRIER DETECT (No Modulation)								
RSSI Output Dynamic Range	56	Mix_1 In	RSSI	RSSI	–	80	–	dB
DC Voltage Range	56	Mix_1 In	RSSI	DC RSSI	–	0.2 to 1.5	–	Vdc
Carrier Detect Threshold CD Threshold Adjust = (10100) (Threshold Relative to Mix_1 In Level)	57	Mix_1 In	CD Out	V_T	–	15	–	μVrms
Hysteresis, CD = (10100) (Threshold Relative to Mix_1 In Level)	57	Mix1 In	CD Out	Hys	–	2.0	–	dB
Output High Voltage CD = (00000), RSSI = 0.2 V	1	RSSI	CD Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage CD = (11111), RSSI = 0.9 V	1	RSSI	CD Out	V_{OL}	–	0.02	0.4	V
Carrier Detect Threshold Adjustment Range (Programmable through MPU Interface)	126	–	–	V_T Range	–	–20 to 11	–	dB
Carrier Detect Threshold – Number of Programmable Levels	126	–	–	V_{Tn}	–	32	–	–

NOTE: 6. Third order intercept calculated for input levels 10 dB below 1.0 dB compression point.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
R_x AUDIO PATH (f_{in} = 1.0 kHz, Active Mode, scrambler bypassed)								
Absolute Gain (V_{in} = –20 dBV)	1, 72	R_x Audio In	SA Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to E Out for V_{in} = –20 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	1, 76	E In	E Out	G_t	 –21 –42	 –20 –40	 –19 –38	dB
Total Harmonic Distortion (V_{in} = –20 dBV)	1, 76	R_x Audio In	SA Out	THD	–	0.7	1.0	%
Maximum Input Voltage (V_{CC} = 2.7 V)	76	R_x Audio In	–	–	–	–11.5	–	dBV
Maximum Output Voltage (Increase input voltage until output voltage THD = 5.0%, then measure output voltage)	1	E In	E Out	V_{Omax}	–2.0	0	–	dBV
Input Impedance	–	R_x Audio In E In	–	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	–	E In	E Out	t_a	–	3.0	–	ms
Release Time E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	–	E In	E Out	t_r	–	13.5	–	ms
Compressor to Expander Crosstalk V_{in} = –10 dBV, $V_{(E\ In)}$ = AC Gnd	1	C In	E Out	C_T	–	–90	–70	dB
R_x Muting (Δ Gain) V_{in} = –20 dBV, R_x Gain Adj = (01111)	1	R_x Audio In	E Out	M_e	–	–84	–60	dB
R_x High Frequency Corner R_x Path, V R_x Audio In = –20 dBV	1	R_x Audio In	Scr Out	R_x f_{ch}	3.779	3.879	3.979	kHz
Low Pass Filter Passband Ripple (V_{in} = –20 dBV)	1, 73	R_x Audio In	Scr Out	Ripple	–	0.4	0.6	dB
R_x Gain Adjust Range (Programmable through MPU Interface)	125	R_x Audio In	Scr Out	R_x Range	–	–9.0 to 10	–	dB
R_x Gain Adjust Steps – Number of Programmable Levels	125	R_x Audio In	Scr Out	R_x n	–	20	–	dB
Audio Path Noise, C–Message Weighting (Input AC–Grounded)	70	R_x Audio In	Scr Out E Out SA Out	EN	– –	–85 <–95 <–95	– –	dBV
Volume Control Adjust Range	123	E In	E Out	$V_{cn\ Range}$	–	–14 to 16	–	dB
Volume Control – Number of Programmable Levels	123	E In	E Out	V_{cn}	–	16	–	–
SPEAKER AMP/SP MUTE (Active Mode)								
Maximum Output Swing R_L = No Load, V_{in} = 3.4 Vpp R_L = 130 Ω, V_{in} = 2.8 Vpp R_L = 620 Ω, V_{in} = 4.0 Vpp	1, 79	SA In	SA Out	V_{Omax}	 2.8 2.0 –	 3.2 2.6 3.4	 – – –	Vpp
Speaker Amp Muting V_{in} = –20 dBV, R_L = 130 Ω	1	SA In	SA Out	M_{sp}	–	–92	–60	dB

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
DATA AMP COMPARATOR								
Hysteresis	1	DA In	DA Out	Hys	30	42	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	–	V_{CC} – 0.7	–	V
Input Impedance	1	–	DA In	Z_I	200	250	280	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	1	DA In	DA Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	1	DA In	DA Out	V_{OL}	–	0.1	0.4	V
Maximum Frequency	–	DA In	DA Out	F_{max}	–	10	–	kHz
MIC AMP (f_{in} = 1.0 kHz, External resistors set to gain of 1, Active Mode)								
Open Loop Gain	–	T_x In	Amp Out	AVOL	–	100,000	–	V/V
Gain Bandwidth	–	T_x In	Amp Out	GBW	–	100	–	kHz
Maximum Output Swing (R_L = 10 kΩ)	–	T_x In	Amp Out	V_{Omax}	–	3.2	–	Vpp
T_x AUDIO PATH (f_{in} = 1.0 kHz, T_x Gain Adj = (01111); ALC, Limiter, and Mutes Disabled; Active Mode, scrambler bypassed)								
Absolute Gain (V_{in} = –10 dBV)	1, 83	T_x In	T_x Out	G	–4.0	0	4.0	dB
Gain Tracking (Referenced to T_x Out for V_{in} = –10 dBV) V_{in} = –30 dBV V_{in} = –40 dBV	1, 87	T_x In	T_x Out	G_t	 –11 –17	 –10 –15	 –9.0 –13	dB
Total Harmonic Distortion (V_{in} = –10 dBV)	1, 87	T_x In	T_x Out	THD	–	0.8	1.8	%
Maximum Output Voltage (Increase input voltage until output voltage THD = 5.0%, then measure output voltage. T_x Gain Adjust = 8 dB)	1	T_x In	T_x Out	V_{Omax}	–2.0	0	–	dBV
Input Impedance	–	–	C In	Z_{in}	–	10	–	kΩ
Attack Time (C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B))	–	C In	T_x Out	t_a	–	3.0	–	ms
Release Time (C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B))	–	C In	T_x Out	t_r	–	13.5	–	ms
Expander to Compressor Crosstalk (V_{in} = –20 dBV, Speaker Amp No Load, $V_{(C\ In)}$ = AC Gnd)	1	E In	T_x Out	C_T	–	–60	–40	dB
T_x Muting (V_{in} – 10 dBV)	1	T_x In	T_x Out	M_c	–	–88	–60	dB
ALC Output Level (ALC enabled) V_{in} = –10 dBV V_{in} = –2.5 dBV	1, 87, 90	T_x In	T_x Out	ALC_{out}	 –15 –13	 –13 –11	 –8.0 –6.0	dBV
ALC Slope (ALC enabled) V_{in} = –10 dBv V_{in} = –2.5 dBv	1	T_x In	T_x Out	Slope	0.1	0.25	0.4	dB/dB
ALC Input Dynamic Range	–	C In	T_x Out	DR	–	–16 to –2.5	–	dBV
Limiter Output Level (V_{in} = –2.5 dBV, Limiter enabled)	1	T_x In	T_x Out	V_{lim}	–10	–8.0	–	dBV
T_x High Frequency Corner [Note 7] (VT_x In = –10 dBV, Mic Amp = Unity Gain)	1	T_x In	T_x Out	T_x f_c	3.6	3.7	3.8	kHz

NOTE: 7. The filter specification is based on a 10.24 MHz 2nd LO, and a switched–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

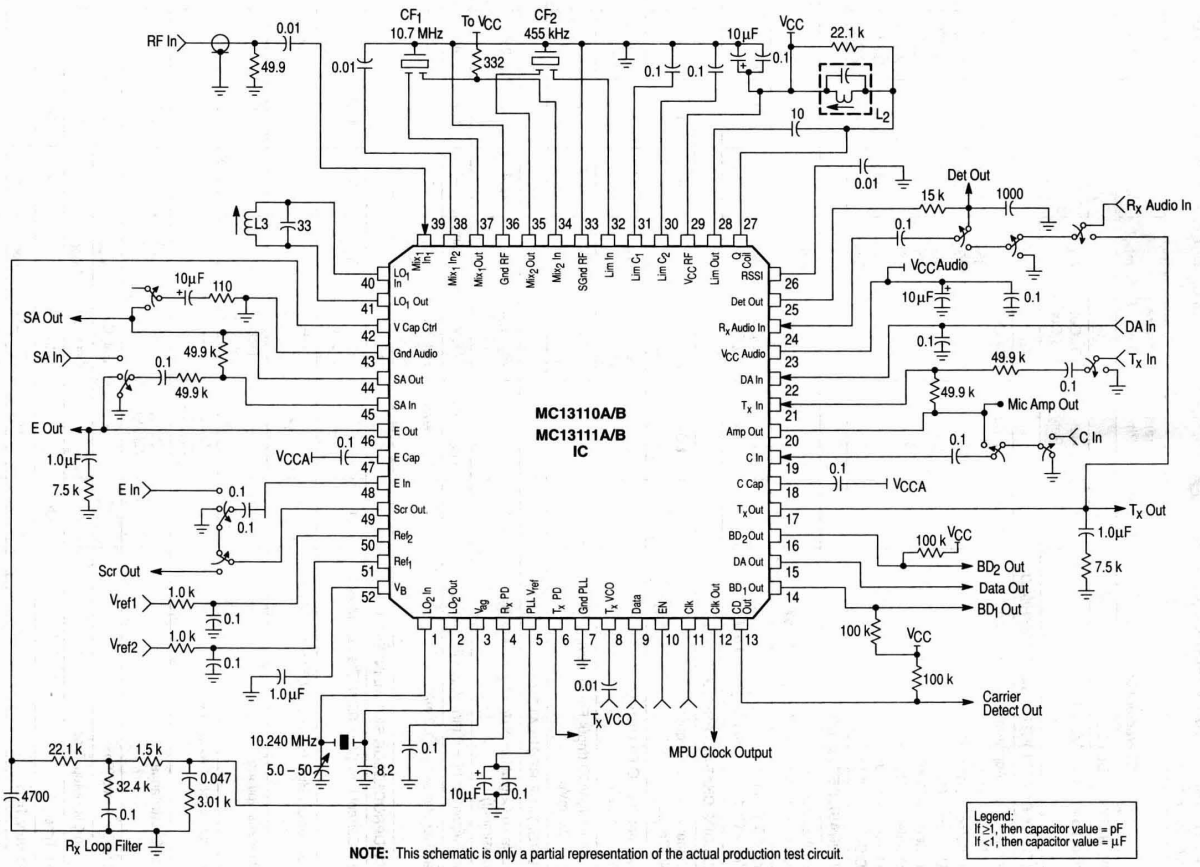
Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
T_x AUDIO PATH (f_{in} = 1.0 kHz, T_x Gain Adj = (01111); ALC, Limiter, and Mutes Disabled; Active Mode, scrambler bypassed)								
Low Pass Filter Passband Ripple (V_{in} = –10 dBV)	1, 84	T_x In	T_x Out	Ripple	–	0.7	1.2	dB
Maximum Compressor Gain (V_{in} = –70 dBV)	–	C In	T_x Out	AV_{max}	–	23	–	dB
T_x Gain Adjust Range (Programmable through MPU Interface)	125	C In	T_x Out	T_x Range	–	–9.0 to 10	–	dB
T_x Gain Adjust Steps – Number of Programmable Levels	125	C In	T_x Out	T_x n	–	20	–	–
R_x AND T_x SCRAMBLER (2nd LO = 10.24 MHz, T_x Gain Adj = (01111), R_x Gain Adj = (01111), Volume Control = (0 dB Default Levels), SCF Clock Divider = 31. Total is divide by 62 for SCF clock frequency of 165.16 kHz)								
R_x High Frequency Corner (Note 8) R_x Path, f = 479 Hz, V R_x Audio In = –20 dBV	–	R_x Audio In	Scr Out	R_x f_{ch}	3.55	3.65	3.75	kHz
T_x High Frequency Corner (Note 8) T_x Path, f = 300 Hz, V T_x In = –10 dBV, Mic Amp = Unity Gain	–	T_x In	T_x Out	T_x f_{ch}	3.829	3.879	3.929	kHz
Absolute Gain R_x: V_{in} = –20 dBV T_x: V_{in} = –10 dBV, Limiter disabled	 – –	 R_x Audio In T_x In	 E Out T_x Out	AV	 –4.0 –4.0	 0.4 –1.0	 4.0 4.0	dB
Pass Band Ripple R_x + T_x Path – 1.0 µF from T_x Out to R_x Audio In, f_{in} = low corner frequency to high corner frequency	–	C In	E Out	Ripple	–	1.9	2.5	dB
Scrambler Modulation Frequency R_x: 100 mV (–20 dBV) T_x: 316 mV (–10 dBV)	 – –	 R_x Audio In C In	 E Out T_x Out	f_{mod}	4.119	4.129	4.139	kHz
Group Delay R_x + T_x Path – 1.0 µF from T_x Out to R_x Audio In, f_{in} = 1.0 kHz	–	C In	E Out	GD	–	1.0	–	ms
f_{in} = low corner frequency to high corner frequency	–	C In	E Out	GD	–	4.0	–	
Carrier Breakthrough R_x + T_x Path – 1.0 µF from T_x Out to R_x Audio In	–	C In	E Out	CBT	–	–60	–	dB
Baseband Breakthrough R_x + T_x Path – 1.0 µF from T_x Out to R_x Audio In, f_{in} = 1.0 kHz, f_{meas} = 3.192 kHz	–	C In	E Out	BBT	–	–50	–	dB
LOW BATTERY DETECT								
Average Threshold Voltage Before Electronic Adjustment (V_{ref}_Adj = (0111))	1, 131	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_i	1.38	1.48	1.58	V
Average Threshold Voltage After Electronic Adjustment (V_{ref}_Adj = (adjusted value))	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_f	1.475	1.5	1.525	V
Hysteresis	–	Ref_1 Ref_2	BD_1 Out BD_2 Out	Hys	–	4.0	–	mV
Input Current (V_{in} = 1.0 and 2.0 V)	1	–	Ref_1 Ref_2	I_{in}	–50	–	50	nA
Output High Voltage (V_{in} = 2.0 V)	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OH}	V_{CC} – 0.1	3.6	–	V

NOTE: 8. The filter specification is based on a 10.24 MHz 2nd LO, and a switch–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Figure	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
LOW BATTERY DETECT								
Output Low Voltage (V_{in} = 1.0 V)	1	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OL}	–	0.2	0.4	V
BATTERY DETECT INTERNAL THRESHOLD								
After Electronic Adjustment of V_B Voltage	1, 128	V_{CC} Audio	BD_2 Out					V
BD Select = (111)				IBS_7	3.381	3.455	3.529	
BD Select = (110)				IBS_6	3.298	3.370	3.442	
BD Select = (101)				IBS_5	3.217	3.287	3.357	
BD Select = (100)				IBS_4	3.134	3.202	3.270	
BD Select = (011)				IBS_3	2.970	3.034	3.098	
BD Select = (010)				IBS_2	2.886	2.948	3.010	
BD Select = (001)				IBS_1	2.802	2.862	2.922	
PLL PHASE DETECTOR								
Output Source Current (V_{PD} = Gnd + 0.5 V to PLL V_{ref} – 0.5 V)	–	–	R_x PD T_x PD	I_{OH}	–	1.0	–	mA
Output Sink Current (V_{PD} = Gnd + 0.5 V to PLL V_{ref} – 0.5 V)	–	–	R_x PD T_x PD	I_{OL}	–	1.0	–	mA
PLL LOOP CHARACTERISTICS								
Maximum 2nd LO Frequency (No Crystal)	–	LO_2 In	–	f_{2ext}	–	12	–	MHz
Maximum 2nd LO Frequency (With Crystal)	–	–	LO_2 In LO_2 Out	f_{2ext}	–	12	–	MHz
Maximum T_x VCO (Input Frequency), V_{in} = 200 mVpp	–	–	T_x VCO	f_{txmax}	–	80	–	MHz
PLL VOLTAGE REGULATOR								
Regulated Output Level (I_L = 0 mA, after V_{ref} Adjustment)	1	–	PLL V_{ref}	V_O	2.4	2.5	2.6	V
Line Regulation (I_L = 0 mA, V_{CC} = 3.0 to 5.5 V)	1	V_{CC} Audio	PLL V_{ref}	V_{Reg} Line	–	11.8	40	mV
Load Regulation (I_L = 1.0 mA)	1	V_{CC} Audio	PLL V_{ref}	V_{Reg} Load	–20	–1.4	–	mV
MICROPROCESSOR SERIAL INTERFACE								
Input Current Low (V_{in} = 0.3 V, Standby Mode)	1	–	Data, Clk, EN	I_{IL}	–5.0	0.4	–	µA
Input Current High (V_{in} = 3.3 V, Standby Mode)	1	–	Data, Clk, EN	I_{IH}	–	1.6	5.0	µA
Hysteresis Voltage	–	–	Data, Clk, EN	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	–	Data, EN, Clk	–	–	–	2.0	–	MHz
Input Capacitance	–	Data, Clk, EN	–	C_{in}	–	8.0	–	pF
EN to Clk Setup Time	106	–	EN, Clk	t_{suEC}	–	200	–	ns
Data to Clk Setup Time	105	–	Data, Clk	t_{suDC}	–	100	–	ns
Hold Time	105	–	Data, Clk	t_h	–	90	–	ns
Recovery Time	106	–	EN, Clk	t_{rec}	–	90	–	ns
Input Pulse Width	–	–	EN, Clk	t_w	–	100	–	ns
MPU Interface Power–Up Delay (90% of PLL V_{ref} to Data,Clk, EN)	108	–	–	t_{puMPU}	–	100	–	µs

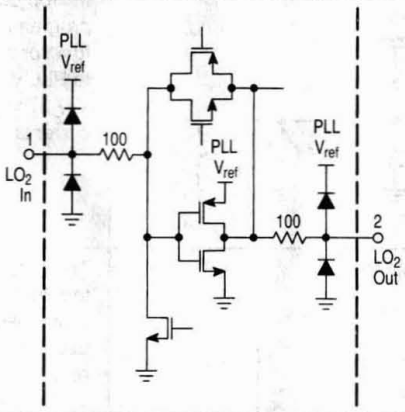
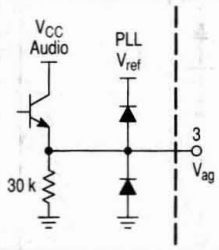
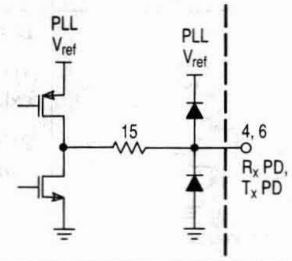
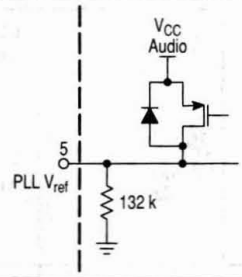
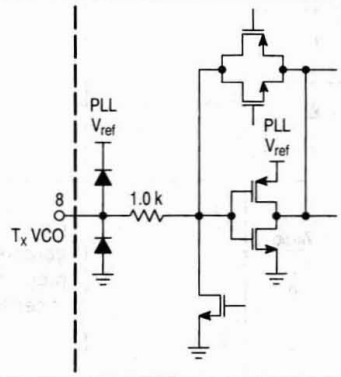
Figure 1. Production Test Circuit (52 Pin QFP)



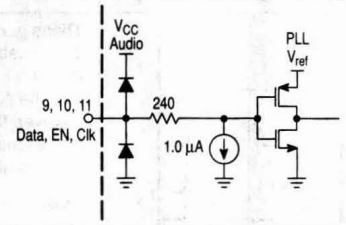
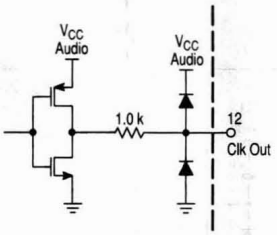
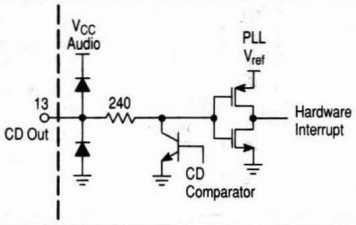
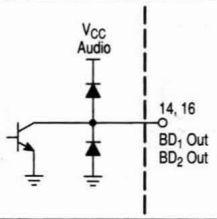
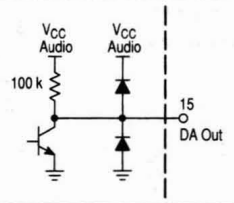
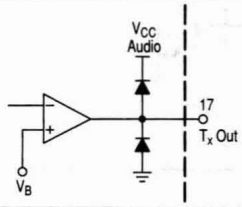
NOTE: This schematic is only a partial representation of the actual production test circuit.

MC13110A/B MC13111A/B

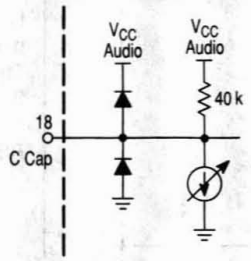
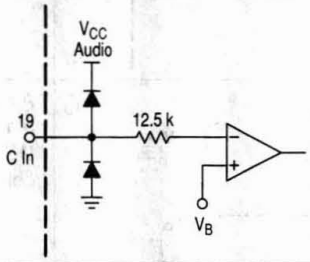
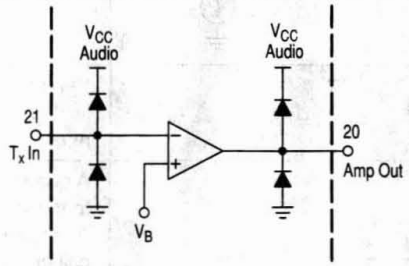
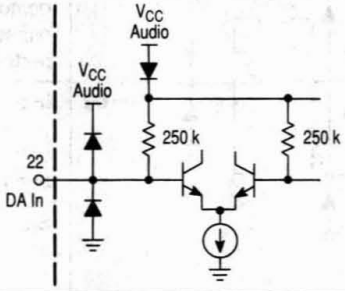
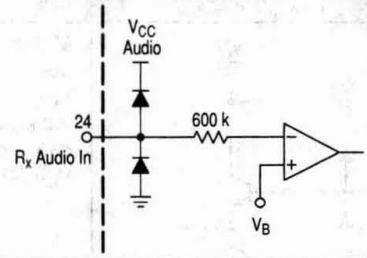
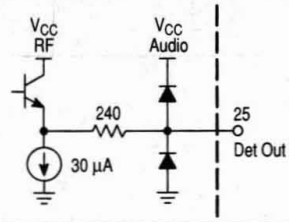
PIN FUNCTION DESCRIPTION

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
48 1	1 2	LO_2 In LO_2 Out		These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver. "LO_2 In" may also serve as an input for an externally generated reference signal which is typically ac–coupled. When the IC is set to the inactive mode, LO_2 In is internally pulled low to disable the oscillator. The input capacitance to ground at each pin (LO_2 In/ LO_2 Out) is 3.0 pF.
2	3	V_{ag}		V_{ag} is the internal reference voltage for the switched capacitor filter section. This pin must be decoupled with a 0.1 µF capacitor.
3 5	4 6	R_x PD (Output) T_x PD (Output)		This pin is a tri–state voltage output of the R_x and T_x Phase Detector. It is either "high", "low", or "high impedance," depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_x and T_x PLL loop filters. R_x and T_x PD outputs can sink or source 1.0 mA.
4	5	PLL V_{ref}		PLL V_{ref} is a PLL voltage regulator output pin. An internal voltage regulator provides a stable power supply voltage for the R_x and T_x PLL's and can also be used as a regulated supply voltage for other IC's. It can source up to 1.0 mA externally. Proper supply filtering is a must on this pin. PLL V_{ref} is pulled up to V_{CC} audio for the standby and inactive modes (Note 1).
6	7	Gnd PLL		Ground pin for digital PLL section of IC.
7	8	T_x VCO (Input)		T_x VCO is the transmit divide counter input which is driven by an ac–coupled external transmit loop VCO. The minimum signal level is 200 mVpp @ 60.0 MHz. This pin also functions as the test mode input for the counter tests.

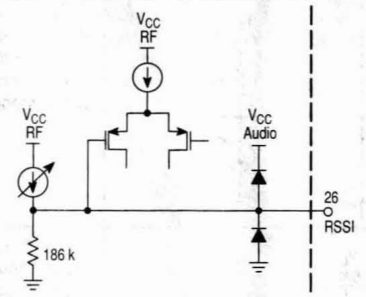
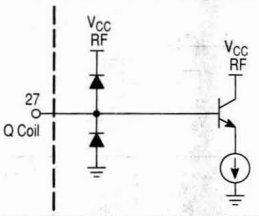
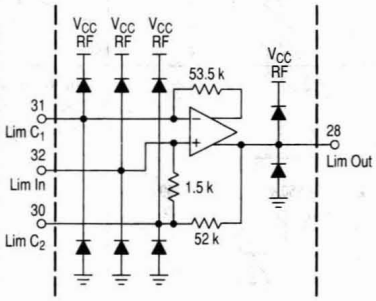
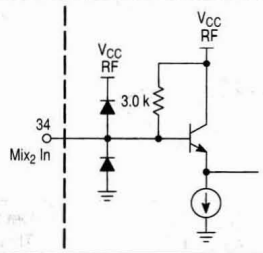
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
8 9 10	9 10 11	Data EN Clk (Input)		Microprocessor serial interface input pins are for programming various counters and control functions. The switching thresholds are referenced to PLL V_{ref} and Gnd PLL. The inputs operate up to V_{CC}. These pins have 1.0 µA internal pull–down currents.
11	12	Clk Out (Output)		The microprocessor clock output is derived from the 2nd LO crystal oscillator and a programmable divider with divide ratios of 2 to 312.5. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes. 1) For the MC13110A/B and MC13111A/B the Clk Out can be disabled via the MPU interface. 2) For the MC13110B and MC13111B this output is always active (on) (Note 2).
12	13	CD Out (I/O)		Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from the Inactive Mode.
–	14	BD_1 Out		Low battery detect output #1 is an open collector with external pull–up resistor.
14	16	BD_2 Out (Output)		Low battery detect output #2 is an open collector with external pull–up resistor.
13	15	DA Out (Output)		Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
15	17	T_x Out (Output)		T_x Out is the T_x path audio output. Internally this pin has a low–pass filter circuitry with –3 dB bandwidth of 4.0 kHz. T_x gain and mute are programmable through the MPU interface. This pin is sensitive to load capacitance.

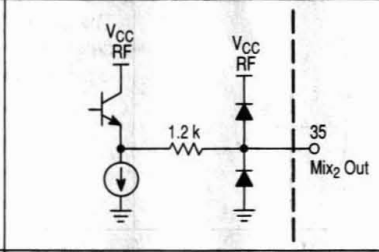
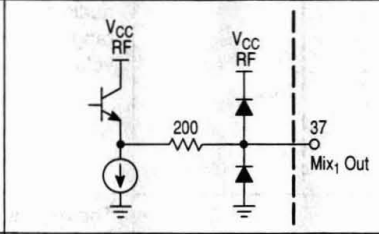
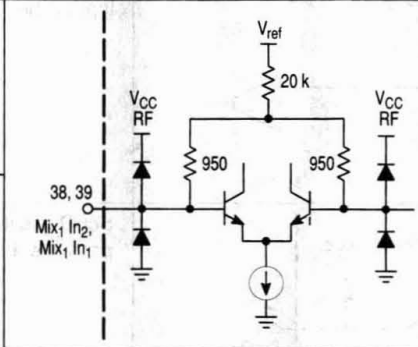
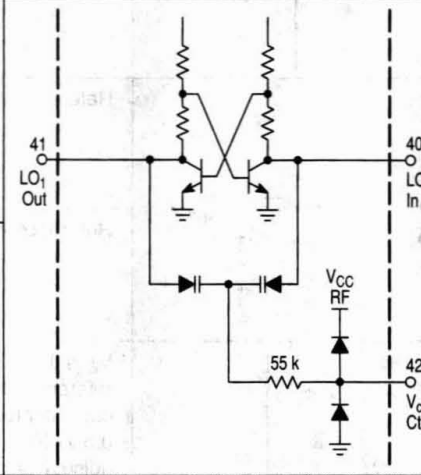
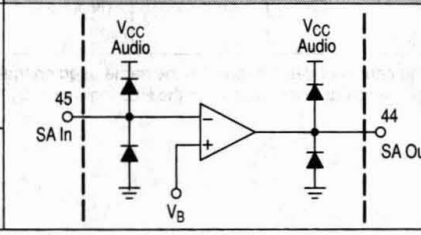
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
16	18	C Cap		C Cap is the compressor rectifier filter capacitor pin. It is recommended that an external filter capacitor to V_{CC} audio be used. A practical capacitor range is 0.1 to 1.0 µF. 0.47 µF is the recommended value.
17	19	C In (Input)		C In is the compressor input. This pin is internally biased and has an input impedance of 12.5 k. C In must be ac–coupled.
18	20	Amp Out (Output)		Microphone amplifier output. The gain is set with external resistors. The feedback resistor should be less than 200 kΩ.
19	21	T_x In (Input)		T_x In is the T_x path input to the microphone amplifier (Mic Amp). An external resistor is connected to this pin to set the Mic Amp gain and input impedance. T_x In must be ac–coupled, too.
20	22	DA In (Input)		The data amplifier input (DA In) resistance is 250 kΩ and must be ac–coupled. Hysteresis is internally provided.
21	23	V_{CC} Audio		V_{CC} audio is the supply for the audio section. It is necessary to adequately filter this pin.
22	24	R_x Audio In (Input)		The R_x audio input resistance is 600 kΩ and must be ac–coupled.
23	25	Det Out (Output)		Det Out is the audio output from the FM detector. This pin is dc–coupled from the FM detector and has an output impedance of 1100 Ω.

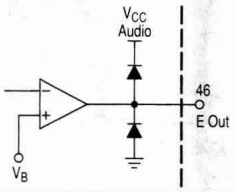
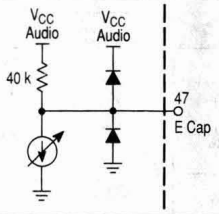
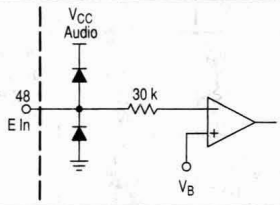
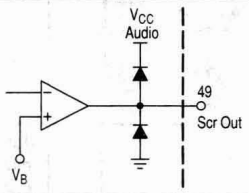
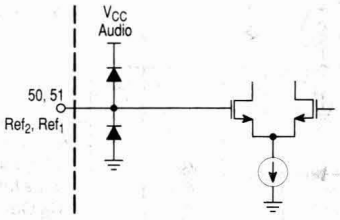
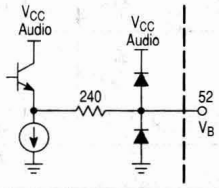
PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
30	26	RSSI		RSSI is the receive signal strength indicator. This pin must be filtered through a capacitor to ground. The capacitance value range should be 0.01 to 0.1 µF. This is also the input to the Carrier Detect comparator. An external R to ground shifts the RSSI voltage.
24	27	Q Coil		A quad coil or ceramic discriminator connects this pin as part of the FM demodulator circuit. DC–couple this pin to V_{CC} RF through the quad coil or the external resistor.
26	29	V_{CC} RF		V_{CC} supply for RF receiver section (1st LO, mixer, limiter, demodulator). Proper supply filtering is needed on this pin too.
25	28	Lim Out		A quad coil or ceramic discriminator are connected to these pins as part of the FM demodulator circuit. A coupling capacitor connects this pin to the quad coil or ceramic discriminator as part of the FM demodulator circuit. This pin can drive coupling capacitors up to 47 pF with no deterioration in performance.
27 28	30 31	Lim C_2 Lim C_1		IF amplifier/limiter capacitor pins. These decoupling capacitors should be 0.1 µF. They determine the IF limiter gain and low frequency bandwidth.
29	32	Lim In (Input)		Signal input for IF amplifier/limiter. Signals should be ac–coupled to this pin. The input impedance is 1.5 kΩ at 455 kHz.
–	33	SGnd RF		This pin is not connected internally but should be grounded to reduce potential coupling between pins.
31	34	Mix_2 In (Input)		Mix_2 In is the second mixer input. Signals are to be ac–coupled to this pin, which is biased internally to V_{CC} RF. The input impedance is 2.8 kΩ at 455 kHz. The input impedance can be reduced by connecting an external resistor to V_{CC} RF.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
32	35	Mix_2 Out (Output)		Mix_2 Out is the second mixer output. The second mixer has a 3 dB bandwidth of 2.5 MHz and an output impedance of 1.5 kΩ. The output current drive is 50 μA.
33	36	Gnd RF		Ground pin for RF section of the IC.
34	37	Mix_1 Out (Output)		The first mixer has a 3 dB IF bandwidth of 13 MHz and an output impedance of 300 Ω. The output current drive is 300 μA and can be programmed for 1.0 mA.
35	38	Mix_1 In_2 (Input)		Signals should be ac–coupled to this pin, which is biased internally to V_{CC} – 1.6 V. The single–ended and differential input impedance are about 1.6 and 1.8 kΩ at 46 MHz, respectively.
36	39	Mix_1 In_1 (Input)		
37 38	40 41	LO_1 In LO_1 Out		Tank Elements, an internal varactor and capacitor matrix for 1st LO multivibrator oscillator are connected to these pins. The oscillator is useable up to 80 MHz.
39	42	V_{cap} Ctrl		V_{cap} Ctrl is the 1st LO varactor control pin. The voltage at this pin is referenced to Gnd Audio and varies the capacitance between LO_1 In and LO_2 Out. An increase in voltage will decrease capacitance.
40	43	Gnd Audio		Ground for audio section of the IC.
41	44	SA Out (Output)		The speaker amplifier gain is set with an external feedback resistor. It should be less than 200 kΩ. The speaker amplifier can be muted through the MPU interface.
42	45	SA In (Input)		An external resistor is connected to the speaker amplifier input (SA In). This will set the gain and input impedance and must be ac–coupled.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol/ Type	Equivalent Internal Circuit (52 Pin QFP)	Description
LQFP–48	QFP–52			
43	46	E Out (Output)		The output level of the expander output is determined by the volume control. Volume control is programmable through the MPU interface.
44	47	E Cap		E Cap is the expander rectifier filter capacitor pin. Connect an external filter capacitor between V_{CC} audio and E Cap. The recommended capacitance range is 0.1 to 1.0 µF. 0.47 µF is the suggested value.
45	48	E In (Input)		The expander input pin is internally biased and has input impedance of 30 kΩ.
46	49	Scr Out (Output)		Scr Out is the R_x audio output. An internal low pass filter has a –3 dB bandwidth of 4.0 kHz.
–	50	Ref_2		Reference voltage input for Low Battery Detect #2.
–	51	Ref_1		Reference voltage input for Low Battery Detect #1.
47	52	V_B		V_B is the internal half supply analog ground reference. This pin must be filtered with a capacitor to ground. A typical capacitor range of 0.5 to 10 µF is desired to reduce crosstalk and noise. It is important to keep this capacitor value equal to the PLL V_{ref} capacitor due to logic timing (Note 9).

NOTE: 9. A capacitor range of 0.5 to 10 µF is recommended. The capacitor value should be the same used on the V_B pin (Pin 52). An additional high quality parallel capacitor of 0.01 µF is essential to filter out spikes originating from the PLL logic circuitry.

The following text, graphics, tables and schematics are provided to the user as a source of valuable technical information about the Universal Cordless Telephone IC. This information originates from thorough evaluation of the device performance for the US and French applications. This data was obtained by using units from typical wafer lots. It is important to note that the forgoing data and information was from a limited number of units. By no means is the user to assume that the data following is a guaranteed parametric. Only the minimum and maximum limits identified in the electrical characteristics tables found earlier in this spec are guaranteed.

General Circuit Description

The MC13110A/B and MC13111A/B are a low power dual conversion narrowband FM receiver designed for applications up to 80 MHz carrier frequency. This device is primarily designated to be used for the 49 MHz cordless phone (CT–0), but has other applications such as low data rate narrowband data links and as a backend device for 900 MHz systems where baseband analog processing is required. This device contains a first and second mixer, limiter, demodulator, extended range receive signal strength (RSSI), receive and transmit baseband processing, dual programmable PLL, low battery detect, and serial interface for microprocessor control. The FM receiver can also be used with either a quadrature coil or ceramic resonator. Refer to the Pin Function Description table for the simplified internal circuit schematic and description of this device.

DC Current and Battery Detect

Figures 3 through 6 are the current consumption for Inactive, Standby, Receive, and Active modes versus supply voltages. Figures 7 and 8 show the typical behavior of current consumption in relation to temperature. The relationship of additional current draw due to IP3 bit set to <1> and supply voltage are shown in Figures 9 and 10.

For the Low Battery Detect, the user has the option to operate the IC in the programmable or non–programmable modes. Note that the 48 pin package can only be used in the programmable mode. Figure 128 describes this operation (refer to the Serial Interface section under Clock Divider Register).

In the programmable mode several different internal threshold levels are available (Figure 2). The bits are set through the SCF Clock Divider Register as shown in Figures 108 and 126. The reference for the internal divider network is V_{CC} Audio. The voltages on the internal divider network are compared to the Internal Reference Voltage, VB, generated by an internal source. Since the internal comparator used is non–inverting, a high at V_{CC} Audio will yield a high at the battery detect output, and vice versa for V_{CC} Audio set to a low level. For the 52 pin package option, the Ref 1 and Ref 2 pins need to be tied to V_{CC} when used in the programmable mode. It is essential to keep the external reference pins above Gnd to prevent any possible power–on reset to be activated.

When considering the non–programmable mode (bits set to <000>) for the 52 pin package, the Ref 1 and Ref 2 pins become the comparators reference. An internal switch is activated when the non–programmable mode is chosen connecting Ref 1 and Ref 2. Here, two external precision resistor dividers are used to set independent thresholds for two battery detect hysteresis comparators. The voltages on Ref 1 and Ref 2 are again compared to the internally generated 1.5 V reference voltage (VB).

The Low Battery Detect threshold tolerance can be improved by adjusting a trim–pot in the external resistor divider (user designed). The initial tolerance of the internal reference voltage (VB) is ±6.0%. Alternately, the tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming (refer to the Serial Interface section, Figure 131). The internal reference can be measured directly at the "VB" pin. During final test of the telephone, the VB internal reference voltage is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the combo IC is powered up. The Low Battery Detect outputs are open collector. The battery detect levels will depend on the accuracy of the VB voltage. Figure 12 indicates that the VB voltage is fairly flat over temperature.

Figure 2. Internal Low Battery Detect Levels (with VB = 1.5 V)

Battery Detect Select	Ramping Up (V)	Ramping Down (V)	Average (V)	Hysteresis (mV)
0	–	–	–	–
1	2.867	2.861	2.864	4.0
2	2.953	2.947	2.950	6.0
3	3.039	3.031	3.035	8.0
4	3.207	3.199	3.204	8.0
5	3.291	3.285	3.288	6.0
6	3.375	3.367	3.371	8.0
7	3.461	3.453	3.457	8.0

NOTE: 10. Battery Detect Select 0 is the non–programmable operating mode.

DC CURRENT

Figure 3. Current versus Supply Voltage Inactive Mode

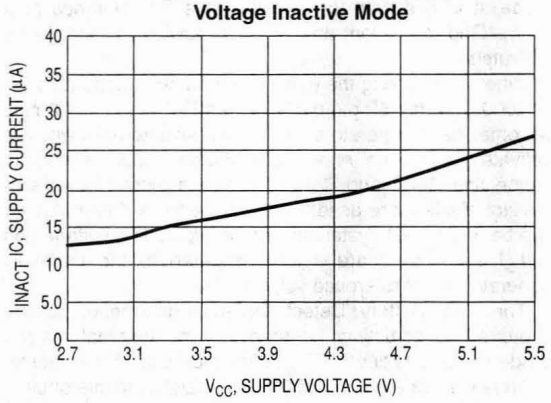


Figure 4. Current versus Supply Voltage Standby Mode, MCU Clock Output – On at 2.048 MHz

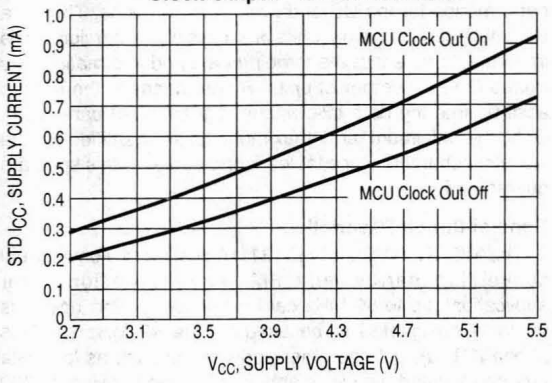


Figure 5. Current versus Supply Voltage Receive Mode

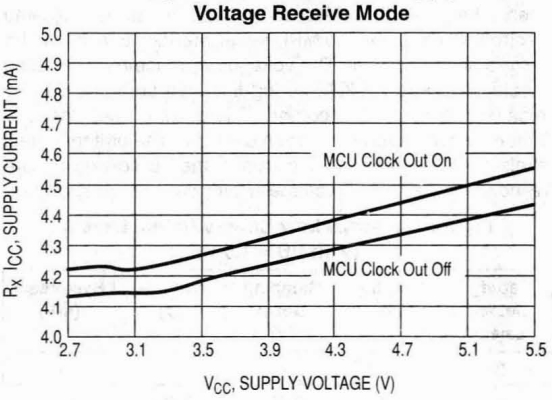


Figure 6. Current versus Supply Voltage Active Mode

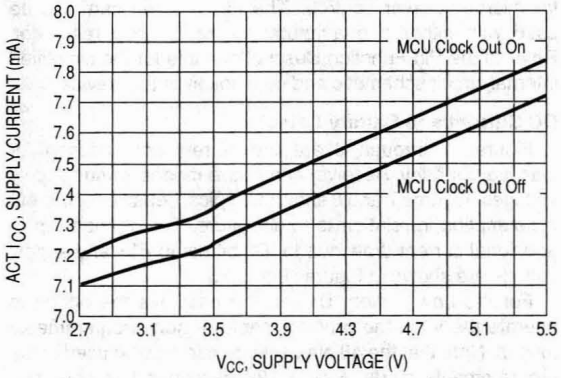


Figure 7. Current versus Temperature Normalized to 25°C

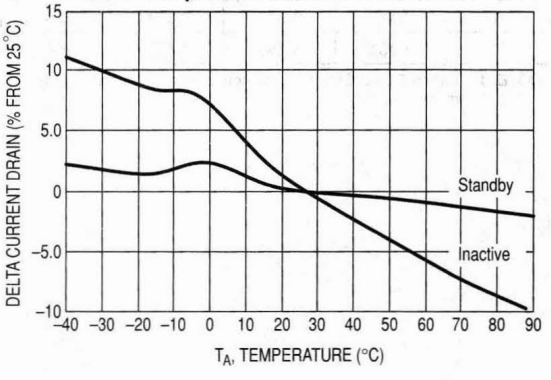


Figure 8. Current versus Temperature Normalized to 25°C

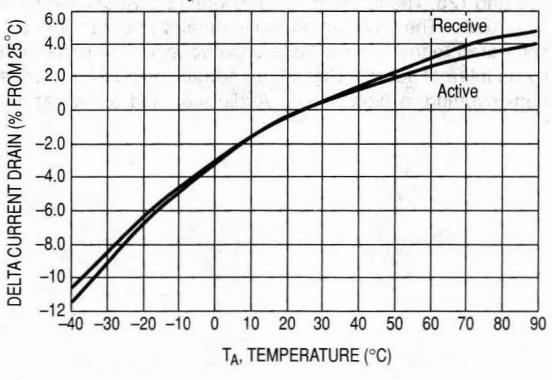


Figure 9. Additional Supply Current Consumption versus Supply Voltage, IP3 = <1>

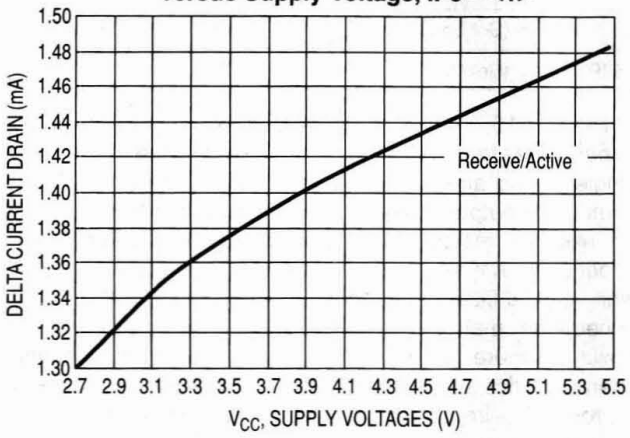


Figure 10. Additional IP3 Supply Current Consumption versus Temperature Normalized to 25°C

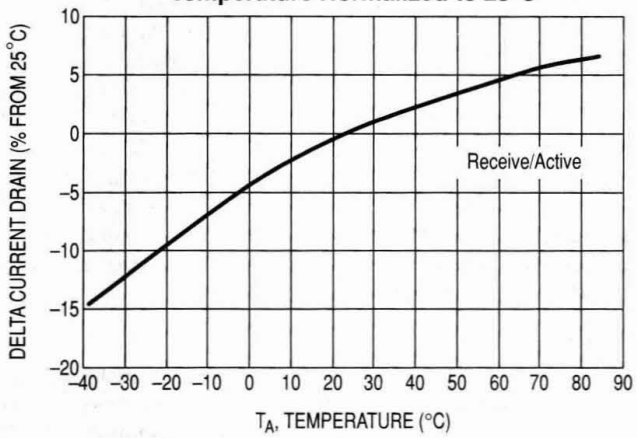


Figure 11. Current Standby Mode versus MCU Clock Output

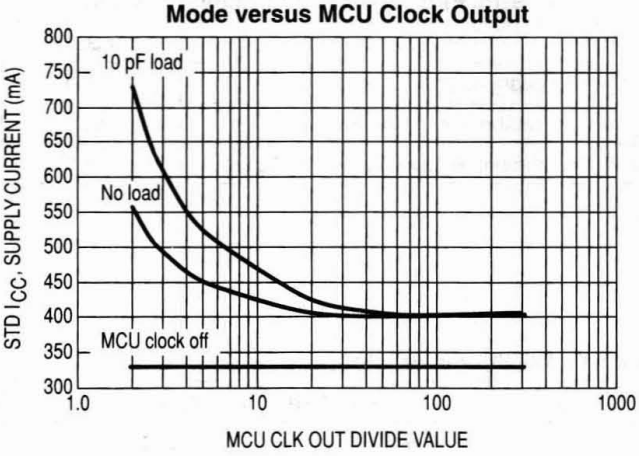
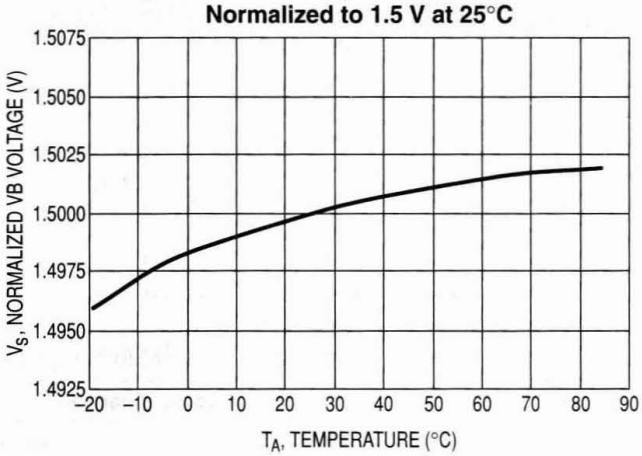


Figure 12. VB Voltage versus Temperature Normalized to 1.5 V at 25°C



FIRST AND SECOND MIXER

Mixer Description

The 1st and 2nd mixers are similar in design. Both are double balanced to suppress the LO and the input frequencies to give only the sum and difference frequencies at the mixer output. Typically the LO is suppressed better than –50 dB for the first mixer and better than –40 dB for the second mixer. The gain of the 1st mixer has a –3.0 dB corner at approximately 13 MHz and is used at a 10.7 MHz IF. It has an output impedance of 300 Ω and matches to a typical 10.7 MHz ceramic filter with a source and load impedance of 330 Ω. A series resistor may be used to raise the impedance for use with crystal filters. They typically have an input impedance much greater than 330 Ω.

First Mixer

Figures 17 through 20 show the first mixer transfer curves for the voltage conversion gain, output level, and intermodulation. Notice that there is approximately 10 dB linearity improvement when the "IP3 Increase" bit is set to <1>. The "IP3 Increase" bit is a programmable bit as shown in the Serial Programmable Interface section under the R_X Counter Latch Register. The IP3 = <1> option will increase the supply current demand by 1.3 mA.

Figure 13. First Mixer Input and Output Impedance Schematic

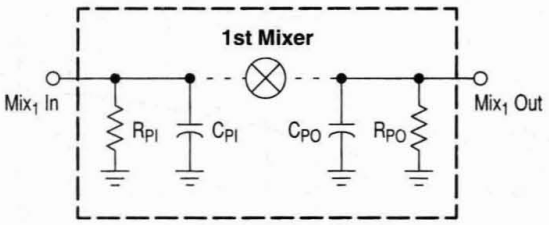


Figure 14. First Mixer Output Impedance

Unit	Output Impedance
B IP3 = <0> (Set Low)	304 Ω // 3.7 pF
B IP3 = <1> (Set High)	300 Ω // 4.0 pF

Figures 13, 14, and 16 represent the input and output impedance for the first mixer. Notice that the input single–ended and differential impedances are basically the same. The output impedance as described in Figure 14 will be used to match to a ceramic or crystal filter's input impedance. A typical ceramic filter input impedance is 330 Ω while crystal filter input impedance is usually 1500 Ω. Exact impedance matching to ceramic filters are not critical, however, more attention needs to be given to the filter characteristics of a crystal filter. Crystal filters are much narrower. It is important to accurately match to these filters to guaranty a reasonable response.

To find the IF bandwidth response of the first mixer refer to Figure 22. The –3.0 dB bandwidth point is approximately 13 MHz. Figure 15 is a summary of the first mixer feedthrough parameters.

Figure 15. First Mixer Feedthrough Parameters

Parameter	(dBm)
1st LO Feedthrough @ Mix_1 In_1	–70.0
1st LO Feedthrough @ Mix_1 Out	–55.5
RF Feedthrough @ Mix_1 Out with –30 dBm	–61.0

Figure 16. First Mixer Input Impedance over Input Frequency

Unit	US Center Channels		France Center Channels	
	49 MHz	46 MHz	41 MHz	26 MHz
Single–Ended	1550 Ω // 3.7 pF	1560 Ω // 3.7 pF	1570 Ω // 3.8 pF	1650 Ω // 3.7 pF
Differential	1600 Ω // 1.8 pF	1610 Ω // 1.8 pF	1670 Ω // 1.8 pF	1710 Ω // 1.8 pF

Note: 11. Single–Ended data is from measured results. Differential data is from simulated results.

FIRST MIXER

Figure 17. First Mixer Voltage Conversion Gain, IP3_bit = 0

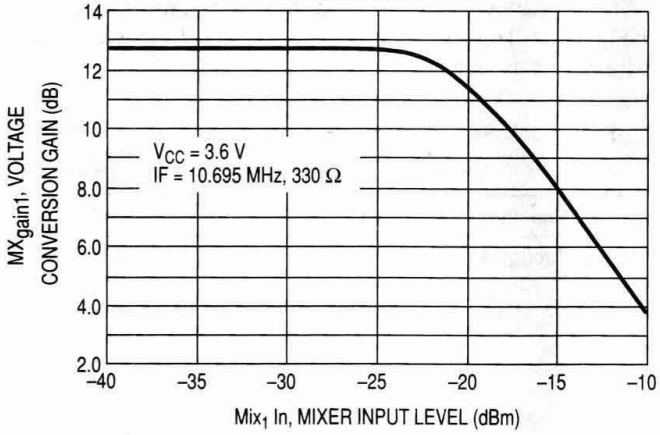


Figure 18. First Mixer Voltage Conversion Gain, IP3_bit = 1

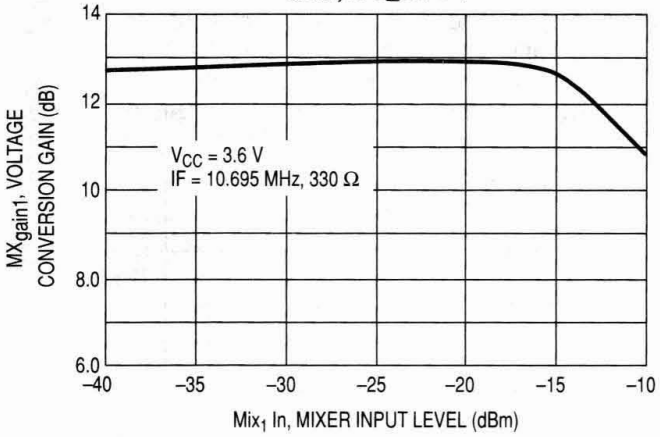


Figure 19. First Mixer Output Level and Intermodulation, IP3_bit = 0

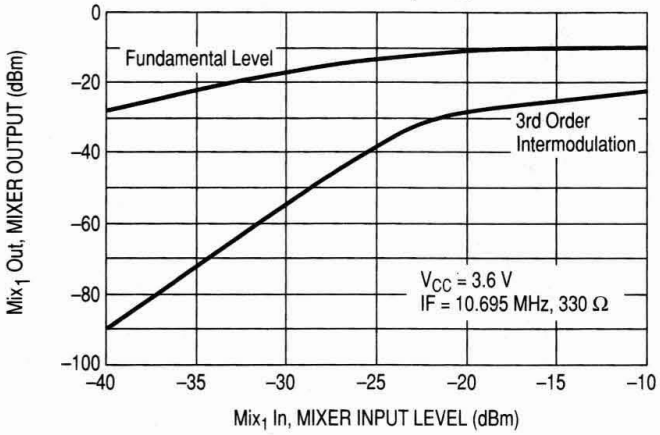


Figure 20. First Mixer Output Level and Intermodulation, IP3_bit = 1

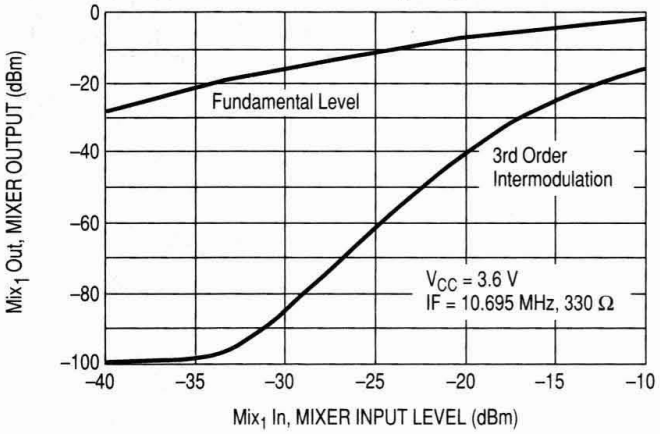


Figure 21. First Mixer Compression versus Supply Voltage

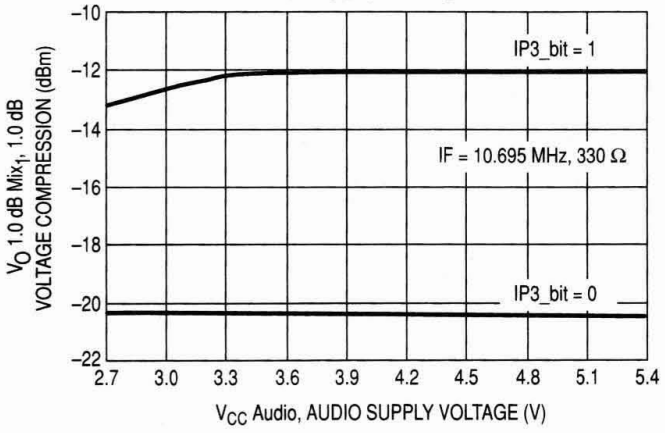
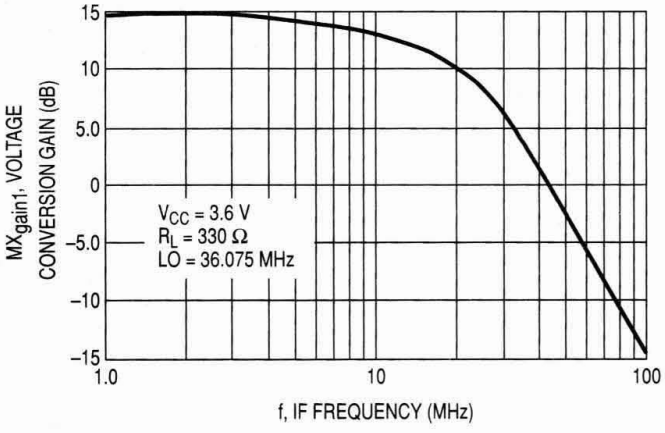


Figure 22. First IF Bandwidth



Second Mixer

Figures 26 through 29 represents the second mixer transfer characteristics for the voltage conversion gain, output level, and intermodulation. There is a slight improvement in gain when the "IP3 bit" is set to <1> for the second mixer. (Note: This is the same programmable bit discussed earlier in the section.)

Figure 23. Second Mixer Input and Output Impedance Schematic

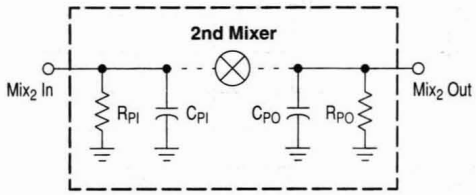


Figure 24. Second Mixer Input and Output Impedances

Unit	Input Impedance R_{PI} // C_{PI}	Output Impedance R_{PO} // C_{PO}
IP3 = <0> (Set Low)	2817 Ω // 3.6 pF	1493 Ω // 6.1 pF
IP3 = <1> (Set High)	2817 Ω // 3.6 pF	1435 Ω // 6.2 pF

The 2nd mixer input impedance is typically 2.8 kΩ. It requires an external 360 Ω parallel resistor for use with a standard 330 Ω, 10.7 MHz ceramic filter. The second mixer output impedance is 1.5 kΩ making it suitable to match standard 455 kHz ceramic filters.

The IF bandwidth response of the second mixer is shown in Figure 31. The –3.0 dB corner is 2.5 MHz. The feedthrough parameters are summarized in Figure 25.

Figure 25. Second Mixer Feedthrough Parameters

Parameter	(dBm)
2nd LO Feedthrough @ Mix_2 Out	–42.9
IF Feedthrough @ Mix_2 Out with –30 dBm	–61.7

SECOND MIXER

Figure 26. Second Mixer Conversion Gain, IP3_bit = 0

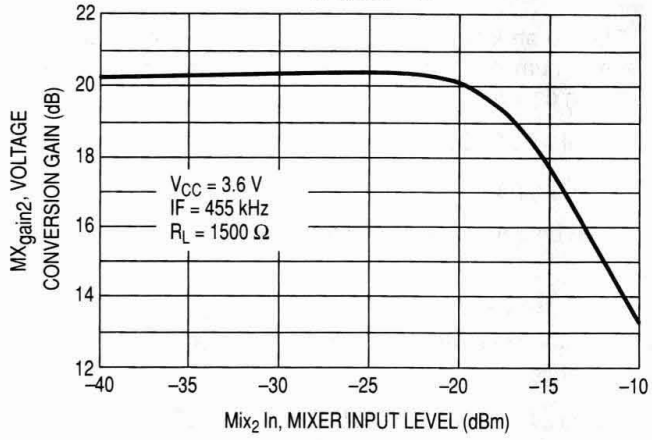


Figure 27. Second Mixer Conversion Gain, IP3_bit = 1

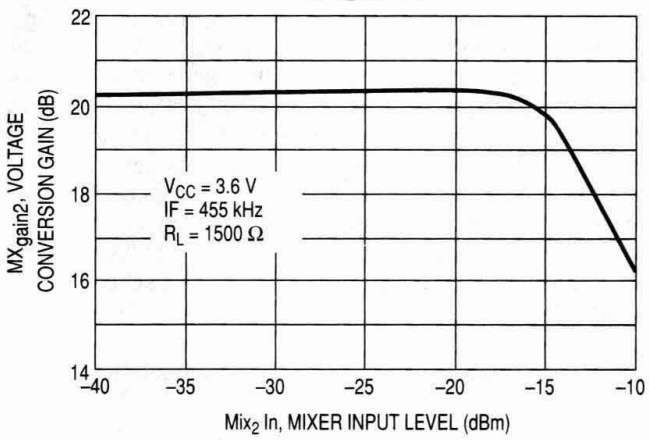


Figure 28. Second Mixer Output Level and Intermodulation, IP3_bit = 0

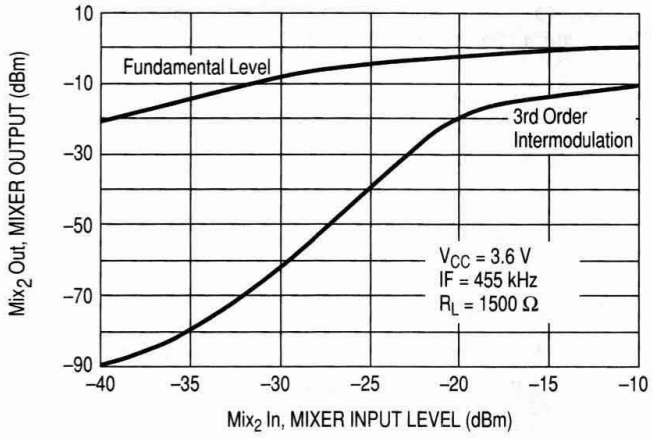


Figure 29. Second Mixer Output Level and Intermodulation, IP3_bit = 1

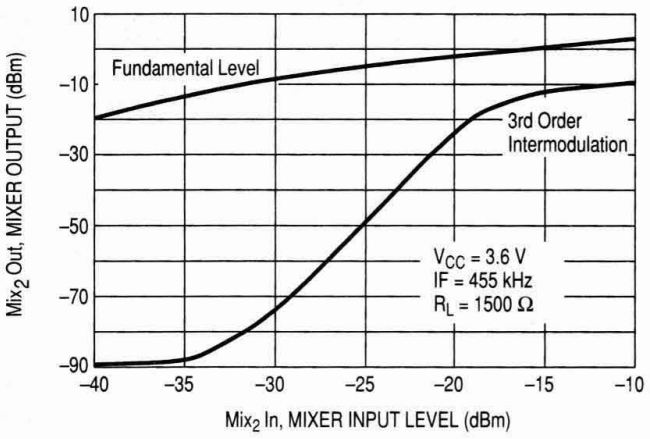


Figure 30. Second Mixer Compression versus Supply Voltage

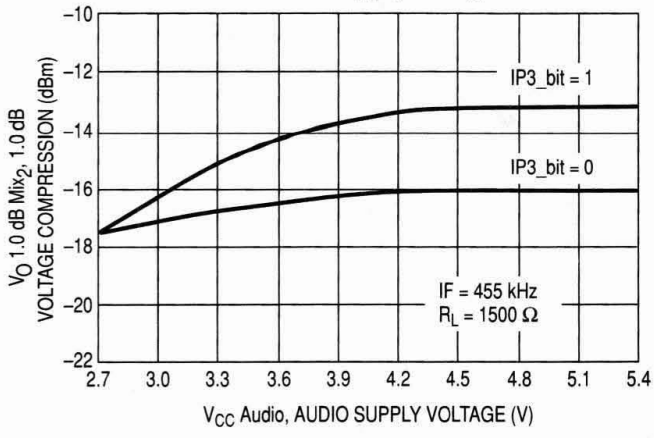
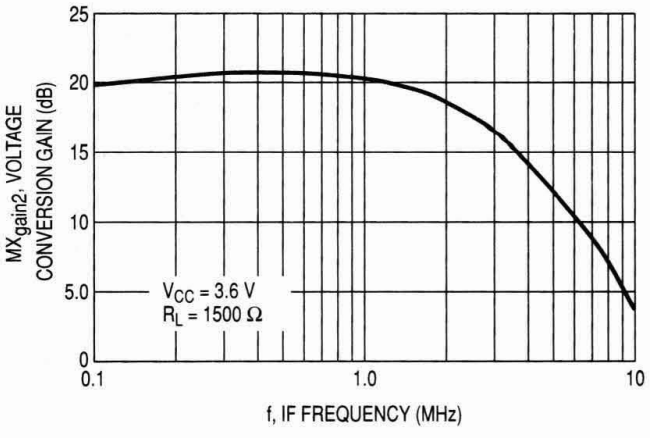


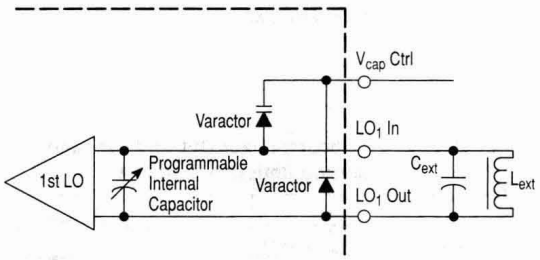
Figure 31. Second IF Bandwidth



First Local Oscillator

The 1st LO is a multi–vibrator oscillator. The tank circuit is composed of a parallel external capacitance and inductance, internal programmable capacitor matrix, and internal varactor. The local oscillator requires a voltage controlled input to the internal varactor and an external loop filter driven by on–board phase–lock control loop (PLL). The 1st LO internal component values have a tolerance of ±15%. A typical dc bias level on the LO Input and LO Output is 0.45 Vdc. The temperature coefficient of the varactor is +0.08%/°C. The curve in Figure 33 is the varactor control voltage range as it relates to varactor capacitance. It represents the expected internal capacitance for a given control voltage (V_{cap}Ctrl) of the MC13110A/B and MC13111A/B. Figure 32 shows a representative schematic of the first LO function.

Figure 32. First Local Oscillator Schematic



To select the proper L_{ext} and C_{ext} we can do the following analysis. From Figure 34 it is observed that an inductor will have a significant affect on first LO performance, especially over frequency. The overall minimum Q required for first LO to function as it relates to the LO frequency is also given in Figure 34.

Choose an inductor value, say 470 nH. From Figure 34, the minimum operating Q is approximately 25. From the following equation:

$$Q\ Coil = R_p/X\ Coil$$

where: R_p = parallel equivalent impedance (Figure 35).

C_{ext} can be determined as follows:

$$f_{LO} = \frac{1}{2\pi\sqrt{L_{ext}C_{ext}}}$$

where: L_{ext} = external inductance, C_{ext} = external capacitance.

Figure 34 clearly indicates that for lower coil values, higher quality factors (Q) are required for the first LO to function properly. Also, lower LO frequencies need higher Q's. In Figure 35 the internal programmable capacitor selection relative to the first LO frequency and the parallel impedance is shown. This information will help the user to decide what inductor (L_{ext}) to choose for best performance in terms of Q.

Refer to the Auxiliary Register in the Serial Interface Section for further discussion on LO programmability.

FIRST LOCAL OSCILLATOR

Figure 33. First LO Varicap Capacitance versus Control Voltage

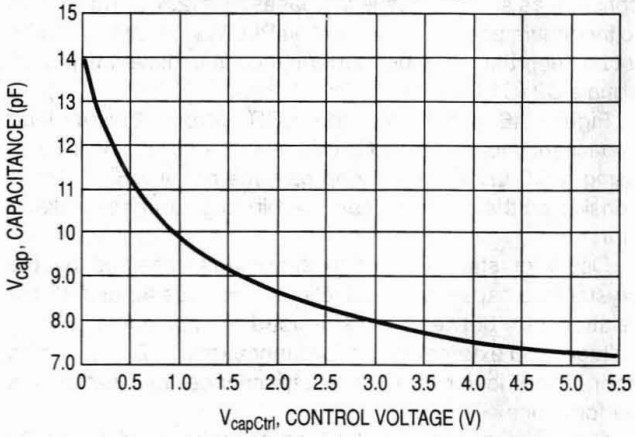


Figure 34. First LO Minimum Required Overall Q Value versus Inductor Value

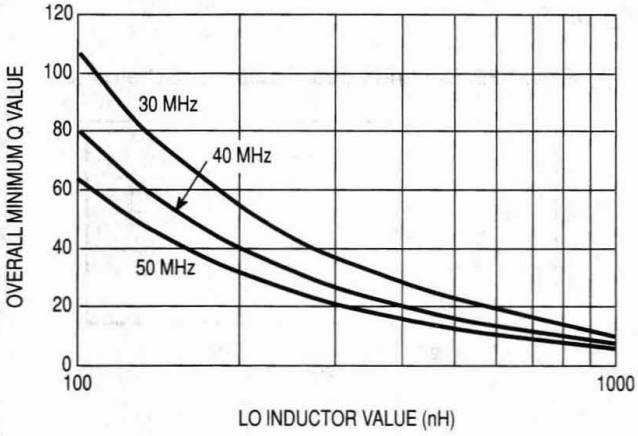


Figure 35. Representative Parallel Impedance versus Capacitor Select

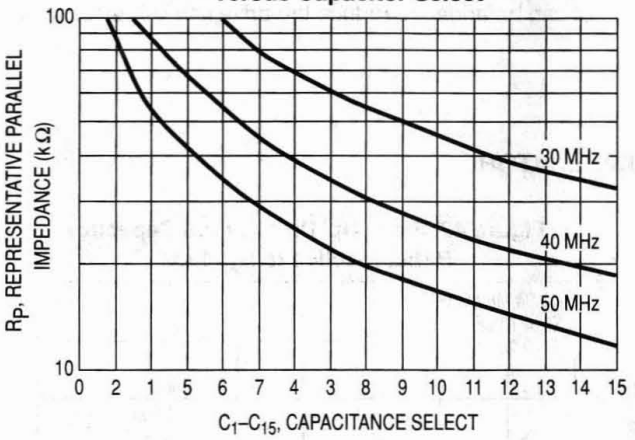


Figure 36. Varicap Value at V_{CV} = 1.0 V Over Temperature

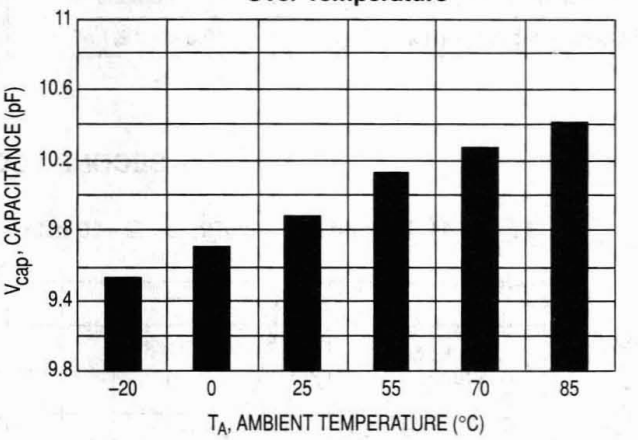


Figure 37. Control Voltage versus Channel Number, U.S. Handset Application

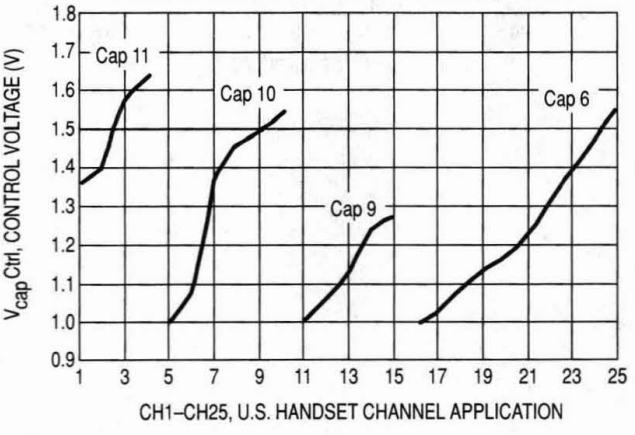
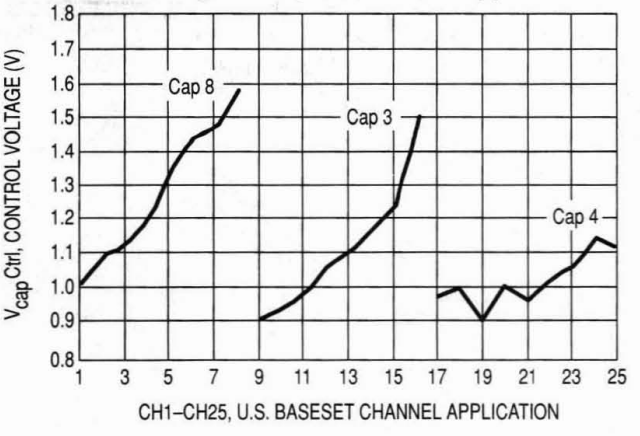


Figure 38. Control Voltage versus Channel Number, U.S. Baseset Application



Second Local Oscillator

The 2nd LO is a CMOS oscillator. It is used as the PLL reference oscillator and local oscillator for the second frequency conversion in the RF receiver. It is designed to utilize an external parallel resonant crystal. See schematic in Figure 39.

Figure 39. Second Local Oscillator Schematic

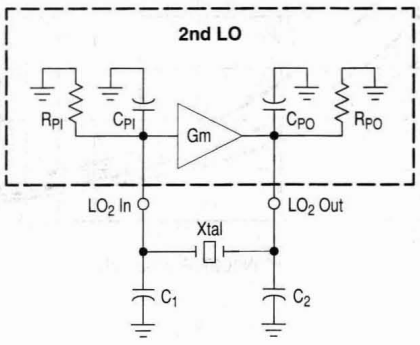


Figure 40. Second Local Oscillator Input and Output Impedance

Input Impedance (R_{PI} // C_{PI})	11.6 kΩ // 2.9 pF
Output Impedance (R_{PO} // C_{PO})	9.6 kΩ // 2.7 pF

Figure 41 shows a typical gain/phase response of the second local oscillator. Load capacitance (C_L), equivalent series resistance (ESR), and even supply voltage will have and affect on the 2nd LO response as shown in Figures 45 and 46. Except for the standby mode open loop gain is fairly constant as supply voltage increases from 2.5 V. This is due to the regulated voltage of 2.5 V on PLL V_{ref}. From the graphs it can seen that optimum performance is achieved when C1 equals C2 (C1/C2 = 1).

Figure 46 represents the ESR versus crystal load capacitance for the 2nd LO. This relationship was defined by using a 6.0 dB minimum loop gain margin at 3.6 V. This is considered the minimum gain margin to guarantee oscillator start–up.

Oscillator start–up is also significantly affected by the crystal load capacitance selection. In Figures 42 and 43 the relationship between crystal load capacitance, supply voltage, and external load capacitance ratio (C2/C1), can be seen. The lower the load capacitance the better the performance.

Given the desired crystal load capacitance, C1 and C2 can be determined from Figure 47. It is also interesting to point out that current consumption increases when C1 ≠ C2, as shown in Figure 44.

Be careful not to overdrive the crystal. This could cause a noise problem. An external series resistor on the crystal output can be added to reduce the drive level, if necessary.

SECOND LOCAL OSCILLATOR

Figure 41. Second LO Gain/Phase @ –10 dBm

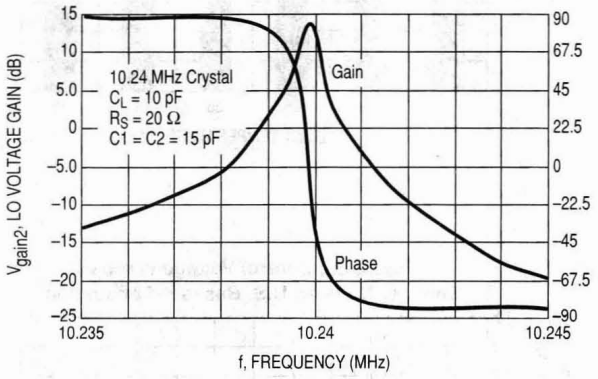
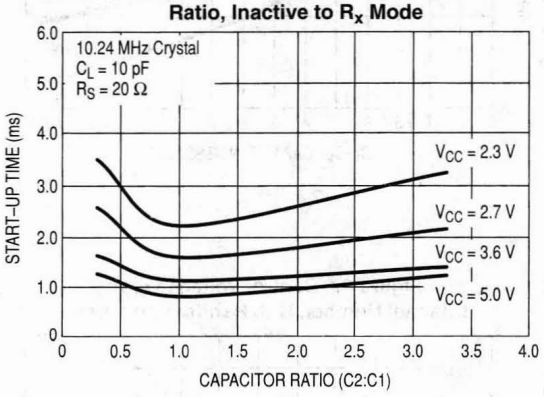


Figure 42. Start–Up Time versus Capacitor Ratio, Inactive to R_x Mode



SECOND LOCAL OSCILLATOR

Figure 43. Start–Up Time versus Capacitor Ratio, Inactive to R_x Mode

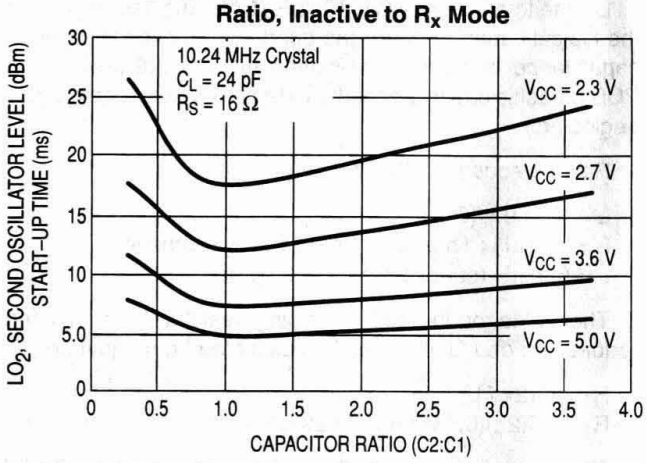


Figure 44. Second LO Current Consumption versus Capacitor Ratio

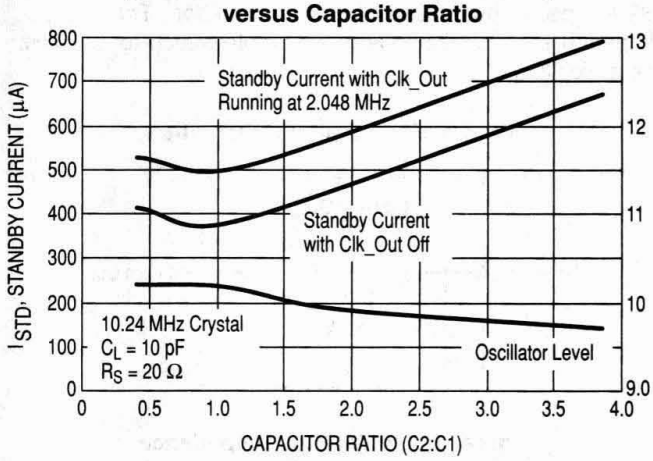

Standby Current with Clk_Out Running at 2.048 MHz
Standby Current with Clk_Out Off
10.24 MHz Crystal
C_L = 10 pF
R_S = 20 Ω
Oscillator Level
I_{STD}, STANDBY CURRENT (μA)
CAPACITOR RATIO (C2:C1)

Figure 45. Maximum Open Loop Gain versus Capacitor Ratio

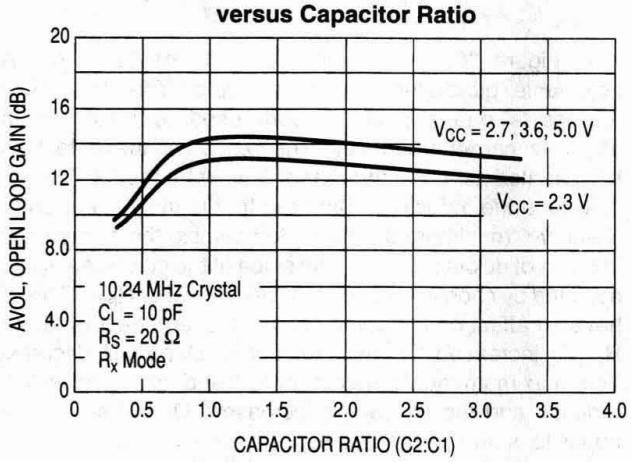


Figure 46. Maximum Allowable Equivalent Series Resistance (ESR) versus Crystal Load Capacitance

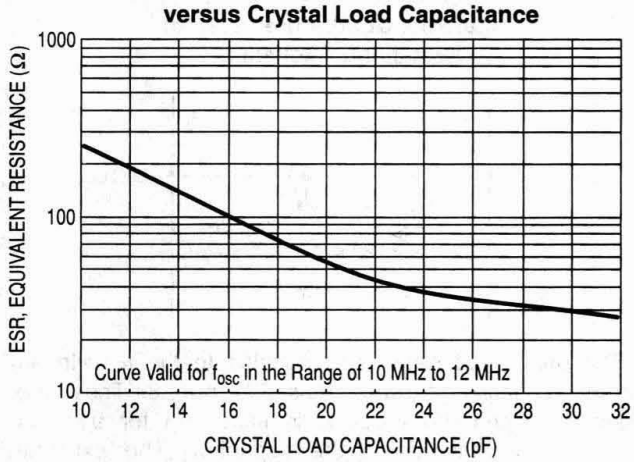
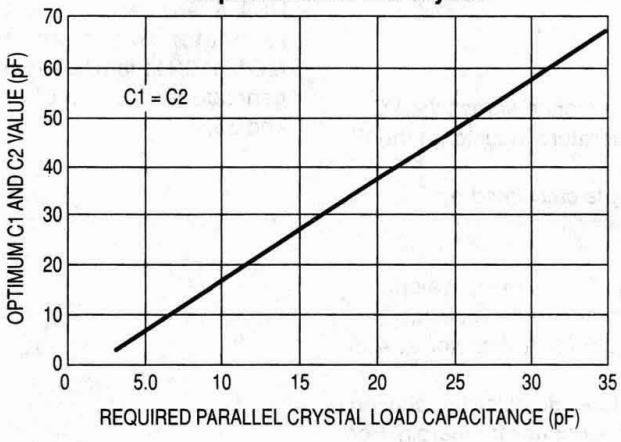


Figure 47. Optimum Value for C1 and C2 versus Equivalent Required Parallel Capacitance of the Crystal



IF Limiter and Demodulator

The limiting IF amplifier typically has about 110 dB of gain; the frequency response starts rolling off at 1.0 MHz. Decoupling capacitors should be placed close to Pins 31 and 32 to ensure low noise and stable operation. The IF input impedance is 1.5 kΩ. This is a suitable match to 455 kHz ceramic filters.

Figure 48. IF Limiter Schematic

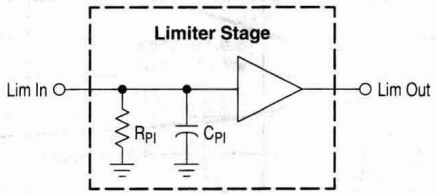
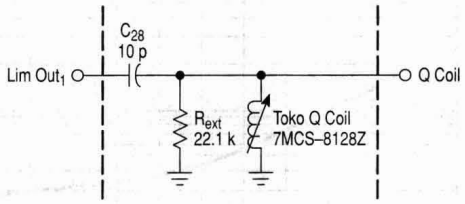


Figure 49. Limiter Input Impedance

Unit	Input Impedance (R_{PI})	Input Impedance (C_{PI})
Lim In	1538 Ω	15.7 pF

Figure 50. Quadrature Detector Demodulator Schematic



The quadrature detector is coupled to the IF with an external capacitor between Pins 27 and 28. Thus, the recovered signal level output is increased for a given bandwidth by increasing the capacitor. The external quadrature component may be either a LCR resonant circuit, which may be adjustable, or a ceramic resonator which is usually fixed tuned. (More on ceramic resonators later.)

The bandwidth performance of the detector is controlled by the loaded Q of the LC tank circuit (Figure 50). The following equation defines the components which set the detector circuit's bandwidth:

(1) $R_T = Q\ X_L$,

where R_T is the equivalent shunt resistance across the LC tank. X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi\ f\ L$).

The 455 kHz IF center frequency is calculated by:

(2) $f_c = [2\pi\ (L\ Cp)^{1/2}] - 1$

where L is the parallel tank inductor. Cp is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a detector at 455 kHz and a specific loaded Q:

The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass for margin. For an IF frequency of 455 kHz and an IF bandpass of 20 kHz, the IF bandpass Q is approximately 23; the loaded Q of the quadrature tank is chosen slightly lower at 15.

Example:

Let the total external C = 180 pF. (Note: the capacitance is the typical capacitance for the quad coil.) Since the external capacitance is much greater than the internal device and PCB parasitic capacitance, the parasitic capacitance may be neglected.

Rewrite equation (2) and solve for L:

$L = (0.159)^2/(C\ f_c^2)$
$L = 678\ \mu H$; Thus, a standard value is chosen:
$L = 680\ \mu H$ (surface mount inductor)

The value of the total damping resistor to obtain the required loaded Q of 15 can be calculated from equation (1):

$R_T = Q(2\pi\ f\ L)$
$R_T = 15(2\pi)(0.455)(680) = 29.5\ k\Omega$

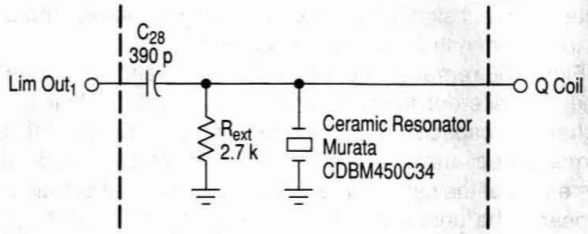
The internal resistance, R_{int} at the quadrature tank Pin 27 is approximately 100 kΩ and is considered in determining the external resistance, R_{ext} which is calculated from:

$R_{ext} = ((R_T)(R_{int}))/(R_{int} - R_T)$
$R_{ext} = 41.8\ k\Omega$;Thus, choose a standard value:
$R_{ext} = 39\ k\Omega$

In Figure 50, the R_{ext} is chosen to be 22.1 kΩ. An adjustable quadrature coil is selected. This tank circuit represents one popular network used to match to the 455 kHz carrier frequency. The output of the detector is represented as a "S–curve" as shown in Figure 52. The goal is to tune the inductor in the area that is most linear on the "S–curve" (minimum distortion) to optimize the performance in terms of dc output level. The slope of the curve can also be adjusted by choosing higher or lower values of R_{ext}. This will have an affect on the audio output level and bandwidth. As R_{ext} is increased the detector output slope will decrease. The maximum audio output swing and distortion will be reduced and the bandwidth increased. Of course, just the opposite is true for smaller R_{ext}.

A ceramic discriminator is recommended for the quadrature circuit in applications where fixed tuning is desired. The ceramic discriminator and a 5.6 kΩ resistor are placed from Pin 27 to V_{CC}. A 22 pF capacitor is placed from Pin 28 to 27 to properly drive the discriminator. MuRata Erie has designed a resonator for this part (CDBM455C48 for USA & A/P regions and CDBM450C48 for Europe). This resonator has been designed specifically for the MC13110/111 family. Figure 51 shows the schematic used to generate the "S–curve" and waveform shown in Figure 54 and 55.

Figure 51. Ceramic Resonator Demodulator Schematic with Murata CDBM450C48



(CDBM455C48 US; CDBM450C48 France)

The "S–curve" for the ceramic discriminator shown in Figure 54 is centered around 450 kHz. It is for the French application. The same resonator is also used for the US application and is centered around 455 kHz. Clearly, the "S–curves" for the resonator and quad coil have very similar limiter outputs. As discussed previously, the slope of the "S–curve" centered around the center frequency can be controlled by the parallel resistor, R_{ext}. Distortion, bandwidth, and audio output level will be affected.

IF LIMITER AND DEMODULATION

Figure 52. S–Curve of Limiter Discriminator with Quadrature Coil

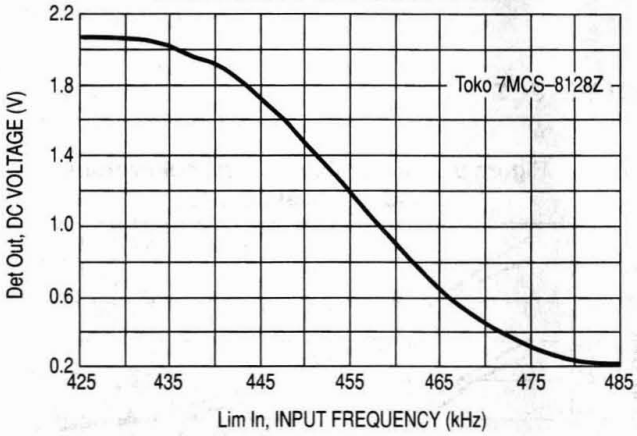


Figure 53. Typical Limiter Output Waveform with Quadrature Coil

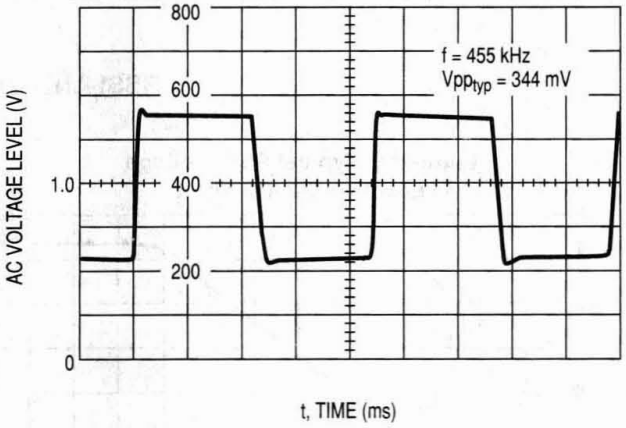


Figure 54. S–Curve of Limiter Discriminator with Ceramic Resonator

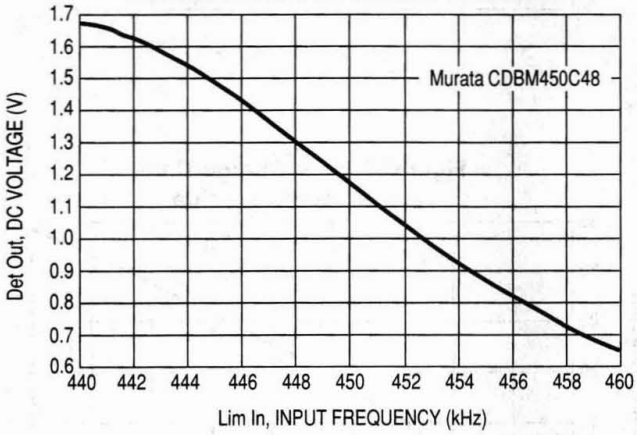
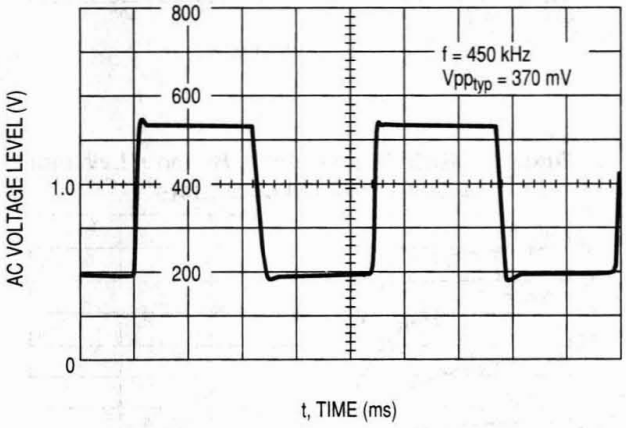


Figure 55. Typical Limiter Output Waveform with Ceramic Resonator



RSSI and Carrier Detect

The Received Signal Strength Indicator (RSSI) indicates the strength of the IF level. The output is proportional to the logarithm of the IF input signal magnitude. RSSI dynamic range is typically 80 dB. A 187 kΩ resistor to ground is provided internally to the IC. This internal resistor converts the RSSI current to a voltage level at the "RSSI" pin. To improve the RSSI accuracy over temperature an internal compensated reference is used. Figure 56 shows the RSSI versus RF input. The slope of the curve is 16.5 mV/dB.

The Carrier Detect Output (CD Out) is an open–collector transistor output. An external pull–up resistor of 100 kΩ will be required to bias this device. To form a carrier detect filter a capacitor needs to be connected from the RSSI pin to ground. The carrier detect threshold is programmable through the MPU interface (see "Carrier Detect Threshold Programming" in the serial interface section). The range can be scaled by connecting additional external resistance from the RSSI pin to ground in parallel with the capacitor. From Figure 57, the affect of an external resistor at RSSI on the carrier detect level can be noticed. Since there is hysteresis in the carrier detect comparator, one trip level can be found when the input signal is increased while the another one can be found when the signal is decreased.

Figure 58 represents the RSSI ripple in relation to the RF input for different filtering capacitors at RSSI. Clearly, the higher the capacitor, the less the ripple. However, at low carrier detect thresholds, the ripple might supersede the hysteresis of the carrier detect. The carrier detect output may appear to be unstable. Using a large capacitor will help to stabilize the RSSI level, but RSSI charge time will be affected. Figure 59 shows this relationship.

The user must decide on a compromise between the RSSI ripple and RSSI start–up time. Choose a 0.01 µf capacitor as a starting point. For low carrier detect threshold settings, a 0.047 µf capacitor is recommended.

RSSI AND CARRIER DETECT

Figure 56. Typical RSSI Voltage Level versus RF Input

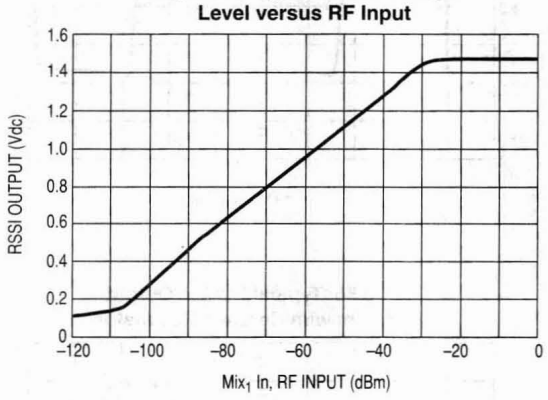


Figure 57. Carrier Detect Threshold versus External RSSI Resistor

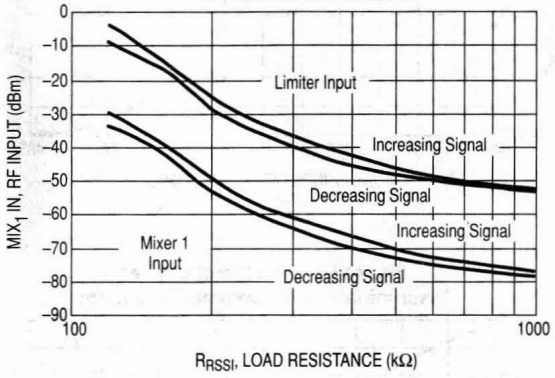


Figure 58. RSSI Ripple versus RF Input Level for Different RSSI Capacitors

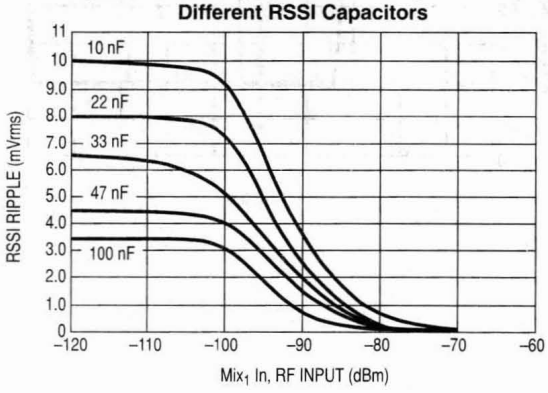
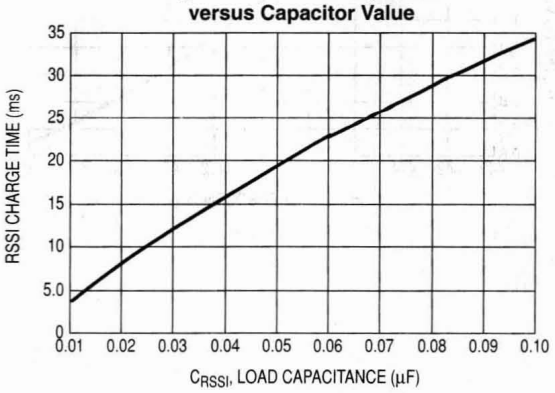


Figure 59. RSSI Charge Time versus Capacitor Value



RF System Performance

The sensitivity of the IC is typically 0.4 μVrms matched (single ended or differential) with no preamp. To achieve suitable system performance, a preamp and passive duplexer may be used. In production final test, each section of the IC is separately tested to guarantee its system performance in the specific application. The preamp and duplexer (differential, matched input) yields typically –115 dBm @ 12 dB SINAD sensitivity performance under full duplex operation. See Figure 45 and 48.

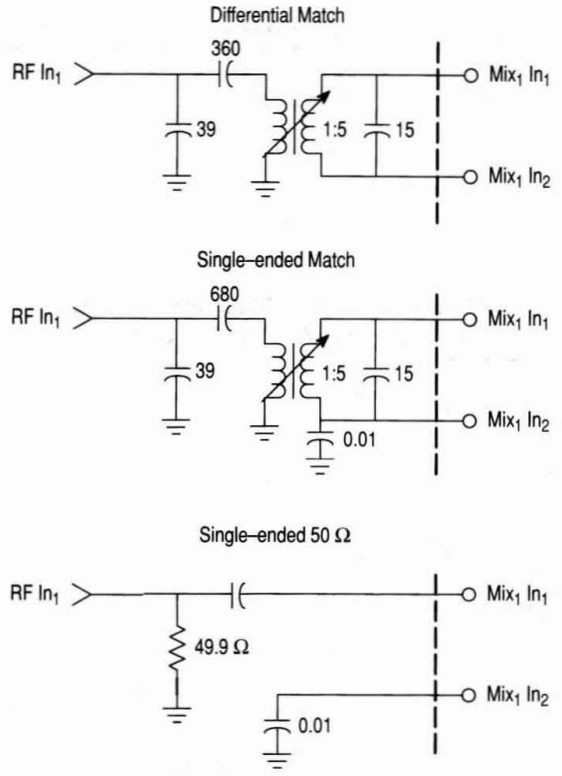
The duplexer is important to achieve full duplex operation without significant "de–sensing" of the receiver by the transmitter. The combination of the duplexer and preamp circuit should attenuate the transmitter power to the receiver by over 60 dB. This will improve the receiver system noise figure without giving up too much IMD performance.

The duplexer may be a two piece unit offered by Shimida, Sansui, or Toko products (designed for 25 channel CT–0 cordless phone). The duplexer frequency response at the receiver port has a notch at the transmitter frequency band of about 35 to 40 dB with a 2.0 to 3.0 dB insertion loss at the receiver frequency band.

The preamp circuit utilizes a tuned transformer at the output side of the amplifier. This transformer is designed to bandpass filter at the receiver input frequency while rejecting the transmitter frequency. The tuned preamp also improves the noise performance by reducing the bandwidth of the pass band and by reducing the second stage contribution of the 1st mixer. The preamp is biased such that it yields suitable noise figure and gain.

The following matching networks have been used to obtain 12 dB SINAD sensitivity numbers:

Figure 60. Matching Input Networks



The exact impedance looking into the RF In1 pin is displayed in the following table along with the sensitivity levels.

Figure 61. 12 dB SINAD Sensitivity Levels, US Handset Application Channel 21

	Sensitivity (dBm)	Input Impedance (dBm)
Differential matched	–115.3	50.2 ± 0.1j
Single–ended match	–114.8	50.2 ± 0.1j
Single–ended 50 Ω	–100.1	50.2 ± 0.1j

The graphs in Figures 64 to 69 are performance results based on Evaluation Board Schematic (Figure 138). This evaluation board did not use a duplexer or preamp stage. Figure 62 is a summary of the RF performance and Figure 63 contains the French RF Performance Summary.

Figure 62. RF Performance Summary for US Applications

MC13110A/MC13111A (fdev = 3.0 kHz, fmod = 1.0 kHz, 50 Ω)			
Parameter	**Handset**	**Baseset**	**Unit**
Sensitivity at 12 dB SINAD	–100.1	–100.1	dBm
Recovered Audio	132	132	mVrms
SINAD @ –30 dBm	41.8	41.4	dB
THD @ –30 dBm	0.8	0.8	%
S/N @ –30 dBm	78.2	78.5	dB
AMRR @ –30 dBm	73.4	72.2	dB
RSSI range	>80	>80	dB

Figure 63. RF Performance Summary for US French Applications

MC13110A/MC13111A (fdev = 1.5 kHz, fmod = 1.0 kHz, 50 Ω)			
Parameter	**Handset**	**Baseset**	**Unit**
Sensitivity at 12 dB SINAD	–91	–90.8	dBm
Recovered Audio	89.8	90	mVrms
SINAD @ –30 dBm	42.1	44.3	dB
THD @ –30 dBm	0.8	0.8	%
S/N @ –30 dBm	75.7	75.1	dB
AMRR @ –30 dBm	56	84.7	dB
RSSI range	>80	>80	dB

RF SYSTEM PERFORMANCE

Figure 64. Typical Receiver Performance Parameters U.S. Handset Application Channel 21

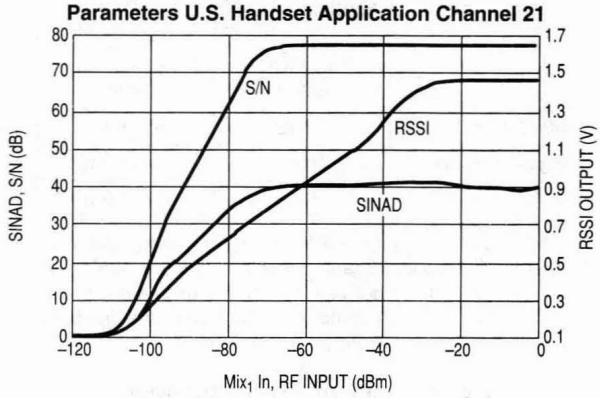


Figure 65. Typical Performance Parameters Over U.S. Handset Channel Frequencies

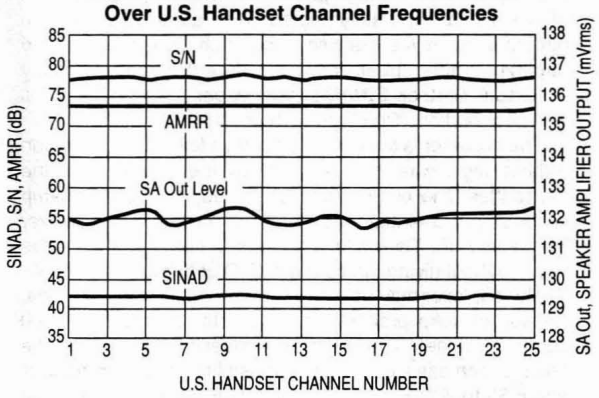


Figure 66. Typical Performance Parameters Over U.S. Baseset Channel Frequencies

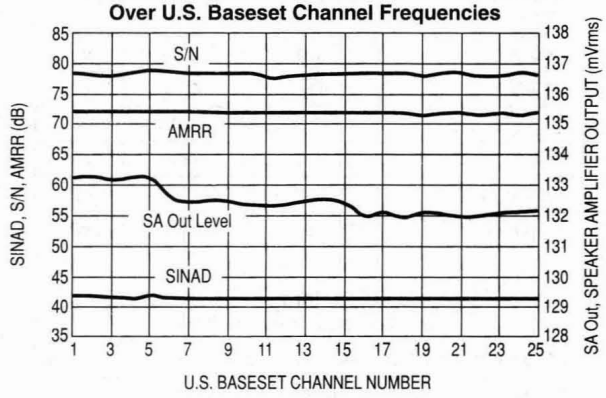


Figure 67. Typical Receiver Performance for US Handset Application Channel 21

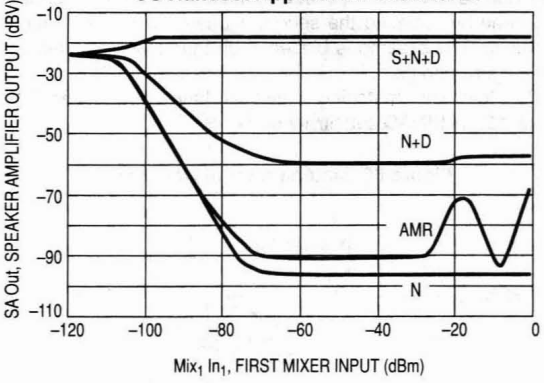


Figure 68. 12 dB SINAD Sensitivity Over US Handset Application Channels

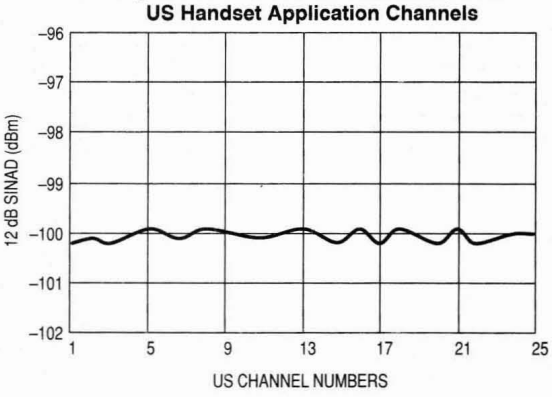
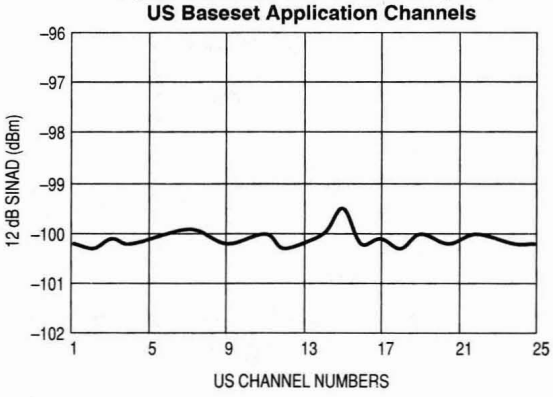


Figure 69. 12 dB SINAD Sensitivity Over US Baseset Application Channels



Receive Audio Path

The R_x Audio signal path begins at "Rx Audio In" and goes through the IC to "E Out". The "R_x Audio In", "Scr Out", and "E In" pins are all ac–coupled. This signal path consists of filters; programmable R_x gain adjust, R_x mute, and volume control, and finally the expander. The typical maximum output voltage at "E Out" should be approximately 0 dBV @ THD = 5.0% .

Figures 71 to 73 represent the receive audio path filter response. The filter response attenuation is very sharp above 3900 Hz, which is the cutoff frequency. Inband (audio), out–of–band, and ripple characteristics are also shown in these graphs.

The group delay (Figure 75) has a peak around 6.5 kHz. This spike is formed by rapid change in the phase at the frequency. In practice this does not cause a problem since the signal is attenuated by at least 50 dB.

The output capability at "Scr Out" and "E Out" are shown in Figures 76, 77, and 78. The results were obtained by increasing the input level for 2.0% distortion at the outputs.

In Figure 70, noise data for the R_x audio path is shown. At Scr Out, the noise level clearly rises when the scrambler is enabled. However, assuming a nominal output level of –20 dBV (100 mVrms) at the 0 dB gain setting, the noise floor is more than 56 dB below the audio signal. However, the noise data at E Out and SA Out is much more improved.

Speaker Amp

The Speaker Amp is an inverting rail–to–rail operational amplifier. The noninverting input is connected to the internal VB reference. External resistors and capacitors are used to set the gain and frequency response. The "SA In" input pin must be ac–coupled. The typical output voltage at "SA Out" is 2.6 V_{pp} with a 130 Ω load. The speaker amp response is shown in Figures 79 and 80.

Data Amp Comparator

The data amp comparator is an inverting hysteresis comparator. Its open collector output has an internal 100 kΩ pull–up resistor. A band pass filter is connected between the "Det Out" pin and the "DA In" pin with component values as shown in the Application Circuit schematic. The "DA In" input signal needs to be ac–coupled, too.

Figure 70. R_x Path Noise Data

Receive Scrambler	Receive Gain (dB)	Volume (dB)	SCR_Out (dBV)	E_Out (dBV)	SA_Out (dBV)
off/on	muted	muted	< –95	< –95	< –95
off	–9.0	–14	–92	< –95	< –95
off	0	0	–85	< –95	< –95
off	1.0	16	–76	< –95	< –95
on (MC13110A/B)	–9.0	–14	–85	< –95	< –95
on (MC13110A/B)	0	0	–77	< –95	< –95
on (MC13110A/B)	10	16	–66	< –95	< –95

R_x AUDIO

Figure 71. R_x Audio Wideband Frequency Response

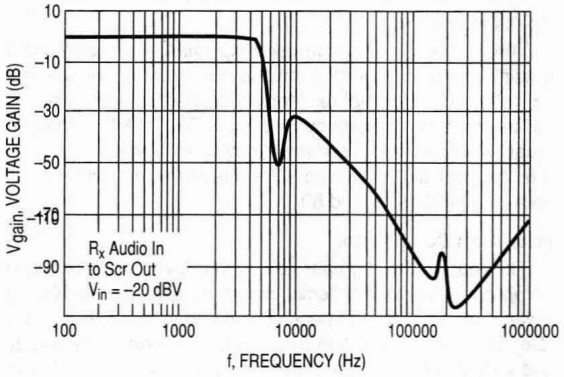


Figure 72. R_x Audio Inband Frequency Response

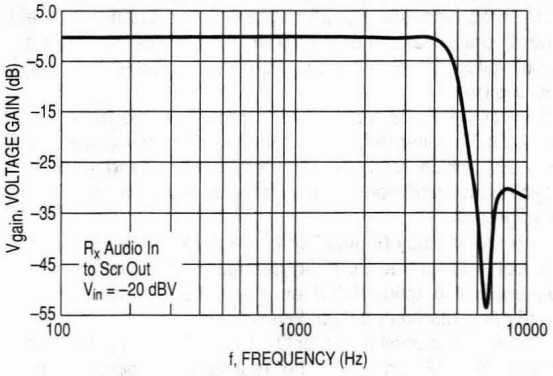


Figure 73. R_x Audio Ripple Response

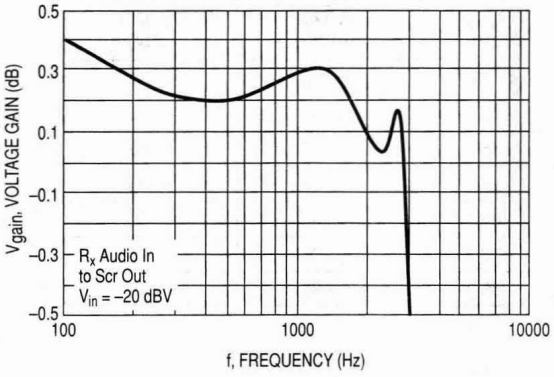


Figure 74. R_x Audio Inband Phase Response

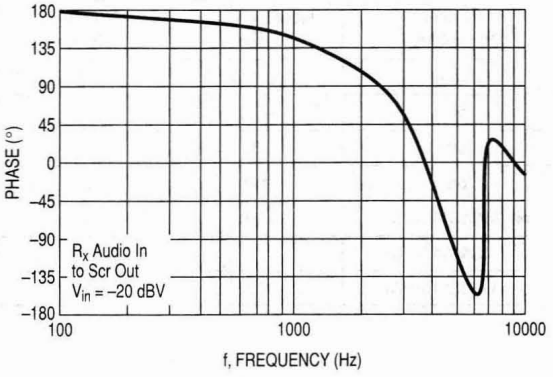


Figure 75. R_x Audio Inband Group Delay

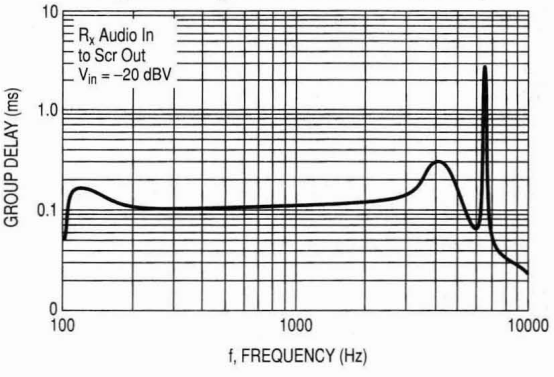
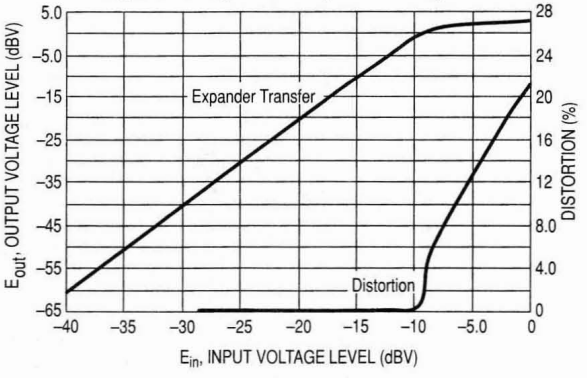


Figure 76. R_x Audio Expander Response



R_x AUDIO

Figure 77. R_x Audio Maximum Output Voltage versus Gain Control Setting

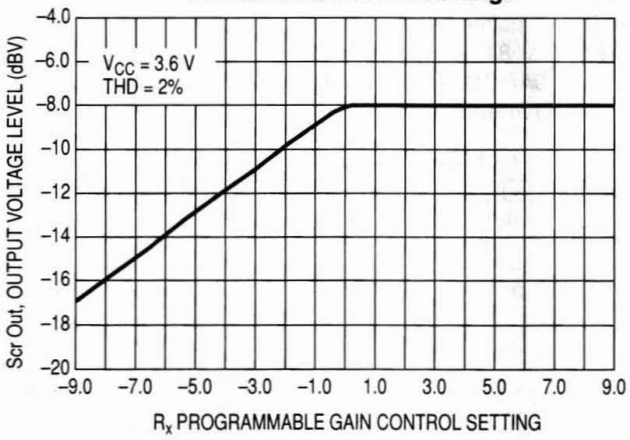


Figure 78. R_x Audio Maximum Output Voltage versus Volume Setting

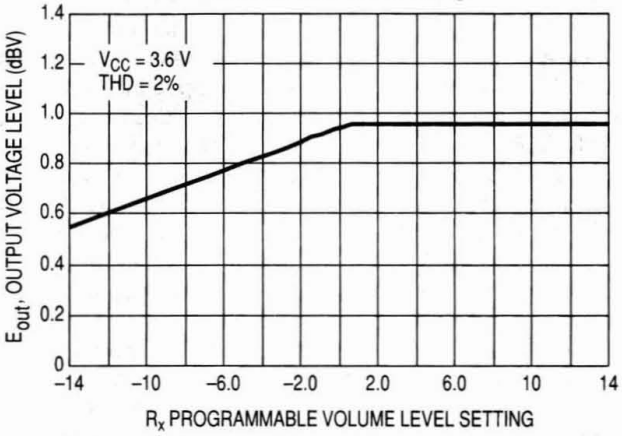


Figure 79. R_x Audio Speaker Amplifier Drive

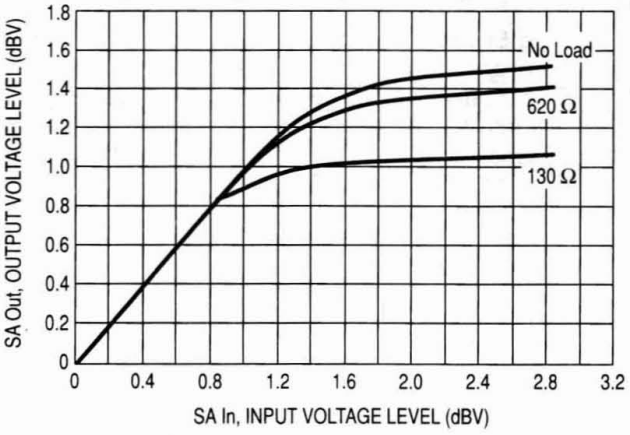
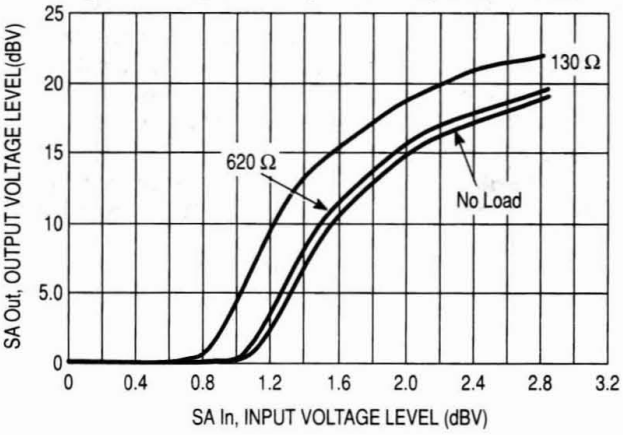


Figure 80. R_x Audio Speaker Amplifier Distortion



Transmit Audio Path

This portion of the audio path goes from "C In" to "T_x Out". The "C In" pin will be ac–coupled. The audio transmit signal path includes automatic level control (ALC) (also referred to as the Compressor), T_x mute, limiter, filters, and T_x gain adjust. The ALC provides "soft" limiting to the output signal swing as the input voltage slowly increases. With this technique the gain is slightly lowered to help reduce distortion of the audio signal. The limiter section provides hard limiting due to rapidly changing signal levels, or transients. This is accomplished by clipping the signal peaks. The ALC, T_x mute, and limiter functions can be enabled or disabled via the MPU serial interface. The T_x gain adjust can also be remotely controlled to set different desired signal levels. The typical maximum output voltage at "T_x Out" should be approximately 0 dBV @ THD = 5.0%.

Figures 82 to 86 represent the transmit audio path filter response. The filter response attenuation, again, is very definite above 3800 Hz. This is the filter cutoff frequency. Inband (audio), wideband, and ripple characteristics are also shown in these graphs.

The compressor transfer characteristics, shown in Figure 87, has three different slopes. A typical compressor slope can be found between –55 and –15 dBV. Here the slope is 2.0. At an input level above –15 dBV the automatic level control (ALC) function is activated and prevents hard clipping of the output. The slope below –55 dBV input level is one. This is where the compressor curve ends. Above 5.0 dBV the output actually begins to decrease and distort. This is due to supply voltage limitations.

In Figure 88 the ALC function is off. Here the compressor curve continues to increase above –15 dBV up to –4.0 dBV. The limiter begins to clip the output signal at this level and distortion is rapidly rising. Similarly, Figure 68 (ALC and Limiter Off) shows to compressor transfer curve extending all the way up to the maximum output. Finally, Figure 90 through 93 show the T_x Out signal versus several combinations of ALC and Limiter selected.

Figure 81 is the noise data measured for the MC13110A/13111A. This data is for 0 dB gain setting and –20 dBV (100 mVrms) audio levels.

Figure 81. T_x Path Noise Data

Transmit Scrambler	Transmit Gain (dB)	Amp_Out (dBV)	T_x_Out (dBV)
off/on	muted	muted	< –95
off	–9.0	< –95	–83
off	0	< –95	–74
off	10	< –95	–64
on (MC13110A)	–9.0	< –95	–82
on (MC13110A)	0	< –95	–73
on (MC13110A)	10	–< –95	–63

Mic Amp

Like the Speaker Amp the Mic Amp is also an inverting rail–to–rail operational amplifier. The noninverting input terminal is connected to the internal VB reference. External resistors and capacitors are used to set the gain and frequency response. The "T_x In" input is ac–coupled.

T_x AUDIO

Figure 82. T_x Audio Wideband Frequency Response

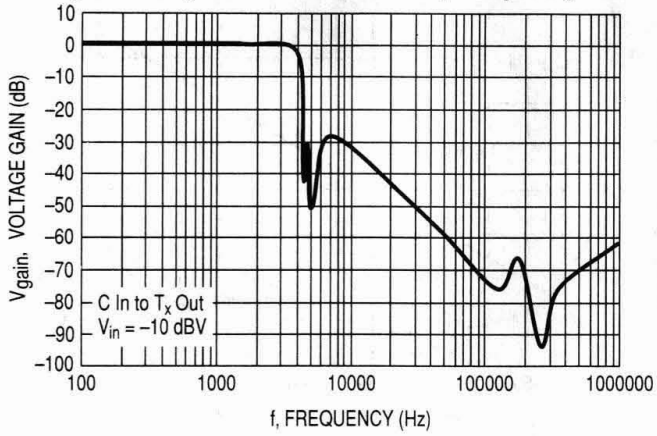


Figure 83. T_x Audio Inband Frequency Response

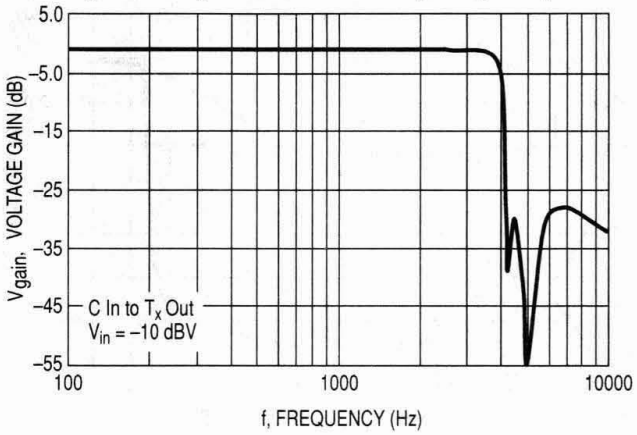


Figure 84. T_x Audio Ripple Response

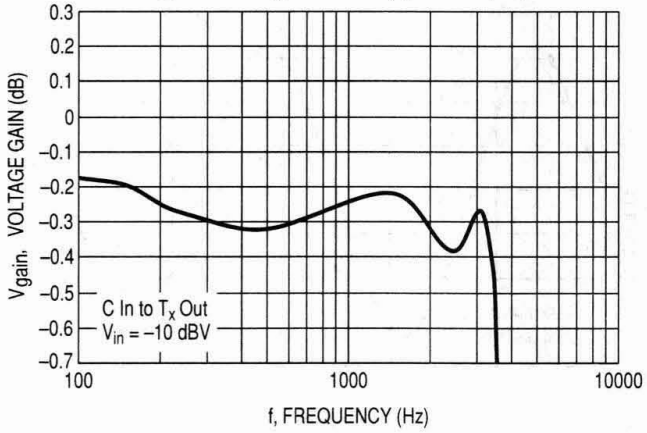


Figure 85. T_x Audio Inband Phase Response

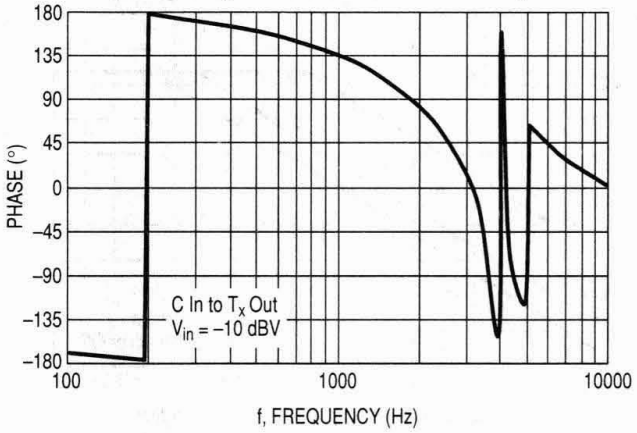


Figure 86. T_x Audio Inband Group Delay

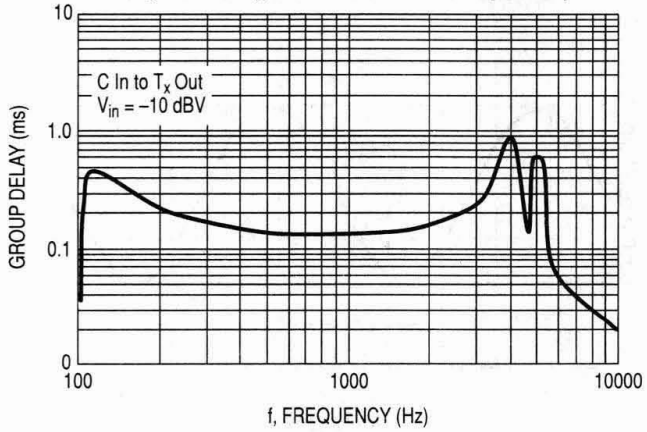
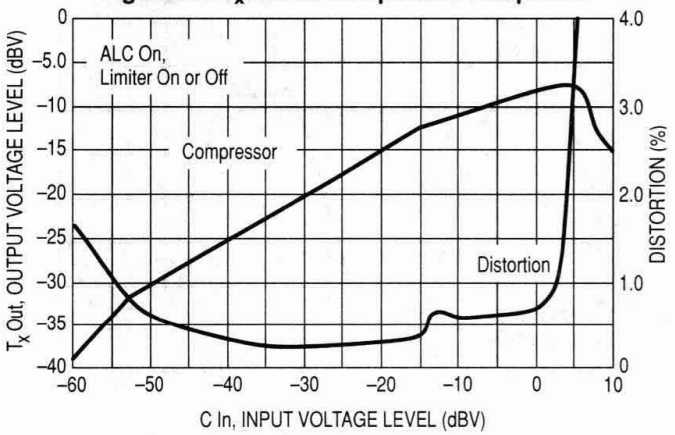


Figure 87. T_x Audio Compressor Response



T_x AUDIO

Figure 88. T_x Audio Compressor Response

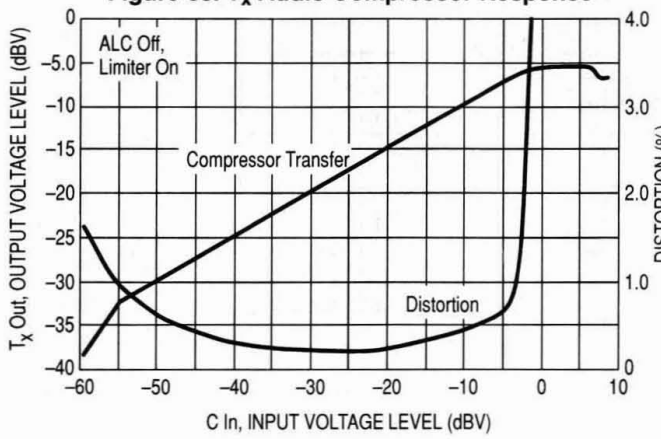


Figure 89. T_x Audio Compressor Response

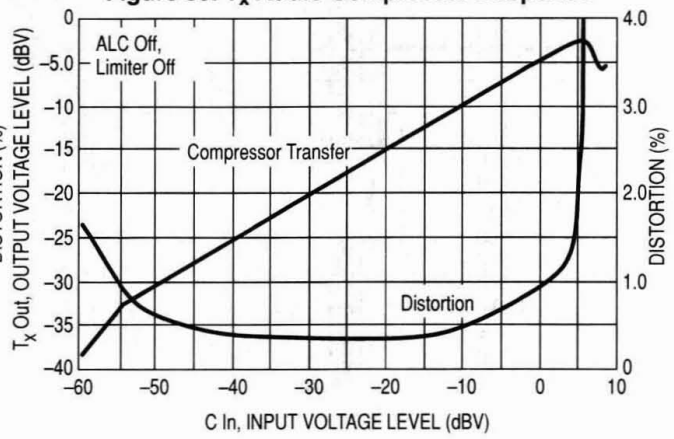


Figure 90. T_x Audio Maximum Output Voltage versus Gain Control Setting

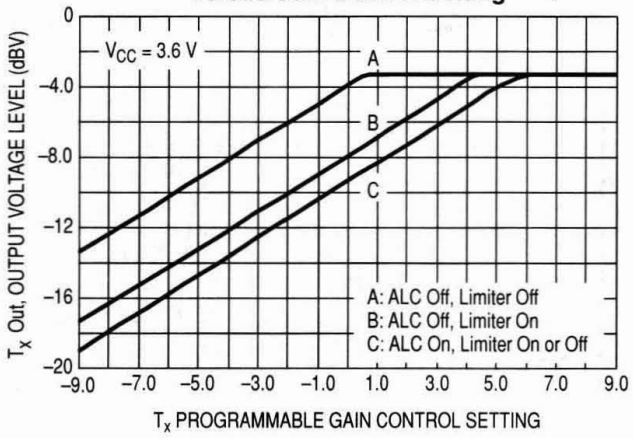


Figure 91. T_x Output Audio Response

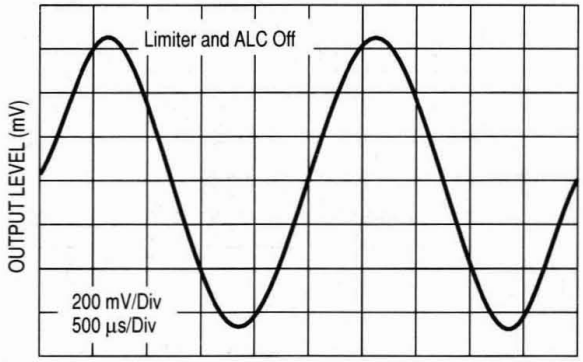


Figure 92. T_x Output Audio Response

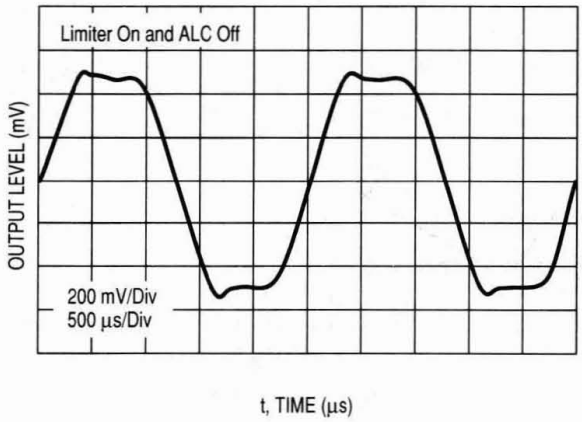
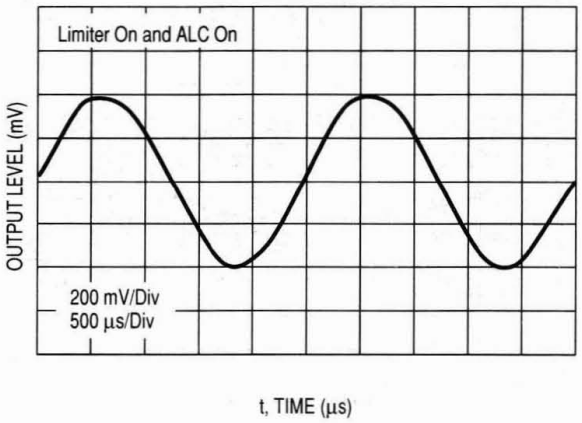


Figure 93. T_x Audio Output Response



PLL SYNTHESIZER SECTION

PLL Frequency Synthesizer General Description

Figure 95 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL) designed into the MC13110A/B and MC13111A/B IC. This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), Spain, Australia, Korea, New Zealand, U.K., Netherlands, France, and China (see channel frequency tables in AN1575, "Worldwide Cordless Telephone Frequencies").

The 2nd local oscillator and reference divider provide the reference frequency signal for the R_x and T_x PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_x and T_x reference frequency values. For the U.K., additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.2 kHz reference frequencies.

The 14–bit R_x counter is programmed for the desired first local oscillator frequency. The 14–bit T_x counter is programmed for the desired transmit channel frequency. All counters power–up to a set default state for USA channel #21 using a 10.24 MHz reference frequency crystal (see power–up default latch register state in the Serial Programmable Interface section).

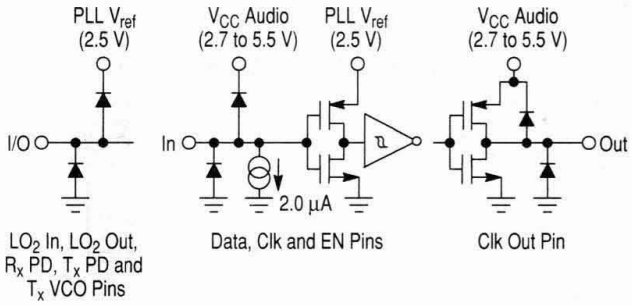
To extend the sensitivity of the 1st LO for U.S. 25 channel operation, internal fixed capacitors can be connected to the tank circuit through microprocessor programmable control. When designing the external PLL loop filters, it is recommended that the T_x and R_x phase detectors be considered as current drive type outputs. The loop filter control voltage must be 0.5 V away from either the positive or negative supply rail.

PLL I/O Pin Configurations

The 2nd LO, R_x and T_x PLL's, and MPU serial interface are powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin. It is regulated by an internal bandgap voltage reference. Therefore, the maximum input and output levels for most of the PLL I/O pins (LO2 In, LO2 Out, R_x PD, T_x PD, T_x VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}".

Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 94 shows a simplified schematic of the I/O pins.

Figure 94. PLL I/O Pin Simplified Schematics

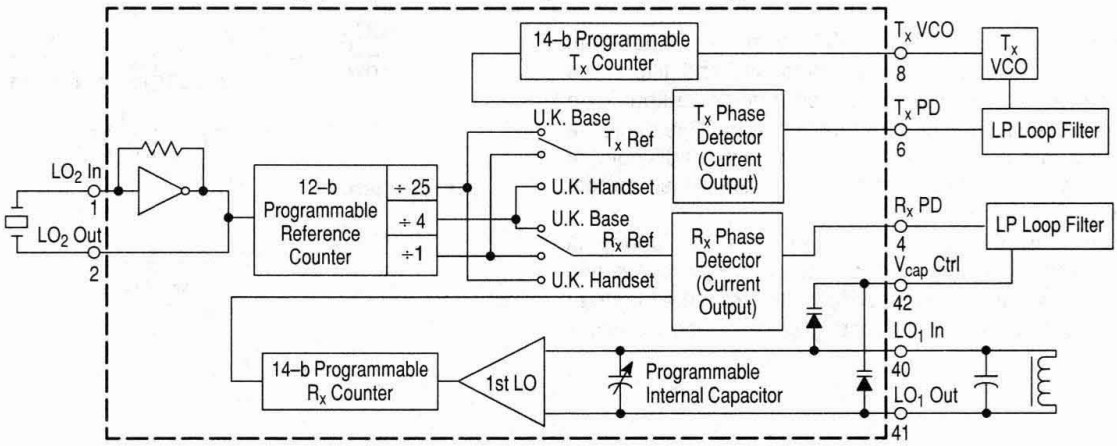

PLL Vref (2.5 V)
VCC Audio (2.7 to 5.5 V)
PLL Vref (2.5 V)
VCC Audio (2.7 to 5.5 V)
I/O
In
2.0 µA
Out
LO2 In, LO2 Out, Rx PD, Tx PD and Tx VCO Pins
Data, Clk and EN Pins
Clk Out Pin

PLL Loop Control Voltage Range

The control voltage for the T_x and R_x loop filters is set by the phase detector outputs which drive the external loop filters. The phase detectors are best considered to have a current mode type output. The output can have three states; ground, high impedance, and positive supply, which in this case is the voltage at "PLL V_{ref}". When the loop is locked the phase detector outputs are at high impedance. An exception of this state is for narrow current pulses, referenced to either the positive or negative supply rails. If the loop voltages get within 0.5 V of either rail the linear current output starts to degrade. The phase detector current source was not designed to operate at the supply rails. VCO tuning range will also be limited by this voltage range

The maximum loop control voltage is the "PLL V_{ref}" voltage which is 2.5 V. If a higher loop control voltage range is desired, the "PLL V_{ref}" pin can be pulled to a higher voltage. It can be tied directly to the V_{CC} voltage (with suitable filter capacitors connected close to each pin). When this is done, the internal voltage regulator is automatically disabled. This is commonly used in the telephone base set where an external 5.0 V regulated voltage is available. It is important to remember, that if "PLL V_{ref}" is tied to V_{CC} and V_{CC} is not a regulated voltage, the PLL loop parameters and lock–up time will vary with supply voltage variation. The phase detector gain constant, K_{pd}, will not be affected if the "PLL V_{ref}" is tied to V_{CC}.

Figure 95. Dual PLL Simplified Block Diagram

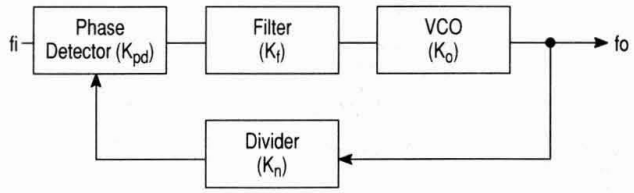


Loop Filter Characteristics

Lets consider the following discussion on loop filters. The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time, and transient response are controlled externally by loop filtering.

Figure 96 is the general model for a Phase Lock Loop (PLL).

Figure 96. PLL Model



Where:

K_{pd} = Phase Detector Gain Constant
K_f = Loop Filter Transfer Function
K_o = VCO Gain Constant
K_n = Divide Ratio (1/N)
fi = Input frequency
fo = Output frequency
fo/N = Feedback frequency divided by N

From control theory the loop transfer function can be represented as follows:

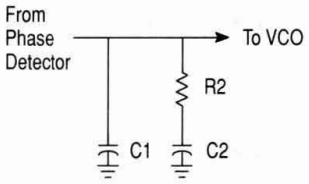
$$A = K_{pd}\, K_f\, K_o\, K_n \quad \text{Open loop gain}$$

K_{pd} can be either expressed as being 2.5 V/4.0 π or 1.0 mA/2.0 π for the CT–0 circuits. More details about performance of different type PLL loops, refer to Motorola application note AN535.

The loop filter can take the form of a simple low pass filter. A current output, type 2 filter will be used in this discussion since it has the advantage of improved step response, velocity, and acceleration.

The type 2 low pass filter discussed here is represented as follows:

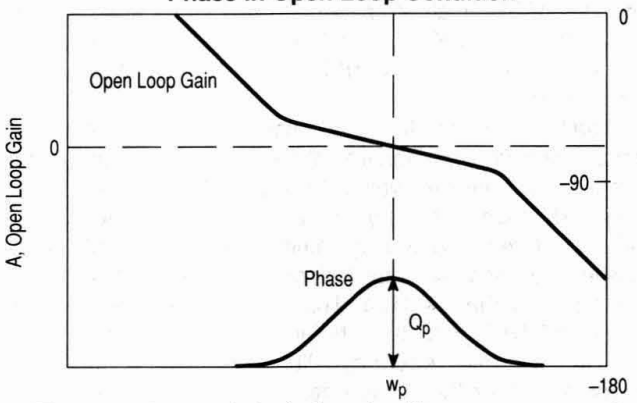
Figure 97. Loop Filter with Additional Integrating Element



From Figure 97, capacitor C1 forms an additional integrator, providing the type 2 response, and filters the discrete current steps from the phase detector output. The function of the additional components R2 and C2 is to create a pole and a zero (together with C1) around the 0 dB point of the open loop gain. This will create sufficient phase margin for stable loop operation.

In Figure 98, the open loop gain and the phase is displayed in the form of a Bode plot. Since there are two integrating functions in the loop, originating from the loopfilter and the VCO gain, the open loop gain response follows a second order slope (–40 dB/dec) creating a phase of –180 degrees at the lower and higher frequencies. The filter characteristic needs to be determined such that it is adding a pole and a zero around the 0 dB point to guarantee sufficient phase margin in this design (Qp in Figure 98).

Figure 98. Bode Plot of Gain and Phase in Open Loop Condition



The open loop gain including the filter response can be expressed as:

$$A_{openloop} = \frac{K_{pd}K_o(1 + jw(R2C2))}{jwK_n\left(jw\left(1 + jw\left(\frac{R2C1C2}{C1+C2}\right)\right)\right)} \quad \textbf{(1)}$$

The two time constants creating the pole and the zero in the Bode plot can now be defined as:

$$T1 = \frac{R2C1C2}{C1 + C2} \qquad T2 = R2C2 \quad \textbf{(2)}$$

By substituting equation (2) into (1), it follows:

$$A_{openloop} = \left(\frac{K_{pd}K_oT1}{w^2C1K_nT2}\right)\left(\frac{1 + jwT2}{1 + jwT1}\right) \quad \textbf{(3)}$$

The phase margin (phase + 180) is thus determined by:

$$Q_p = \arctan(wT2) - \arctan(wT1) \quad \textbf{(4)}$$

At $w=w_p$, the derivative of the phase margin may be set to zero in order to assure maximum phase margin occurs at w_p (see also Figure 98). This provides an expression for w_p:

$$\frac{dQ_p}{dw} = 0 = \frac{T2}{1 + (wT2)^2} - \frac{T1}{1 + (wT1)^2} \quad \textbf{(5)}$$

$$w = w_p = \frac{1}{\sqrt{T2T1}} \quad \textbf{(6)}$$

Or rewritten:

$$T1 = \frac{1}{w_p{}^2T2} \quad \textbf{(7)}$$

By substituting into equation (4), solve for T2:

$$T2 = \frac{\tan\left(\frac{Q_p}{2} + \frac{\pi}{4}\right)}{w_p} \quad (8)$$

By choosing a value for w_p and Q_p, T1 and T2 can be calculated. The choice of Q_p determines the stability of the loop. In general, choosing a phase margin of 45 degrees is a good choice to start calculations. Choosing lower phase margins will provide somewhat faster lock–times, but also generate higher overshoots on the control line to the VCO. This will present a less stable system. Larger values of phase margin provide a more stable system, but also increase lock–times. The practical range for phase margin is 30 degrees up to 70 degrees.

The selection of w_p is strongly related to the desired lock–time. Since it is quite complicated to accurately calculate lock time, a good first order approach is:

$$T\_lock \approx \frac{3}{w_p} \quad (9)$$

Equation (9) only provides an order of magnitude for lock time. It does not clearly define what the exact frequency difference is from the desired frequency and it does not show the effect of phase margin. It assumes, however, that the phase detector steps up to the desired control voltage without hesitation. In practice, such step response approach is not really valid. The two input frequencies are not locked. Their phase maybe momentarily zero and force the phase detector into a high impedance mode. Hence, the lock times may be found to be somewhat higher.

In general, w_p should be chosen far below the reference frequency in order for the filter to provide sufficient attenuation at that frequency. In some applications, the reference frequency might represent the spacing between channels. Any feedthrough to the VCO that shows up as a spur might affect adjacent channel rejection. In theory, with the loop in lock, there is no signal coming from the phase detector. But in practice leakage currents will be supplied to both the VCO and the phase detector. The external capacitors may show some leakage, too. Hence, the lower w_p, the better the reference frequency is filtered, but the longer it takes for the loop to lock.

As shown in Figure 98, the open loop gain at w_p is 1 (or 0 dB), and thus the absolute value of the complex open loop gain as shown in equation (3) solves C1:

$$C1 = \left(\frac{K_{pd}K_oT1}{w^2K_nT2}\right)\sqrt{\frac{\left(1 + w_pT2\right)^2}{\left(1 + w_pT1\right)^2}} \quad (10)$$

With C1 known, and equation (2) solve C2 and R2:

$$C2 = C1\left(\frac{T2}{T1} - 1\right) \quad (11)$$

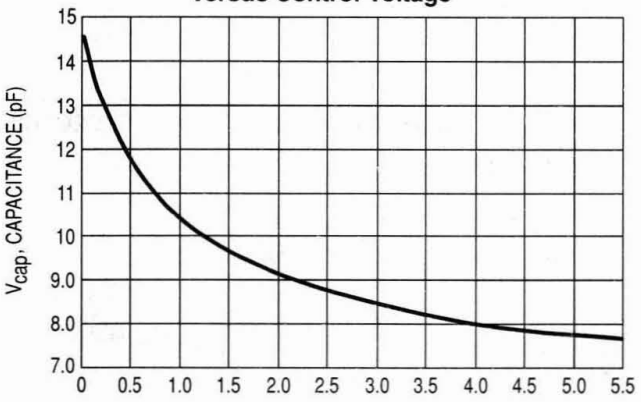
$$R2 = \frac{T2}{C2} \quad (12)$$

The VCO gain is dependent on the selection of the external inductor and the frequency required. The free running frequency of the VCO is determined by:

$$f = \frac{1}{2\pi\sqrt{LC_T}} \quad (13)$$

In which L represents the external inductor value and C_T represents the total capacitance (including internal capacitance) in parallel with the inductor. The VCO gain can be easily calculated via the internal varicap transfer curve shown below.

Figure 99. Varicap Capacitance versus Control Voltage



As can be derived from Figure 99, the varicap capacitance changes 1.3 pF over the voltage range from 1.0 V to 2.0 V:

$$\Delta Cvar = \frac{1.3\ pF}{V} \quad (14)$$

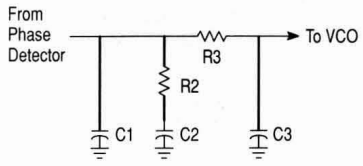
Combining (13) with (14) the VCO gain can be determined by:

$$K_O = \frac{1}{jw}\left\{\frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}} - \frac{1}{2\pi\sqrt{L\left(C_T + \frac{\Delta Cvar}{2}\right)}}\right\} \quad (15)$$

Although the basic loopfilter previously described provides adequate performance for most applications, an extra pole may be added for additional reference frequency filtering. Given that the channel spacing in a CT–0 telephone set is based on the reference frequency, and any feedthrough to

the first LO may effect parameters like adjacent channel rejection and intermodulation. Figure 100 shows a loopfilter architecture incorporating an additional pole.

Figure 100. Loop Filter with Additional Integrating Element



For the additional pole formed by R3 and C3 to be efficient, the cut–off frequency must be much lower than the reference frequency. However, it must also be higher than w_p in order not to compromise phase margin too much. The following equations were derived in a similar manner as for the basic filter previously described.

Similarly, it can be shown:

$$A_{openloop} = -\frac{K_{pd}K_o}{K_n w^2\left((C1 + C2 + C3) - w^2C1C2C3R2R3\right)} + \frac{1 + jwT2}{1 + jwT1} \quad (16)$$

In which:

$$T1 = \frac{(C1 + C2)T2 + (C1C2)T3}{C1 + C2 + C3 - w^2C1T2T3} \quad (17)$$

$$T2 = R2C2 \quad (18) \qquad T3 = R3C3 \quad (19)$$

From T1 it can be derived that:

$$C2 = \frac{(T1 + T2)C3 - C1\left(T2 + T3 - T1 + w^2T1T2T3\right)}{T3 - T1} \quad (20)$$

In analogy with (10), by forcing the loopgain to 1 (0 dB) at w_p, we obtain:

$$C1(T1 + T2) + C2T3 + C3T2 = \left(\frac{K_{pd}K_o}{K_n {w_p}^2}\right)\sqrt{\frac{1 + \left(w_pT2\right)^2}{1 + \left(w_pT1\right)^2}} \quad (21)$$

Solving for C1:

$$C1 = \frac{(T2 - T1)T3C3 - (T3 - T1)T2C3 + (T3 - T1)\left(\frac{K_{pd}K_oT1}{{w_p}^2K_n}\right)\sqrt{\frac{1+\left(w_pT2\right)^2}{1+\left(w_pT1\right)^2}}}{(T3 - T1)T2 + (T3 - T1)T3 - \left(T2 + T3 - T1 + {w_p}^2T1T2T3\right)T3} \quad (22)$$

By selecting w_p via (9), the additional time constant expressed as T3, can be set to:

$$T3 = \frac{1}{Kw_p} \quad (23)$$

The K–factor shown determines how far the additional pole frequency will be separated from w_p. Selecting too small of a K–factor, the equations may provide negative capacitance or resistor values. Too large of a K–factor may not provide the maximum attenuation.

By selecting R3 to be 100 kΩ, C3 becomes known and C1 and C2 can be solved from the equations. By using equations (8) and (7), time constants T2 and T1 can be derived by selecting a phase margin. Finally, R2 follows from T2 and C2.

The following pages, the loopfilter components are determined for both handset and baseset the US application based on the equations described. Choose K to be approximately five times w_p ($5.0w_p$).

In an application, w_p is chosen to be 20 times less than the reference frequency of 5.0 kHz and the phase margin has been set to 45 degrees. This provides a lock time according to (9) of about 2.0 ms (order of magnitude). With the adjacent channels spaced at least 15 kHz away, reference feedthrough at w_p will not be directly disastrous but still, the additional pole may be added in the loopfilter design for added safety.

In an application, w_p is chosen to be 20 times less than the reference frequency of 5.0 kHz and the phase margin has been set to 45 degrees. This provides a lock time according to (9) of about 2.0 ms (order of magnitude). With the adjacent channels spaced at least 15 kHz away, reference feedthrough at w_p will not be directly disastrous but still, the additional pole may be added in the loopfilter design for added safety.

Figure 101. Open Loop Response Handset US with Selected Values

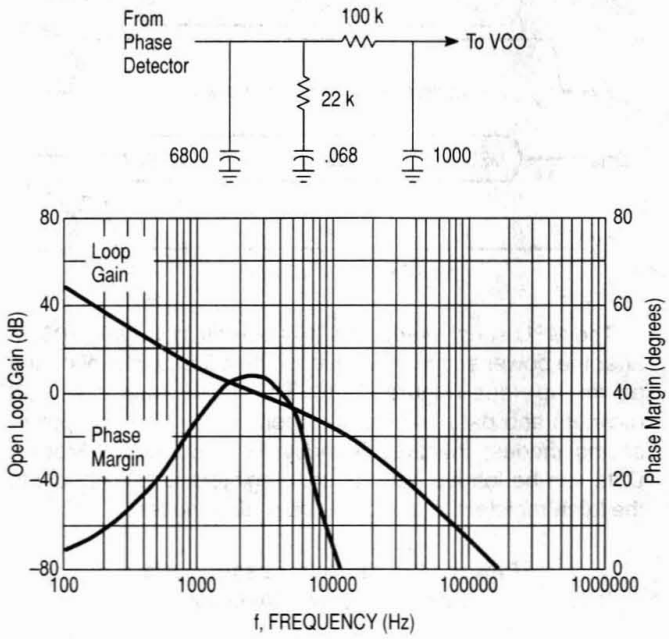


Figure 102. Open Loop Response Baseset US with Selected Values

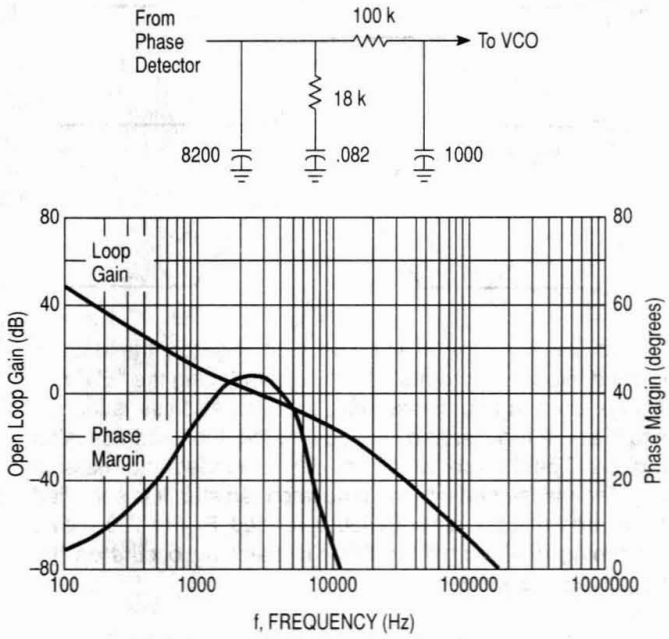


Figure 103. Handset US

Conditions		
L = 470 uH	F_{ref} = 5.0 kHz	
RF = 46.77 MHz	Q_p = 45 degrees	
VCO center = 36.075 MHz	$w_p = w_{ref} / 20$ radians	
Results	**Equations**	**Select**
K_{pd} = 159.2 uA/rad K_{VCO} = 3.56 Mrad/V T2 = 1540 µs T1 = 264 µs T3 = 91 µs	 (14), (15) (8) (7) with K = 7	
C1 = 7.6 nF C2 = 70.9 nF R2 = 21.7 kΩ R3 = 100 kΩ C3 = 909.5 pF	(21) (20) (18) choose: (19)	C1 = 6.8 nF C2 = 68 nF R2 = 22 kΩ R3 = 100 kΩ C3 = 1 nf

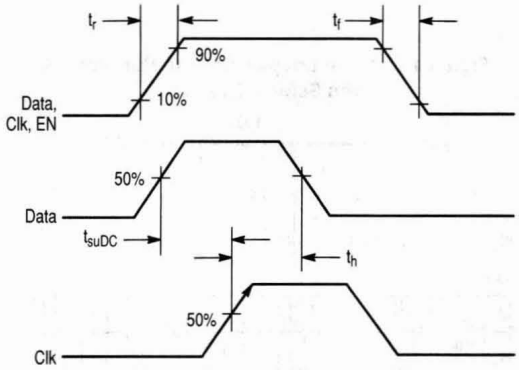
Figure 104. Baseset US

Conditions		
L = 470 uH	F_{ref} = 5.0 kHz	
RF = 49.83 MHz	Q_p = 45 degrees	
VCO center = 39.135 MHz	$w_p = w_{ref} / 20$ radians	
Results	**Equations**	**Select**
K_{pd} = 159.2 uA/rad K_{VCO} = 4.54 Mrad/V T2 = 1540 µs T1 = 264 µs T3 = 91 µs	 (14), (15) (8) (7) with K = 7	
C1 = 9.1 nF C2 = 83.5 nF R2 = 18.4 kΩ R3 = 100 kΩ C3 = 909.5 pF	(21) (20) (18) choose: (19)	C1 = 8.2 nF C2 = 82 nF R2 = 18 kΩ R3 = 100 kΩ C3 = 1 nf

Microprocessor Serial Interface

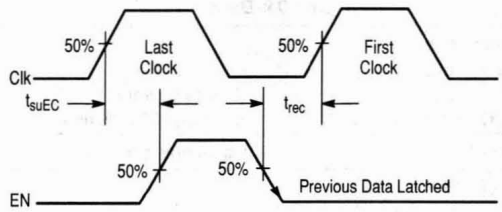
The Data, Clock, and Enable ("Data", "Clk", and "EN" respectively) pins provide a MPU serial interface for programming the reference counters, the transmit and receive channel divide counters, the switched capacitor filter clock counter, and various other control functions. The "Data" and "Clk" pins are used to load data into the MC13111A/B shift register (Figure 109). Figure 105 shows the timing required on the "Data" and "Clk" pins. Data is clocked into the shift register on positive clock transitions.

Figure 105. Data and Clock Timing Requirement



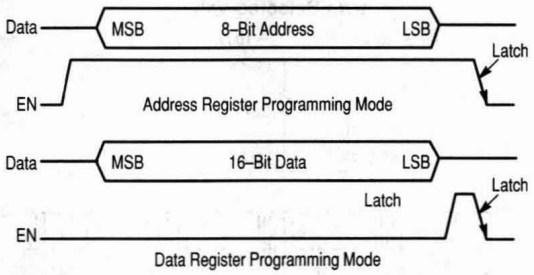
After data is loaded into the shift register, the data is latched into the appropriate latch register using the "EN" pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register. It is specified by the address that was previously loaded. Figure 106 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 106. Enable Timing Requirement



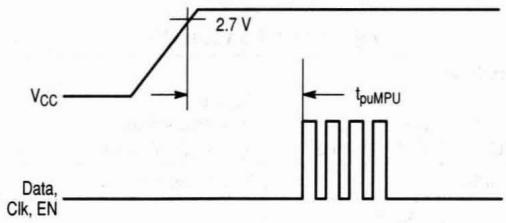
The state of the "EN" pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 107 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when "EN" is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the "EN" high state. The convention in these figures is that latch bits to the left are loaded into the shift register first. A minimum of four "Clk" rising edge transition must occur before a negative "EN" transition will latch data or an address into a register.

Figure 107. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 µs after the power supply has reached its minimum level during power–up (see Figure 108). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_x, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 108. Microprocessor Serial Interface Power–Up Delay



Data Registers

Figure 109 shows the data latch registers and addresses which are used to select each of each registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. Bits proceeding the register must be "0's" as shown.

Power–Up Defaults for Data Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The device is initially placed in the R_x mode with all mutes active. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The switched capacitor filter clock counter is set properly for operation with a 10.24 MHz crystal. The T_x and R_x counter registers are set for USA handset channel frequency, number 21 (Channel 6 for previous FCC 10 Channel Band). Figure 110 shows the initial power–up states for all latch registers.

Figure 109. Microprocessor Interface Data Latch Registers

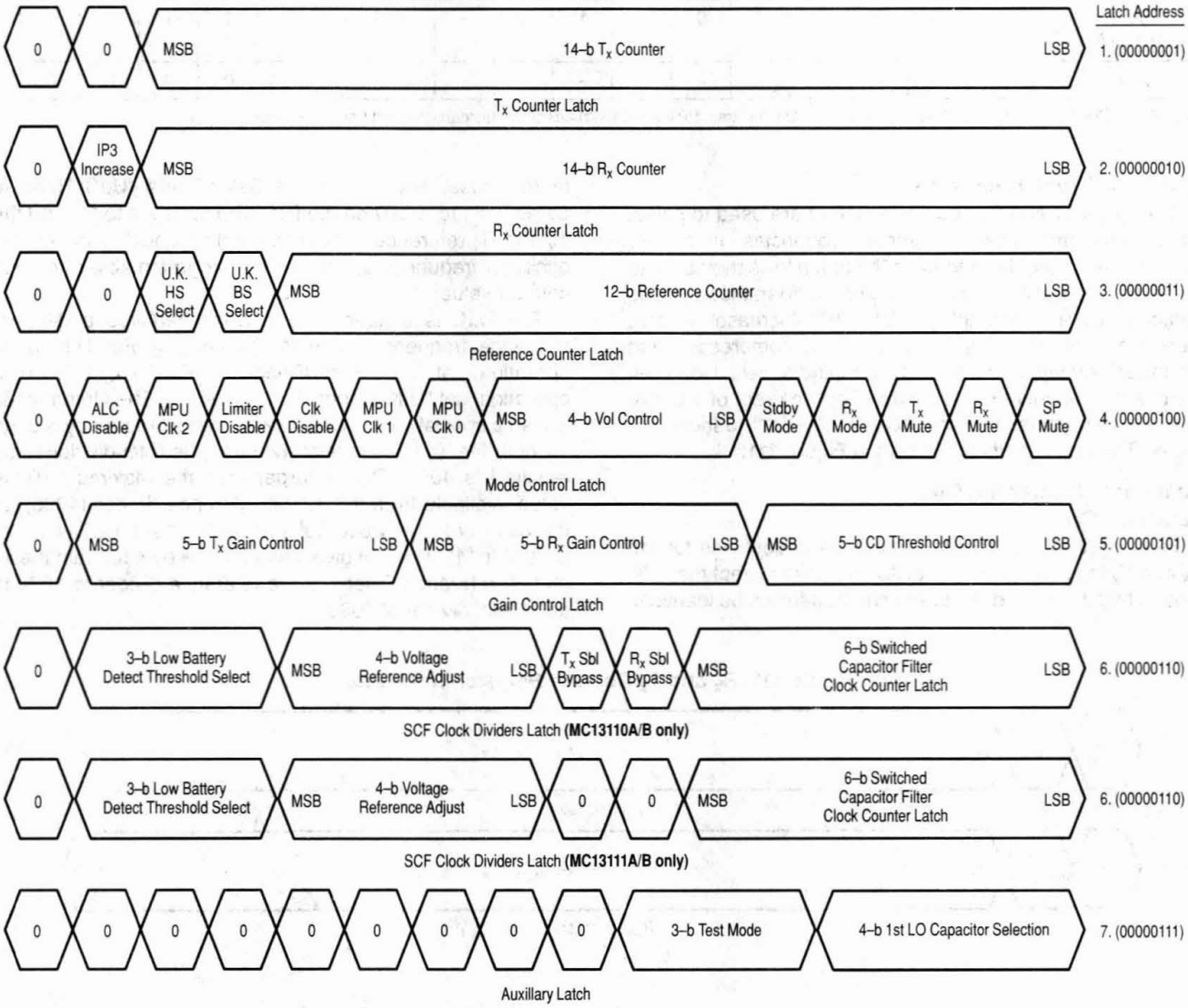

Latch Address
0 0 MSB 14–b Tx Counter LSB 1. (00000001)
Tx Counter Latch
0 IP3 Increase MSB 14–b Rx Counter LSB 2. (00000010)
Rx Counter Latch
0 0 U.K. HS Select U.K. BS Select MSB 12–b Reference Counter LSB 3. (00000011)
Reference Counter Latch
0 ALC Disable MPU Clk 2 Limiter Disable Clk Disable MPU Clk 1 MPU Clk 0 MSB 4–b Vol Control LSB Stdby Mode Rx Mode Tx Mute Rx Mute SP Mute 4. (00000100)
Mode Control Latch
0 MSB 5–b Tx Gain Control LSB MSB 5–b Rx Gain Control LSB MSB 5–b CD Threshold Control LSB 5. (00000101)
Gain Control Latch
0 3–b Low Battery Detect Threshold Select MSB 4–b Voltage Reference Adjust LSB Tx Sbl Bypass Rx Sbl Bypass MSB 6–b Switched Capacitor Filter Clock Counter Latch LSB 6. (00000110)
SCF Clock Dividers Latch (MC13110A/B only)
0 3–b Low Battery Detect Threshold Select MSB 4–b Voltage Reference Adjust LSB 0 0 MSB 6–b Switched Capacitor Filter Clock Counter Latch LSB 6. (00000110)
SCF Clock Dividers Latch (MC13111A/B only)
0 0 0 0 0 0 0 0 0 3–b Test Mode 4–b 1st LO Capacitor Selection 7. (00000111)
Auxillary Latch

Figure 110. Latch Register Power–Up Defaults

Register	Count	MSB								LSB							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_x	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_x	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	0	1	1	1	1	0	1	1	1	1	1	0	1	0	0
SCF (MC13110A/B)	31	–	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1
SCF (MC13111A/B)	31	–	0	0	0	0	1	1	1	–	–	0	1	1	1	1	1
Aux	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

NOTE: 12. Bits 6 and 7 in the SCF latch register are "Don't Cares" for the MC13111A/B since this part does not have a scrambler.

T_x and R_x Counter Registers

The 14 bit T_x and R_x counter registers are used to select the transmit and receive channel frequencies. In the R_x counter there is an "IP3 Increase" bit that allows the ability to trade off increased receiver mixer performance versus reduced power consumption. With "IP3 increase" = <1>, there is about a 10 dB improvement in 1 dB compression and 3rd order intercept for both the 1st and 2nd mixers. However, there is also an increase in power supply current of 1.3 mA. The power–up default for the MC13111A/B is "IP3 Increase" = <0>. The register bits are shown in Figure 111.

Reference Counter Register

Reference Counter

Figure 113 shows how the reference frequencies for the R_x and T_x loops are generated. All countries except the U.K. require that the T_x and R_x reference frequencies be identical. In this case, set "U.K. Base Select" and "U.K. Handset Select" bits to "0". Then the fixed divider is set to "1" and the T_x and R_x reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value.

The U.K. is a special case which requires a different reference frequency value for T_x and R_x. For U.K. base operation, set "U.K. Base Select" to "1". For U.K. handset operation, set "U.K. Handset Select" to "1". The Netherlands is also a special case. A 2.5 kHz reference frequency is used for both the T_x and R_x reference and the total divider value required is 4096. This is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set "U.K. Base Select" to "1" and set "U.K. Handset Select" to "1". This will give a fixed divide by 4 for both the T_x and R_x reference. Then set the reference divider to 1024 to get a total divider of 4096.

Figure 111. R_x and T_x Counter Register Latch Bits

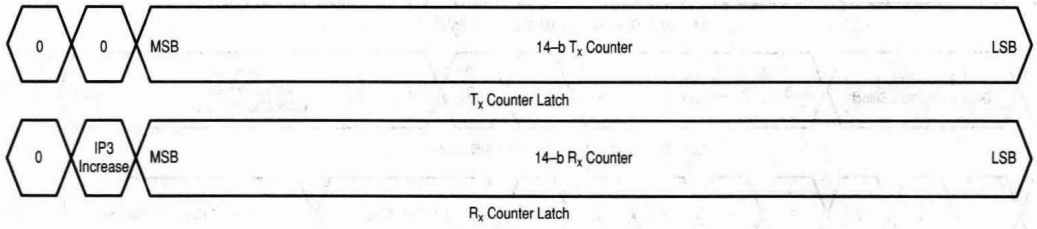


Figure 112. Reference Counter Register

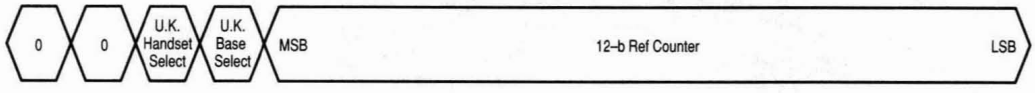
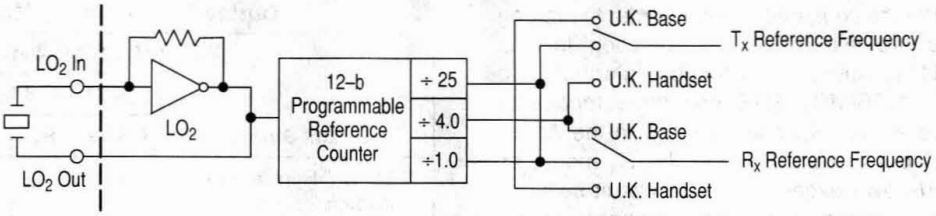


Figure 113. Reference Counter Register Programming Mode

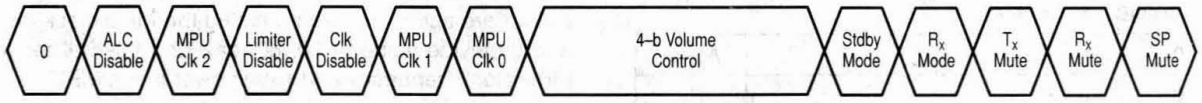


U.K. Handset Select	U.K. Base Select	T_x Divider Value	R_x Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Base Set
1	0	4	25	U.K. Hand Set
1	1	4	4	Netherlands Base and Hand Set

Figure 114. Reference Frequency and Divider Values

MC13110A/B / MC13111A/B Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency	SC Filter Clock Divider	SC Filter Clock Frequency	Scrambler Modulation Divider	Scrambler Modulation Frequency
10.24 MHz	2048	1	5.0 kHz	31	165.16 kHz	40	4.129 kHz
10.24 MHz	1024	4	5.0 kHz	31	165.16 kHz	40	4.129 kHz
11.15 MHz	2230	1	5.0 kHz	34	163.97 kHz	40	4.099 kHz
12.00 MHz	2400	1	5.0 kHz	36	166.67 kHz	40	4.167 kHz
11.15 MHz	1784	1	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	4	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	25	1.0 kHz	34	163.97 kHz	40	4.099 kHz

Figure 115. Mode Control Register



Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 114 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries. "LO_2 In" may also serve as an input for an externally generated reference signal which is ac–coupled. The switched capacitor filter 6–bit programmable counter must be programmed for the crystal frequency that is selected since this clock is derived from the crystal frequency and must be held constant regardless of the crystal that is selected. The actual switched capacitor clock divider ratio is twice the programmed divider ratio due to the a fixed divide by 2.0 after the programmable counter. The scrambler mixer modulation frequency is the switched capacitor clock divided by 40 for the MC13110A/B.

Mode Control Register

The power saving modes; mutes, disables, volume control, and microprocessor clock output frequency are all set by the Mode Control Register. Operation of the Control Register is explained in Figures 115 through 119.

Figure 116. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
T_x Limiter Disable	1 0	T_x Limiter Disabled Normal Operation
Clock Disable (MC13110A/111A)	1 0	MPU Clock Output Disabled Normal Operation
Clock Disable (MC13110B/111B)	1 0	Don't Care Normal Operation
T_x Mute	1 0	Transmit Channel Muted Normal Operation
R_x Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13110A/B or MC13111A/B are used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation for the MC13110A/MC13111A; Active, R_x, Standby, Interrupt, and Inactive. The MC13110B/MC13111B has three modes of operation. They are Active, R_x, and Standby. In the Active mode, all circuit blocks are powered. In the R_x mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In the Inactive Mode, all circuitry is powered down except the MPU serial interface. Latch memory is maintained in all modes. All mode functions are the same for the MC13110B/MC13111B, except that there is no Inactive mode. With the "B" version the MPU Clock is always running so that there can never be a register reset if the memory is disturbed. Figure 118 shows the control register bit values for selection of each power saving mode and Figure 118 shows the circuit blocks which are powered in each of these operating modes.

Figure 117. Power Saving Mode Selection

Stdby Mode Bit	R_x Mode Bit	"CD Out/ Hardware Interrupt" Pin	Power Saving Mode
MC13110A/MC13111A			
0	0	X	Active
0	1	X	R_x
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Interrupt
MC13110B/MC13111B [Note 14]			
0	0	X	Active
0	1	X	R_x
1	X	X	Standby
1	1	0	Interrupt

NOTES: 13. "X" is a don't care
14. MPU Clock Out is "Always On"

Figure 118. Circuit Blocks Powered During Power Saving Modes

Circuit Blocks	MC13110A/MC13111A / MC13110B/MC13111B Active	R_x	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1, 2]
MPU Serial Interface	X	X	X	X[2]
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver and 1st LO VCO	X	X		
R_x PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_x PLL	X			
R_x and T_x Audio Paths	X			

NOTES: 15. In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.
16. There is no Inactive mode for MC13110B/MC13111B.

Power Saving Application – Option 1 (MC13110B and MC13111B Only)

When the handset is in standby, power can be reduced by entering a "low power" mode and periodically switching to "sniff" mode to check for incoming calls. Figure 119. shows an application where the "Clk Out" pin provides the clock for the MPU. In this application, the 2nd LO and MPU clock run continuously. The MPU maintains control at all times and sets the timing for transitions into the "sniff" mode. Power is saved in the low power mode by putting the MC13110B/MC13111B into its "Standby" mode. Only the 2nd LO and MPU clock divider are active. By programming the MPU clock divider to a large divide value of 20, 80, or 312.5 this will reduce the MPU clock frequency and save power in the MPU.

Power Saving Application – Option 2 (MC13110A and MC13111A Only)

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13110A/MC13111A into the Inactive mode. This turns off the MPU Clock Output (see Figure 120) and disables the microprocessor. Once a command is given to switch the IC into an "Inactive" mode, the MPU Clock output will remain active for a minimum of one reference counter cycle (about 200 μs) and up to a maximum of two reference counter cycles (about 400 μs). This is performed in order to give the MPU adequate time to power down.

An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_x modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state, because of an external pull–up resistor. In the Inactive mode, the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low", by the external timing circuit, the IC switches from the Inactive to the Interrupt mode. Thereby turning on the MPU Clock Output. The MPU can then resume control of the IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active, or R_x modes.

Figure 119. Power Saving Application – Option 1

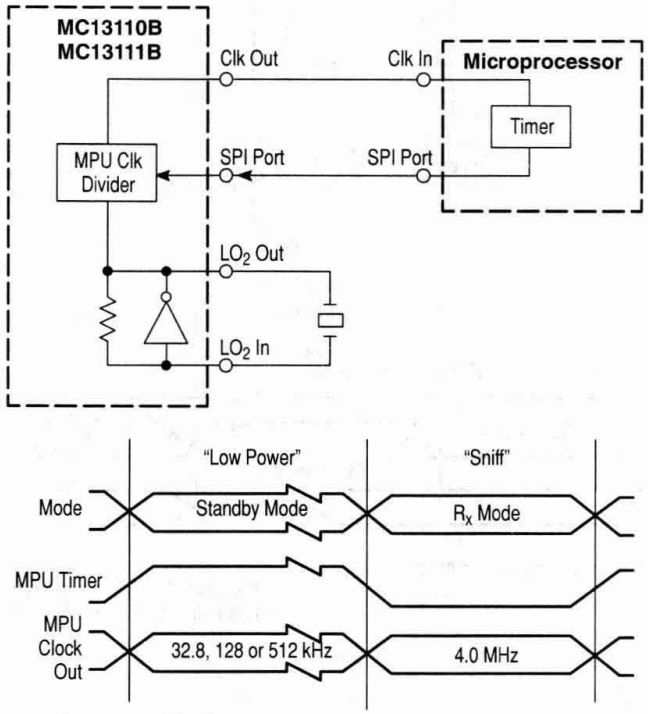
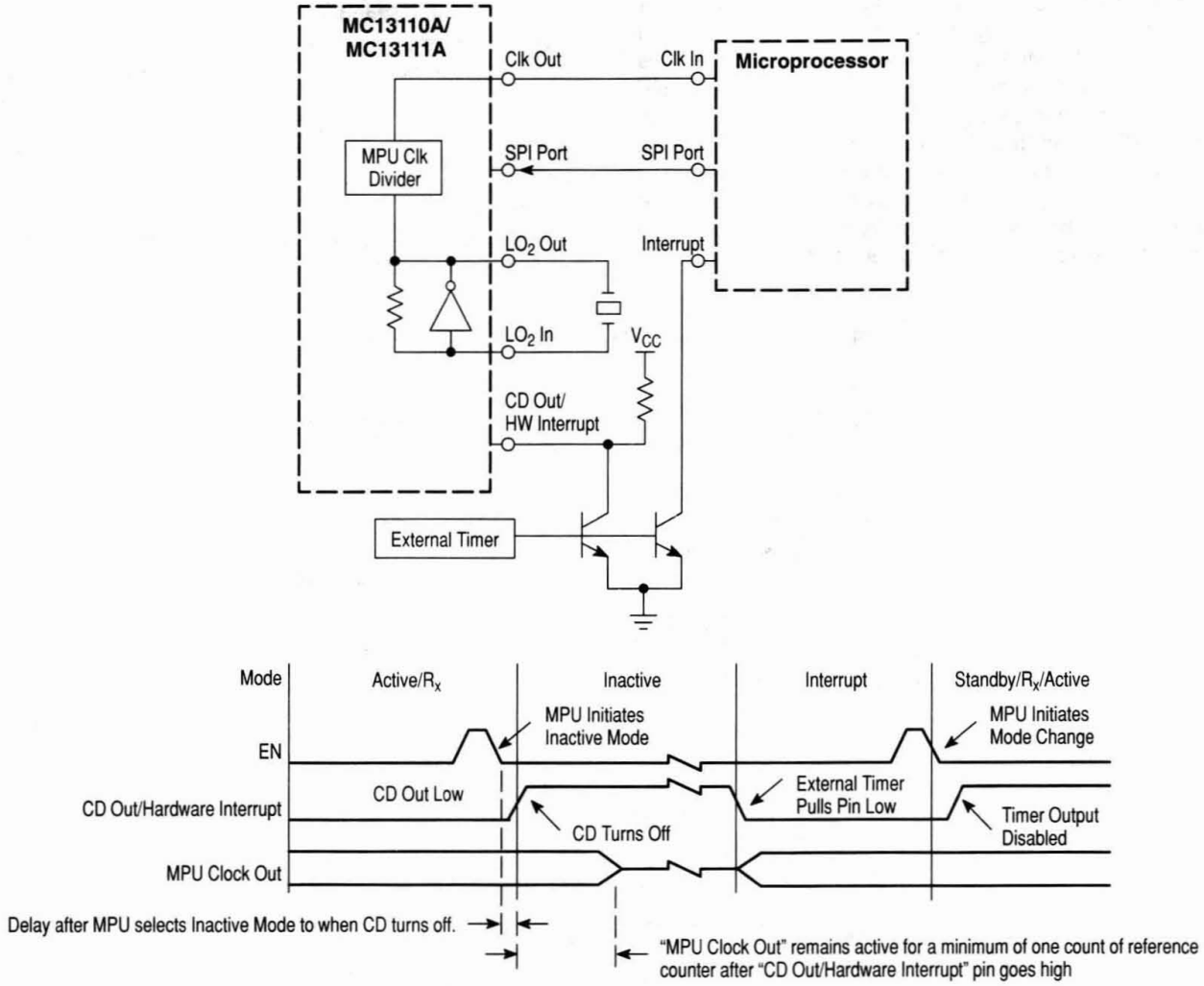


Figure 120. Power Saving Application – Option 2 (MC13110A/MC13111A Only)



MPU "Clk Out" Divider Programming

The "Clk Out" signal is derived from the second local oscillator. It can be used to drive a microprocessor (MPU) clock input. This will eliminate the need for a separate crystal to drive the MPU, thus reducing system cost. Figure 121 shows the relationship between the second LO crystal frequency and the clock output for each divide value. Figure 122 shows the "Clk Out" register bit values. With a 10.24 MHz crystal, the divide by 312.5 gives the same clock frequency as a clock crystal and allows the MPU to display the time on a LCD display without additional external components.

Figure 121. Clock Output Values

Crystal Frequency	Clock Output Divider							
	2	2.5	3	4	5	20	80	312.5
10.24 MHz	5.120 MHz	4.096 MHz	3.413 MHz	2.560 MHz	2.048 MHz	512 kHz	128 kHz	32.768 kHz
11.15 MHz	5.575 MHz	4.460 MHz	3.717 MHz	2.788 MHz	2.230 MHz	557 kHz	139 kHz	35.680 kHz
12.00 MHz	6.000 MHz	4.800 MHz	4.000 MHz	3.000 MHz	2.400 MHz	600 kHz	150 kHz	38.400 kHz

Figure 122. Clock Output Divider

MPU Clk Bit #2	MPU Clk Bit #1	MPU Clk Bit #0	Clk Out Divider Value
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	2.5
1	0	1	20
1	1	0	80
1	1	1	312.5

MPU "Clk Out" Power–Up Default Divider Value

The power–up default divider value is "divide by 5". This provides a MPU clock of about 2.0 MHz after initial power–up. The reason for choosing a relatively low clock frequency at initial power–up is because some microprocessors operate using a 3.0 V power supply and have a maximum clock frequency of 2.0 MHz. After initial power–up, the MPU can change the clock divider value and set the clock to the desired operating frequency. Special care was taken in the design of the clock divider to insure that the transition between one clock divider value and another is "smooth" (i.e. there will be no narrow clock pulses to disturb the MPU).

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13110A/B or MC13111A/B and the microprocessor has the potential to radiate noise. Problems in the system can occur, especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize the radiated noise, a 1000 Ω resistor is included on–chip in series with the "Clk Out" output driver. A small capacitor or inductor with a capacitor can be connected to the "Clk Out" line on the PCB to form a one or two pole low pass filter. This filter should significantly reduce noise radiated by attenuating the high frequency harmonics on the signal line. The filter can also be used to attenuate the signal level so that it is only as large as required by the MPU clock input. To further reduce radiated noise, the PCB signal trace length should be kept to a minimum.

Volume Control Programming

The volume control adjustable gain block can be programmed in 2 dB gain steps from –14 dB to +16 dB. The power–up default value for the MC13110A/B and MC13111A/B is 0 dB. (see Figure 123)

Figure 123. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8 dB
0	1	0	0	4	–6 dB
0	1	0	1	5	–4 dB
0	1	1	0	6	–2 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2 dB
1	0	0	1	9	4 dB
1	0	1	0	10	6 dB
1	0	1	1	11	8 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the T_x Voltage Gain, R_x Voltage Gain, and Carrier Detect threshold. Operation of these latch bits are explained in Figures 124, 125 and 126.

T_x and R_x Gain Programming

The T_x and R_x audio signal paths each have a programmable gain block. If a T_x or R_x voltage gain, other than the nominal power–up default, is desired, it can be programmed through the MPU interface. Alternately, these programmable gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system (see Figure 125). In this case, the T_x and R_x gain register values should be stored in ROM during final test so that they can be reloaded each time the IC is powered up.

Figure 124. Gain Control Latch Bits

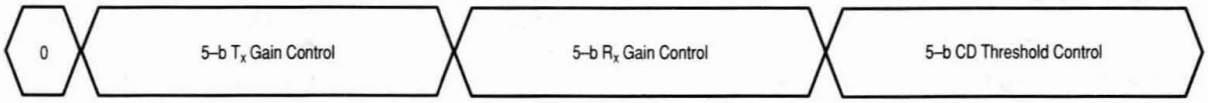


Figure 125. T_x and R_x Gain Control

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Control #	Gain/Attenuation Amount
–	–	–	–	–	<6	–9 dB
0	0	1	1	0	6	–9 dB
0	0	1	1	1	7	–8 dB
0	1	0	0	0	8	–7 dB
0	1	0	0	1	9	–6 dB
0	1	0	1	0	10	–5 dB
0	1	0	1	1	11	–4 dB
0	1	1	0	0	12	–3 dB
0	1	1	0	1	13	–2 dB
0	1	1	1	0	14	–1 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1 dB
1	0	0	0	1	17	2 dB
1	0	0	1	0	18	3 dB
1	0	0	1	1	19	4 dB
1	0	1	0	0	20	5 dB
1	0	1	0	1	21	6 dB
1	0	1	1	0	22	7 dB
1	0	1	1	1	23	8 dB
1	1	0	0	0	24	9 dB
1	1	0	0	1	25	10 dB
–	–	–	–	–	>25	10 dB

Carrier Detect Threshold Programming

The "CD Out" pin gives an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be programmed through the MPU interface as shown in Figure 126 below. Alternately, the carrier detect threshold can be electronically adjusted during final test of the telephone to reduce the tolerance of the carrier detect threshold. This is done by measuring the threshold and then by adjusting the threshold through the MPU interface. In this case, it is necessary to store the carrier detect register value in ROM so that the CD register can be reloaded each time the combo IC is powered up. If a preamp is used before the first mixer it may be desirable to scale the carrier detect range by connecting an external resistor from the "RSSI" pin to ground. The internal resistor is 187 kΩ.

Figure 126. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9 dB
0	1	1	0	0	12	–8 dB
0	1	1	0	1	13	–7 dB
0	1	1	1	0	14	–6 dB
0	1	1	1	1	15	–5 dB
1	0	0	0	0	16	–4 dB
1	0	0	0	1	17	–3 dB
1	0	0	1	0	18	–2 dB
1	0	0	1	1	19	–1 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1 dB
1	0	1	1	0	22	2 dB
1	0	1	1	1	23	3 dB
1	1	0	0	0	24	4 dB
1	1	0	0	1	25	5 dB
1	1	0	1	0	26	6 dB
1	1	0	1	1	27	7 dB
1	1	1	0	0	28	8 dB
1	1	1	0	1	29	9 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Clock Divider/Voltage Adjust Register

This register controls the divider value for the programmable switched capacitor filter clock divider, the low battery detect threshold select, the voltage reference adjust, and the scrambler bypass mode (MC13110A/B only). Operation is explained in Figures 127 through 134. The T_x and R_x Audio bits are don't cares for either the MC13111A or the MC13111B device. However, for the MC13110A/B, these bits are defined. Figure 129 describes the operation. Note the power–up default bit is set to <0>, which is the scrambler bypass mode.

Low Battery Detect

The low battery detect circuit can be operated in programmable and non–programmable threshold modes. The non–programmable threshold mode is only available in the 52 QFP package. In this mode, there are two low battery detect comparators and the threshold values are set by external resistor dividers which are connected to the REF1 and REF2 pins. In the programmable threshold mode, several different threshold levels may be selected through the "Low Battery Detect Threshold Register" as shown in Figure 128. The power–on default value for this register is <0,0,0> and is the non–programmable mode. Figure 130 shows equivalent schematics for the programmable and non–programmable operating modes.

Figure 127. Clock Divider/Voltage Adjust Latch Bits

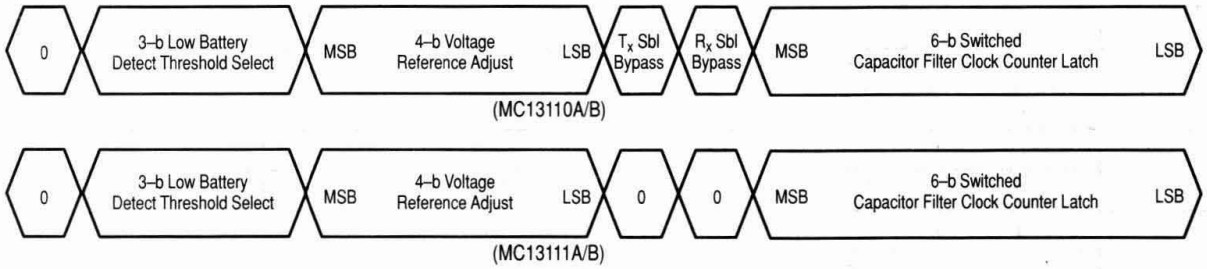


Figure 128. Low Battery Detect Threshold Selection

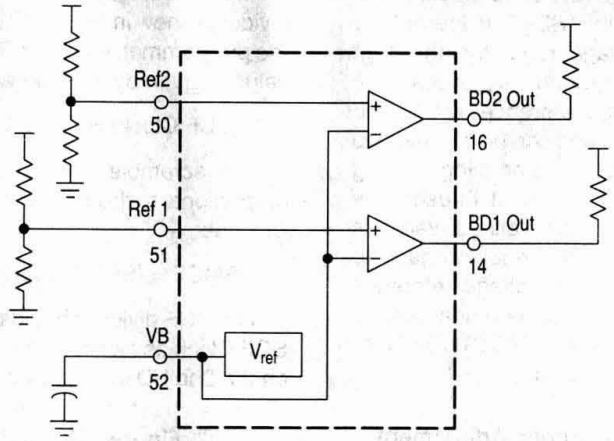
Low Battery Detect Threshold Select Bit #2	Low Battery Detect Threshold Select Bit #1	Low Battery Detect Threshold Select Bit #0	Select #	Operating Mode	Nominal Low Battery Detect Threshold Value (V)
0	0	0	0	Non–Programmable	N/A
0	0	1	1	Programmable	2.850
0	1	0	2	Programmable	2.938
0	1	1	3	Programmable	3.025
1	0	0	4	Programmable	3.200
1	0	1	5	Programmable	3.288
1	1	0	6	Programmable	3.375
1	1	1	7	Programmable	3.463

NOTE: 17. Nominal Threshold Value is before electronic adjustment.

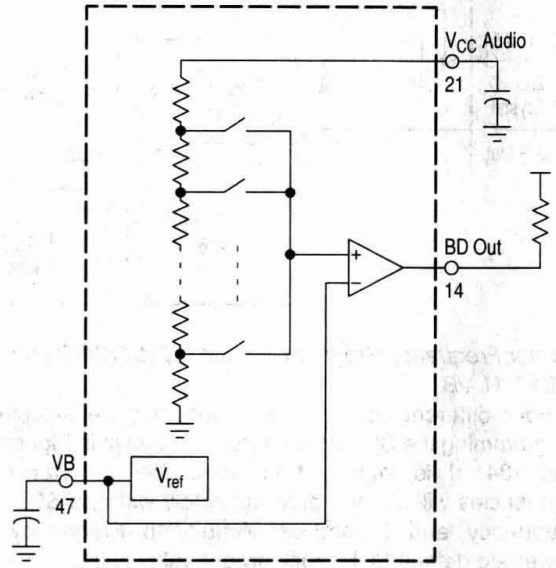
Figure 129. MC13110A/B Bypass Mode Bit Description (MC13110A/B Only)

T_x Scrambler Bypass	1	T_x Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation with T_x Scrambler
R_x Scrambler Bypass	1	R_x Scrambler Post–Mixer LPF and Mixer Bypassed
	0	Normal Operation R_x Scrambler

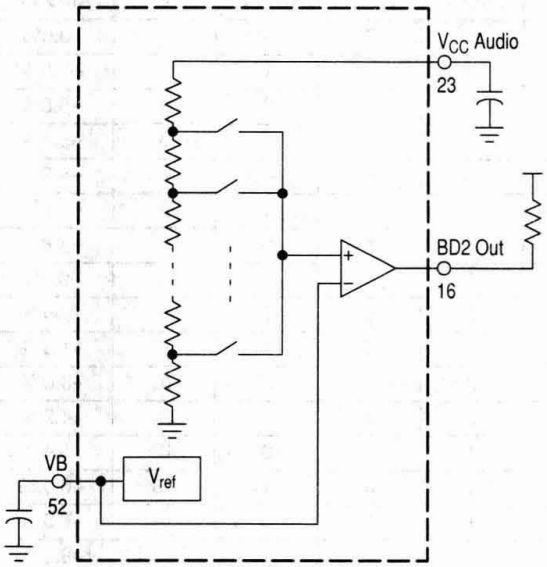
Figure 130. Low Battery Detect Equivalent Schematics



Non–Programmable Threshold Mode: 52–QFP Package



Programmable Threshold Mode: 48–LQFP Package



Programmable Threshold Mode: 52–QFP Package

Voltage Reference Adjustment

An internal 1.5 V bandgap voltage reference provides the voltage reference for the "BD_1 Out" and "BD_2 Out" low battery detect circuits, the "PLL V_{ref}" voltage regulator, the "V_B" reference, and all internal analog ground references. The initial tolerance of the bandgap voltage reference is ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming. During final test of the telephone, the battery detect threshold is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110A/B or MC13111A/B is powered up (see Figure 131).

Figure 131. Bandgap Voltage Reference Adjustment

V_{ref} Adj. Bit #3	V_{ref} Adj. Bit #2	V_{ref} Adj. Bit #1	V_{ref} Adj. Bit #0	V_{ref} Adj. #	V_{ref} Adj. Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	+0.6 %
1	0	0	1	9	+1.8 %
1	0	1	0	10	+3.0 %
1	0	1	1	11	+4.2 %
1	1	0	0	12	+5.4 %
1	1	0	1	13	+6.6 %
1	1	1	0	14	+7.8 %
1	1	1	1	15	+9.0 %

Switched Capacitor Filter Clock Programming

A block diagram of the switched capacitor filter clock divider is show in Figure 132. There is a fixed divide by 2 after the programmable divider. The switched capacitor filter clock value is given by the following equation;

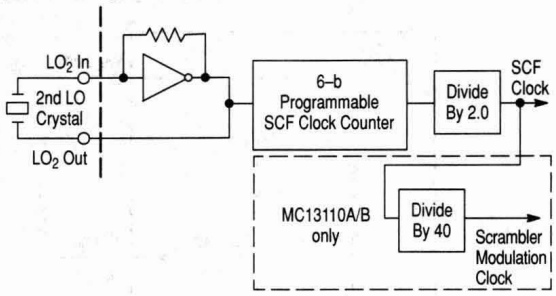
(SCF Clock) = F(2nd LO) / (SCF Divider Value * 2).

The scrambler modulation clock frequency (SMCF) is proportional to the SCF clock. The following equation defines its value:

SMCF = (SCF Clock)/40

The SCF divider should be set to a value which brings the SCF Clock as close to 165.16 kHz as possible. This is based on the 2nd LO frequency which is chosen in Figure 114.

Figure 132. SCF Clock Divider Circuit



Corner Frequency Programming for MC13110A/B and MC13111A/B

Four different corner frequencies may be selected by programming the SCF Clock divider as shown in Figures 133 and 134. It is important to note, that all filter corner frequencies will change proportionately with the SCF Clock Frequency and Scrambler Modulation Frequency. The power–up default SCF Clock divider value is 31.

Figure 133. Corner Frequency Programming for 10.240 MHz 2nd LO

MC13110A/B							
MC13111A/B							
SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_x Upper Corner Frequency (kHz)	T_x Upper Corner Frequency (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
29	58	176.55	4.147	3.955	4.414	267.2	3.902
30	60	170.67	4.008	3.823	4.267	258.3	3.772
31	62	165.16	3.879	3.700	4.129	250.0	3.650
32	64	160.00	3.758	3.584	4.000	242.2	3.536

NOTE: 18. All filter corner frequencies have a tolerance of ±3%.
19. R_x and T_x Upper Corner Frequencies are the same corner frequencies for the MC13110A/B in scrambler bypass

Figure 134. Corner Frequency Programming for 11.15 MHz 2nd LO

MC13110A/B MC13111A/B SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_x Upper Corner Frequency (kHz)	T_x Upper Corner Frequency (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
32	64	174.22	4.092	3.903	4.355	263.7	3.850
33	66	168.94	3.968	3.785	4.223	255.7	3.733
34	68	163.97	3.851	3.673	4.099	248.2	3.624
35	70	159.29	3.741	3.568	3.982	241.1	3.520

NOTES: 20. All filter corner frequencies have a tolerance of ±3%.
21. R_x and T_x Upper Corner Frequencies are the same corner frequencies for the MC13110A/B in scrambler bypass

Figure 135. Auxiliary Register Latch Bits

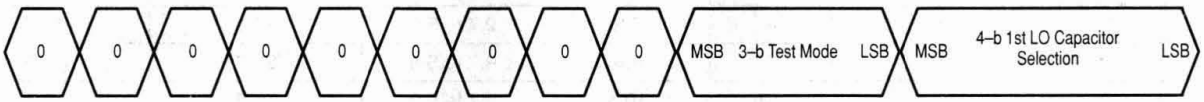


Figure 136. Digital Test Mode Description

TM #	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_x V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	Normal Operation	>200 mVpp	–
1	0	0	1	R_x Counter	0 to 2.5 V	Input Frequency/R_x Counter Value
2	0	1	0	T_x Counter	0 to 2.5 V	Input Frequency/T_x Counter Value
3	0	1	1	Reference Counter + Divide by 4/25	0 to 2.5 V	Input Frequency/Reference Counter Value * 100
4	1	0	0	SC Counter	0 to 2.5 V	Input Frequency/SC Counter Value * 2
5	1	0	1	ALC Gain = 10 Option	N/A	N/A
6	1	1	0	ALC Gain = 25 Option	N/A	N/A

Auxiliary Register

The auxiliary register contains a 4–bit First LO Capacitor Selection latch and a 3–bit Test Mode latch. Operation of these latch bits are explained in Figures 135, 136 and 137.

Test Modes

Test modes are be selected through the 3–bit Test Mode Register. In test mode, the "T_x VCO" input pin is multiplexed to the input of the counter under test. The output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. **Make sure test mode bits are set to "0's" for normal operation.** Test mode operation is described in Figure 136. During normal operation, the "T_x VCO" input can be a minimum of 200 mVpp at 80 MHz and should be AC coupled. Input signals should be standard logic levels of 0 to 2.5 V and a maximum frequency of 16 MHz.

First Local Oscillator Programmable Capacitor Selection

There is a very large frequency difference between the minimum and maximum channel frequencies in the 25 Channel U.S. standard. The internal varactor adjustment range is not large enough to accommodate this large frequency span. An internal capacitor with 15 programmable capacitor values can be used to cover the 25 channel frequency span without the need to add external capacitors and switches. The programmable internal capacitor can also be used to eliminate the need to use an external variable capacitor to adjust the 1st LO center frequency during telephone assembly. Figure 32 shows the schematic of the 1st LO tank circuit. Figure 137 shows the register control bit values.

The internal programmable capacitor is composed of a matrix bank of capacitors that are switched in as desired. Programmable capacitor values between about 0 and 16 pF can be selected in steps of approximately 1.1 pF. The internal parallel resistance values in the table can be used to calculate the quality factor (Q) of the oscillator if the Q of the external inductor is known. The temperature coefficient of the varactor is 0.08%/°C. The temperature coefficient of the internal programmable capacitor is negligible. Tolerance on the varactor and programmable capacitor values is ±15%.

Figure 137. First Local Oscillator Internal Capacitor Selection

1st LO Cap. Bit 3	1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap. Bit 0	1st LO Cap. Select	Internal Programmable Capacitor Value (pF)	Varactor Value over 0.3 to 2.5 V (pF)	Equivalent Internal Parallel Resistance at 40 MHz (kΩ)	Equivalent Internal Parallel Resistance at 51 MHz (kΩ)
0	0	0	0	0	0.0	9.7 to 5.8	1200	736
0	0	0	1	1	0.6	9.7 to 5.8	79.3	48.8
0	0	1	0	2	1.7	9.7 to 5.8	131	80.8
0	0	1	1	3	2.8	9.7 to 5.8	31.4	19.3
0	1	0	0	4	3.9	9.7 to 5.8	33.8	20.8
0	1	0	1	5	4.9	9.7 to 5.8	66.6	41
0	1	1	0	6	6.0	9.7 to 5.8	49.9	30.7
0	1	1	1	7	7.1	9.7 to 5.8	40.7	25.1
1	0	0	0	8	8.2	9.7 to 5.8	27.1	16.7
1	0	0	1	9	9.4	9.7 to 5.8	21.6	13.3
1	0	1	0	10	10.5	9.7 to 5.8	20.5	12.6
1	0	1	1	11	11.6	9.7 to 5.8	18.6	11.5
1	1	0	0	12	12.7	9.7 to 5.8	17.2	10.6
1	1	0	1	13	13.8	9.7 to 5.8	15.8	9.7
1	1	1	0	14	14.9	9.7 to 5.8	15.3	9.4
1	1	1	1	15	16.0	9.7 to 5.8	14.2	8.7

OTHER APPLICATIONS INFORMATION

PCB Board Lay–Out Considerations

The ideal printed circuit board (PCB) lay out would be double–sided with a full ground plane on one side. The ground plane would be divided into separate sections to prevent any audio signal from feeding into the first local oscillator via the ground plane. Leaded components, can likewise, be inserted on the ground plane side to improve shielding and isolation from the circuit side of the PCB. The opposite side of the PCB is typically the circuit side. It has the interconnect traces and surface mount components. In cases where cost allows, it may be beneficial to use multi–layer boards to further improve isolation of components and sensitive sections (i.e. RF and audio). For the CT–0 band, it is also permissible to use single–sided PC layouts, but with continuous full ground fill in and around the components.

The proper placement of certain components specified in the application circuit may be very critical. In a lay–out design, these components should be placed before the other less critical components are inserted. It is also imperative that all RF paths be kept as short as possible. Finally, the MC13110A/B and MC13111A/B ground pins should be tied to ground at the pins and V_{CC} pins should have adequate decoupling to ground as close to the IC as possible. In mixed mode systems where digital and RF/Analog circuitry are present, the V_{CC} and V_{EE} buses need to be ac–decoupled and isolated from each other. The design must also take great caution to avoid interference with low level analog circuits. The receiver can be particularly susceptible to interference as they respond to signals of only a few microvolts. Again, be sure to keep the dc supply lines for the digital and analog portions separate. Avoid ground paths carrying common digital and analog currents. as well.

Component Selection

The evaluation circuit schematics specify particular components that were used to achieve the results shown in the typical curves and tables, but alternate components should give similar results. The MC13110A/B and MC13111A /B IC are capable of matching the sensitivity, IMD, adjacent channel rejection, and other performance criteria of a multi–chip analog cordless telephone system. For the most part, the same external components are used as in the multi–chip solution.

VB and PLL V_{ref}

VB is an internally generated bandgap voltage. It functions as an ac reference point for the operational amplifiers in the audio section as well as for the battery detect circuitry. This pin needs to be sufficiently filtered to reduce noise and prevent crosstalk between R_x audio to T_x audio signal paths. A practical capacitor range to choose that will minimize crosstalk and noise relative to start up time is 0.5 µf to 10 µf. The start time for a 0.5 µf capacitor is approximately 5.0 ms, while a 10µf capacitor is about 10 ms.

The "PLL V_{ref}" pin is the internal supply voltage for the R_x and T_x PLL's. It is regulated to a nominal 2.5 V. The "V_{CC} Audio" pin is the supply voltage for the internal voltage regulator. Two capacitors with 10 µF and 0.01 µF values must be connected to the "PLL V_{ref}" pin to filter and stabilize this regulated voltage. The "PLL V_{ref}" pin may be used to power other IC's as long as the total external load current does not exceed 1.0 mA. The tolerance of the regulated voltage is initially ±8.0%, but is improved to ±4.0% after the internal Bandgap voltage reference is adjusted electronically through the MPU serial interface. The voltage regulator is turned off in the Standby and Inactive modes to reduce current drain. In these modes, the "PLL V_{ref}" pin is internally connected to the "V_{CC} Audio" pin (i.e., the power supply voltage is maintained but is now unregulated).

It is important to note that the momentary drop in voltage below 2.5 V during this transition may affect initial PLL lock times and also may trigger the reset. To prevent this, the PLL V_{ref} capacitor described above should be kept the same or larger than the VB capacitor, say 10 µf as shown in the evaluation and application diagrams.

DC Coupling

Choosing the right coupling capacitors for the compander is also critical. The coupling capacitors will have an affect on the audio distortion, especially at lower audio frequencies. A useful capacitor range for the compander timing capacitors is 0.1 µf to 1.0 µf. It is advised to keep the compander capacitors the same value in both the handset and baseset applications.

All other dc coupling capacitors in the audio section will form high pass filters. The designer should choose the overall cut off frequency (–3.0 dB) to be around 200 Hz. Designing for lower cut off frequencies may add unnecessary cost and capacitor size to the design, while selecting too high of a cut off frequency may affect audio quality. It is not necessary or advised to design each audio coupling capacitors for the same cut off frequency. Design for the overall system cut off frequency. (Note: Do not expect the application, evaluation, nor production test schematics to necessarily be the correct capacitor selections.) The goals of these boards may be different than the systems approach a designer must consider.

For the supply pins (V_{CC} Audio and V_{CC} RF) choose a 10 µf in parallel with a high quality 0.01 µf capacitor. Separation of the these two supply planes is essential, too. This is to prevent interference between tne RF and audio sections. It is always a good design practice to add additional coupling on each supply plane to ground as well.

The IF limiter capacitors are recommended to be 0.1 µf. Smaller values lower the gain of the limiter stage. The –3.0 dB limiting sensitivity and SINAD may be adversely affected.

Figure 138. Evaluation Board Schematic

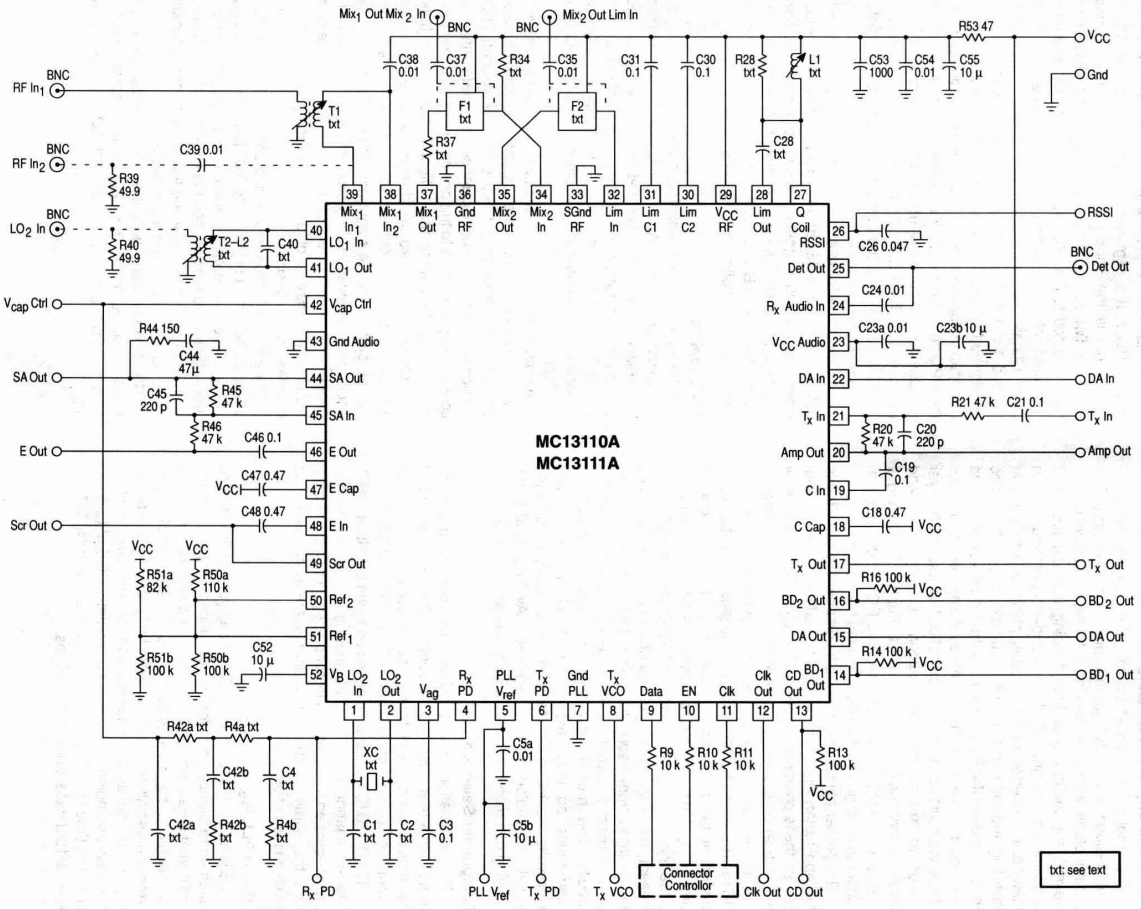


Figure 139. Evaluation Board Bill of Materials for U.S. and French Application

Comp. Number	USA Application Handset		French Application Base		
	RF (50 Ω)	RF Matched	RF Crystal (50 Ω)	RF Ceramic (50 Ω)	RF Matched
INPUT MATCHING					
T1	n.m.	Toko 1:5 292GNS–765A0	n.m.	n.m.	Toko 1:5 292GNS–765A0
C38	0.01	n.m.	0.01	0.01	n.m.
C39	0.01	n.m.	0.01	0.01	n.m.
10.7 MHz FILTER					
F1	Ceramic	Ceramic	Crystal	Ceramic	Ceramic
R37	0	0	1.2 k	0	0
R34	360	360	3.01 k	360	360
450 kHz FILTER					
F2	4 Element Murata E	4 Element Murata E	4 Element Murata G	4 Element Murata G	4 Element Murata G
DEMODULATOR					
L1	Q Coil Toko 7MCS–8128Z	Q Coil Toko 7MCS–8128Z	Ceramic Murata CDBM 450C34	Ceramic Murata CDBM 450C34	Ceramic Murata CDBM 450C34
R28	22.1 k	22.1 k	2.7 k	2.7 k	2.7 k
C28	10 p	10 p	390 p	390 p	390 p
OSCILLATOR					
Xtal	10.24 C1 = 10 p	10.24 C1 = 10 p	11.15 C1 = 18 p	11.15 C1 = 18 p	11.15 C1 = 18 p
C2	18 p	18 p	33 p	33 p	33 p
C1	5–25 p	5–25 p	15 p + 5–25 p	15 p + 5–25 p	15 p + 5–25 p
FIRST LO					
L2	0.47 Toko T1370	0.47 Toko T1370	0.22 Toko T1368	0.22 Toko T1368	0.22 Toko T1368
C40 HS/BS	HS: 27 pF BS: 22 pF	HS: 27 pF BS: 22 pF	BS: 100 p HS: 68 pF	BS: 100 p HS: 68 pF	BS: 100 p HS: 68 pF
LOOP FILTER HANDSET/BASESET					
R4a	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0
R4b	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0	HS: 0 BS: 0
C4	HS: 6800 BS: 8200	HS: 6800 BS: 8200	HS: 8600 BS: 6800	HS: 8600 BS: 6800	HS: 8600 BS: 6800
R42a	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k	HS: 100 k BS: 100 k
R42b	HS: 22 k BS: 18 k	HS: 22 k BS: 18 k	HS: 18 k BS: 22 k	HS: 18 k BS: 22 k	HS: 18 k BS: 22 k
C42a	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000	HS: 1000 BS: 1000
C42b	HS: 0.068 BS: 0.082	HS: 0.068 BS: 0.082	HS: 0.082 BS: 0.068	HS: 0.082 BS: 0.068	HS: 0.082 BS: 0.068

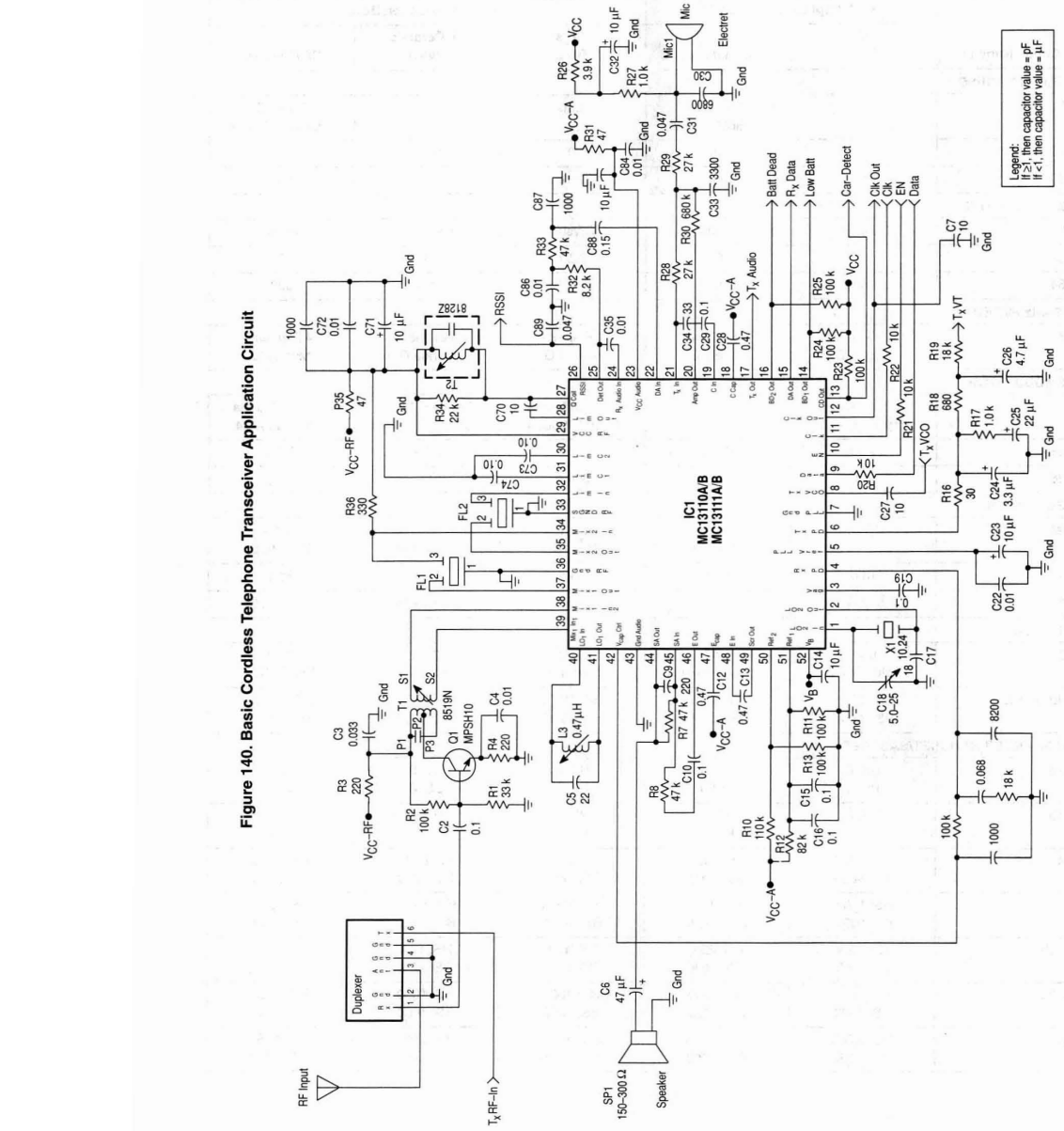
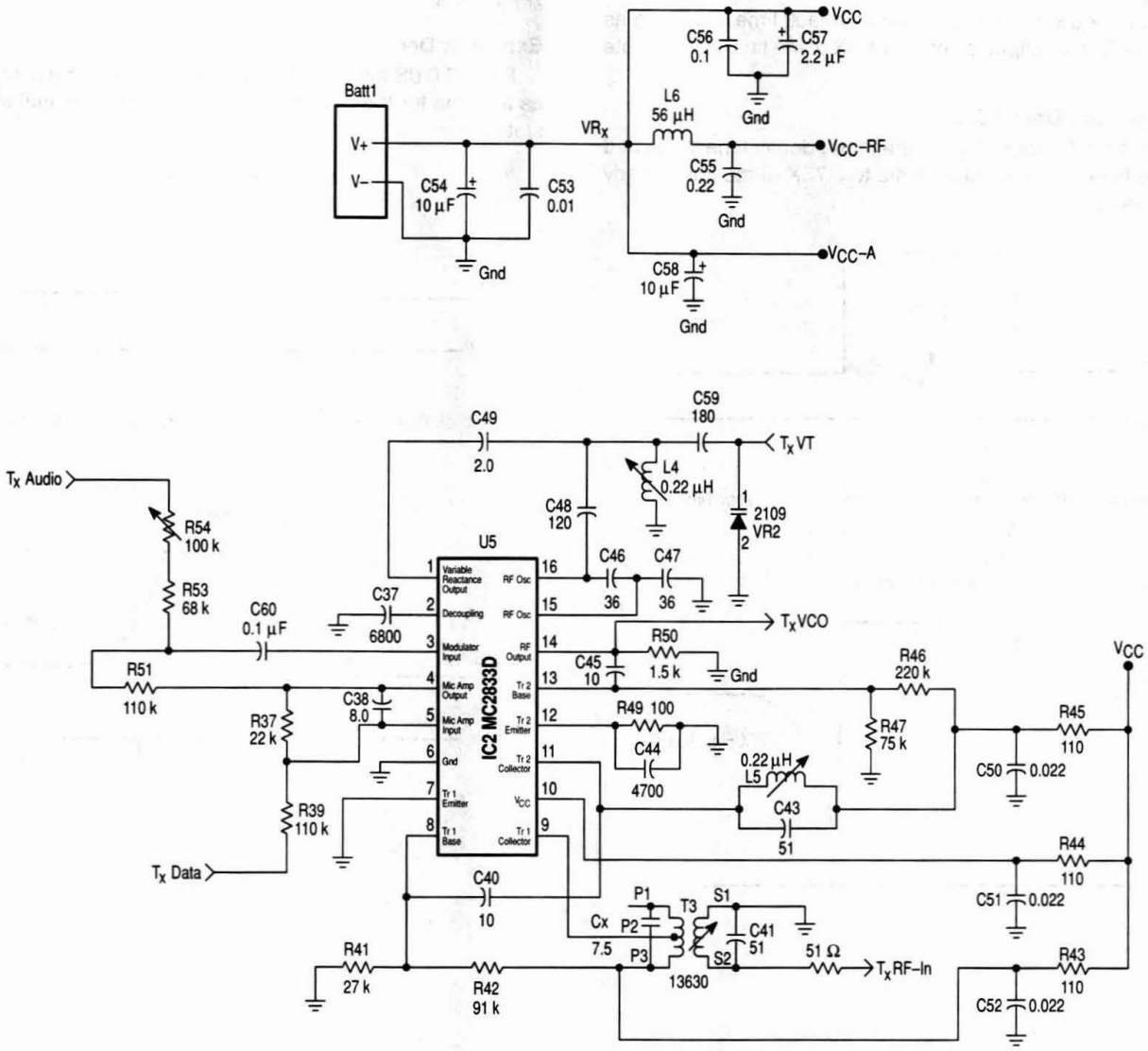


Figure 140. Basic Cordless Telephone Transceiver Application Circuit

Figure 140. Basic Cordless Telephone Transceiver Application Circuit (continued)



APPENDIX C – MEASUREMENT OF COMPANDER ATTACK/DECAY TIME

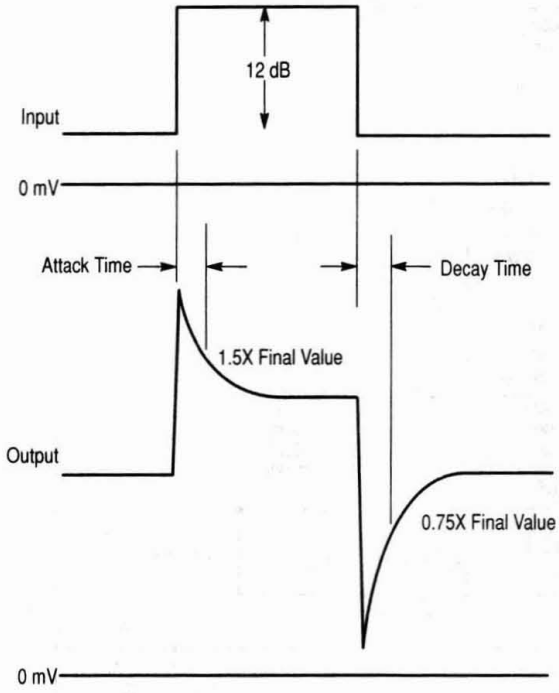
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

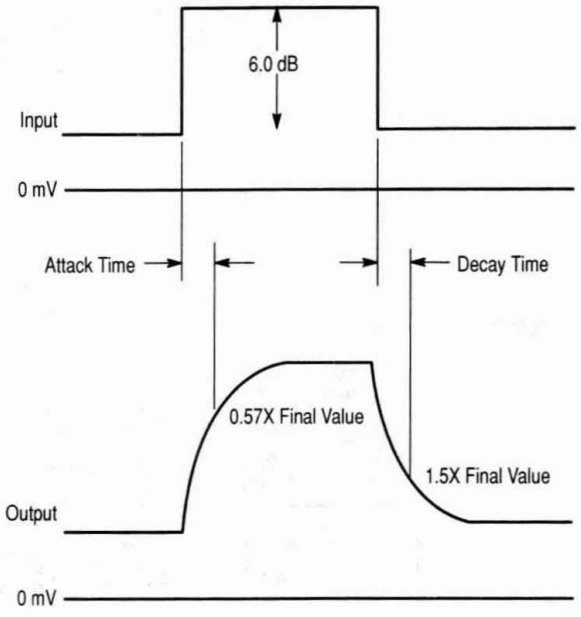


Expander Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expander Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

FM Communications Receivers

MC13135
MC13136

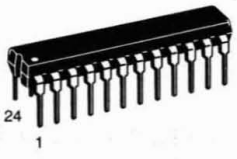
DUAL CONVERSION NARROWBAND FM RECEIVERS

The MC13135/MC13136 are the second generation of single chip, dual conversion FM communications receivers developed by Motorola. Major improvements in signal handling, RSSI and first oscillator operation have been made. In addition, recovered audio distortion and audio drive have improved. Using Motorola's MOSAIC™ 1.5 process, these receivers offer low noise, high gain and stability over a wide operating voltage range.

Both the MC13135 and MC13136 include a Colpitts oscillator, VCO tuning diode, low noise first and second mixer and LO, high gain limiting IF, and RSSI. The MC13135 is designed for use with an LC quadrature detector and has an uncommitted op amp that can be used either for an RSSI buffer or as a data comparator. The MC13136 can be used with either a ceramic discriminator or an LC quad coil and the op amp is internally connected for a voltage buffered RSSI output.

These devices can be used as stand–alone VHF receivers or as the lower IF of a triple conversion system. Applications include cordless telephones, short range data links, walkie–talkies, low cost land mobile, amateur radio receivers, baby monitors and scanners.

- Complete Dual Conversion FM Receiver – Antenna to Audio Output
- Input Frequency Range – 200 MHz
- Voltage Buffered RSSI with 70 dB of Usable Range
- Low Voltage Operation – 2.0 to 6.0 Vdc (2 Cell NiCad Supply)
- Low Current Drain – 3.5 mA Typ
- Low Impedance Audio Output < 25 Ω
- VHF Colpitts First LO for Crystal or VCO Operation
- Isolated Tuning Diode
- Buffered First LO Output to Drive CMOS PLL Synthesizer



P SUFFIX
PLASTIC PACKAGE
CASE 724

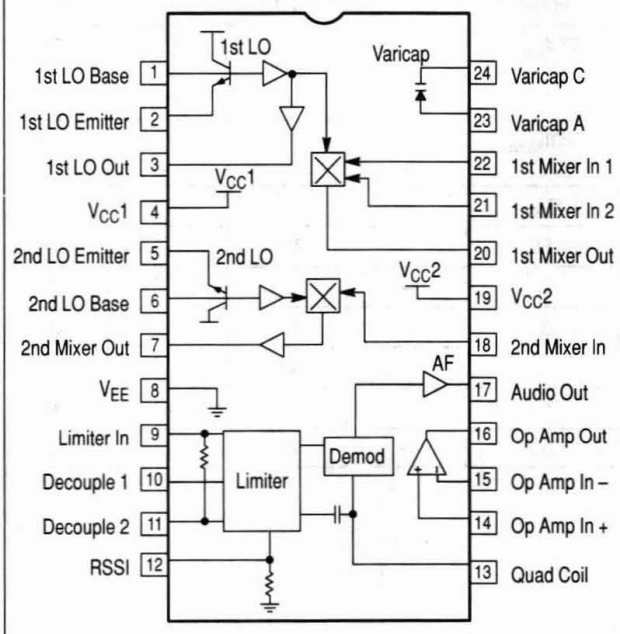
DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

ORDERING INFORMATION

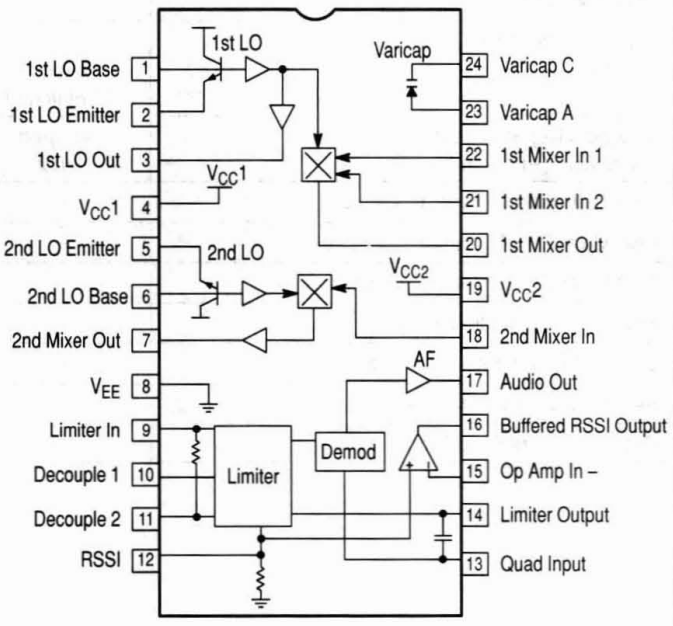
Device	Operating Temperature Range	Package
MC13135P	T_A = – 40° to +85°C	Plastic DIP
MC13135DW		SO–24L
MC13136P		Plastic DIP
MC13136DW		SO–24L

PIN CONNECTIONS

MC13135



MC13136



Each device contains 142 active transistors.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC} (max)	6.5	Vdc
RF Input Voltage	22	RF_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC}	2.0 to 6.0	Vdc
Maximum 1st IF	–	f_{IF1}	21	MHz
Maximum 2nd IF	–	f_{IF2}	3.0	MHz
Ambient Temperature Range	–	T_A	– 40 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 4.0 Vdc, f_o = 49.7 MHz, f_{MOD} = 1.0 kHz, Deviation = ±3.0 kHz, $f_{1st\ LO}$ = 39 MHz, $f_{2nd\ LO}$ = 10.245 MHz, IF1 = 10.7 MHz, IF2 = 455 kHz, unless otherwise noted. All measurements performed in the test circuit of Figure 1.)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Total Drain Current	No Input Signal	I_{CC}	–	4.0	6.0	mAdc
Sensitivity (Input for 12 dB SINAD)	Matched Input	V_{SIN}	–	1.0	–	µVrms
Recovered Audio MC13135 MC13136	V_{RF} = 1.0 mV	AF_O	 170 215	 220 265	 300 365	mVrms
Limiter Output Level (Pin 14, MC13136)		V_{LIM}	–	130	–	mVrms
1st Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain1}	–	12	–	dB
2nd Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain2}	–	13	–	dB
First LO Buffered Output	–	V_{LO}	–	100	–	mVrms
Total Harmonic Distortion	V_{RF} = – 30 dBm	THD	–	1.2	3.0	%
Demodulator Bandwidth	–	BW	–	50	–	kHz
RSSI Dynamic Range	–	RSSI	–	70	–	dB
First Mixer 3rd Order Intercept (Input)	 Matched Unmatched	TOI_{Mix1}	 – –	 –17 –11	 – –	dBm
Second Mixer 3rd Order Intercept (RF Input)	Matched Input	TOI_{Mix2}	–	– 27	–	dBm
First LO Buffer Output Resistance	–	R_{LO}	–	–	–	Ω
First Mixer Parallel Input Resistance	–	R	–	722	–	Ω
First Mixer Parallel Input Capacitance	–	C	–	3.3	–	pF
First Mixer Output Impedance	–	ZO	–	330	–	Ω
Second Mixer Input Impedance	–	Z_I	–	4.0	–	kΩ
Second Mixer Output Impedance	–	ZO	–	1.8	–	kΩ
Detector Output Impedance	–	ZO	–	25	–	Ω

TEST CIRCUIT INFORMATION

Although the MC13136 can be operated with a ceramic discriminator, the recovered audio measurements for both the MC13135 and MC13136 are made with an LC quadrature detector. The typical recovered audio will depend on the external circuit; either the Q of the quad coil, or the RC matching network for the ceramic discriminator. On the MC13136, an external capacitor between Pins 13 and 14 can be used with a quad coil for slightly higher recovered audio. See Figures 10 through 13 for additional information.

Since adding a matching circuit to the RF input increases the signal level to the mixer, the third order intercept (TOI) point is better with an unmatched input (50 Ω from Pin 21 to Pin 22). Typical values for both have been included in the Electrical Characterization Table. TOI measurements were taken at the pins with a high impedance probe/spectrum analyzer system. The first mixer input impedance was measured at the pin with a network analyzer.

Figure 1a. MC13135 Test Circuit

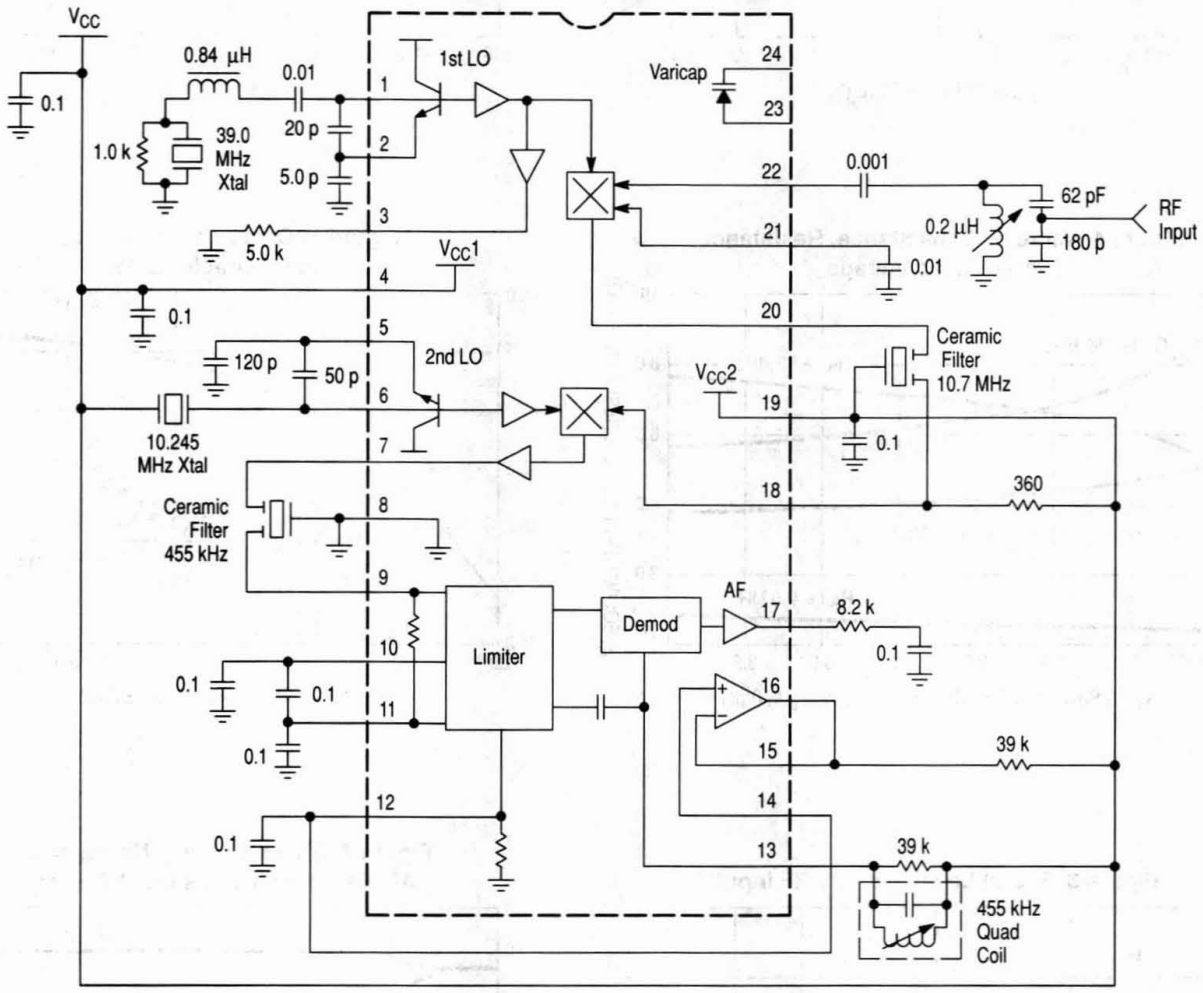


Figure 1b. MC13136 Quad Detector Test Circuit

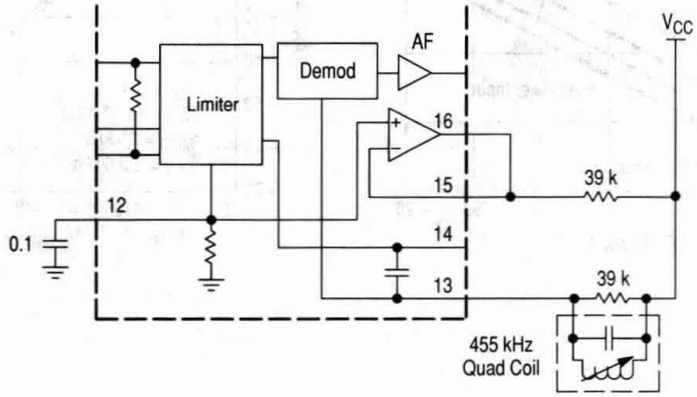


Figure 2. Supply Current versus Supply Voltage

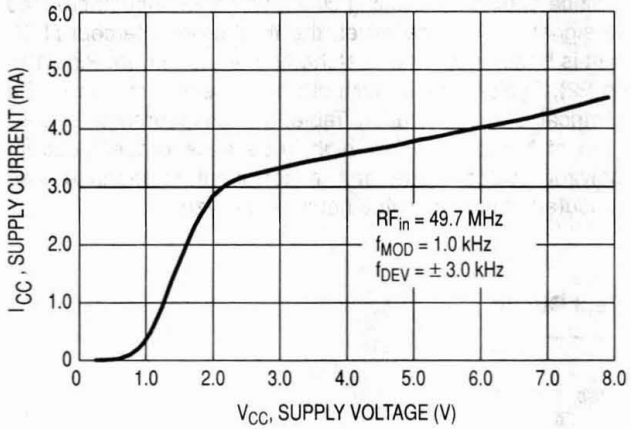


Figure 3. RSSI Output versus RF Input

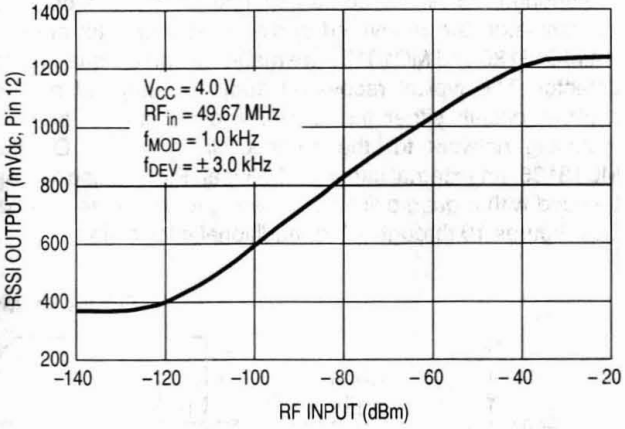


Figure 4. Varactor Capacitance, Resistance versus Bias Voltage

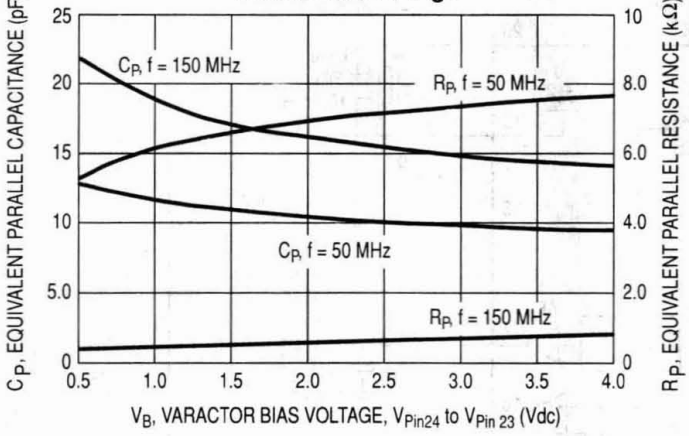

C_P, EQUIVALENT PARALLEL CAPACITANCE (pF)
R_P, EQUIVALENT PARALLEL RESISTANCE (kΩ)
V_B, VARACTOR BIAS VOLTAGE, V_{Pin24} to $V_{Pin\ 23}$ (Vdc)
C_P, f = 150 MHz
R_P, f = 50 MHz
C_P, f = 50 MHz
R_P, f = 150 MHz

Figure 5. Oscillator Frequency versus Varactor Bias

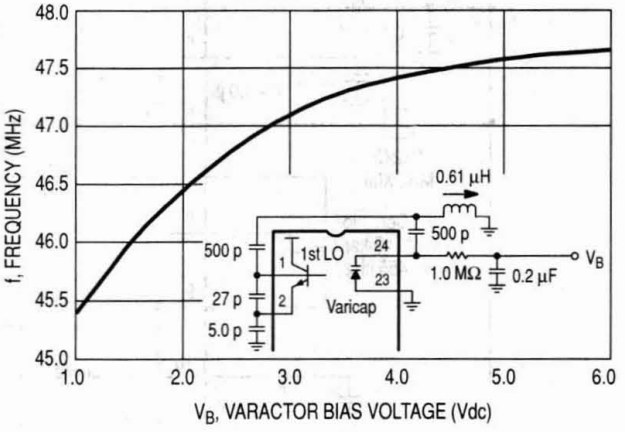


Figure 6. Signal Levels versus RF Input

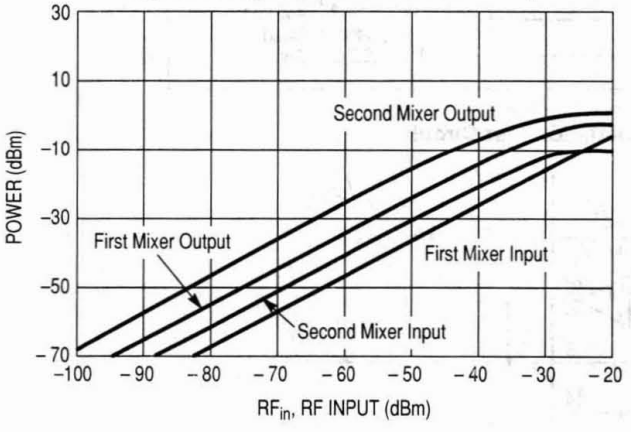


Figure 7. Signal + Noise, Noise, and AM Rejection versus Input Power

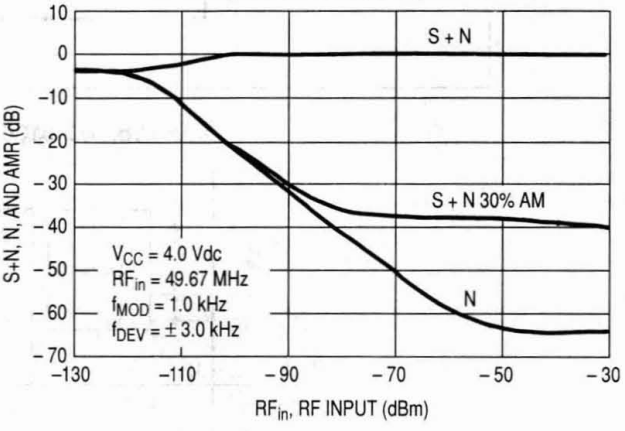


Figure 8. Op Amp Gain and Phase versus Frequency

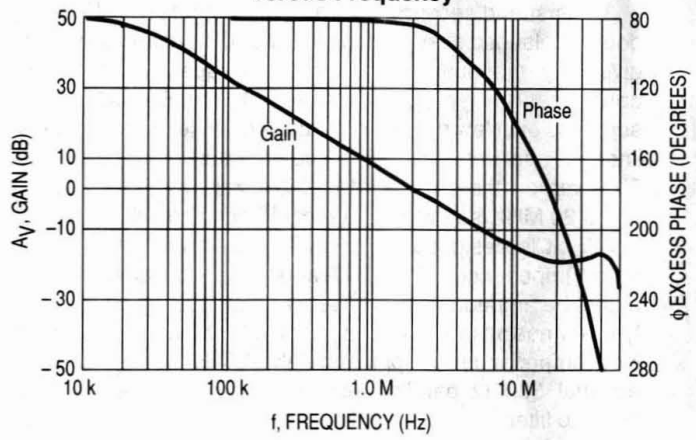


Figure 9. First Mixer Third Order Intermodulation (Unmatched Input)

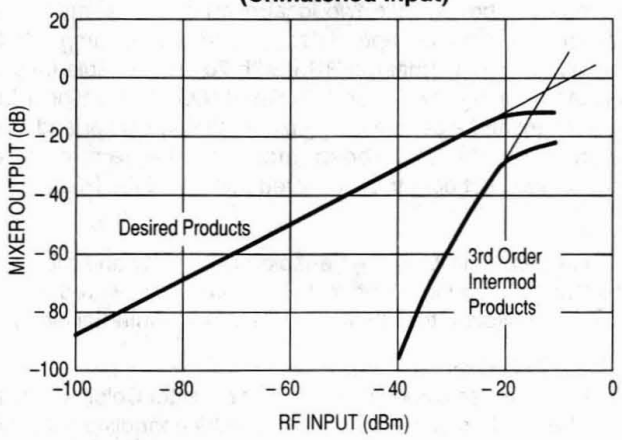


Figure 10. Recovered Audio versus Deviation for MC13135

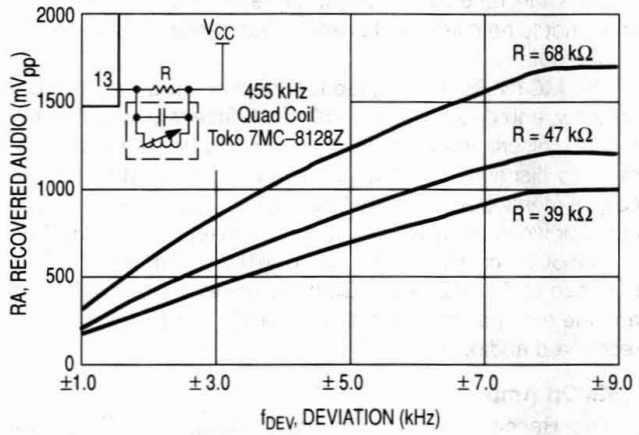


Figure 11. Distortion versus Deviation for MC13135

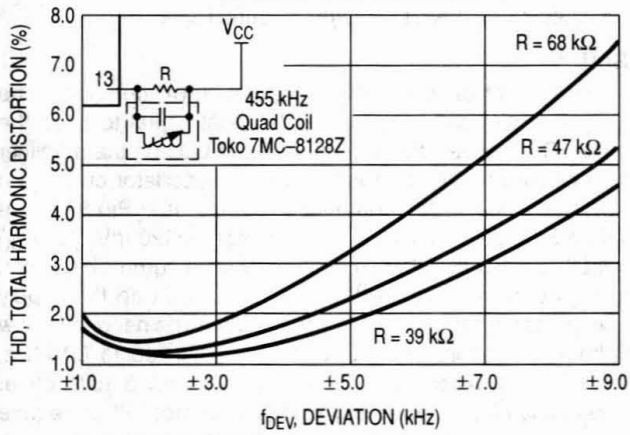


Figure 12. Recovered Audio versus Deviation for MC13136

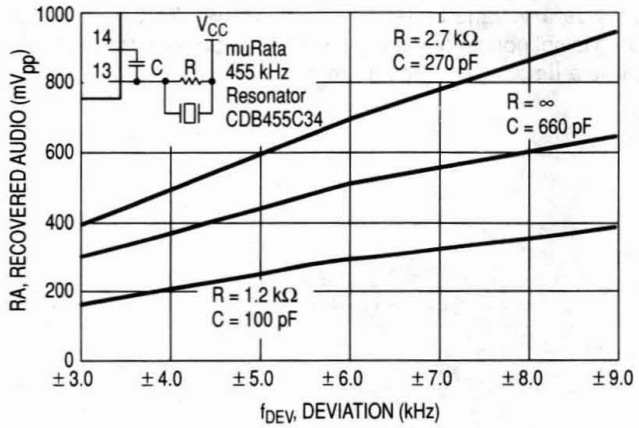
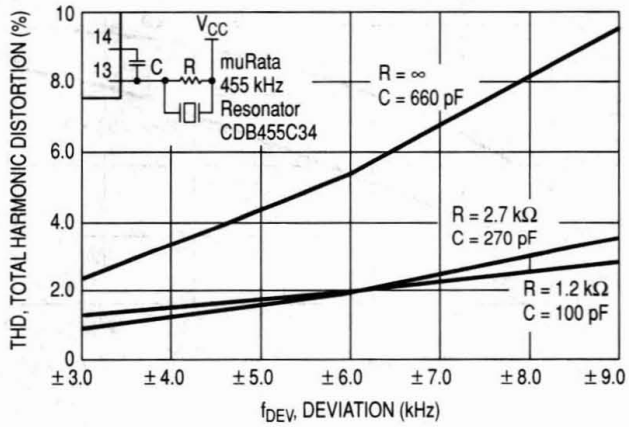


Figure 13. Distortion versus Deviation for MC13136



CIRCUIT DESCRIPTION

The MC13135/13136 are complete dual conversion receivers. They include two local oscillators, two mixers, a limiting IF amplifier and detector, and an op amp. Both provide a voltage buffered RSSI with 70 dB of usable range, isolated tuning diode and buffered LO output for PLL operation, and a separate V_{CC} pin for the first mixer and LO. Improvements have been made in the temperature performance of both the recovered audio and the RSSI.

V_{CC}

Two separate V_{CC} lines enable the first LO and mixer to continue running while the rest of the circuit is powered down. They also isolate the RF from the rest of the internal circuit.

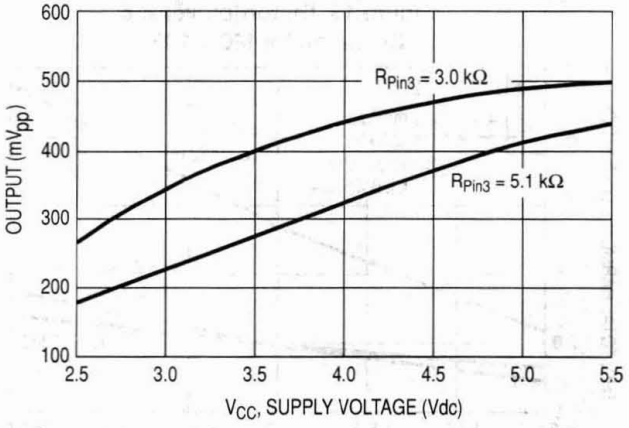
Local Oscillators

The local oscillators are grounded collector Colpitts, which can be easily crystal–controlled or VCO controlled with the on–board varactor and external PLL. The first LO transistor is internally biased, but the emitter is pinned–out and I_Q can be increased for high frequency or VCO operation. The collector is not pinned out, so for crystal operation, the LO is generally limited to 3rd overtone crystal frequencies; typically around 60 MHz. For higher frequency operation, the LO can be provided externally as shown in Figure 16.

Buffer

An amplifier on the 1st LO output converts the single–ended LO output to a differential signal to drive the mixer. Capacitive coupling between the LO and the amplifier minimizes the effects of the change in oscillator current on the mixer. Buffered LO output is pinned–out at Pin 3 for use with a PLL, with a typical output voltage of 320 mV_{pp} at V_{CC} = 4.0 V and with a 5.1 k resistor from Pin 3 to ground. As seen in Figure 14, the buffered LO output varies with the supply voltage and a smaller external resistor may be needed for low voltage operation. The LO buffer operates up to 60 MHz, typically. Above 60 MHz, the output at Pin 3 rolls off at approximately 6.0 dB per octave. Since most PLLs require about 200 mV_{pp} drive, an external amplifier may be required.

Figure 14. Buffered LO Output Voltage versus Supply Voltage



Mixers

The first and second mixer are of similar design. Both are double balanced to suppress the LO and input frequencies to give only the sum and difference frequencies out. This configuration typically provides 40 to 60 dB of LO suppression. New design techniques provide improved mixer linearity and third order intercept without increased noise. The gain on the output of the 1st mixer starts to roll off at about 20 MHz, so this receiver could be used with a 21 MHz first IF. It is designed for use with a ceramic filter, with an output impedance of 330 Ω. A series resistor can be used to raise the impedance for use with a crystal filter, which typically has an input impedance of 4.0 kΩ. The second mixer input impedance is approximately 4.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard ceramic filter.

Limiting IF Amplifier and Detector

The limiter has approximately 110 dB of gain, which starts rolling off at 2.0 MHz. Although not designed for wideband operation, the bandwidth of the audio frequency amplifier has been widened to 50 kHz, which gives less phase shift and enables the receiver to run at higher data rates. However, care should be taken not to exceed the bandwidth allowed by local regulations.

The MC13135 is designed for use with an LC quadrature detector, and does not have sufficient drive to be used with a ceramic discriminator. The MC13136 was designed to use a ceramic discriminator, but can also be run with an LC quad coil, as mentioned in the Test Circuit Information section. The data shown in Figures 12 and 13 was taken using a muRata CDB455C34 ceramic discriminator which has been specially matched to the MC13136. Both the choice of discriminators and the external matching circuit will affect the distortion and recovered audio.

RSSI/Op Amp

The Received Signal Strength Indicator (RSSI) on the MC13135/13136 has about 70 dB of range. The resistor needed to translate the RSSI current to a voltage output has been included on the internal circuit, which gives it a tighter tolerance. A temperature compensated reference current also improves the RSSI accuracy over temperature. On the MC13136, the op amp on board is connected to the output to provide a voltage buffered RSSI. On the MC13135, the op amp is not connected internally and can be used for the RSSI or as a data slicer (see Figure 17c).

Figure 15. PLL Controlled Narrowband FM Receiver at 46/49 MHz

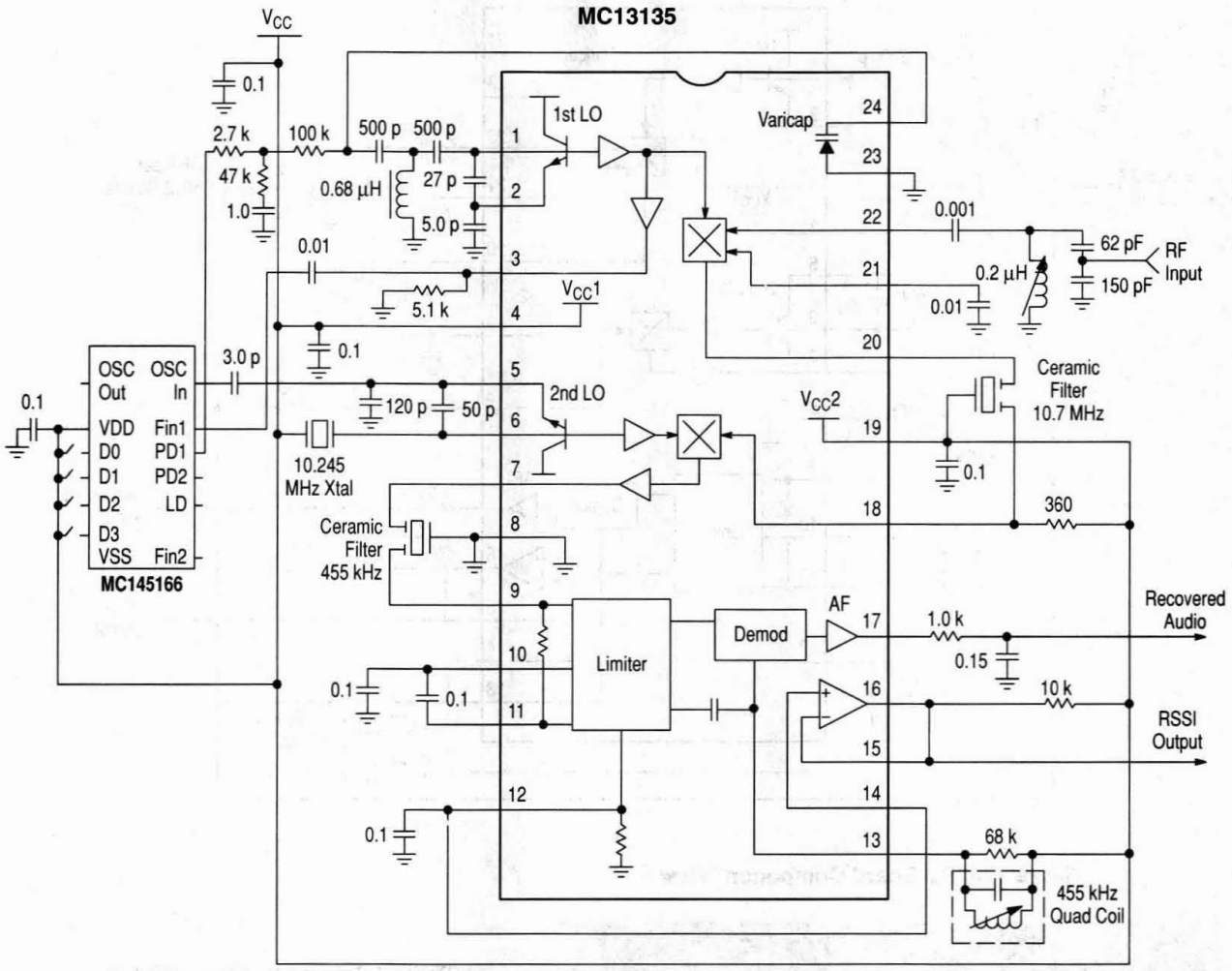
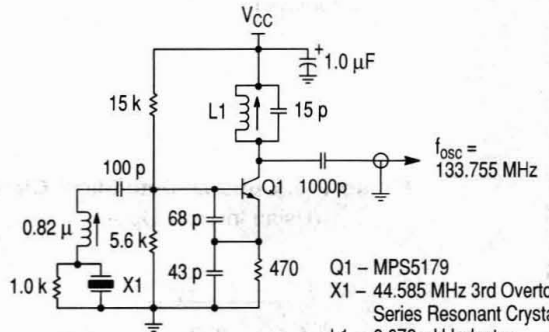


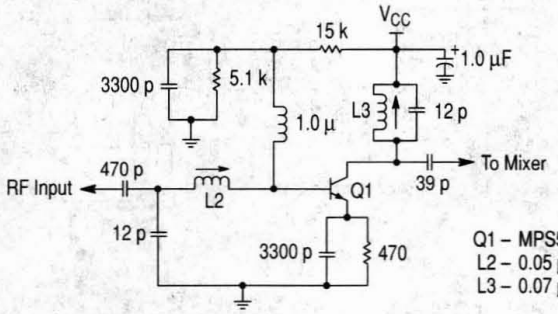
Figure 16. 144 MHz Single Channel Application Circuit

1st LO External Oscillator Circuit



Q1 – MPS5179
X1 – 44.585 MHz 3rd Overtone Series Resonant Crystal
L1 – 0.078 µH Inductor (Coilcraft Part # 146–02J08)

Preamp for MC13135 at 144.455 MHz



Q1 – MPS5179
L2 – 0.05 µH
L3 – 0.07 µH

Figure 17a. Single Channel Narrowband FM Receiver at 49.7 MHz

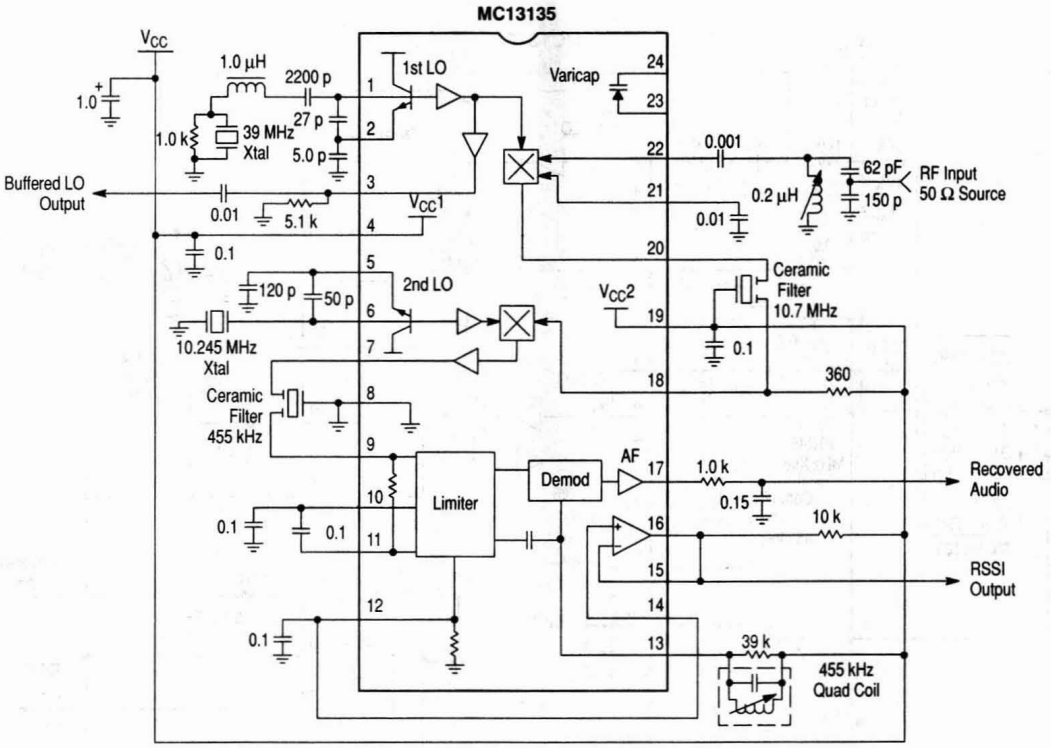
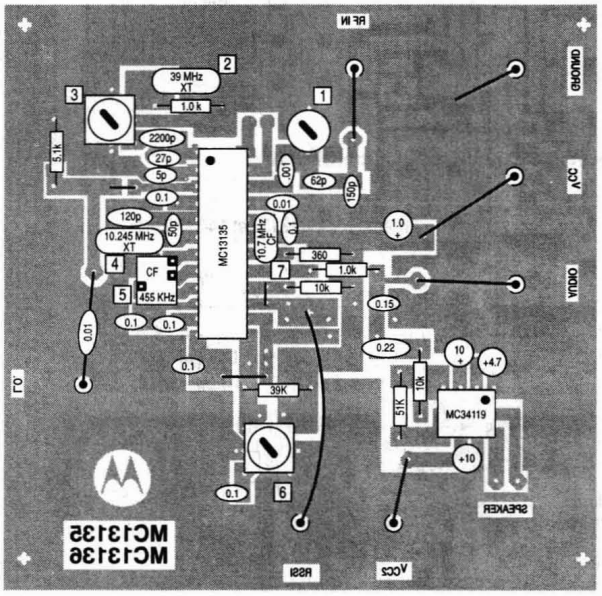


Figure 17b. PC Board Component View



NOTES: 1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Quadrature coil, Toko 7MC–8128Z (7mm) or Toko RMC–2A6597HM (10mm)
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 17c. Optional Data Slicer Circuit
(Using Internal Op Amp)

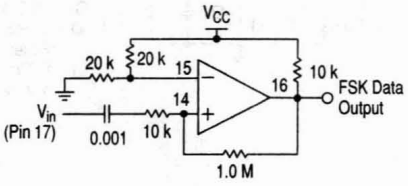
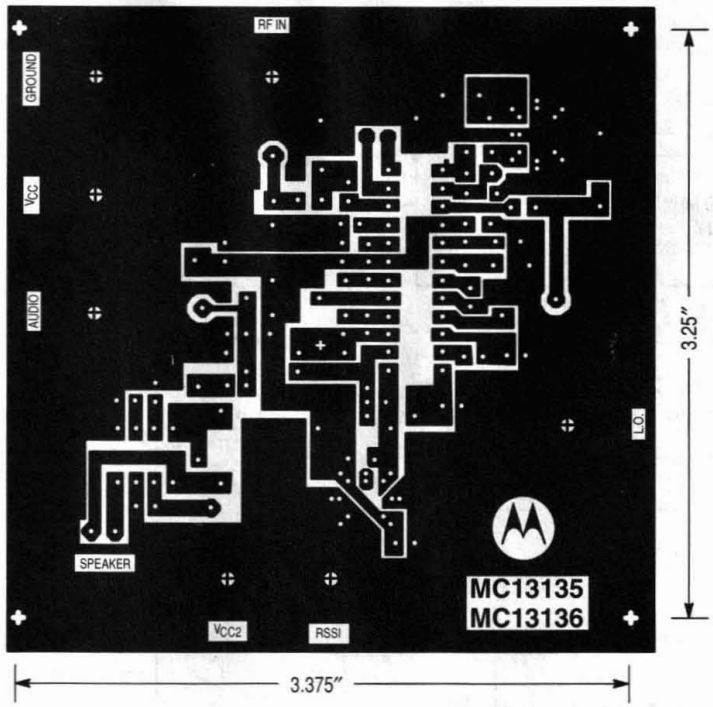
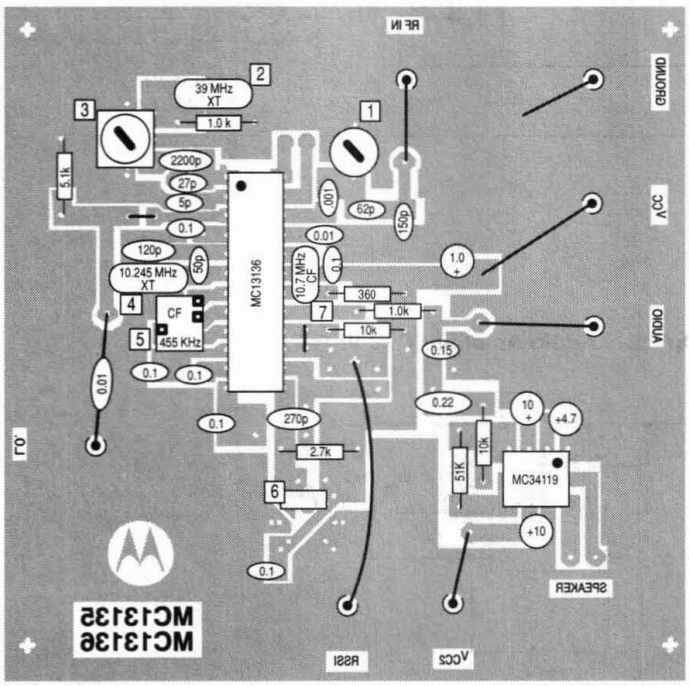


Figure 18. PC Board Solder Side View



(Circuit Side View)

Figure 19. PC Board Component View



NOTES: 1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Ceramic discriminator, muRata CDB455C34 or equivalent
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 20a. Single Channel Narrowband FM Receiver at 49.7 MHz

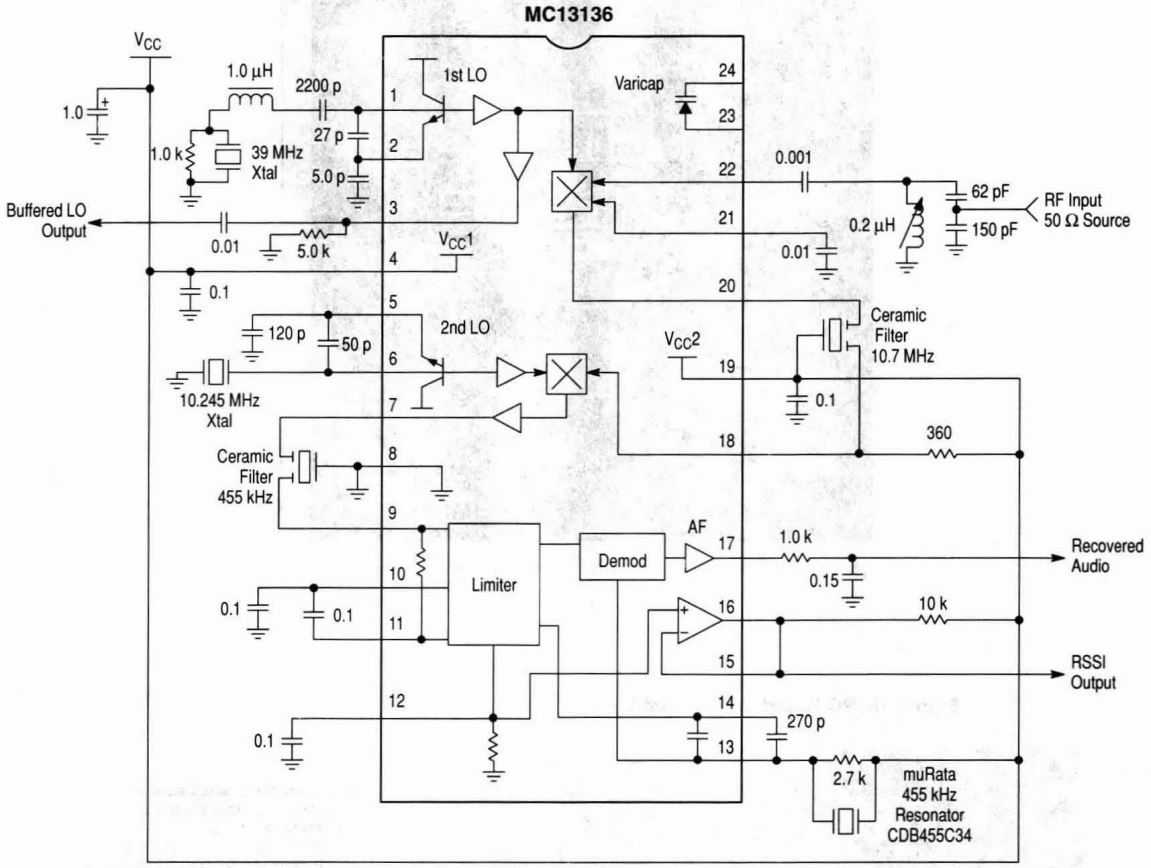


Figure 20b. Optional Audio Amplifier Circuit

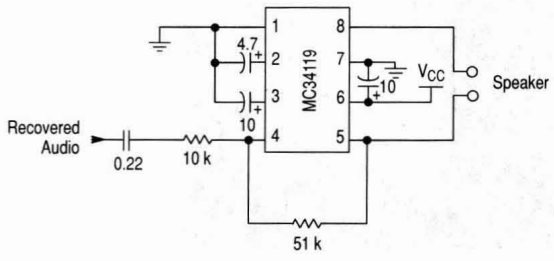
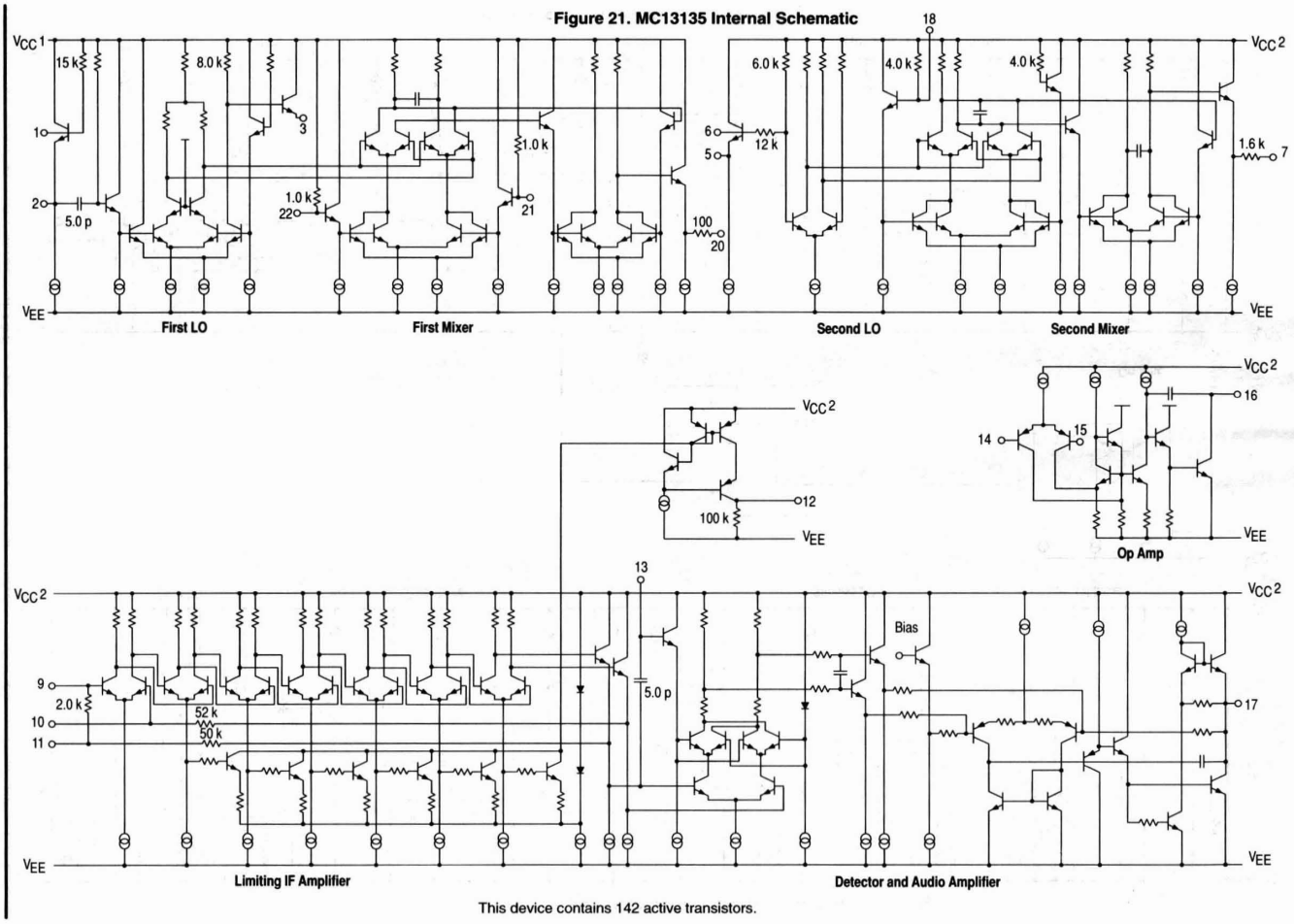
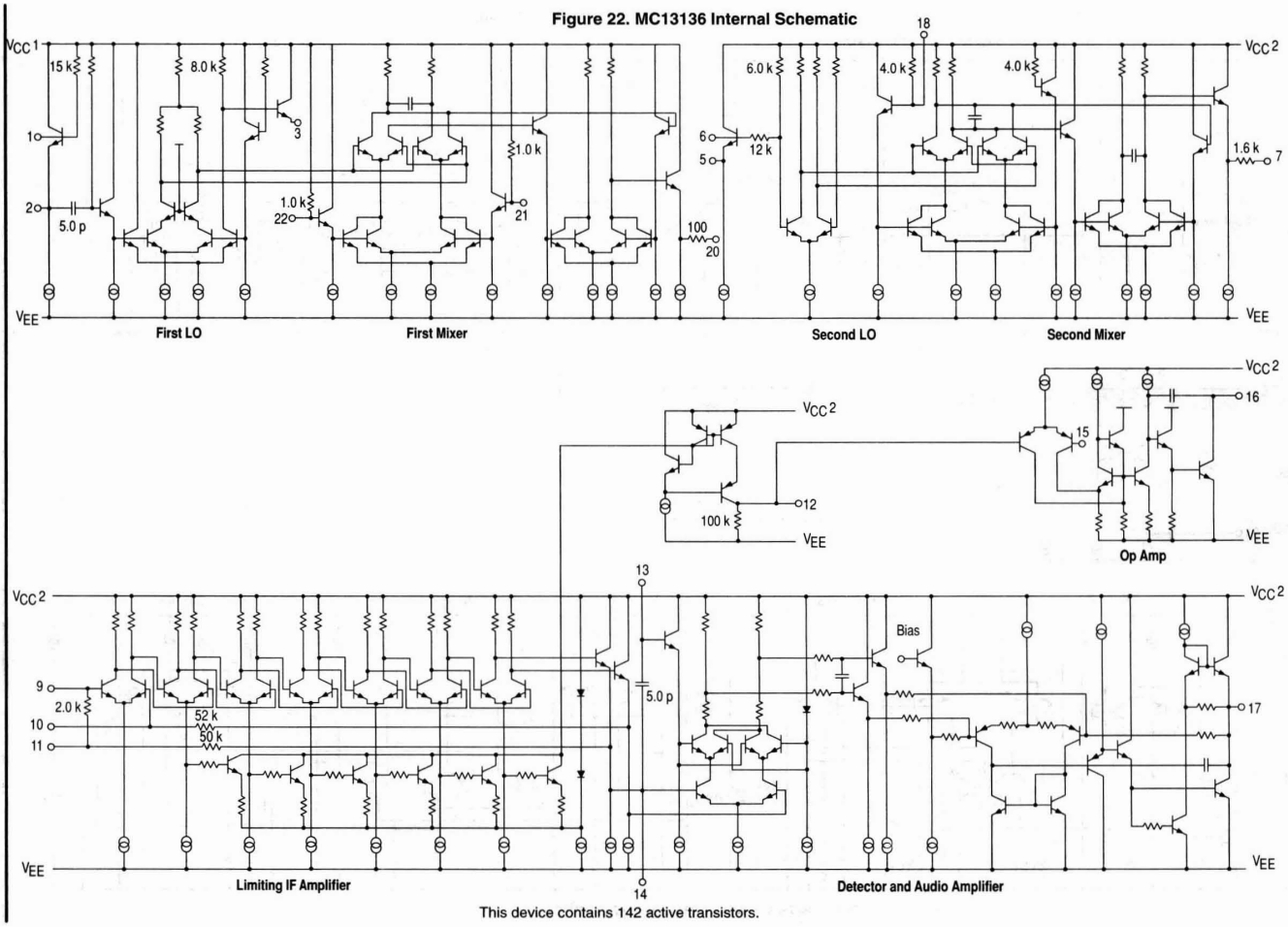


Figure 21. MC13135 Internal Schematic



This device contains 142 active transistors.

Figure 22. MC13136 Internal Schematic



This device contains 142 active transistors.

MOTOROLA

MC13142

Advance Information

Low Power DC - 1.8 GHz LNA, Mixer and VCO

LOW POWER DC – 1.8 GHz LNA, MIXER and VCO

SEMICONDUCTOR TECHNICAL DATA

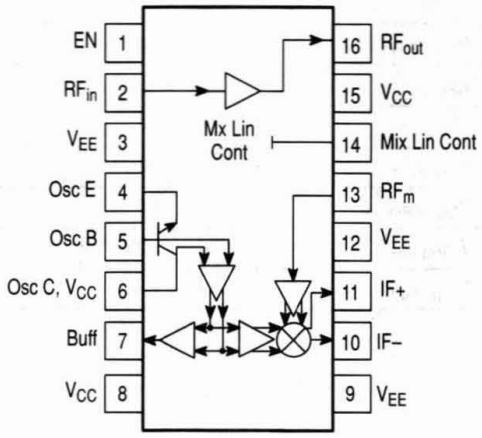
The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7 – 6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm
- Linearity Adjustment Increases IP_{3in} Up to 20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS

SO–16



This device contains 176 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13142D	T_A = –40° to +85°C	SO–16

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range	V_{CC}	2.7 to 6.5	Vdc

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Disable) Pin 15 with Pin 1 @ 0 V Pin 10 and 11 with Pin 1 @ 0 V Pin 6 with Pin 1 @ 0 V	I_{CC_Total} I_{CC_15} I_{CC_Mix} I_{CC_6}	–230 –110 –20 –100	– – – –	230 110 20 100	µA
Supply Current (Enable) Pin 15 with Pin 1 @ 3.0 V Pin 10 with Pin 1 @ 3.0 V Pin 6 with Pin 1 @ 3.0 V	I_{CC_Total} I_{CC_15} I_{CC_Mix} I_{CC_6}	8.25 1.0 1.25 6.0	13.5 – – –	26 4.5 7.5 14	mA
Amplifier Gain (50 Ω Insertion Gain)	S_{21}	6.5	12	13	dB
Amplifier Reverse Isolation	S_{12}	–	–33	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{-1.0\ dB}$	–18	–15	–8.0	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	–5.0	–	dBm
Amplifier Noise Figure (Application Circuit)	NF	1.0	1.8	4.0	dB
Amplifier Gain @ N.F.	G_{NF}	–	17	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–7.0	–3.0	–2.0	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{-1.0\ dBM}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{InM}$	–	–1.0	–	dBm
Oscillator Buffer Drive (50 Ω)	P_{VCO}	–19.5	–16	–12	dBm
Oscillator Phase Noise @ 25 kHz Offset	N_Φ	–	–90	–	dBc/Hz
RF_{in} Feedthrough to RF_m	$P_{RFin–RFm}$	–	–35	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	–35	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	–35	–	dBm
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	–35	–	dBm
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	–35	–	dBm
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	–25	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	–25	–	dB

CIRCUIT DESCRIPTION

General

The MC13142 is a low power LNA, double–balanced Mixer, and VCO. This device is designated for use as the frontend section in analog and digital FM systems such as Digital European Cordless Telephone (DECT), PHS, PCS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter. Further details are covered in the Pin by Pin Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators are controlled by the enable function in which "high" powers up the IC.

Low Noise Amplifier (LNA)

The LNA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal noise figure and gain. The LNA output is biased internally with a 600 Ω resistor to V_{CC}. Input and output matching may be achieved at various frequencies using few external components. Matching the LNA for Maximum stable gain (MSG) yields noise performance within a few tenths of a dB of the minimum noise figure.

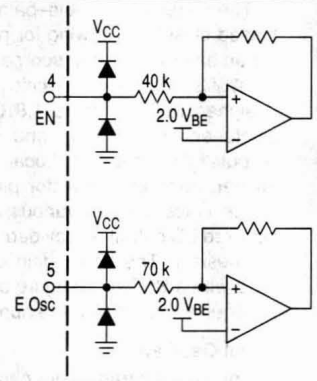
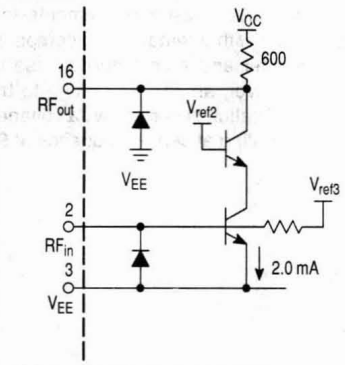
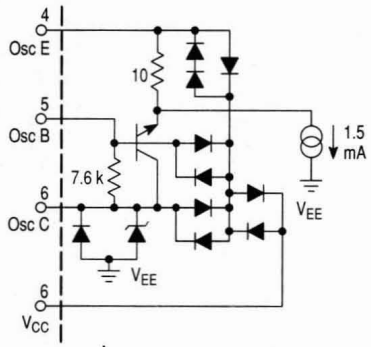
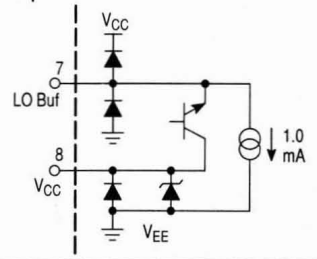
Mixer

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 1.8 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs. An on–board Local Oscillator transistor has the emitter, base and collector pinned out to implement a low phase noise VCO in various configurations. Additionally, a buffered LO output is provided for operation with a frequency synthesizer. The linear gain of the mixer is approximately 0 dB with a SSB noise figure of 12 dB in the IF output circuit configuration shown in the application example.

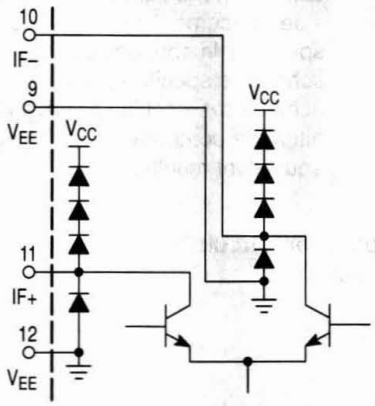
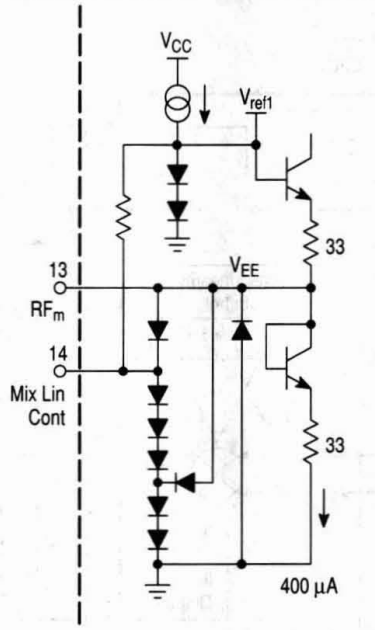
Local Oscillator

The on–chip transistor operates with coaxial transmission line or LC resonant elements to over 2.0 GHz. Biasing is done with a temperature compensated current source in the emitter and a collector to base internal resistor of 7.6 kΩ; however, an RFC from V_{CC} to base is recommended. The application circuit shows a voltage controlled Clapp oscillator operating at center frequency of 975 MHz.

PIN FUNCTION DESCRIPTION j

Pin 16 Pin SOIC	Symbol	Equivalent Internal Circuit (20 Pin LQFP)	Description
1	EN E Osc		**Enable, E Osc** In SO–16, both enables, (for the Oscillator/LO Buffer and LNA/Mixer) are bonded to Pin 1. In the LQFP, two pins are provided, Pin 5, E Osc enables the oscillator and buffer while Pin 4, EN enables the LNA/Mixer. Enable by pulling up to V_{CC} or to greater than 2.0 V_{BE}.
2	RF_{in}		**RF Input** The input is the base of an NPN low noise amplifier. Minimum external matching is required to optimize the input return loss and gain.
3	V_{EE}		**V_{EE} – Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
16	RF_{out}		**RF Output** The output is from the collector of the LNA; it is internally biased with a 600 Ω resistor to V_{CC}. As shown in the 926 MHz application receiver the output is conjugately matched with a shunt L, and series L and C network.
4 5 6	Osc E Osc B Osc C		**On–Board VCO Transistor** The transistor has the emitter, base and collector + V_{CC} pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to V_{CC} through an RFC chosen for the particular oscillator center frequency. The application circuit shows a modified Colpitts or Clapp oscillator configuration and its design is discussed in detail in the application section.
6 8	V_{CC} V_{CC}		**Supply Voltage (V_{CC})** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin as shown in the component placement view.
7	LO Buff		**Local Oscillator Buffer** This is a buffered output providing –16 dBm (50 Ω termination) to drive the f_{in} pin of a PLL synthesizer. Impedance matching to the synthesizer may be necessary to deliver the optimal signal and to improve the phase noise performance of the VCO.

PIN FUNCTION DESCRIPTION (continued)

Pin 16 Pin SOIC	Symbol	Equivalent Internal Circuit (20 Pin LQFP)	Description
9, 12	V_{EE}		**V_{EE}, Negative Supply** These pins are V_{EE} supply for the mixer IF output. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
10, 11	IF–, IF+		**IF Output** The IF is a differential open collector configuration which designed to use over a wide frequency range for up conversion as well as down conversion. Differential to single–ended circuit configuration and matching options are discussed in the application section. 6.0 dB of additional Mixer gain can be achieved by conjugately matching at the desired IF frequency.
13	RF_m		**Mixer RF Input** The mixer input impedance is broadband 50 Ω for applications up to 1.8 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.
14	Mix Lin Cont		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).

APPLICATIONS INFORMATION

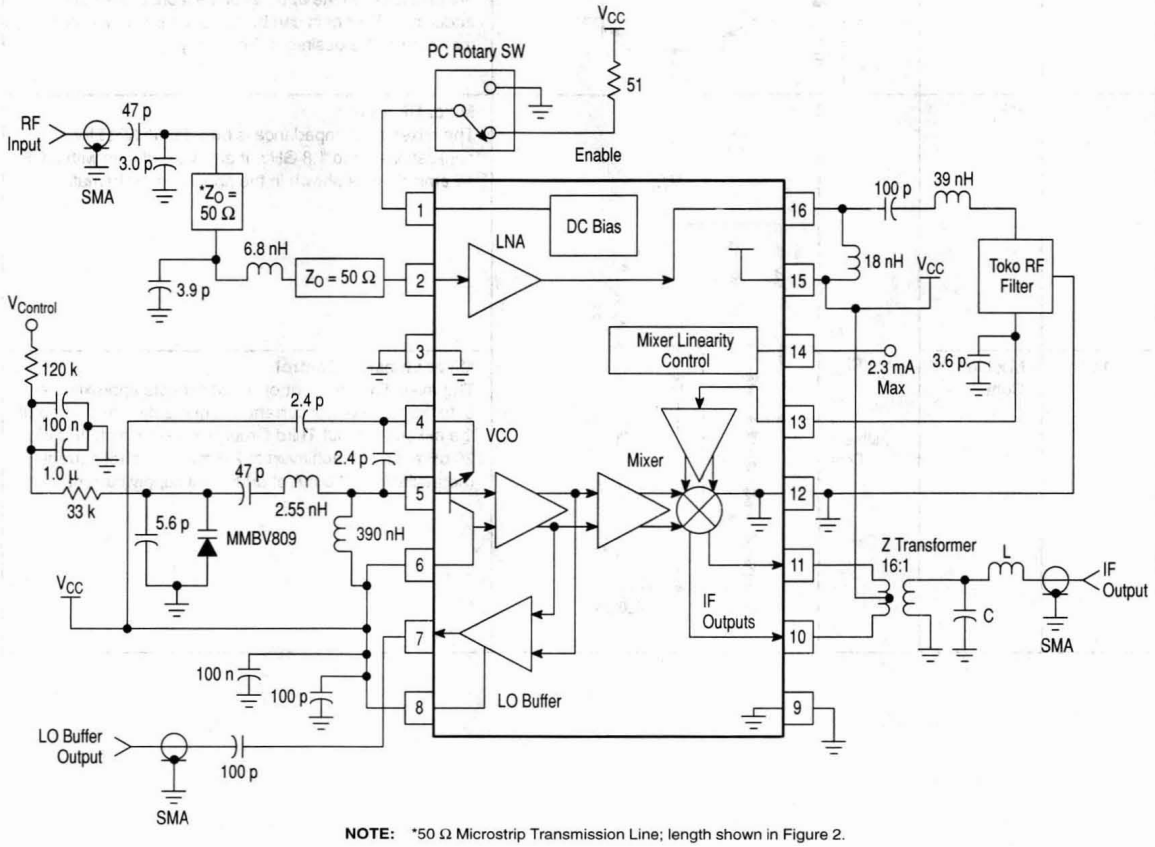
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board accommodates all SMT components on the circuit side (see Circuit Side Component Placement View). This evaluation board will be discussed and referenced in this section.

Component Selection

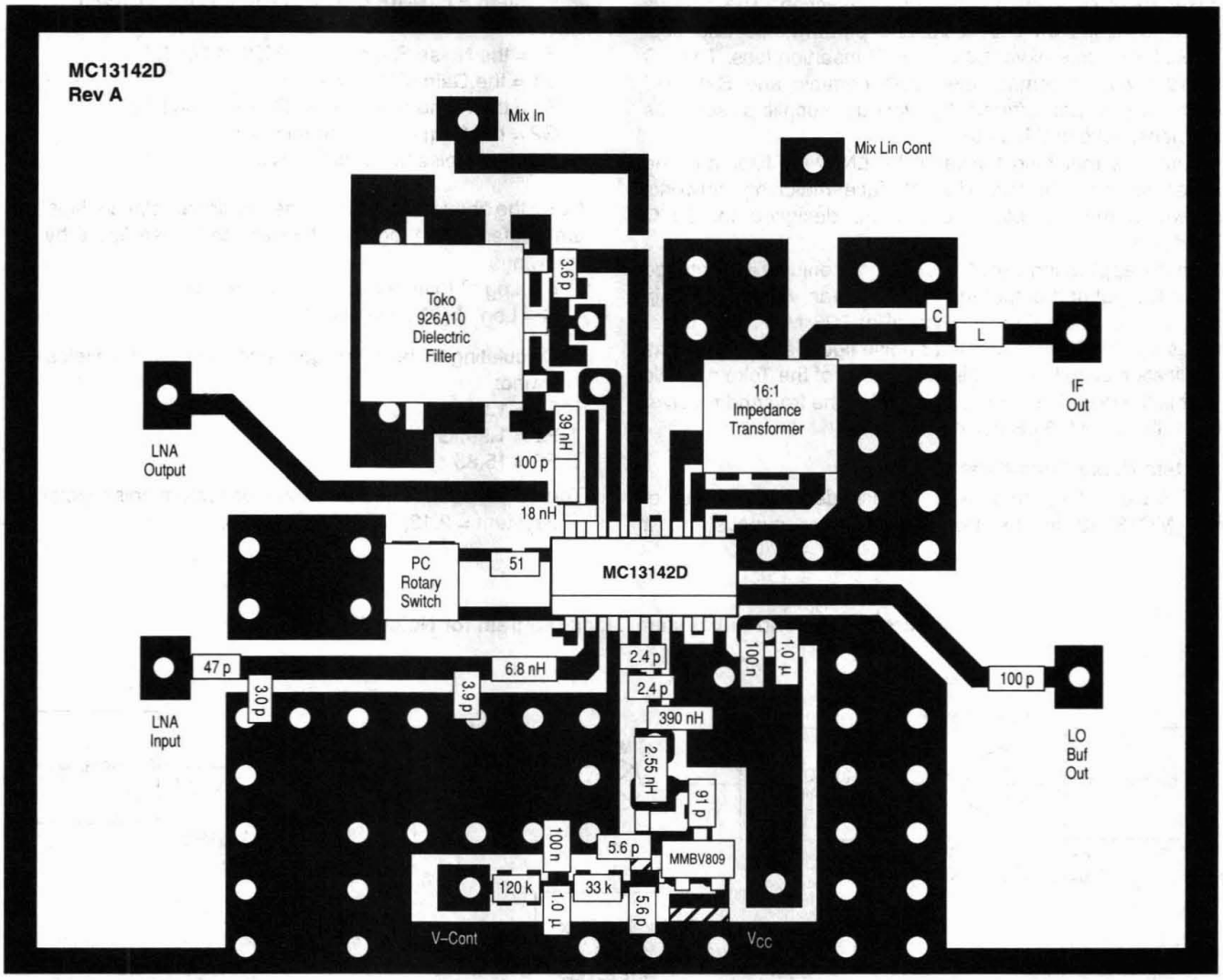
The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The application circuit schematic specifies particular components that were used to achieve the results given and specified in the tables but alternate components of the same Q and value should give equivalent results.

Figure 1. Application Circuit
(926.5 MHz)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 2.

Figure 2. 900 MHz Circuit Side Component Placement View



NOTES: The PCB is laidout for the 4DFA (2 pole SMD type) and 4DFB (3 pole SMD type) filters which are available for applications in cellular and GSM,GPS (1.2–1.5 GHz), DECT, PHS and PCS (1.8–2.0 GHz) and ISM Bands (902–928 MHz and 2.4–2.5 GHz). In the component placement shown above, the 926.5 MHz dielectric type image filter is used (Toko Part # 4DFA–926A10).

The PCB also accommodates a surface mount SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used for the 926.5 MHz application circuit. Note: some traces must be cut to accommodate placement of components; likewise some traces must be shorted. The voltage controlled oscillator is shown with the varactor referenced to V_{EE} ground. The PCB is modified as shown to do this.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount "TX" package. Components L and C comprise a low pass filter used to provide narrowband matching at a given IF frequency. For example at 49 MHz C = 36 p and L = 330 nH.
The microstrip trace on the ground side of the PCB is intended for a microstrip resonator; it is cut free when using a lump inductor as done above.

Input Matching/Components

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

In the application circuit, the LNA is conjugately matched to 50 Ω input and output for 3.0 to 5.0 Vdc V_{CC}. 17 dB gain and 1.8 dB noise figure is typical at 926 MHz. The mixer measures 0 dB gain and 12 dB noise figure as shown in the application circuit. Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the frontend receiver is 14 dB with a 3.3 dB noise figure.

System Noise Considerations

The block diagram shows the cascaded noise stages of the MC13142 in the frontend receiver subsystem; it represents the application circuit. In the cascaded noise analysis the system noise equation is:

Fsystem = F1 + [(F2 –1)/G1] + [(F3–1)]/[(G1)(G2)]

where:

F1 = the Noise Factor of the MC13142 LNA
G1 = the Gain of the LNA
F2 = the Noise factor of the RF Ceramic Filter
G2 = the Gain of the Ceramic Filter
F3 = the Noise factor of the Mixer

Note: the above terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

F = Log $^{-1}$ [(NF in dB)/10] and similarly
G = Log $^{-1}$ [(Gain in dB)/10].

Calculating in terms of gain and noise factor yields the following:

F1 = 1.51; G1 = 50.11
F2 = 1.99; G2 = 0.5
F3 = 15.85

Thus, substituting in the equation for system noise factor:

Fsystem = 2.12; NFsystem = 3.3 dB

Figure 3. Frontend Subsystem Block Diagram for Noise Analysis

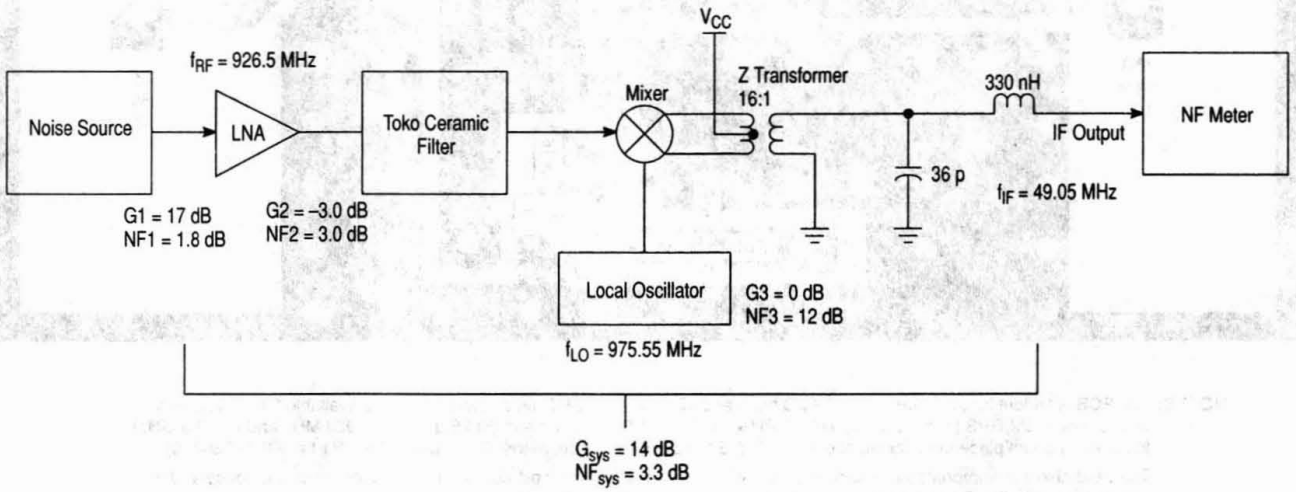
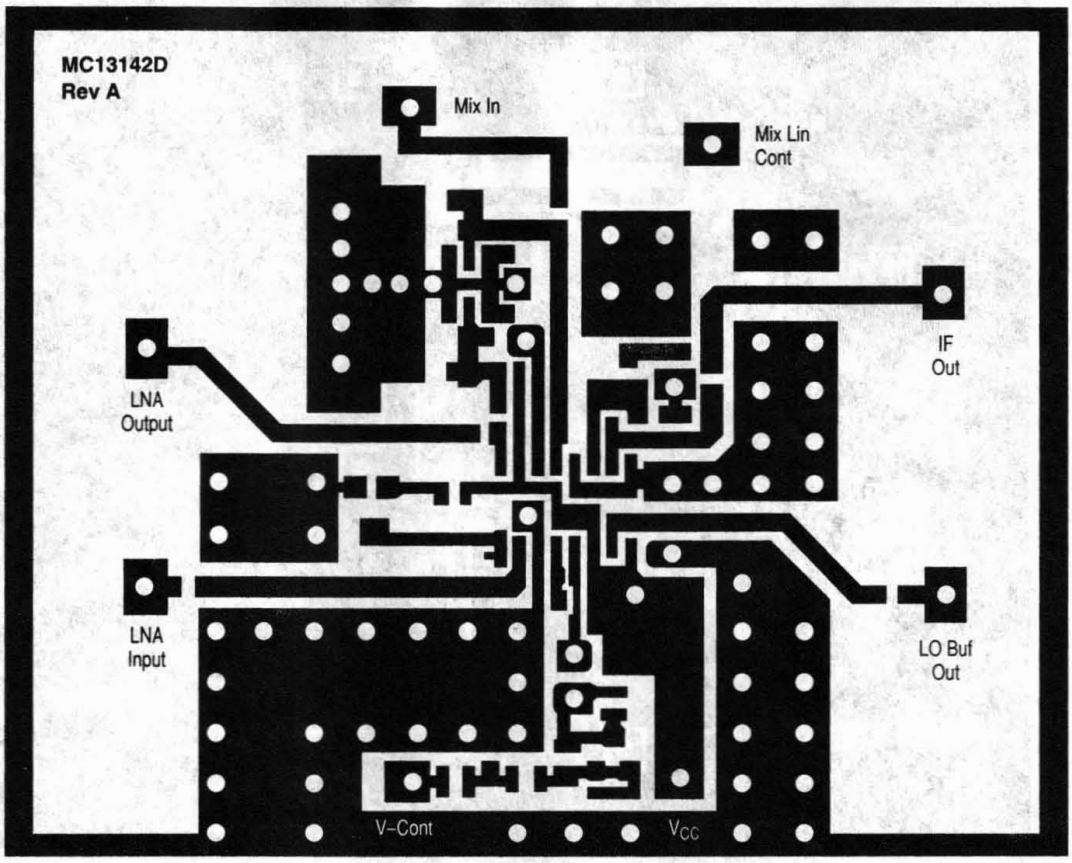
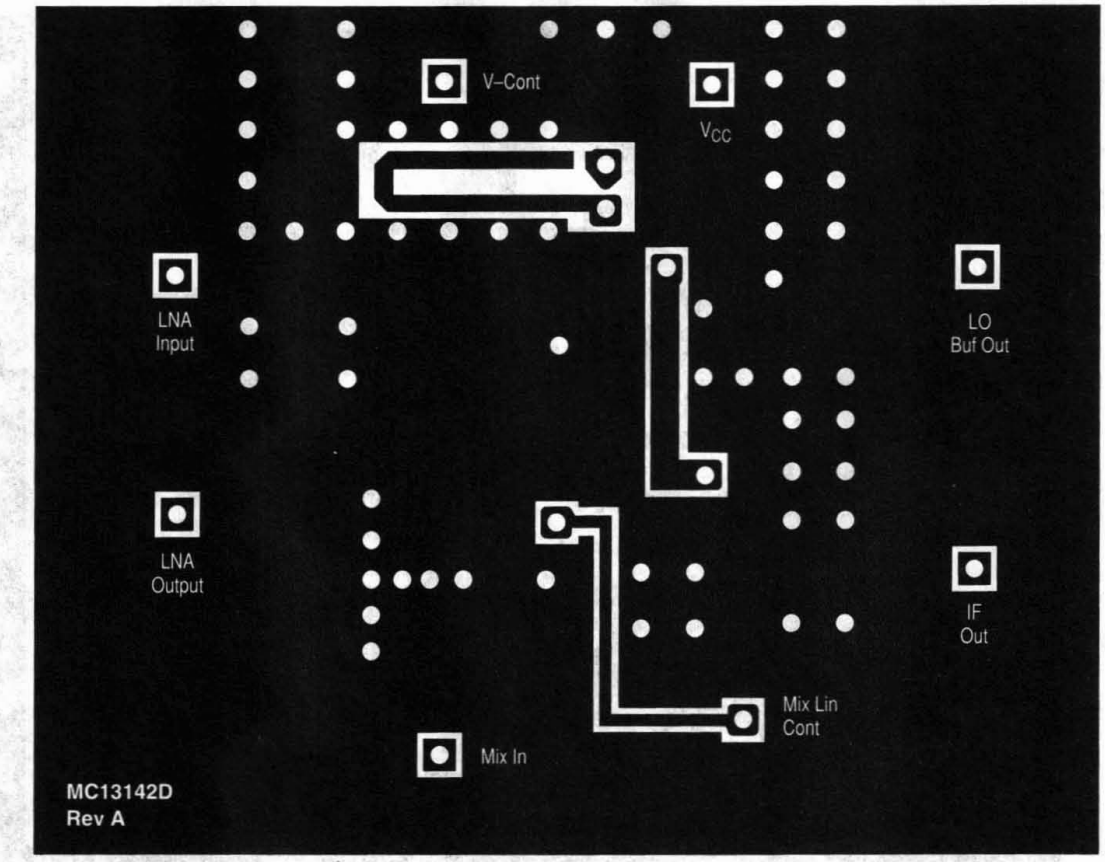


Figure 4. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–16 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 5. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

1.9 GHz FRONT–END FOR WIRELESS SYSTEMS

This application is applicable to both Analog and Digital systems. With the correct VCO tuning and the appropriate filter, it will do the front–end for DECT, PHS or PCS. The MC13142D is available in a SOIC 16 pin package. The part requires minimal external components, leading to a low cost system. A circuit board layout with a circuit diagram to evaluate the IC is shown. Except for the PLL control, all the wireless systems front–ends will look the same and have the same basic performance characteristic as the test circuit.

Circuit Operation:

LNA Input/Output

An LC filter is incorporated before the LNA to provide some selectivity. In addition to selectivity, its other function is to match the antenna impedance (50 Ω) to the LNA input for best gain and sensitivity (low noise figure). The network reflects about a 200 Ω source impedance to the device.

The output circuit is a pie network consisting of; the LNA output capacity, the inductance (the bond wire, package pin and L2), and the input capacity of the dielectric filter, along with some added shunt. A 2.4 pF with Toko 4DFA 2 pole filter. The 2.4 pF is for matching the in–band filter impedance to the LNA output and has little effect on tuning.

Both networks are tuned to band center by adjusting L1 and L2. L1 and L2, as well as L3, are short length of wire formed in a half loop. Once the correct length is determined in centering the tuning range, adjustment is accomplished by moving the loop toward or away from some conductive surface such as a ground plane.

The dielectric filter is referenced to the dc supply which lessen the parts count and adds distributive capacity for high frequency bypassing. DC feed to the LNA is through a low value resistor (220 to 330 Ω) tapped at the filter input, so as not to load the circuit unnecessarily. There is a small voltage drop across the resistor, as well as some signal loss. The signal loss is about 0.73 dB for a 220 Ω resistor and less for larger values. If one can not afford the voltage drop, an inductor could replace the resistor at a somewhat increased cost.

Mixer

Looking from the dielectric filter's output, the Mixer input is 50 Ω in series with an inductor. This inductor consists of the printed circuit run, the package pin and bond wire, all in series. It is modified, to some extent, by the package pin distributive capacity, but overall at the bandpass frequency remains inductive. Matching the filter impedance to the Mixer input only requires a capacitor with a value that, when placed in series, will resonate with this inductor at the filter bandpass frequency.

The single–ended input signal is converted internally into balanced current signals. The two signals drive the two low impedance inputs (emitters) of a Gilbert Cell. They appear as

current sources to the Cell and can be programmed (via Pin 15) for more current. The current is often adjusted for minimum third order response. In this Fixture it is fixed biased for most conversion gain.

The Mixer circuit is balanced where both oscillator and RF are suppressed. This provides IF signals at Pins 9 and 10 which are equal in amplitude and 180 degrees out of phase. To realize a positive gain one needs to reflect a higher impedance from the load impedance (50 Ω for this fixture) to the Mixer output or outputs. Maximum signal transfer would require a balance to unbalance network. Center tapped tuned transformers can perform this function but are quite expensive. If one can afford 3.0 dB less signal, a simple LC circuit at one of the outputs will work well. The other output is unused and bypassed to ground.

The most gain is realized when no shunt capacity is added and L4 is selected to resonate with the terminal capacity. Adding shunt capacity will lower the gain and increase the circuit's bandwidth. A small value series capacitor C4 to the 50 Ω output will control the reflected impedance and complete the circuit. L4 and C4 will vary in value depending on the IF frequency.

VCO

The base of the device is the source for driving both the Gilbert cell and prescaler buffer stages. Because of this, the oscillator device will operate and drive the Mixer only in the grounded collector configuration. Additional dc bias is added through a 1.3 kΩ resistor (tapped for minimum VCO loading) to reduce the off–set between base and supply.

The external circuit is a modified Colpitts where the capacitance between base and emitter (Pins 4 and 5), along with a capacitor from emitter to ac ground, forms the circuit capacity and the feedback that sustains oscillations. The effective circuit inductance (looking from the top of the circuit, the transistor base) consist of L3 in series with varactor diode D1 and a blocking capacitor. This circuit must appear inductive for the VCO to operate properly. If the capacity is too small, the feedback ratio is reduced and the VCO can cease oscillating. When it becomes to large, it will not vary the frequency due to the limiting effect of the series loop capacitance.

In this application, the VCO is not required to cover a large tuning range. Limiting the tuning range to no more than is required to cover the band (making allowance for temperature and aging effects) will result in a VCO less susceptible to on board noise sources. To assure oscillation while controlling the tuning range the varactor (plus series capacitor) minimum capacity is chosen to be about equal to the capacity from Pin 5 (transistor base) to RF ground. The maximum tuning ratio could be no greater than 1.41 because the circuit capacity could only double whatever the upper value capacity the varactor attained. An upper limit on the varactor capacity along with the effects of the series capacitor reduces the VCO tuning range to about 1.2 times. The varactors chosen for the test fixtures were Loral KV2111.

The VCO buffer, as most emitter follower circuits, has the potential of generating a parasitic oscillation. When a collector is RF bypassed, a tuned LC circuit is formed consisting of the bypass capacitor, bond wire plus package pin inductance and the device effective output capacity. If the base is low impedance, there is normally enough distributive collector to emitter capacity for the device to oscillate in the common base mode. A simple fix without affecting the buffer otherwise, is to place a small value series resistor in the collector lead. This will lower the Q of the circuit where it cannot sustain oscillations. Without the series resistor at Pin 8 or some other damping element, the buffer will oscillate.

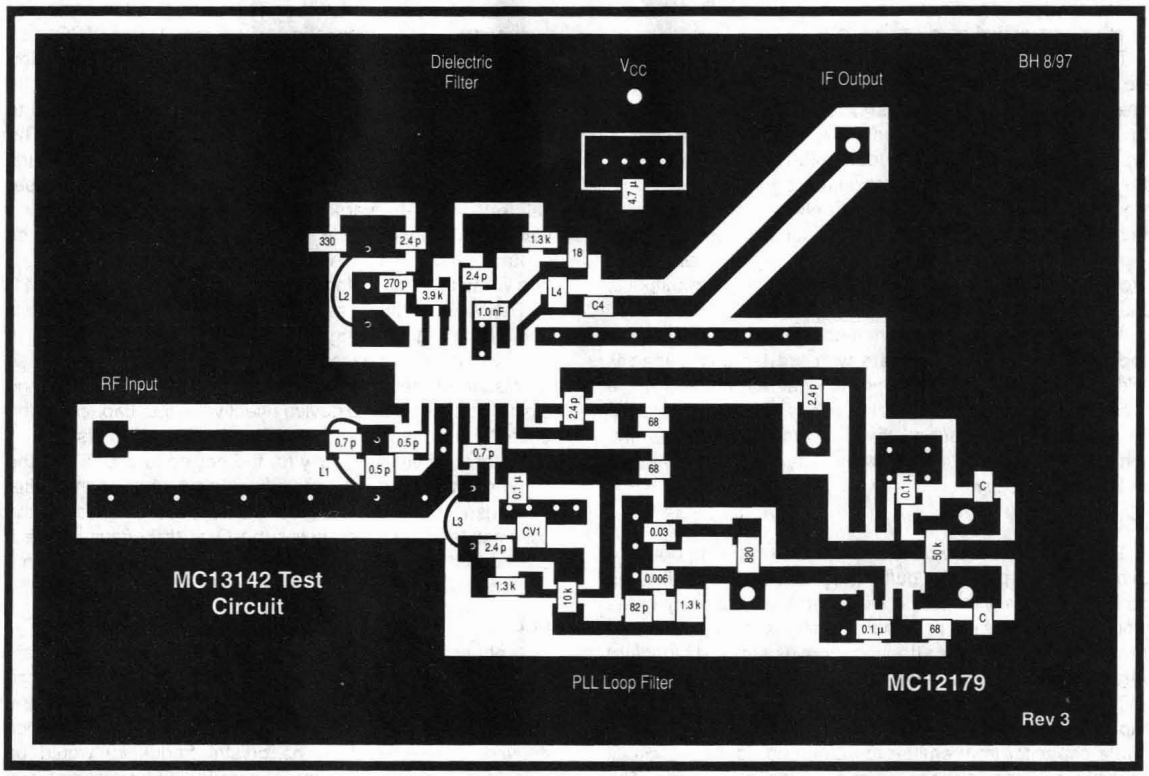
PLL

A phase lock loop is added to the test board to evaluate the VCO. The MC12179 multiplies the crystal reference frequency by 256 to obtain lock. In a frequency agile system, the MC12210 would control the VCO and its reference derived from a crystal. The crystal frequency would be selected to coincide with the required VCO frequencies and channels spacing requirements.

Expected Performance

As stated earlier, the MC13142 performance in any of the systems should mirror the performance obtained in the test fixture. Fixture power gains of 15 dBm and noise figures of 5.5 dB are typical. The Mixer current can be varied to enhances battery life as well as alter its output characteristic for peak performance of a desired or undesired response.

Figure 6. 1.9 GHz Circuit Component Placement View



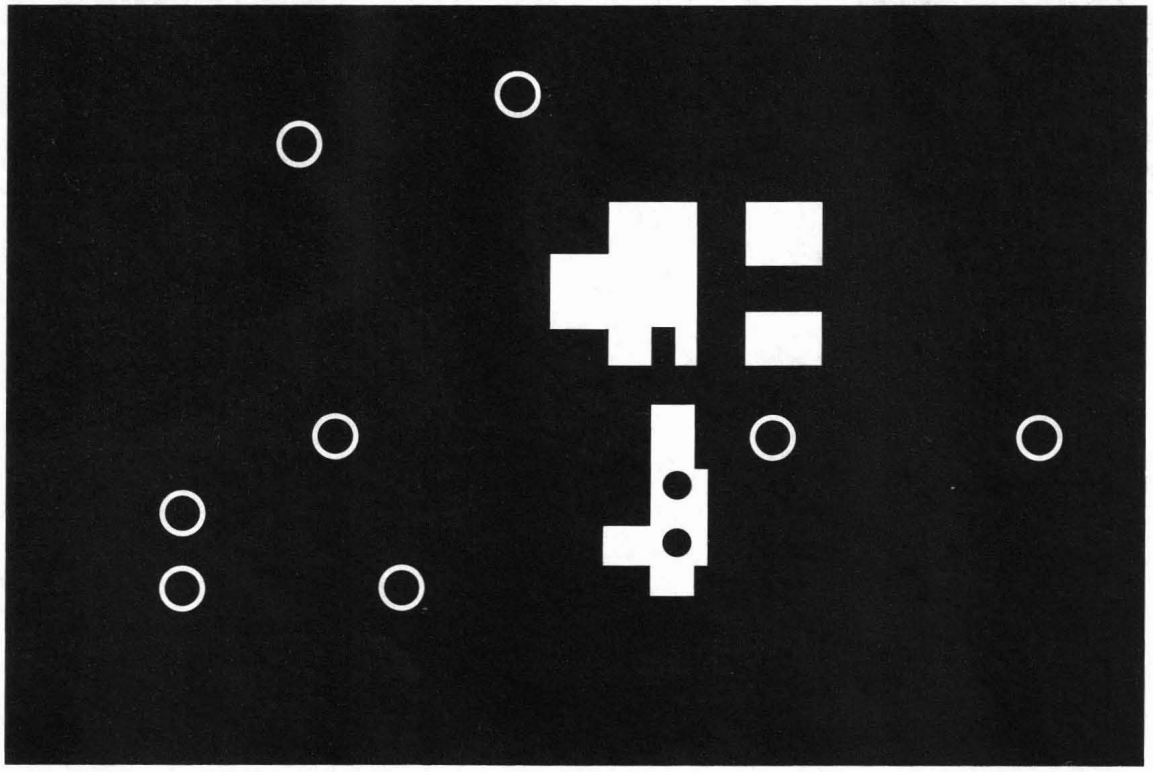
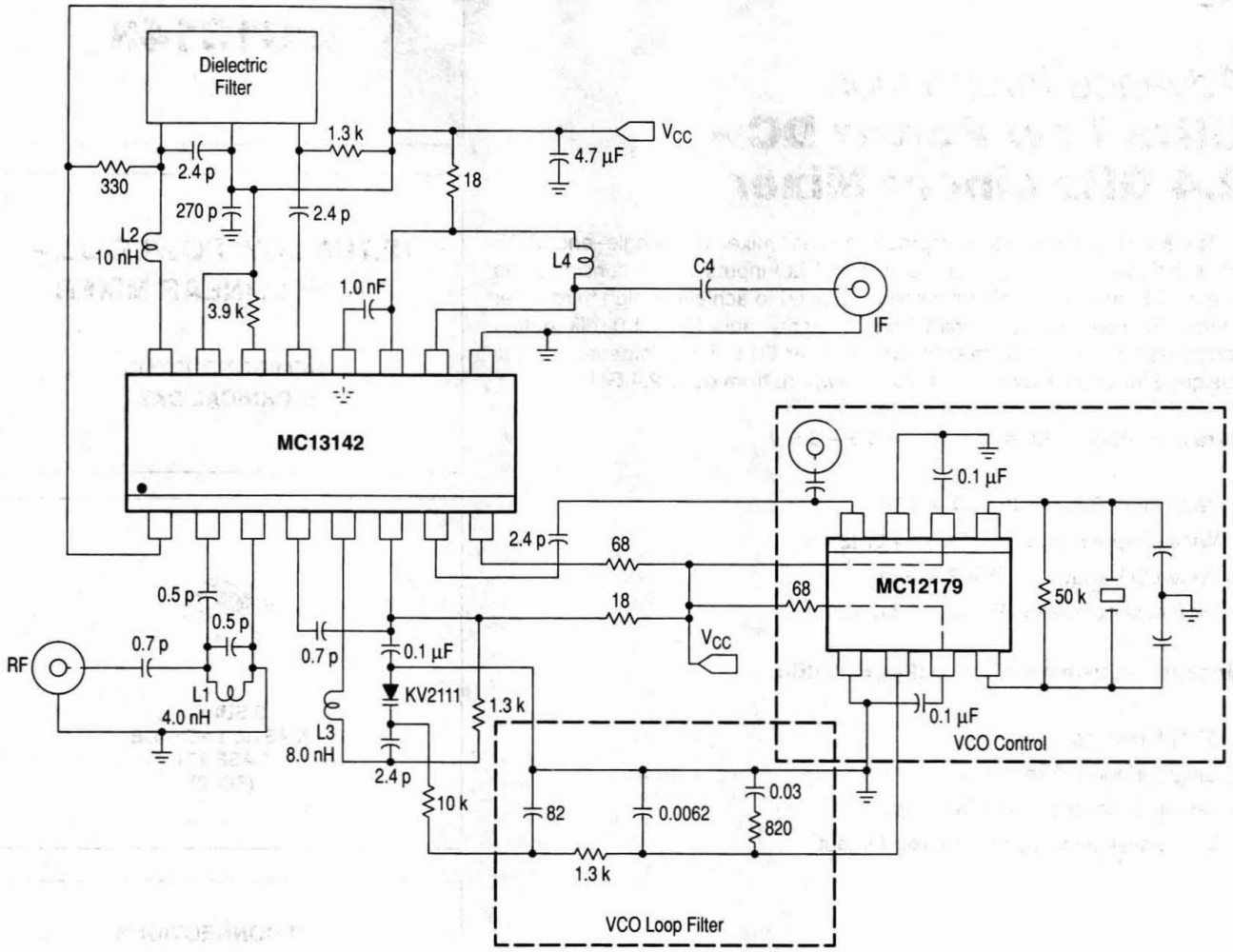


Figure 7. 1.9 GHz Application Circuit



MOTOROLA

MC13143

Advance Information

Ultra Low Power DC - 2.4 GHz Linear Mixer

The MC13143 is a high compression linear mixer with single–ended RF input, differential IF output and differential LO inputs which consumes as little as 1.8 mW. A new circuit topology is used to achieve a high third order intermodulation intercept point, high linearity and high 1.0 dB output compression point while maintaining a linear 50 Ω input impedance. It is designed for Up or Down conversion anywhere from dc to 2.4 GHz.

Ultra Low Power: 1.0 mA @ V_{CC} = 1.8 – 6.5 V

- Wide Input Bandwidth: DC–2.4 GHz
- Wide Output Bandwidth: DC–2.4 GHz
- Wide LO Bandwidth: DC–2.4 GHz
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm

Linearity Adjustment of up to IP_{3in} = 20 dBm

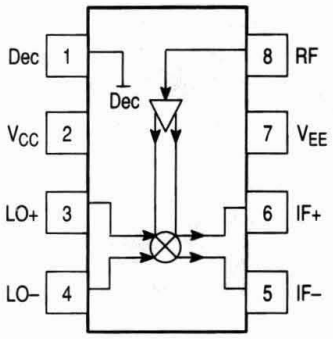
- 50 Ω Mixer Input
- Single–Ended Mixer Input
- Double Balanced Mixer Operation
- Differential Open Collector Mixer Output

ULTRA LOW POWER DC – 2.4 GHz LINEAR MIXER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

This device contains 29 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13143D	T_A = –40° to +85°C	SO–8

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	1.8	–	6.0	Vdc

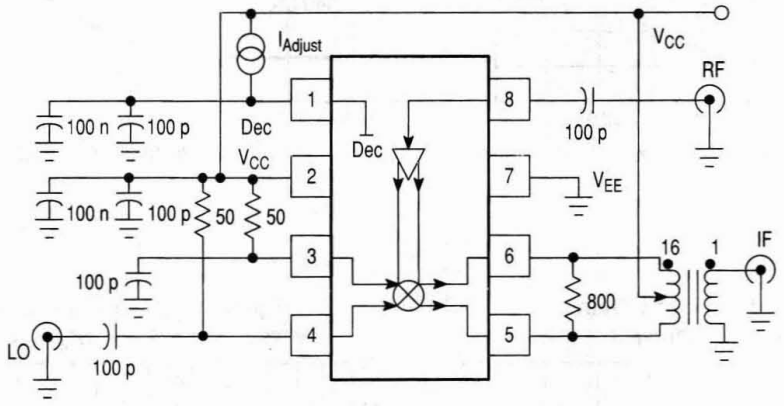
DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, f_{RF} = 1.0 GHz, Pin = –25 dBm.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Lin Control Current = 0)	I_{CC1}	–	1.0	–	mA
Supply Current (Lin Control Current = 1.6 mA)	I_{CC2}	–	4.1	–	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, f_{RF} = 1.0 GHz, Pin = –25 dBm.)

Characteristic	Symbol	Min	Typ	Max	Unit
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–3.5	–2.6	–1.5	dB
Mixer Input Return Loss	Γin_{mx}	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSB}	–	14	15	dB
Mixer 1.0 dB Compression Point (Mx Lin Control Current = 1.6 mA)	$Pin_{-1.0\ dB}$	–1	0	–	dBm
Mixer Input Third Order Intercept Point (d_f = 1.0 MHz, $I_{control}$ = 1.6 mA)	$IP3_{in}$	–	16	–	dBm
LO Drive Level	LO_{in}	–	–5.0	–	dBm
LO Leakage to Mixer IF Outputs	P_{LO-IF}	–	–33	–25	dB
Mixer Input Feedthrough Output	P_{RFm-IF}	–	–25	–	dB
LO Leakage to Mixer Input	P_{LO-RFm}	–	–40	–25	dB
Mixer Input Leakage to LO	P_{RFm-LO}	–	–35	–	dB

Figure 1. Test Circuit



TYPICAL PERFORMANCE CURVES

Figure 2. Power Conversion Gain and Supply Current versus Supply Voltage

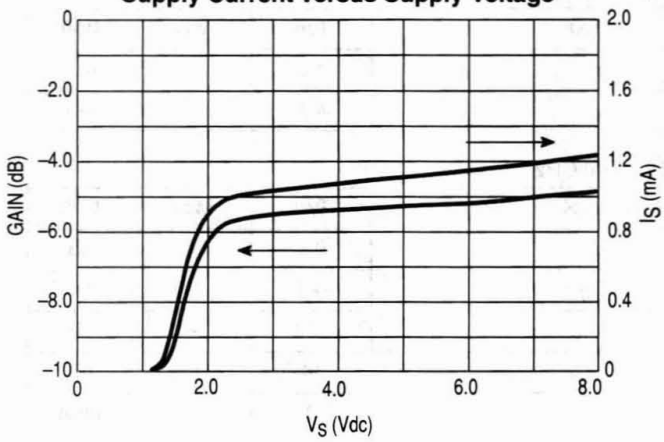


Figure 3. Noise Figure and Gain versus LO Power

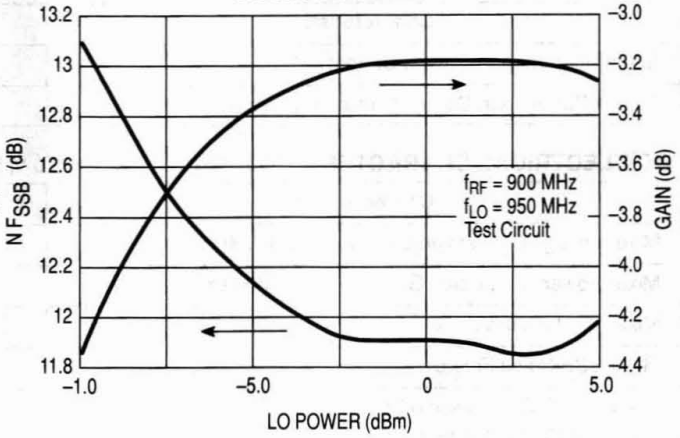


Figure 4. Mixer Input Return Loss versus RF Input Frequency

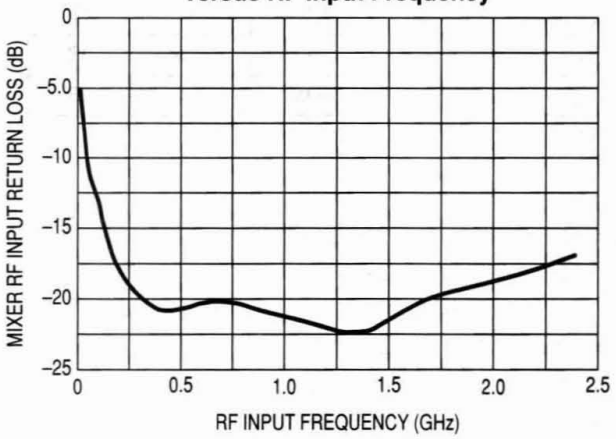


Figure 5. Power Conversion Gain and Supply Current versus RF Input Power

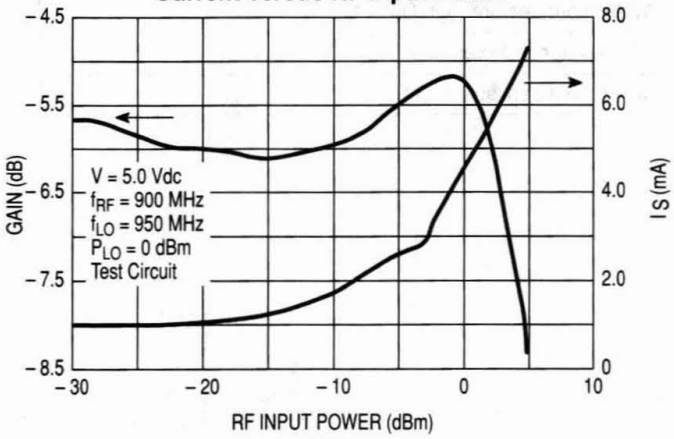


Figure 6. Noise Figure and Gain versus RF Frequency

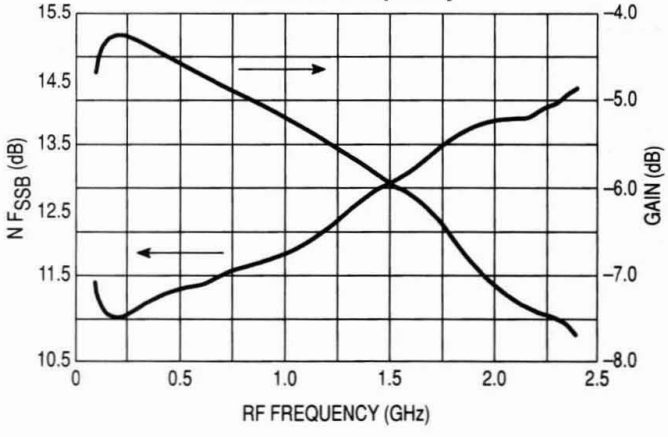
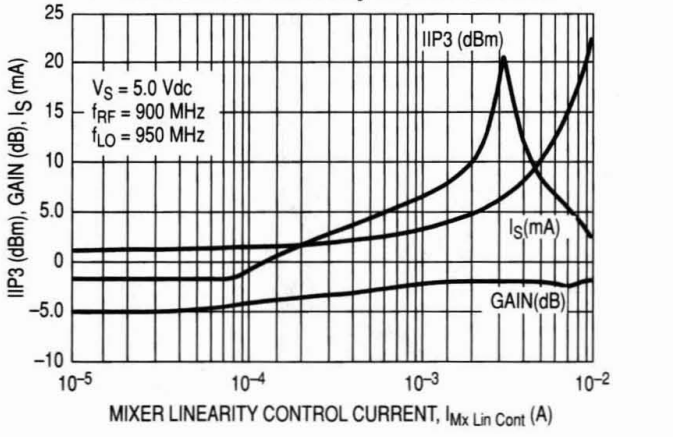


Figure 7. IIP3, Gain, Supply Current versus Mixer Linearity Control Current



CIRCUIT DESCRIPTION

General

The MC13143 is a double–balanced Mixer. This device is designated for use as the frontend section in analog and digital FM systems such as Wireless Local Area Network (LAN), Digital European Cordless Telephone (DECT), PHS, PCS, GPS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter.

Current Regulation

Temperature compensating voltage independent current regulators provide typical supply current at 1.0 mA with no mixer linearity control current.

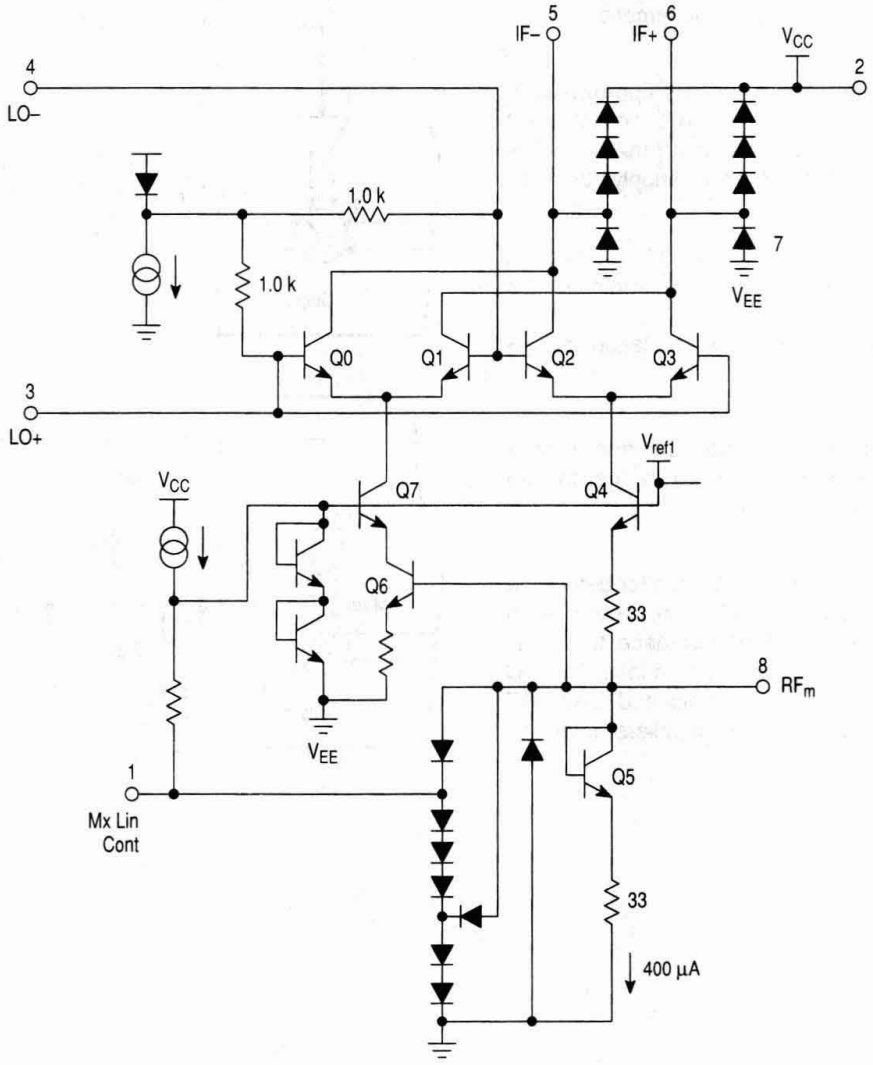
Mixer

The mixer is a unique and patented double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 2.4 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs (see Internal Circuit Schematic for details). The linear gain of the mixer is approximately –5.0 dB with a SSB noise figure of 12 dB.

Local Oscillator

The local oscillator has differential input configuration that requires typically –10 dBm input from an external source to achieve the optimal mixer gain.

Figure 8. MC13143 Internal Circuit*



NOTE: * The MC13143 uses a unique and patented circuit topology.

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board is laid out to accommodate all SMT components on the circuit side (see Circuit Side Component Placement View).

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The Component Placement View specifies particular components that were used to achieve the results shown in the typical curves and tables.

Mixer Input

The mixer input impedance is broadband 50 Ω for applications up to 2.4 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.

Mixer Linearity Control

The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).

Local Oscillator Inputs

The differential LO inputs are internally biased at $V_{CC} - 1.0\ V_{BE}$; this is suitable for high voltage and high gain operation.

For low voltage operation, the inputs are taken to V_{CC} through 51 Ω.

IF Output

The IF is a differential open collector configuration which is designed to use over a wide frequency range for up conversion as well as down conversion.

Input/Output Matching

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the RF input, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

Differential to single–ended circuit configuration is shown in the test circuit. 6.0 dB of additional mixer gain can be achieved by conjugately matching the output of the MiniCircuits transformer to 50 Ω at the desired IF frequency. With narrowband IF output matching the mixer performance is 3.0 dB gain and 12 dB noise figure (see Narrowband 49 and 83 MHz IF Output Matching Options). Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the circuit is 0 dB with a 15 dB noise figure.

Figure 9. Narrowband IF Output Matching with 16:1 Z Transformer and LC Network

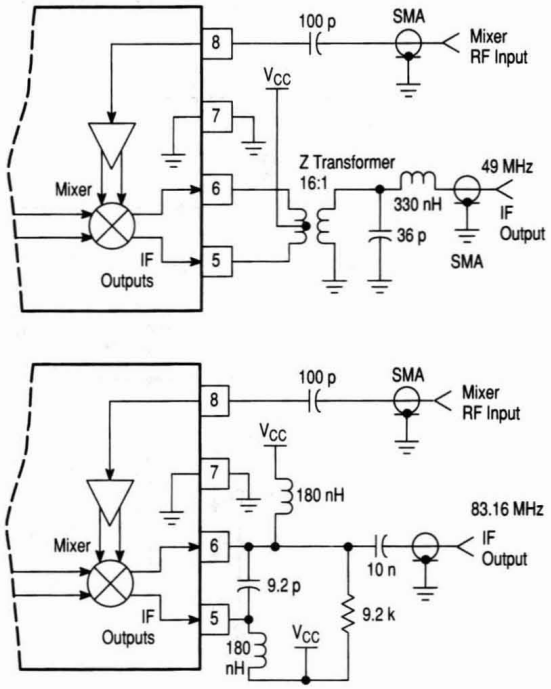
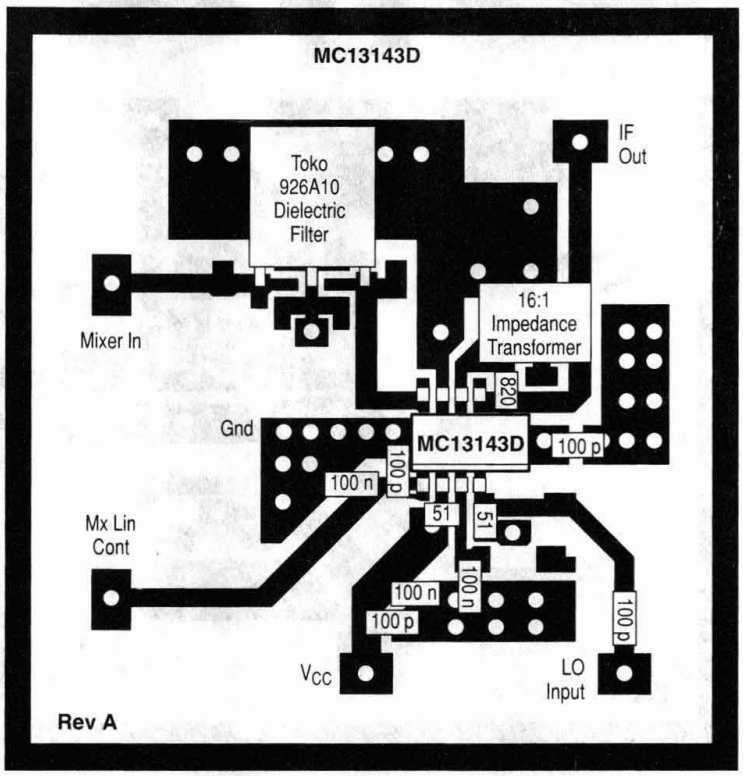


Figure 10. Circuit Side Component Placement View



NOTES: 926.5 MHz preselect dielectric filter is Toko part # 4DFA–926A10; the 4DFA (2 and 3 pole SMD type) filters are available for applications in cellular and GSM, GPS, DECT, PHS, PCS and ISM bands at 902–928 MHz, 1.8–1.9 GHz at 2.4–2.5 GHz.

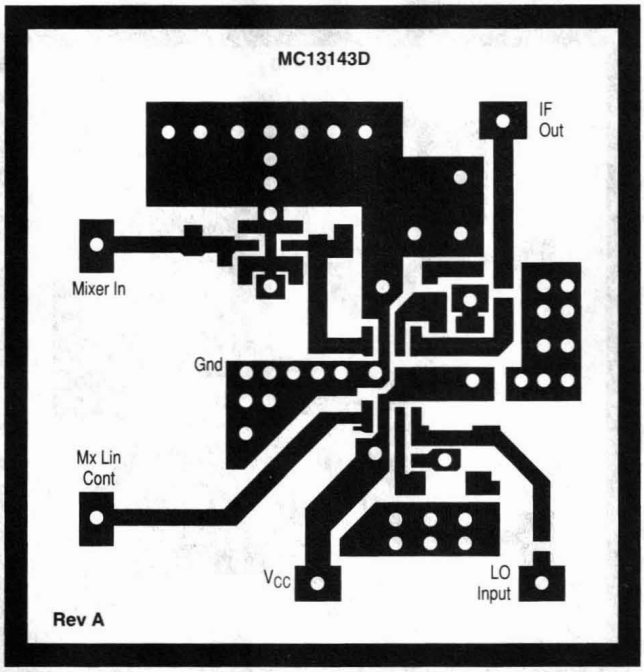
The PCB also accommodates a surface mount RF SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

The PCB may also be used without a preselector filter; AC coupled to the mixer as shown in the test circuit schematic. All other external circuit components shown in the PCB layout above are the same as used in the test circuit schematic.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount "TX" package. For a more selective narrowband match, a lowpass filter may be used after the transformer. The PCB is designed to accommodate lump inductors and capacitors in more selective narrowband matching of the mixer differential outputs to a single–ended output at a given IF frequency.

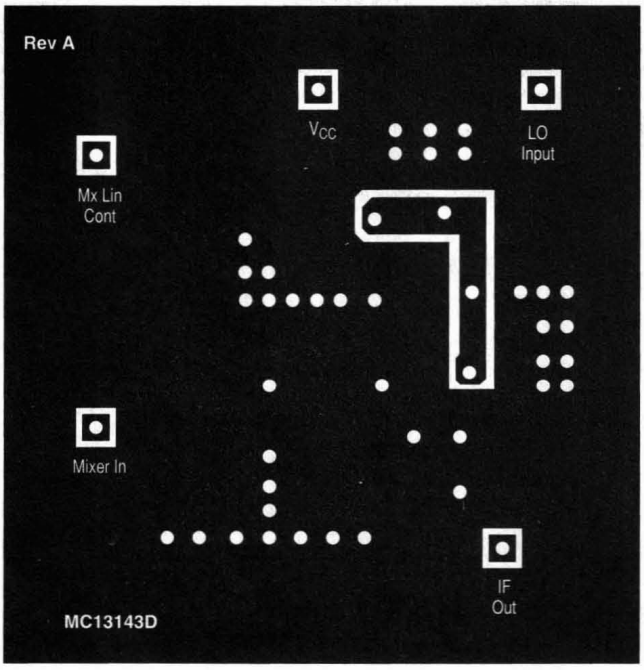
The local oscillator may also be driven in a differential configuration using a coaxial transformer. Recommended sources are the Toko Balun transformers type B4F, B5FL and B5F (SMD component).

Figure 11. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil.

Figure 12. Ground Side View



MOTOROLA

MC13144

Advance Information

VHF - 2.0 GHz Low Noise Amplifier with Programmable Bias

The MC13144 is designed in the Motorola High Frequency Bipolar MOSIAC V™ wafer process to provide excellent performance in analog and digital communication systems. It includes a cascoded LNA usable up to 2.0 GHz and at 1.8 Vdc, with 2 bit digital programming of the LNA bias. Targeted applications are in the UHF Family Radio Services, UHF and 800 MHz Special Mobile Radio, 800 MHz Cellular and GSM, PCS, DECT and PHS at 1.8 to 2.0 GHz and Cordless Telephones in the 902 to 928 MHz band covered by FCC Title 47; Part 15. The MC13144 offers the following features:

- 17 dB Gain at 900 MHz
- 1.4 dB Noise Figure at 900 MHz
- 1.0 dB Compression Point of –7.0 dBm; Input Third Order Intercept Point of –5.0 dBm
- Low Operating Supply Voltage (1.8 to 6.0 Vdc)
- Programmable Bias with Enable 1 and Enable 2
- Enable 1 and Enable 2 Programmed High for Optimal Noise Figure and Gain Associated with NF
- Can Override Enable and Externally Program In Up to 15 mA

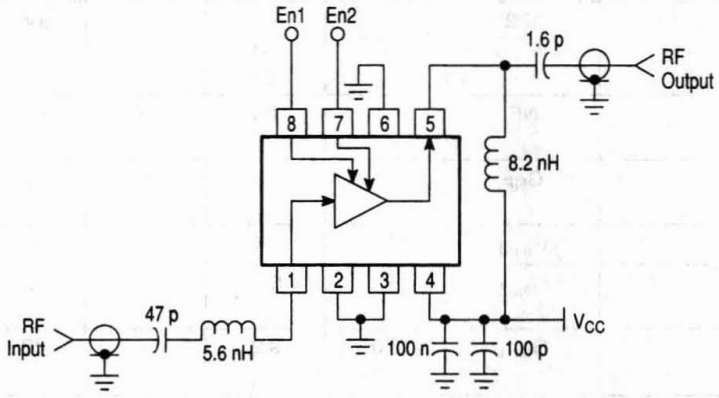
MOSAIC V is a trademark of Motorola, Inc.

VHF – 2.0 GHz LOW NOISE AMPLIFIER WITH PROGRAMMABLE BIAS

SEMICONDUCTOR TECHNICAL DATA

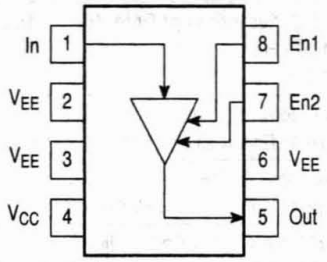
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Typical Application as 900 MHz Low Noise Amplifier



This device contains 67 active transistors.

PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13144D	T_A = – 40° to +85°C	SO–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	1.8	–	6.0	Vdc

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; f_{RF} = 1.0 GHz; Pin = –25 dBm)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down) (En1 = En2 = Low)	I_{CC0}	–	0.0001	20	µA
Supply Current (Power Up) (En1 = High; En2 = Low)	I_{CC1}	–	1.2	2.0	mA
Supply Current (Power Up) (En1 = High; En2 = Low)	I_{CC2}	–	3.4	5.0	mA
Supply Current (Power Up) (En1 = High; En2 = Low)	I_{CC3}	–	8.2	12	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; f_{RF} = 1.0 GHz; Pin = –25 dBm)

Characteristic	Symbol	Min	Typ	Max	Unit
Amplifier Gain (50 Ω Insertion Gain) (En1 = En2 = High)	$S_{21}{}^2$	–	12	–	dB
Amplifier Reverse Isolation (En1 = En2 = High)	S12	–	–35	–	dB
Amplifier Input Return Loss (En1 = En2 = High)	Γin_{amp}	–	–10	–	dB
Amplifier Output Return Loss (En1 = En2 = High)	Γout_{amp}	–	–15	–	dB
Input 3rd Order Intercept Point (En1 = En2 = High) df = 100 kHz df = 1.0 MHz	IIP3	 – –	 –11 –5.0	 – –	dBm
Amplifier Noise Figure (Figure 1; En1 = En2 = High)	NF	–	1.4	2.0	dB
Amplifier Gain @ NF (Figure 1; En1 = En2 = High)	G_{NF}	–	17	–	dB
Amplifier Gain (En1 = En2 = High)	G_{ain3}	14	17	–	dB
Amplifier Gain (En1 = High; En2 = Low)	G_{ain2}	10	13.3	–	dB
Amplifier Gain (En1 = High; En2 = Low)	G_{ain1}	6.0	9.2	–	dB

CIRCUIT DESCRIPTION

General

The MC13144 is a low noise amplifier with programmable bias. This device is designated for use in the front end section in analog and digital FM systems such as Wireless Local Area Network (LAN), Digital European Cordless Telephone (DECT), PHS, PCS, GPS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones.

Current Regulation/Enable

Temperature compensating voltage independent current regulation is digitally controlled by a 2 bit programmable bias/enable circuit.

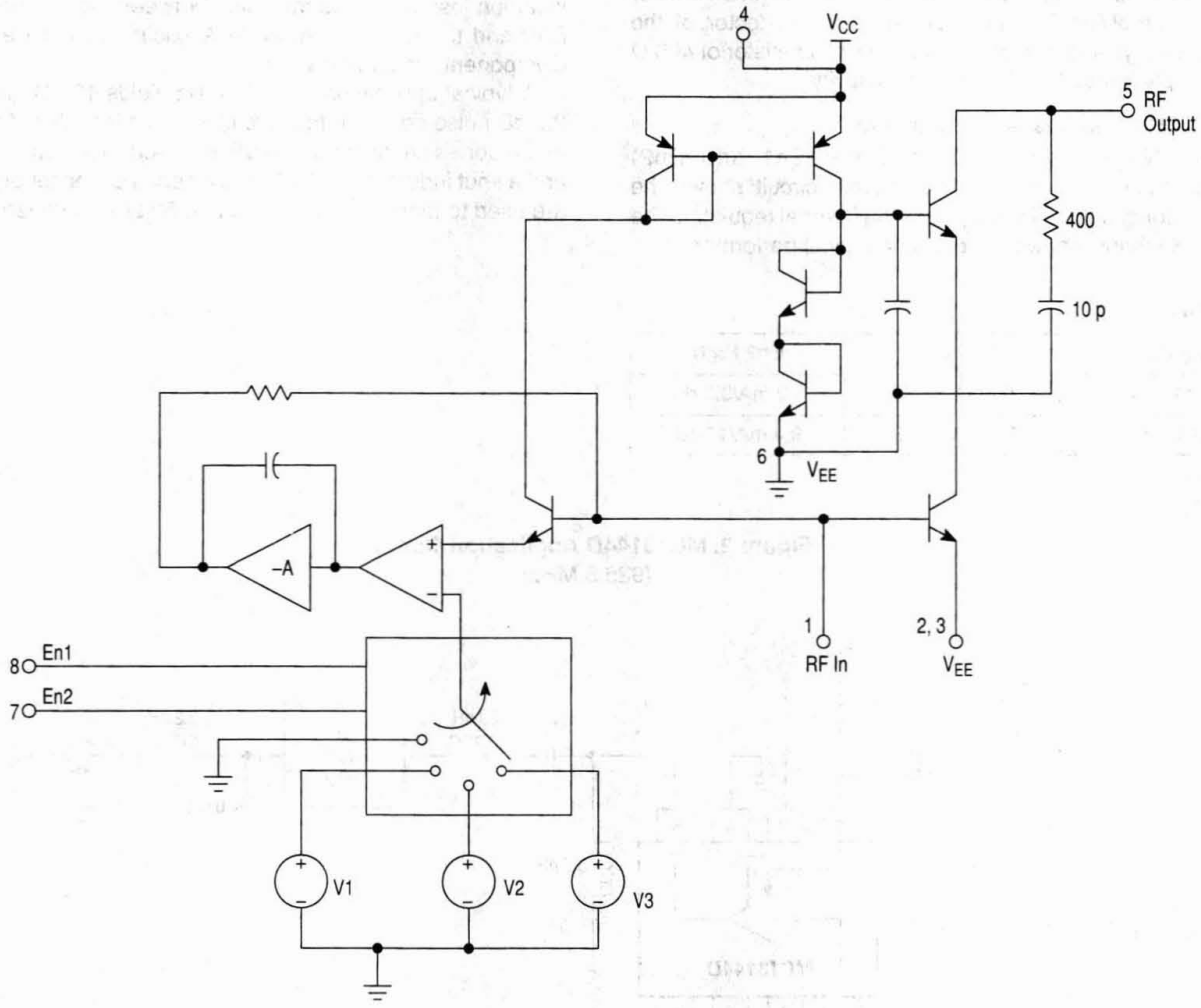
LNA

The LNA is a unique and patented cascode amplifier with digitally (2 bit) programmable bias (see Internal Circuit Schematic). Typical gain of the LNA is 17 dB for minimum noise figure of 1.4 dB at 900 MHz.

Programmable Bias/Enable Circuit

This unique circuit allows for 3 bias levels and a standby mode in which the LNA can be externally biased as desired.

Figure 1. MC13144 Internal Circuit*



NOTE: * The MC13144 uses a unique and patent pending circuit topology.

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board layout accommodates all SMT components on the circuit side (see Circuit Side Component Placement View).

Component Selection

The evaluation PC board is laid out for the 4DFA (2 pole SMD Type) and 4DFB (3 pole SMD Type) filters which are available for applications in Cellular and GSM, GPS (1.2 to 1.5 GHz), DECT, PHS and PCS (1.8 to 2.0 GHz) and ISM Bands (902 to 928 MHz and 2.4 to 2.5 GHz). In the 926.5 MHz Application Circuit, a ceramic deielectric filter is used (Toko part # 4DFA–926A10).

LNA Input/Output

The LNA input impedance is the base of a common emitter cascode amplifier. The LNA output is the collector of the cascode stage and it is loaded with a series resistor of 400 Ω and a capacitor of 10 pF to provide stability.

Digitally Programmable Bias/Enable

The LNA is enabled by a 2 bit (En1 and En2) programmable bias circuit. The internal circuit shows the comparator circuit which programs the internal regulator. The logic table below shows the bias and typical performance.

f = 900 mHz

I_{CC}/Gain	En2 Low	En2 High
En1 Low	0 mA/–22 dB	1.2 mA/9.2 dB
En1 High	3.4 mA/13 dB	9.4 mA/17 dB

f = 1900 mHz

I_{CC}/Gain	En2 Low	En2 High
En1 Low	0 mA/–22 dB	1.2 mA/7.5 dB
En1 High	3.4 mA/10 dB	8.2 mA/13 dB

Input/Output Matching

A typical application at 900 MHz yields 17 dB gain and 1.4 dB noise figure. In this circuit a series inductor of 5.6 nH is used to match the input and a shunt inductor of 8.2 nH which also serves as an RFC and a series capacitor of 0.9 p is used to match the LNA output to 50 Ω load impedance.

It may be desirable to use a RF ceramic or SAW filter after the LNA when driving a mixer to provide image frequency rejection. The image filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. Interface matching between the RF input, RF filter and the mixer is shown in Application Circuit and the Component Placement View.

A typical application at 1900 MHz yields 13 dB gain and 2.7 dB noise figure. In this circuit a series inductor of 5.6 nH and a series capacitor of 1.0 pF are used to match the input and a shut inductor of 2.0 nH and a series capacitor of 2.0 pF are used to match the LNA output to 50 Ω load impedance.

Figure 2. MC13144D Application Circuit
(926.5 MHz)

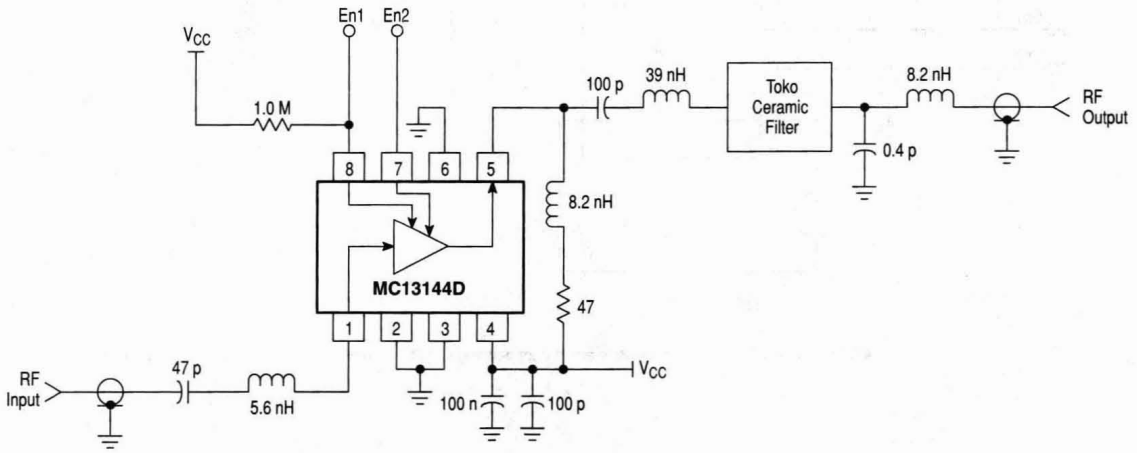


Figure 3. Typical S–Parameters VCC = 3.0 Vdc; En1 = En2 =1

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
100	0.91	–11	4.2	143	0.00028	24	0.80	–10
125	0.92	–14	4.2	136	0.00033	71	0.79	–10
150	0.90	–16	4.2	127	0.0006	60	0.79	–11
175	0.89	–19	4.2	118	0.0011	80	0.78	–12
200	0.89	–22	4.0	108	0.0014	35	0.78	–13
250	0.88	–26	3.8	97	0.0015	39	0.78	–14
300	0.86	–32	4.1	77	0.0022	52	0.78	–17
350	0.85	–36	3.5	59	0.0017	65	.078	–19
400	0.84	–41	3.7	50	0.0024	68	0.79	–21
450	0.83	–46	3.7	26	0.0021	63	0.79	–24
500	0.81	–50	3.2	15	0.0028	56	0.79	–26
550	0.80	–55	3.5	–3.0	0.0027	51	0.80	–29
600	0.79	–59	3.1	–22	0.0038	46	0.81	–32
650	0.77	–63	3.0	–36	0.0057	30	0.82	–35
700	0.77	–67	2.8	–52	0.0067	32	0.83	–39
750	0.77	–72	2.5	–68	0.0095	26	0.83	–43
800	0.76	–77	2.2	–77	0.014	13	0.80	–49
850	0.74	–82	2.2	–86	0.019	12	0.75	–51
900	0.71	–85	2.3	–100	0.020	38	0.73	–51
950	0.69	–88	2.3	–117	0.021	55	0.74	–51
1000	0.67	–91	2.3	–132	0.020	72	0.76	–54
1100	0.67	–98	2.2	–163	0.022	87	0.76	–59
1200	0.66	–106	2.1	168	0.026	107	0.79	–65
1300	0.79	–72	1.9	136	0.030	134	0.64	–73
1400	0.64	–121	1.9	100	0.038	150	0.80	–80
1500	0.62	–128	1.9	74	0.053	170	0.81	–87
1600	0.61	–135	1.7	40	0.068	157	0.82	–96
1700	0.59	–145	1.5	7.0	0.076	120	0.81	–105
1800	0.58	–152	1.4	–24	0.092	97	0.80	–115
1900	0.54	–125	1.2	–57	0.11	59	0.74	–125
2000	0.47	–130	1.0	–79	0.093	195	0.68	–130

Figure 4. Circuit Side Component Placement View

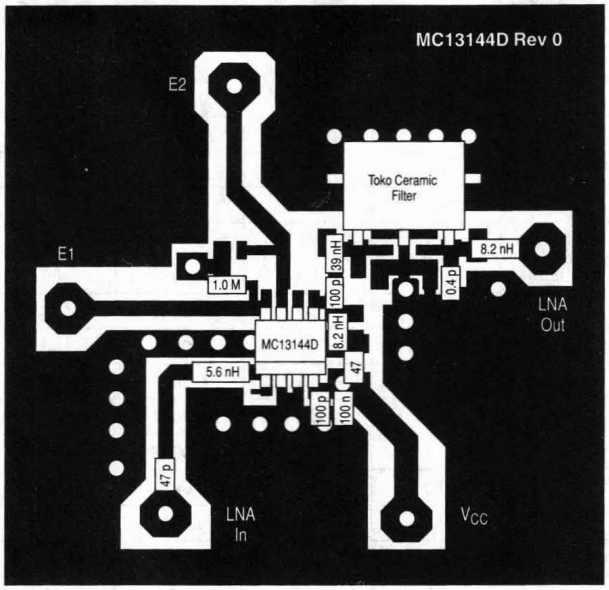
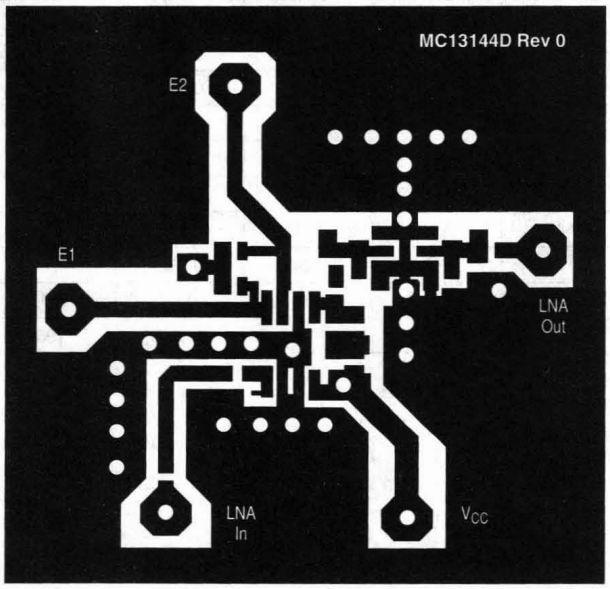
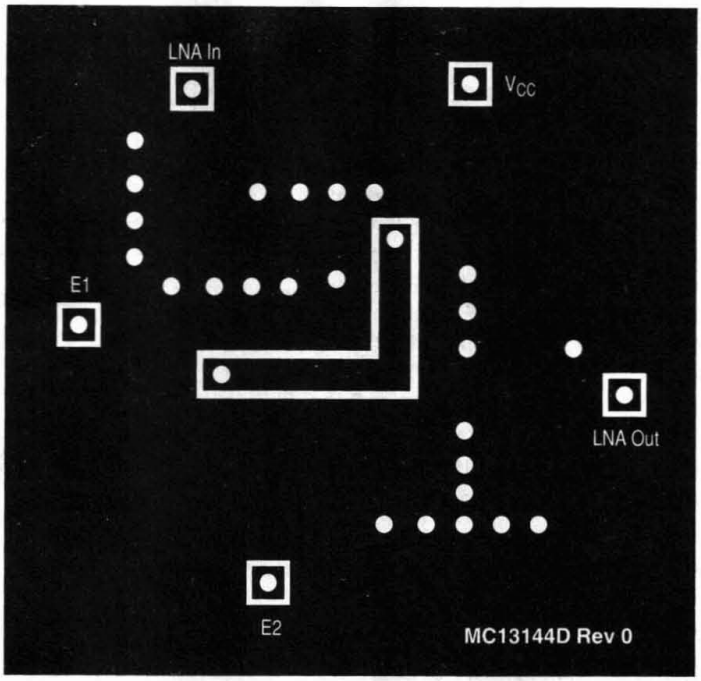


Figure 5. Circuit Side View



NOTES: Critical dimensions are 50 MIL centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC}, E1 and E2 are 50 MIL (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 6. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

MOTOROLA

MC13145

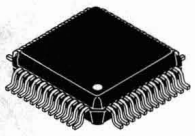
Product Preview

Low Power Integrated Receiver for ISM Band Applications

UHF WIDEBAND RECEIVER SUBSYSTEM (LNA, Mixer, VCO, Prescalar, IF Subsystem, Coilless Detector)

The MC13145 is a dual conversion integrated RF receiver intended for ISM band applications. It features a Low Noise Amplifier (LNA), two 50 Ω linear Mixers with linearity control, Voltage Controlled Oscillator (VCO), second LO amplifier, divide by 64/65 dual modulus Prescalar, split IF Amplifier and Limiter, RSSI output, Coilless FM/FSK Demodulator and power down control. Together with the transmit chip (MC13146) and the baseband chip (MC33410), a complete 900 MHz cordless phone system can be implemented. This device may be used in applications within 2.0 GHz since its RF bandwidth is greater than 2.4 GHz.

- Low (<1.8 dB @ 900 MHz) Noise Figure LNA with 14 dB Gain
- Externally Programmable Mixer linearity: IIP3 = 10(nom.) to +20 dBm (Mixer1); IIP3 = 10 (nom.) to 20 dBm (Mixer2)
- 50 Ω Mixer Input Impedance and Open Collector Output (Mixer 1 and Mixer 2); 50 Ω Second LO (LO2) Input Impedance
- Low Power 64/65 Dual Modulus Prescalar (MC12053 type)
- Split IF for Improved Filtering and Extended RSSI Range
- Internal 330 Ω Terminations for 10.7 MHz Filters
- Linear Coilless FM/FSK Demodulator with Externally Programmable Bandwidth, Center Frequency and Audio level
- 2.7 V to 6.5 V Operation, Low Current Drain (<30 mA @ 3.0 V) with Power Down Mode (<1.0 μA)
- 2.4 GHz RF, 1.0 GHz IF1 and 50 MHz IF2 Bandwidth



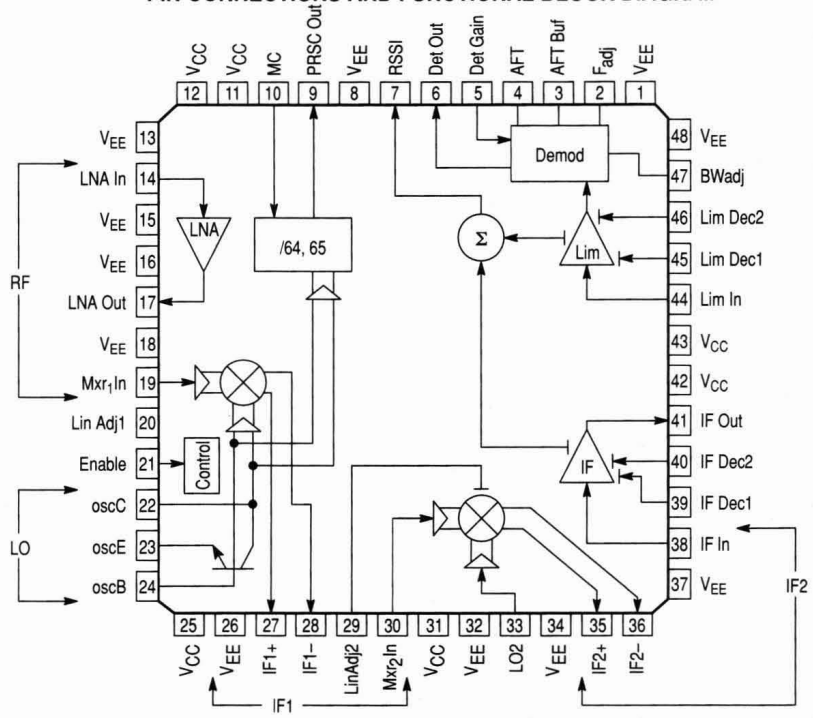
FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Temperature Range	Package
XC13145FTA	–40° to +85°C	LQFP–48

ESD Sensitive — Handle with Care

PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



OVERALL RECEIVER SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_J(max)	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (T_A = 25°C)	V_{CC} V_{EE}	2.7 to 6.5 0	Vdc
Input Frequency	f_{in}	100 to 2000	MHz
Ambient Temperature Range	T_A	−40 to +85	°C
Maximum Input Signal Level: – with no damage – with minor performance degradation	P_{in}	 5.0 −10	dBm

RECEIVER DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; No Input Signal, unless otherwise noted)

Characteristics	Symbol	Typical	Unit
Total Supply Current (Enable = V_{CC})	I_{total}	30	mA
Power Down Current (Enable = V_{EE})	I_{total}	<1.0	μA

RECEIVER AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; F_{mod} = 1.0 kHz; F_{dev} = ±25 kHz; IF filter bandwidth = 150 kHz, unless otherwise noted)

Characteristics	Symbol	Typical		Unit MHz
		900	1900	
12 dB SINAD Sensitivity (with C–message filter at DetOut)		−115	TBD	dBm
30 dB SINAD Sensitivity (No IF filter distortion within ±40 kHz)		−100	TBD	dBm
SINAD Variation with IF Offset of ±40 kHz (No IF filter distortion within ±40 kHz)		5.0	TBD	dB
RSSI Dynamic Range		80	TBD	dB
Input 1.0 dB Compression Point(Measured at IF output)	P_{in-1dB}	−18	TBD	dBm
Input 3rd Order Intercept Point (Measured at IF output)	IIP3	−8.0	TBD	dBm
Demodulator Output Swing (5.0 k Load)		0.5	0.5	V_{pp}
Demodulator Bandwidth (±1.0 dB bandwidth)		100	100	kHz
Prescalar Output Level (10 kΩ//8.0 pF load)		0.5	0.5	V_{pp}
Modulus Control Input Level		0.5	0.5	V_{pp}
SNR @ −30 dBm Signal Input (<25 kHz deviation;with C–Message Filter)		50	TBD	dB
Total Harmonic Distortion (<25 kHz deviation;with C–Message Filter)		1.0	TBD	%
Spurious Response SINAD (RF In: −50 dBm)		12	TBD	dB

INDIVIDUAL BLOCK SPECIFICATIONS

LOW NOISE AMPLIFIER ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Typical		Unit MHz
		900	1900	
Amplifier Gain	S21	14	TBD	dB
Noise Figure	NF	1.8	TBD	dB
1.0 dB Gain Compression Point	P_{in-1dB}	–8.0	TBD	dBm
3rd Order Intercept Point	IIP3	–5.0	TBD	dBm
Reverse Isolation	S12	–35	TBD	dB
Input Impedance (with externals)		50	50	Ω
Output Impedance (with externals)		50	50	Ω
Input Match (with externals)	S11	15	TBD	dB
Output Match (with externals)	S22	15	TBD	dB
LO1 to LNA Input Leakage		–45	TBD	dBm

FIRST MIXER ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Typical		Unit MHz
		900	1900	
Power Conversion Gain (P_{in} = –30 dBm)	Pgc	0	TBD	dB
Noise Figure	NF	13	TBD	dB
1.0 dB Gain Compression Point	P_{in-1dB}	–1.0	TBD	dBm
3rd Order Intercept Point	IIP3	9.0	TBD	dBm
Input Impedance (single–ended)		50	50	Ω
Output Impedance (differential with externals)		50	50	Ω
Input Match		20	TBD	dB
Output Match (with externals)		20	TBD	dB
RF to IF1 Leakage		–38	TBD	dB
LO to IF1 Leakage		–33	TBD	dBm
LO to RF Leakage		–33	TBD	dBm
Mixer Out to IF in Leakage		–80	TBD	dB

SECOND MIXER ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Typical	Unit
Noise Figure	NF	13	dB
1.0 dB Gain Compression Point	P_{in-1dB}	–1.0	dBm
3rd Order Intercept Point	IIP3	9.0	dBm
Input Impedance (single–ended)		50	Ω
Output Impedance (differential with externals)		330	Ω
Input Match		20	dB
Output Match (with externals)		20	dB

INDIVIDUAL BLOCK SPECIFICATIONS (continued)

LOCAL OSCILLATOR ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Typical		Unit
		900	1900	MHz
LO Emitter Current (Enable = high)		2.0	TBD	mA
Phase Noise @ 10 kHz Offset		–80	–75	dBc/Hz
Modulation Sideband		–40	TBD	dBc

PRESCALAR ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Typical		Unit
		900	1900	MHz
Divide Ratio – MC = low – MC = high		 65 64	 65 64	
Output Impedance		50	50	Ω
Prescalar Output Level (10 kΩ//8pF load)		0.5	0.5	V_{pp}
MC Input Level		0.5	0.5	V_{pp}
MC Current Input (optional)		200	200	μA_{pp}
Prescalar Out to IF Amp and Lim Amp Input Leakage		–85	TBD	dBm

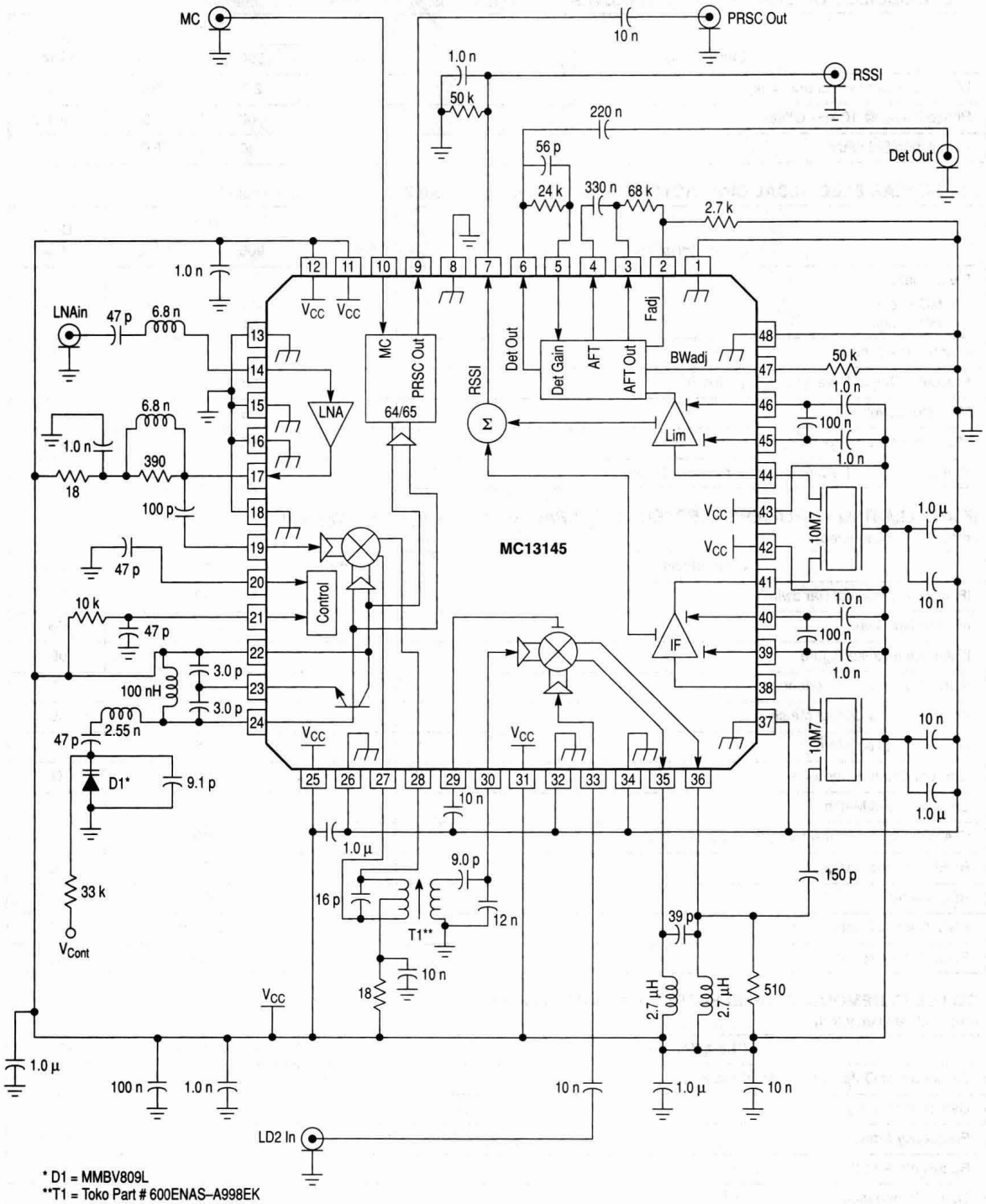
IF AND LIMITING AMPLIFIERS ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Typical	Unit
IF and Lim Amplifier Bandwidth		40	MHz
IF Amplifier Gain		40	dB
IF Amplifier Noise Figure		7.0	dB
IF Input & Output Impedance		330	Ω
IF Amp Input & Output Match		20	dB
Limiting Amplifier Gain		85	dB
Lim Amp Input Impedance		330	Ω
Lim Amp Input Match		15	dB
IF Amp Output to Lim Amp Input Leakage (at 10.7 MHz)		80	dB
RSSI Dynamic Range		80	dB
RSSI Slope		0.5	µA/dB
RSSI Current Range		0 to 40	µA
RSSI Response Time		1.0	µs

COILLESS DEMODULATOR ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Typical	Unit
Demodulator Output (at 25 kHz deviation)	DetOut	0.5	V_{pp}
Center Frequency		10.7	MHz
Frequency Adjust		<20	MHz
Bandwidth Adjust		100 to 600	kHz
Output Impedance		2000	Ω
Settling Time (assert Enable pin)		TBD	ms

Figure 1. Application Diagram



* D1 = MMBV809L
**T1 = Toko Part # 600ENAS–A998EK

MOTOROLA

MC13146

Product Preview

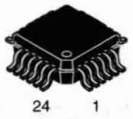
Low Power Integrated Transmitter for ISM Band Applications

LOW POWER DC – 2.0 GHz TRANSMITTER

SEMICONDUCTOR TECHNICAL DATA

The MC13146 is an integrated RF transmitter targeted at ISM band applications. It features a 50 Ω linear Mixer with linearity control, voltage controlled oscillator, divide by 64/65 dual modulus Prescaler and Exciter. Together with the receiver chip (MC13145) and the baseband chip (MC33410), a complete 900 MHz cordless phone system can be implemented. This device may be used in applications within 2 GHz since its RF bandwidth is greater than 2.4 GHz.

- Low Distortion Exciter: $P_{out\_1\ dB}$ Compression Point ≈ 8 dBm
- HIgh Mixer Linearity: IIP3 = 10 dBm
- 50 Ω Mixer Input Impedance
- Differential Open Collector Mixer Output
- 20 dB Power Conversion Gain
- Low Power 64/65 Dual Modulus Prescaler (MC12054 type)
- 2.7 to 6.5 V Operation, Low Current Drain (25 mA @ 2.0 GHz)
- Powerdown Mode: <1.0 µA
- 2.4 GHz RF Bandwidth
- 1.8 GHz IF Bandwidth

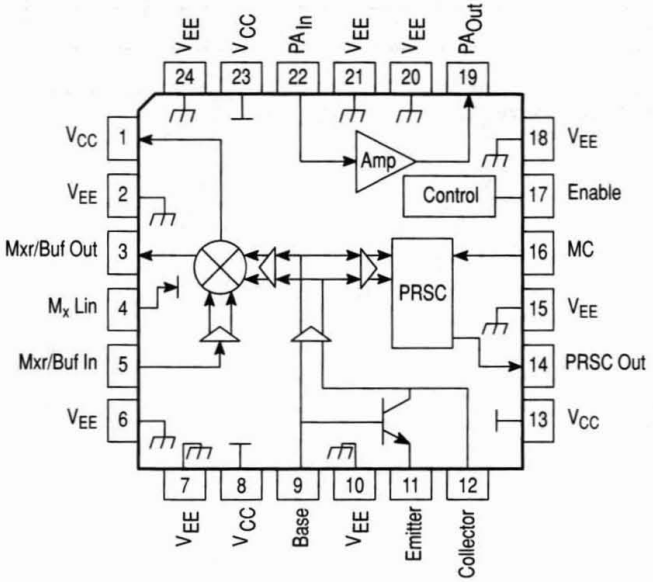


FTA SUFFIX
PLASTIC PACKAGE
CASE 977
(LQFP–24)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
XC13146FTA	T_A = –40 ° to +85°C	LQFP–24

PIN CONNECTIONS
LQFP–24



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_J(max)	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (TA = 25°C)					
	VCC	2.7	–	6.5	Vdc
	VEE	–	0	–	Vdc
RF Frequency Range	f_{RF}	1.0	–	2500	MHz
Ambient Temperature Range	T_A	–40	–	85	°C
Maximum Input Signal Level	P_{IF}				
– with no damage		–	–10	–	dBm
– with minor performace degradation		–	15	–	dBm

TRANSMITTER DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 Vdc, no input signal, unless otherwise noted)

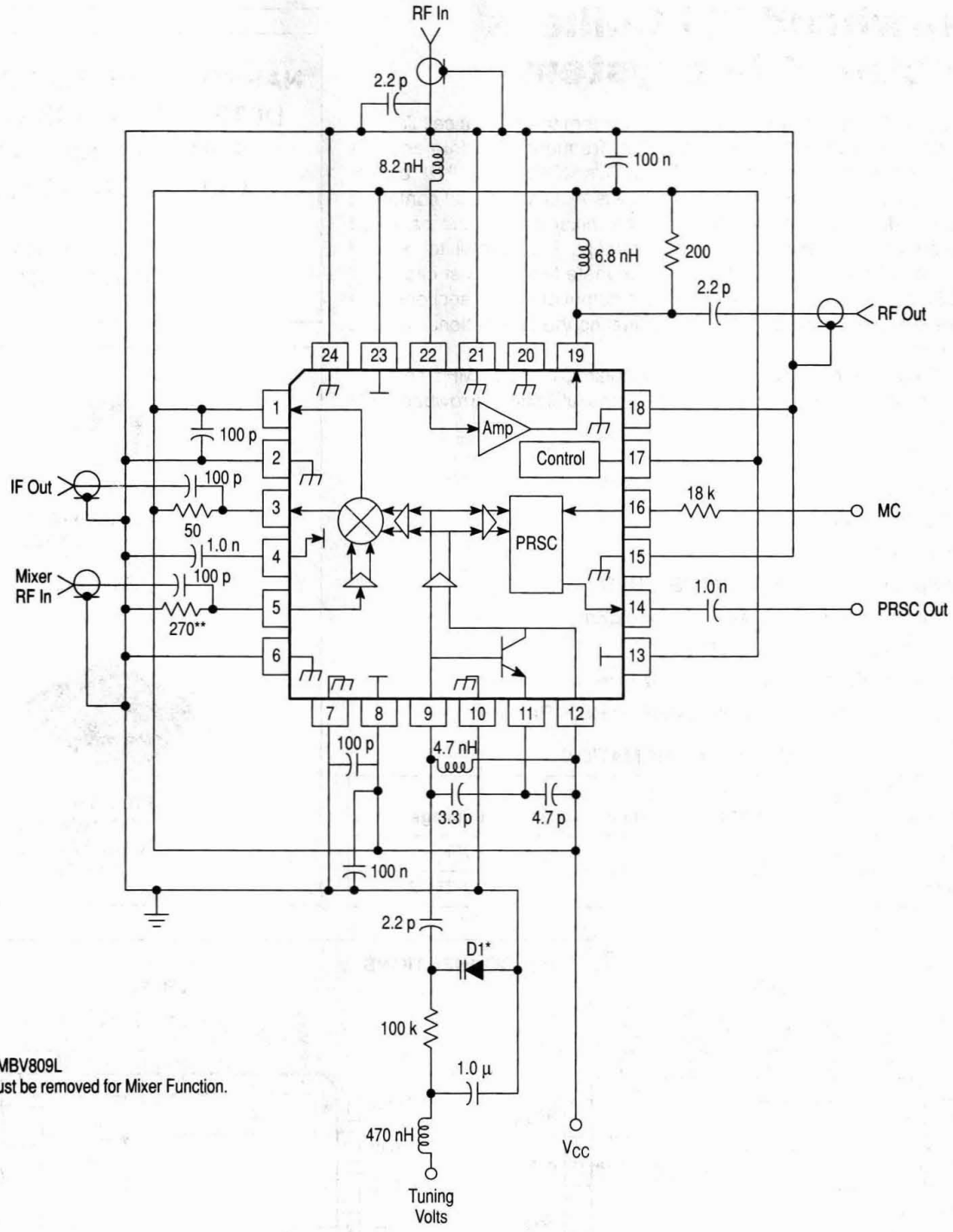
Characteristic	Symbol	Min	Typ	Max	Unit
Total Supply Current (Enable = V_{CC})	I_{total}	-	25	-	mA
Power Down Current (Enable = V_{EE})	I_{total}	-	0.1	-	µA

TRANSMITTER AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 Vdc, Enable = 3.0 Vdc, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Power (with external matching)	$P_{A\_}P_O$	–	0	–	dBm
Distortion (@ 820 MHz = f_{IF_out}) (Note 1)	$P_{1dBC.Pt.}$	–	8.0	–	dBm
Mixer/Buffer (@ 900 MHz = f_{osc}) (Note 1)	P_{Mx/Buf_out}	–	–18	–	dBm
Output Harmonics (with external matching @ 820 MHz)					
2nd	P_{A-2f}	–	–25	–	dBc
3rd	P_{A-3f}	–	–35	–	dBc
VCO Phase Noise (@ 10 kHz offset) (Note 1)		–	–80	–	dBc/Hz
Mixer/Buffer Output Impedance		–	50	–	Ω
Prescalar Output Level (10 k ‖ 8.0 pF load)		–	0.5	–	V_{pp}
MC Current Input (optional)		–	200	–	$µA_{pp}$

NOTE: Tests run during test system/device characterization.

Figure 1. Test Circuit



* MMBV809L
** Must be removed for Mixer Function.

MOTOROLA

MC13150

Narrowband FM Coilless Detector IF Subsystem

NARROWBAND FM COILLESS DETECTOR IF SUBSYSTEM FOR CELLULAR AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 μV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range

FTA SUFFIX
PLASTIC PACKAGE
CASE 977
(LQFP–24)

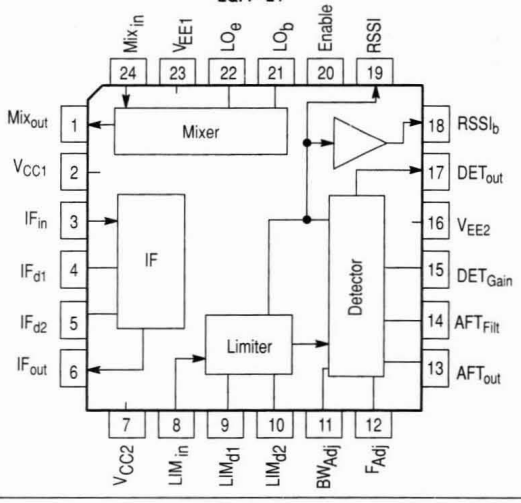
FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(LQFP–32)

ORDERING INFORMATION

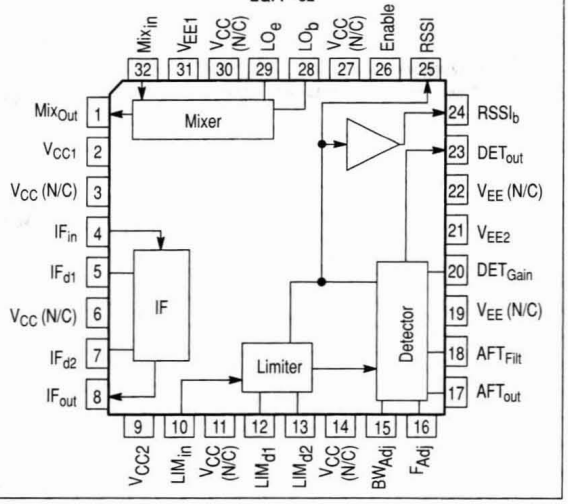
Device	Operating Temperature Range	Package
MC13150FTA	T_A = –40 ° to +85°C	LQFP–24
MC13150FTB		LQFP–32

PIN CONNECTIONS

LQFP–24



LQFP–32



MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	2, 9	V_{CC}(max)	6.5	Vdc
Junction Temperature	–	T_{Jmax}	+150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

NOTE: 1. Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25°C –40°C ≤ T_A ≤ 85°C (See Figure 22)	2, 9 21, 31	V_{CC} V_{EE}	2.5 to 6.0 0	Vdc
Input Frequency	32	f_{in}	10 to 500	MHz
Ambient Temperature Range	–	T_A	–40 to +85	°C
Input Signal Level	32	V_{in}	0	dBm

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 3.0 Vdc, No Input Signal.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	V_S = 3.0 Vdc	2 + 9	I_{TOTAL}	–	1.7	3.0	mA
Supply Current, Power Down (See Figure 3)	–	2 + 9	–	–	40	–	nA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figure 15)	f_{mod} = 1.0 kHz; f_{dev} = ±5.0 kHz	32	–	–	–100	–	dBm
RSSI Dynamic Range (See Figure 7)	–	25	–	–	100	–	dB
Input 1.0 dB Compression Point Input 3rd Order Intercept Point (See Figure 18)	– –	– –	1.0 dB C. Pt. IIP3	– –	–11 –1.0	– –	dBm
Coilless Detector Bandwidth Adjust (See Figure 11)	Measured with No IF Filters	–	ΔBW adj	–	26	–	kHz/μA
MIXER							
Conversion Voltage Gain (See Figure 5)	P_{in} = –30 dBm; PLO = –10 dBm	32	–	–	10	–	dB
Mixer Input Impedance	Single–Ended	32	–	–	200	–	Ω
Mixer Output Impedance	–	1	–	–	1.5	–	kΩ
LOCAL OSCILLATOR							
LO Emitter Current (See Figure 26)	–	29	–	30	63	100	μA
IF & LIMITING AMPLIFIERS SECTION							
IF and Limiter RSSI Slope	Figure 7	25	–	–	0.4	–	μA/dB
IF Gain	Figure 8	4, 8	–	–	42	–	dB
IF Input & Output Impedance	–	4, 8	–	–	1.5	–	kΩ
Limiter Input Impedance	–	10	–	–	1.5	–	kΩ
Limiter Gain	–	–	–	–	96	–	dB

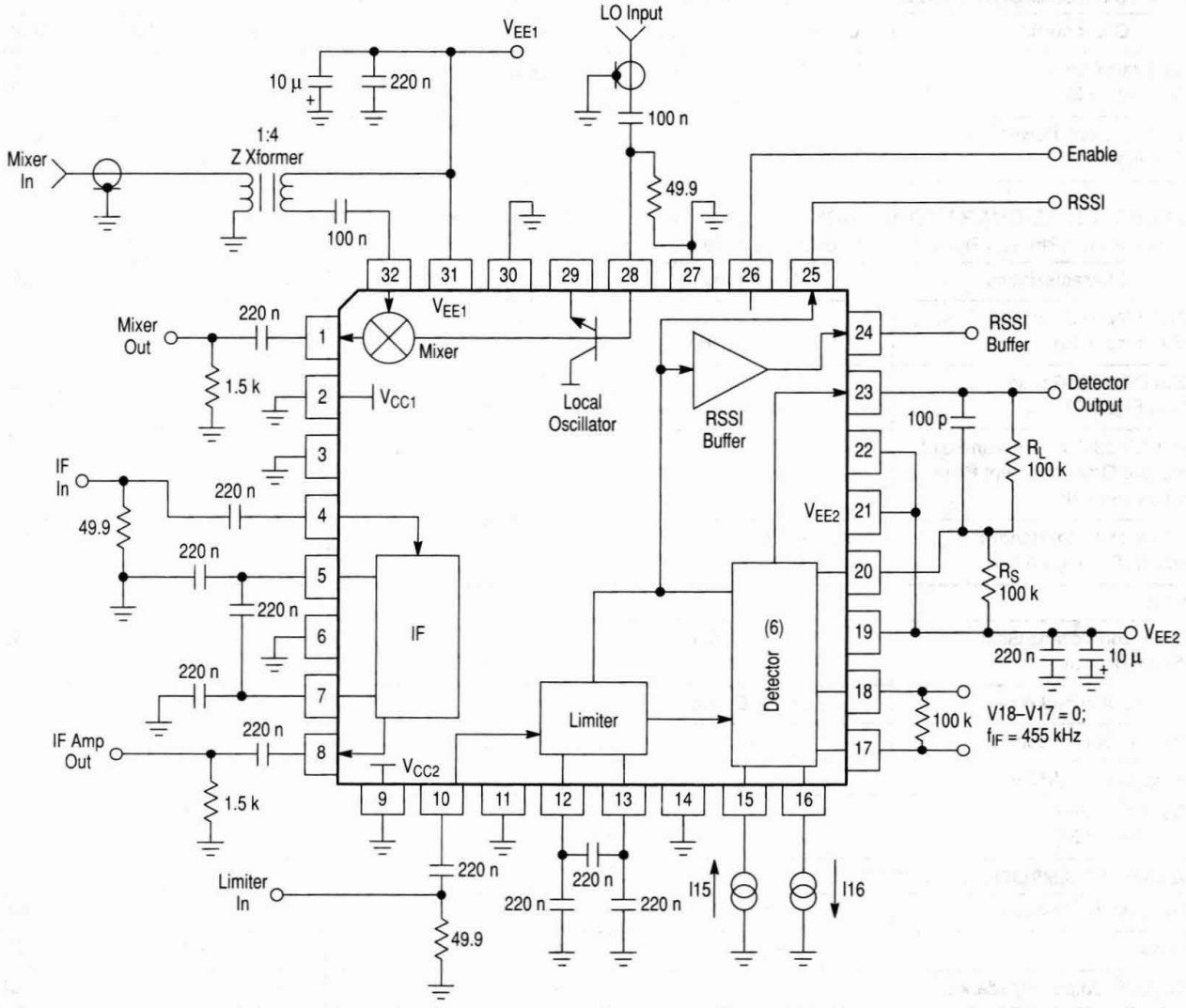
* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
DETECTOR							
Frequency Adjust Current	Figure 9, f_{IF} = 455 kHz	16	–	41	49	56	µA
Frequency Adjust Voltage	Figure 10, f_{IF} = 455 kHz	16	–	600	650	700	mVdc
Bandwidth Adjust Voltage	Figure 12, I_{15} = 1.0 µA	15	–	–	570	–	mVdc
Detector DC Output Voltage (See Figure 25)	–	23	–	–	1.36	–	Vdc
Recovered Audio Voltage	f_{dev} = ±3.0 kHz	23	–	85	122	175	mVrms

* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

Figure 1. Test Circuit



This device contains 292 active transistors.

MC13150 CIRCUIT DESCRIPTION

General

The MC13150 is a very low power single conversion narrowband FM receiver incorporating a split IF. This device is designated for use as the backend in analog narrowband FM systems such as cellular, 900 MHz cordless phones and narrowband data links with data rates up to 9.6 k baud. It contains a mixer, oscillator, extended range received signal strength indicator (RSSI), RSSI buffer, IF amplifier, limiting IF, a unique coilless quadrature detector and a device enable function (see Package Pin Outs/Block Diagram).

Low Current Operation

The MC13150 is designed for battery and portable applications. Supply current is typically 1.7 mAdc at 3.0 Vdc. Figure 2 shows the supply current versus supply voltage.

Enable

The enable function is provided for battery powered operation. The enabled pin is pulled down to enable the regulators. Figure 3 shows the supply current versus enable voltage, V_{enable} (relative to V_{CC}) needed to enable the device. Note that the device is fully enabled at $V_{CC} - 1.3$ Vdc. Figure 4 shows the relationship of enable current, I_{enable} to enable voltage, V_{enable}.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It has a single ended input. Figure 5 shows the mixer gain and saturated output response as a function of input signal drive and for –10 dBm LO drive level. This is measured in the application circuit shown in Figure 15 in which a single LC matching network is used. Since the single–ended input impedance of the mixer is 200 Ω, an alternate solution uses a 1:4 impedance transformer to match the mixer to 50 Ω input impedance. The linear voltage gain of the mixer alone is approximately 4.0 dB (plus an additional 6.0 dB for the transformer). Figure 6 shows the mixer gain versus the LO input level for various mixer input levels at 50 MHz RF input.

The buffered output of the mixer is internally loaded, resulting in an output impedance of 1.5 kΩ.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 200 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 29 (in 32 pin QFP package) to V_{EE} to keep the oscillator on continuously or it may be taken to the enable pin to shut it off when the receiver is disabled. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 6). The oscillator configurations specified above are described in the application section.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 25 (in 32 pin QFP package) sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB. The RSSI circuit is designed to provide 100+ dB of dynamic range with temperature compensation (see Figures 7 and 23 which show the RSSI response of the applications circuit).

RSSI Buffer

The RSSI buffer has limitations in what loads it can drive. It can pull loads well towards the positive and negative supplies, but has problems pulling the load away from the supplies. The load should be biased at half supply to overcome this limitation.

Figure 2. Supply Current versus Supply Voltage

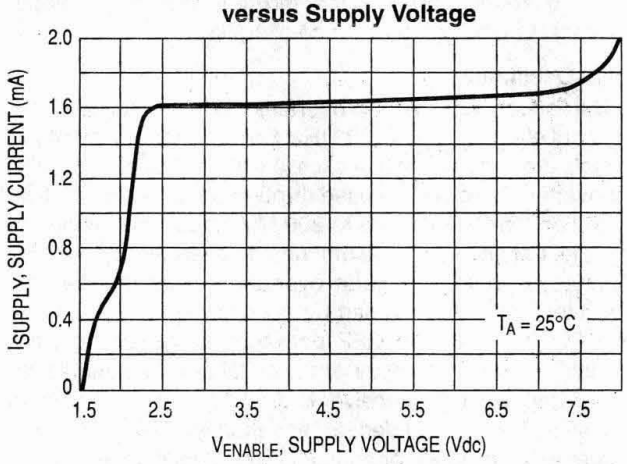


Figure 3. Supply Current versus Enable Voltage

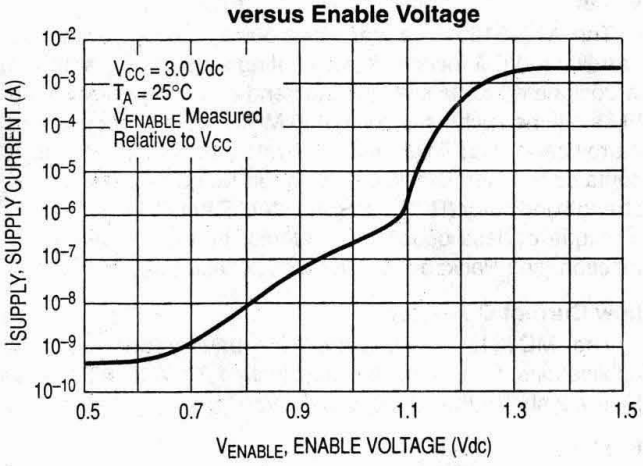


Figure 4. Enable Current versus Enable Voltage

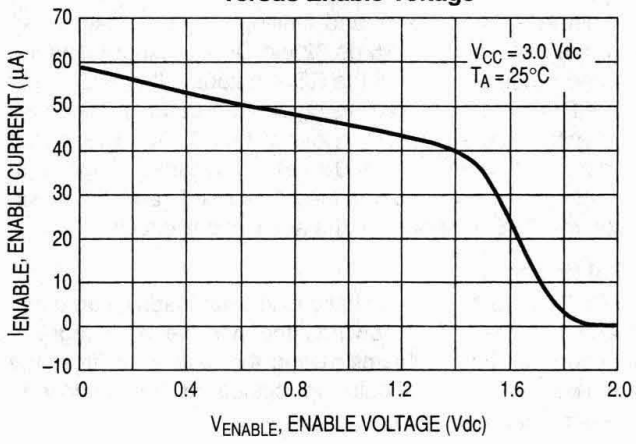


Figure 5. Mixer IF Output Level versus RF Input Level

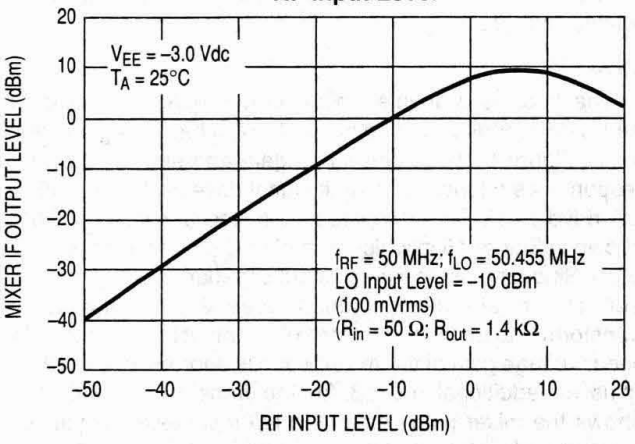


Figure 6. Mixer IF Output Level versus Local Oscillator Input Level

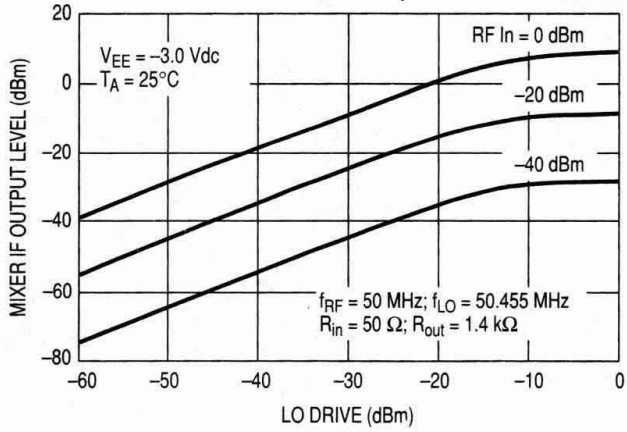
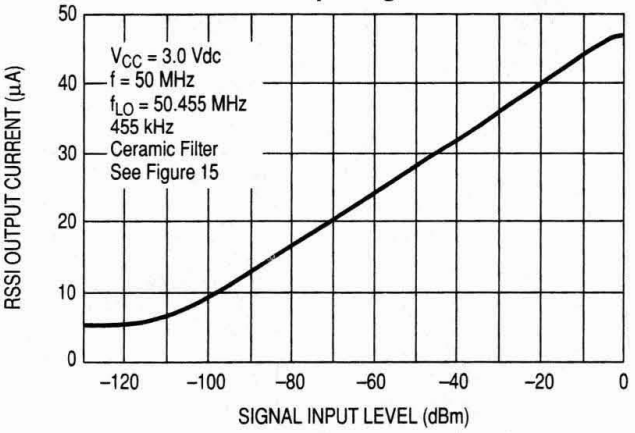


Figure 7. RSSI Output Current versus Input Signal Level



IF Amplifier

The first IF amplifier section is composed of three differential stages. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 42 dB at 455 kHz. Figure 8 shows the gain of the IF amplifier as a function of the IF frequency.

The fixed internal input impedance is 1.5 kΩ; it is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.5 kΩ source and load impedance.

Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 1.5 kΩ.

Limiter

The limiter section is similar to the IF amplifier section except that six stages are used. The fixed internal input impedance is 1.5 kΩ. The total gain of the limiting amplifier section is approximately 96 dB. This IF limiting amplifier section internally drives the quadrature detector section.

Figure 8. IF Amplifier Gain versus IF Frequency

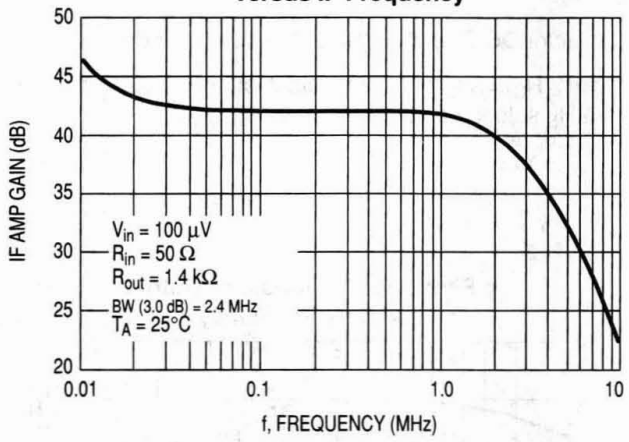


Figure 9. F_{adj} Current versus IF Frequency

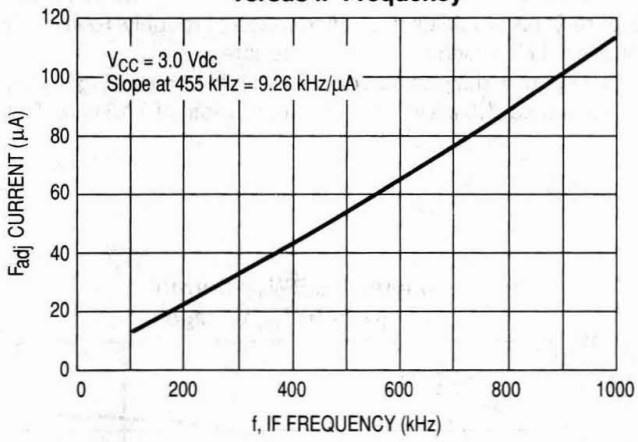


Figure 10. F_{adj} Voltage versus F_{adj} Current

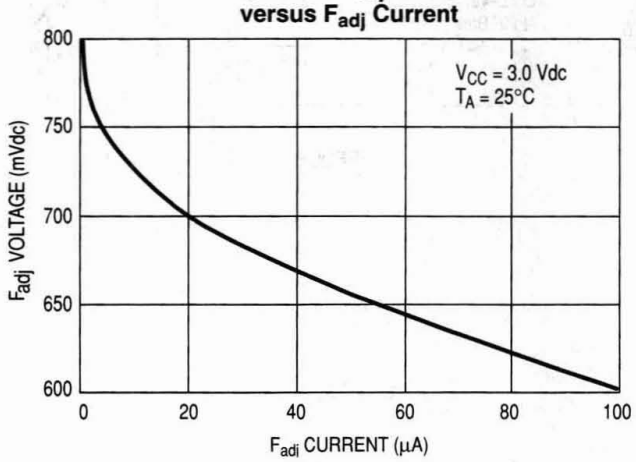
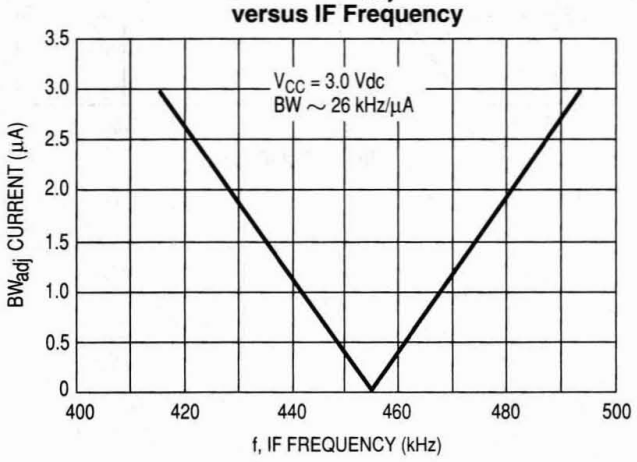


Figure 11. BW_{adj} Current versus IF Frequency



Coilless Detector

The quadrature detector is similar to a PLL. There is an internal oscillator running at the IF frequency and two detector outputs. One is used to deliver the audio signal and the other one is filtered and used to tune the oscillator.

The oscillator frequency is set by an external resistor at the F_{adj} pin. Figure 9 shows the control current required for a particular frequency; Figure 10 shows the pin voltage at that current. From this the value of R_F is chosen. For example, 455 kHz would require a current of around 50 μA. The pin voltage (Pin 16 in the 32 pin QFP package) is around 655mV giving a resistor of 13.1 kΩ. Choosing 12 kΩ as the nearest standard value gives a current of approximately 55 μA. The 5.0 μA difference can be taken up by the tuning resistor, R_T.

The best nominal frequency for the AFT_{out} pin (Pin 17) would be half supply. A supply voltage of 3.0 Vdc suggests a resistor value of (1.5 – 0.655)V/5.0 μA = 169 kΩ. Choosing 150 kΩ would give a tuning current of 3/150 k = 20 μA. From Figure 9 this would give a tuning range of roughly 10 kHz/μA or ± 100 kHz which should be adequate.

The bandwidth can be adjusted with the help of Figure 11. For example, 1.0 μA would give a bandwidth of ± 13 kHz. The voltage across the bandwidth resistor, R_B from Figure 12 is V_{CC} – 2.44 Vdc = 0.56 Vdc for V_{CC} = 3.0 Vdc, so R_B = 0.56V/1.0 μA = 560 kΩ. Actually the locking range will be ±13 kHz while the audio bandwidth will be approximately ±8.4 kHz due to an internal filter capacitor. This is verified in Figure 13. For some applications it may be desirable that the audio bandwidth is increased; this is done by reducing R_B. Reducing R_B widens the detector bandwidth and improves the distortion at high input levels at the expense of 12 dB SINAD sensitivity. The low frequency 3.0dB point is set by the tuning circuit such that the product

$$R_T C_T = 0.68/f3dB.$$

So, for example, 150 k and 1.0 μF give a 3.0 dB point of 4.5 Hz. The recovered audio is set by R_L to give roughly 50mV per kHz deviation per 100 k of resistance. The dc level can be shifted by R_S from the nominal 0.68 V by the following equation:

$$\text{Detector DC Output} = ((R_L + R_S)/R_S)\ 0.68\ \text{Vdc}$$

Thus, $R_S = R_L$ sets the output at 2 x 0.68 = 1.36 V; $R_L = 2R_S$ sets the output at 3 x 0.68 = 2.0 V.

Figure 12. BW_{adj} Current versus BW_{adj} Voltage

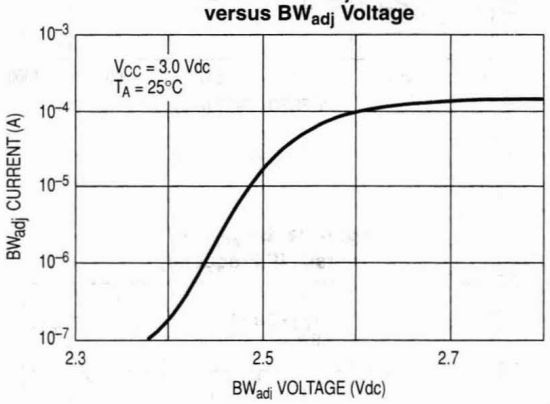
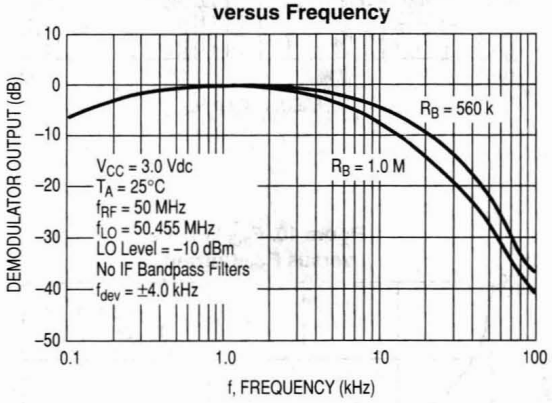


Figure 13. Demodulator Output versus Frequency



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. There is an area dedicated for a LNA preamp. This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. The applications circuit schematic (Figure 15) specifies particular components that were used to achieve the results shown in the typical curves but equivalent components should give similar results. Component placement views are shown in Figures 27 and 28 for the application circuit in Figure 15 and for the 83.616 MHz crystal oscillator circuit in Figure 16.

Input Matching Components

The input matching circuit shown in the application circuit schematic (Figure 15) is a series L, shunt C single L section which is used to match the mixer input to 50 Ω. An alternative input network may use 1:4 surface mount transformers or BALUNs. The 12 dB SINAD sensitivity using the 1:4 impedance transformer is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±5.0 kHz at f_{in} = 50 MHz and f_{LO} = 50.455 MHz (see Figure 14).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. SAW filters sourced from Toko (Part # SWS083GBWA) and Murata (Part # SAF83.16MA51X) are excellent choices to easily interface with the MC13150 mixer. They are packaged in a 12 pin low profile surface mount ceramic package. The center frequency is 83.161 MHz and the 3.0 dB bandwidth is 30 kHz.

Figure 14. S+N+D, N+D, N, 30% AMR versus Input Signal Level

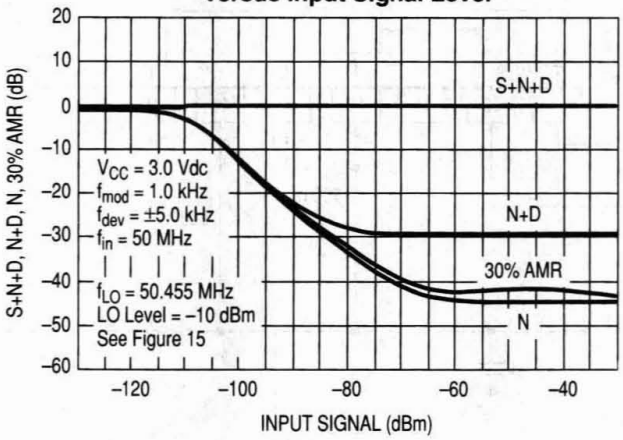
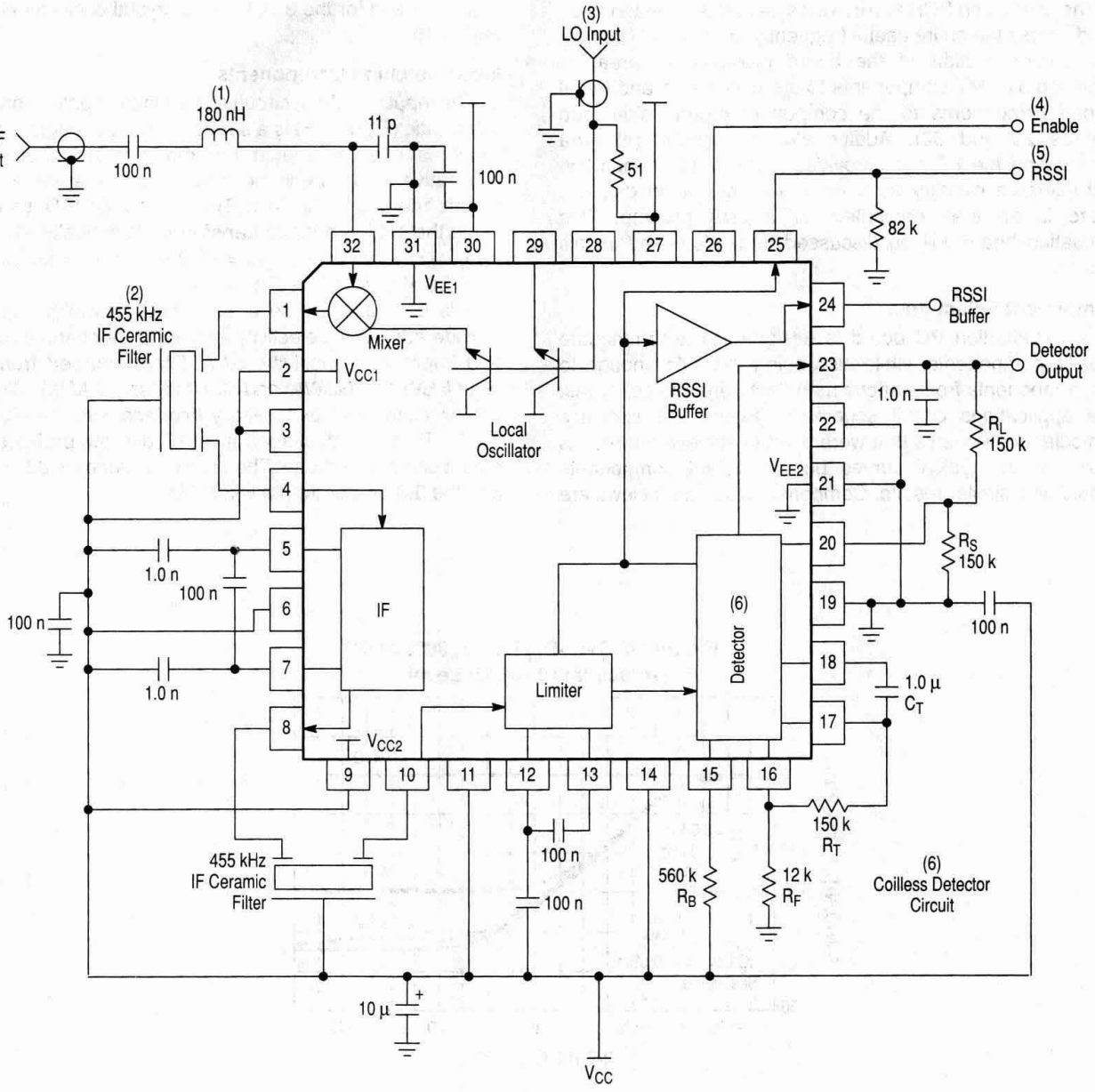


Figure 15. Application Circuit



NOTES: 1. Alternate solution is 1:4 impedance transformer (sources include Mini Circuits, Coilcraft and Toko).
2. 455 kHz ceramic filters (source Murata CFU455 series which are selected for various bandwidths).
3. For external LO source, a 51 Ω pull–up resistor is used to bias the base of the on–board transistor as shown in Figure 15. Designer may provide local oscillator with 3rd, 5th, or 7th overtone crystal oscillator circuit. The PC board is laid out to accommodate external components needed for a Butler emitter coupled crystal oscillator (see Figure 16).
4. Enable IC by switching the pin to V_{EE}.
5. The resistor is chosen to set the range of RSSI voltage output swing.
6. Details regarding the external components to setup the coilless detector are provided in the application section.

Local Oscillators

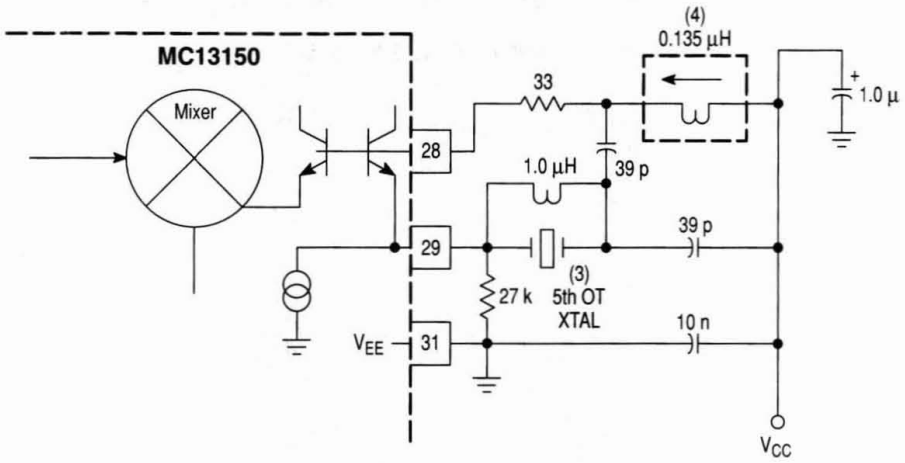
HF & VHF Applications

In the application schematic, an external sourced local oscillator is utilized in which the base is biased via a 51 Ω resistor to V_{CC}. However, the on–chip grounded collector transistor may be used for HF and VHF local oscillators with higher order overtone crystals. Figure 16 shows a 5th overtone oscillator at 83.616 MHz. The circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ac ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large, a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_o, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_o has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor, which forms the resonant tank with the tap capacitors, is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_o, is placed in parallel with the crystal. L_o is chosen to resonant with the crystal parallel capacitance, C_o, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

Figure 16. MC13150FTB Overtone Oscillator
f_{RF} = 83.16 MHz; f_{LO} = 83.616 MHz
5th Overtone Crystal Oscillator



Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 17. This information helps determine the network topology and gain blocks required ahead of the MC13150 to achieve the desired sensitivity and dynamic range of the receiver system. The PCB is laid out to accommodate a low noise preamp followed by the 83.16 MHz SAW filter. In the application circuit (Figure 15), the input 1.0 dB compression point is –10 dBm and the input third order intercept (IP3) performance of the system is approximately 0 dBm (see Figure 18).

Typical Performance Over Temperature

Figures 19–26 show the device performance over temperature.

Figure 17. Signal Levels versus RF Input Signal Level

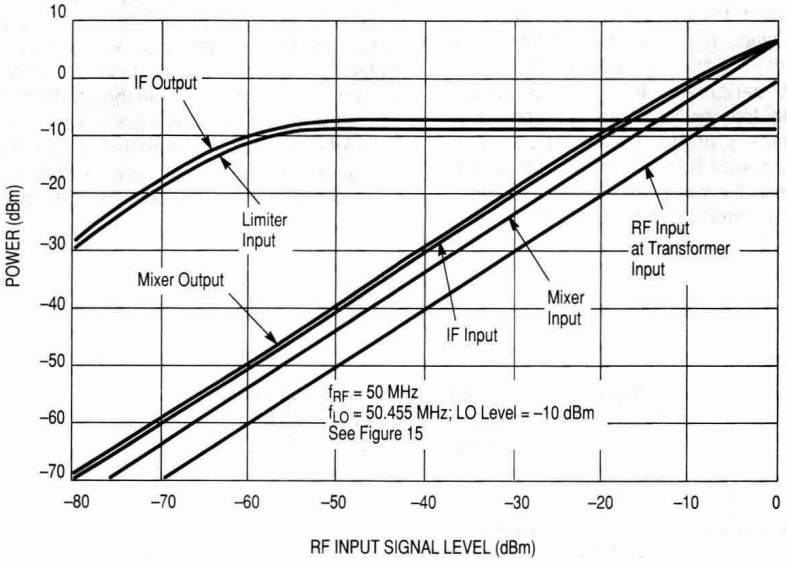
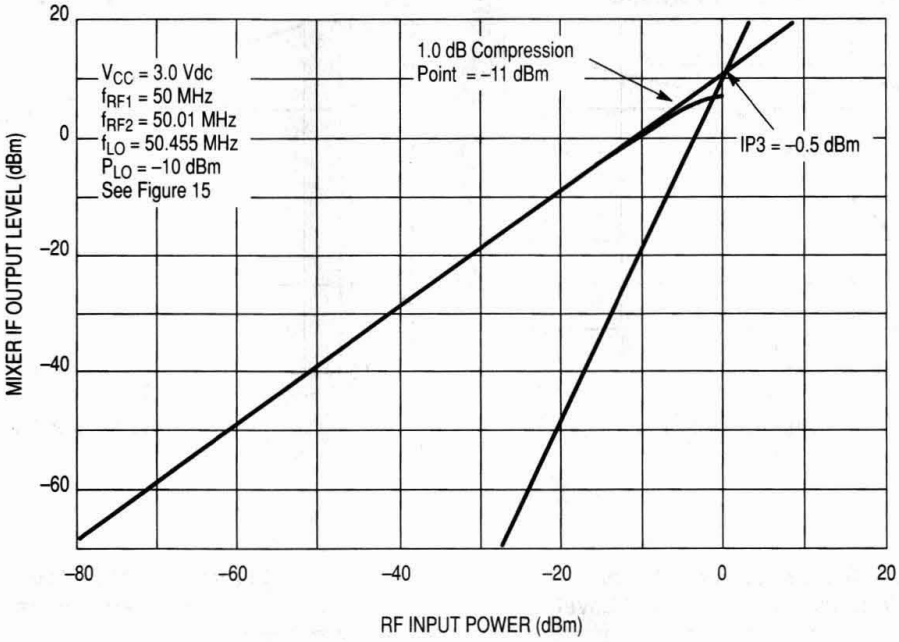


Figure 18. 1.0 dB Compression Point and Input Third Order Intercept Point versus Input Power



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 19. Supply Current, I_{VEE1} versus Signal Input Level

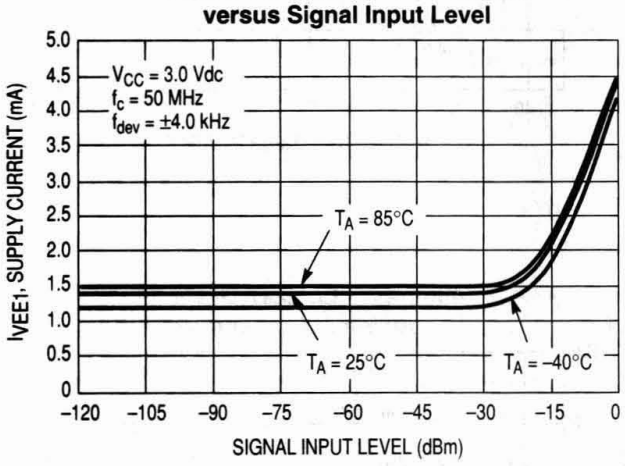
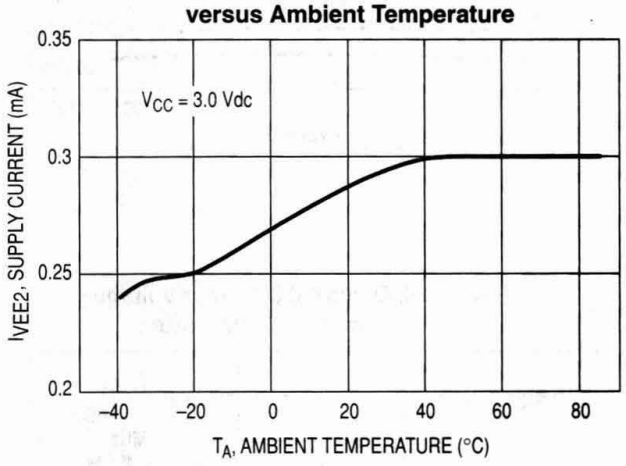


Figure 20. Supply Current, I_{VEE2} versus Ambient Temperature



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 21. Total Supply Current versus Ambient Temperature

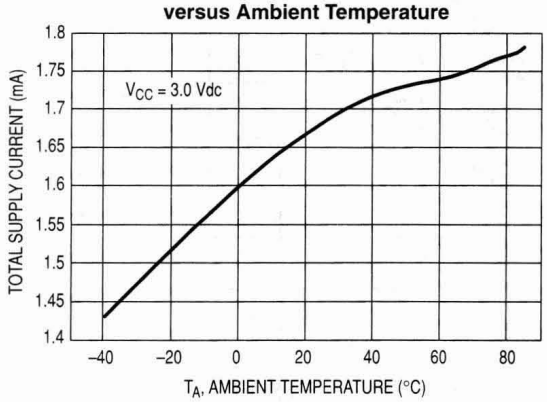


Figure 22. Minimum Supply Voltage versus Ambient Temperature

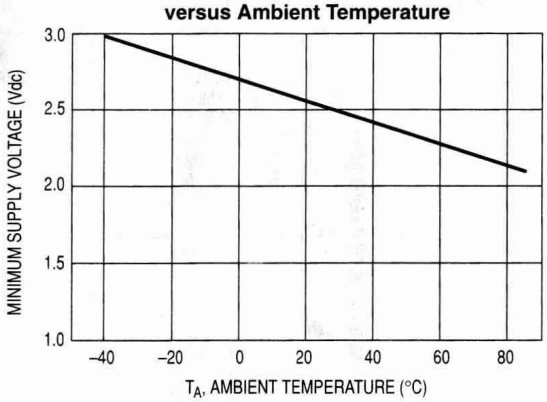


Figure 23. RSSI Current versus Ambient Temperature and Signal Level

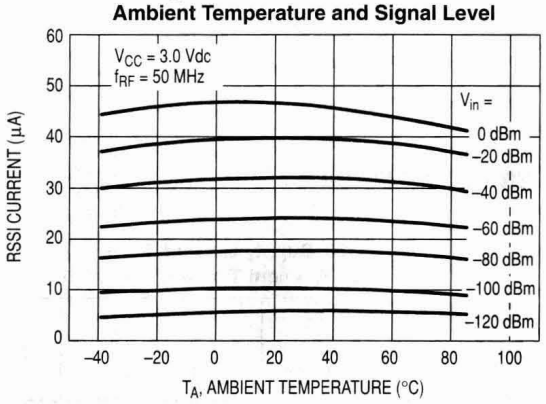


Figure 24. Recovered Audio versus Ambient Temperature

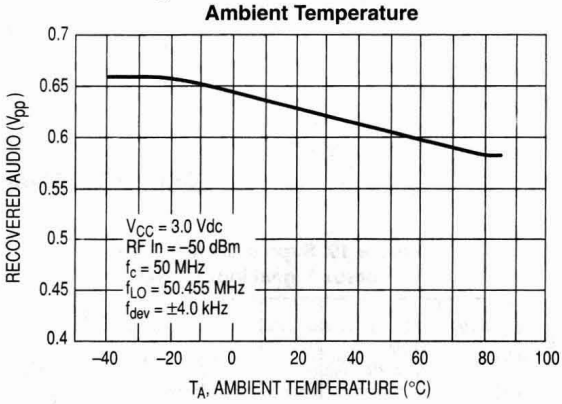


Figure 25. Demod DC Output Voltage versus Ambient Temperature

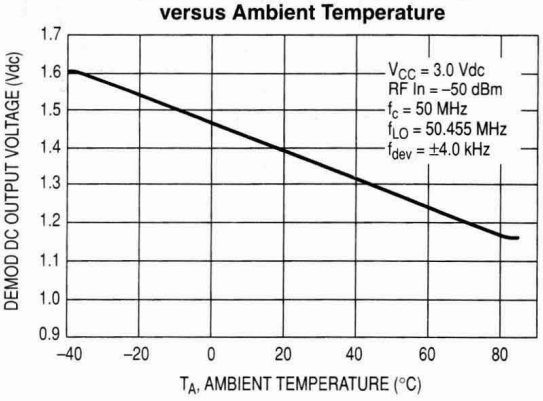


Figure 26. LO Current versus Ambient Temperature

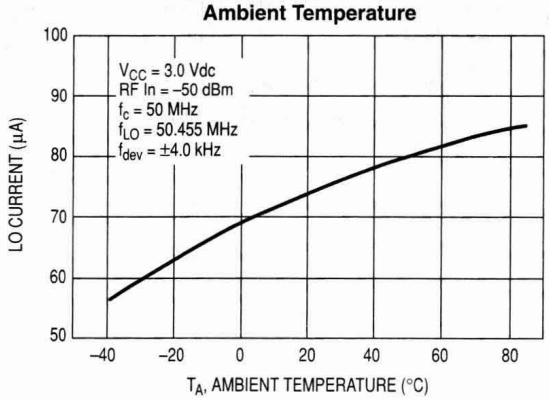


Figure 27. Component Placement View – Circuit Side

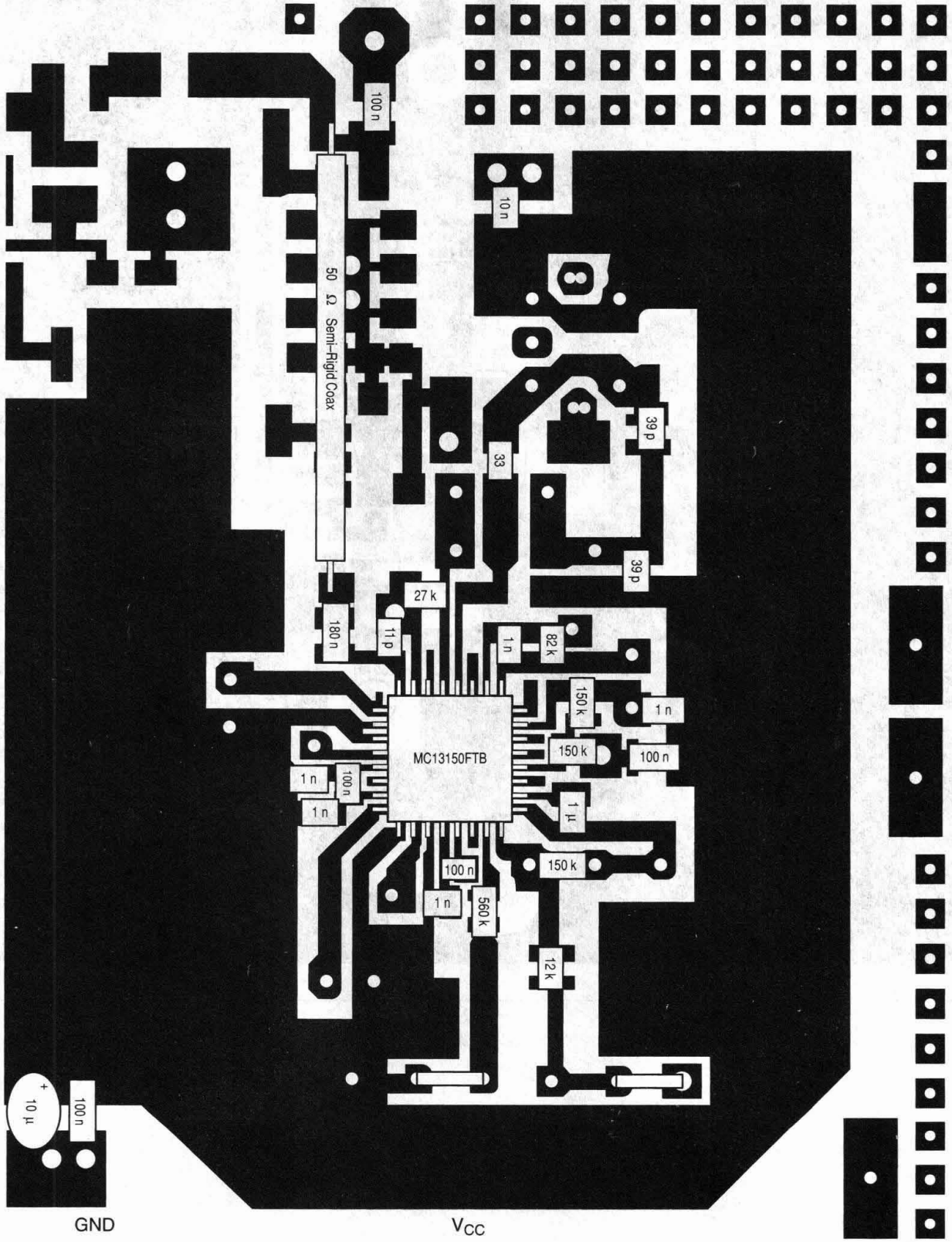


Figure 28. Component Placement View – Ground Side

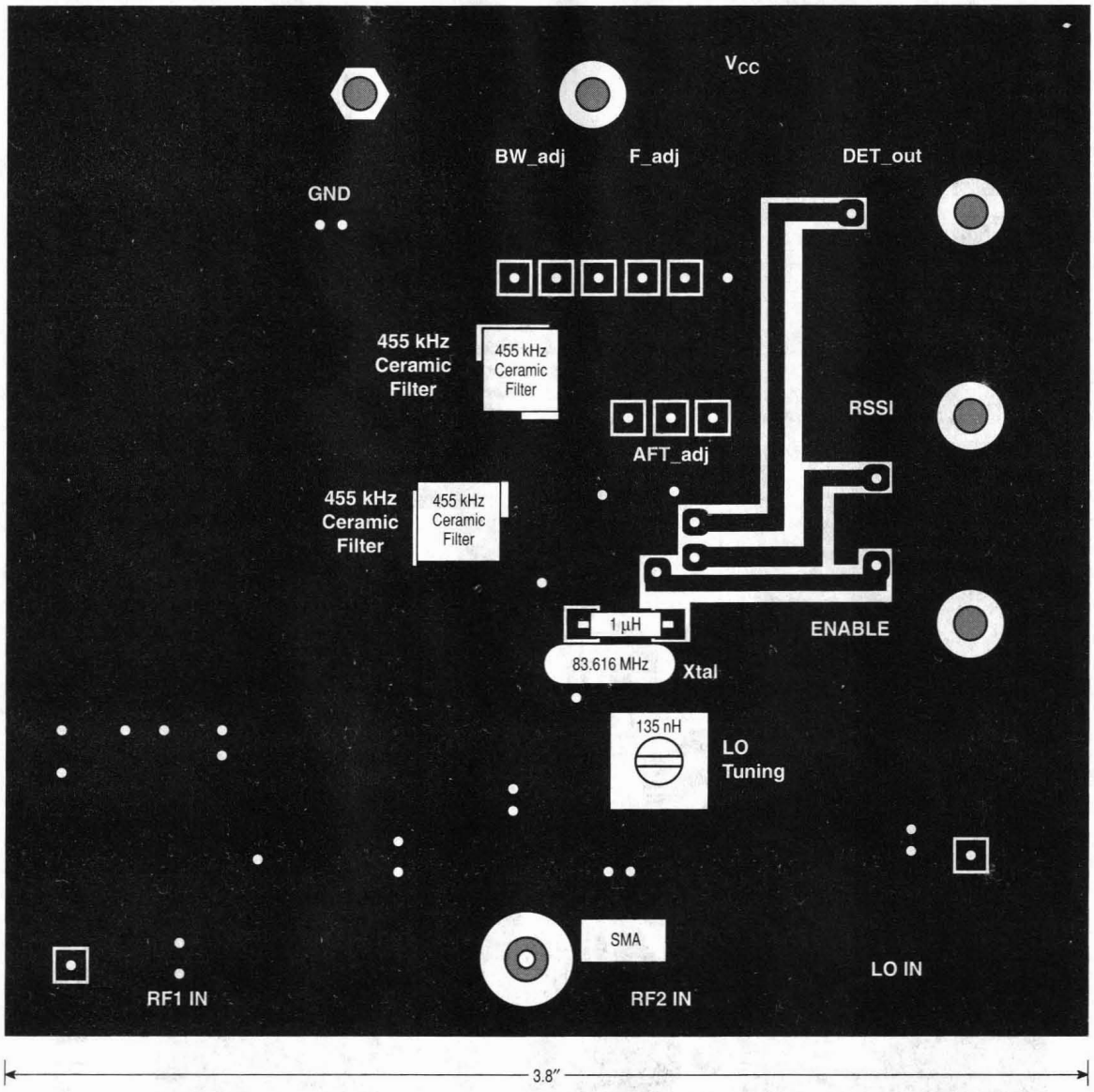


Figure 29. PCB Circuit Side View

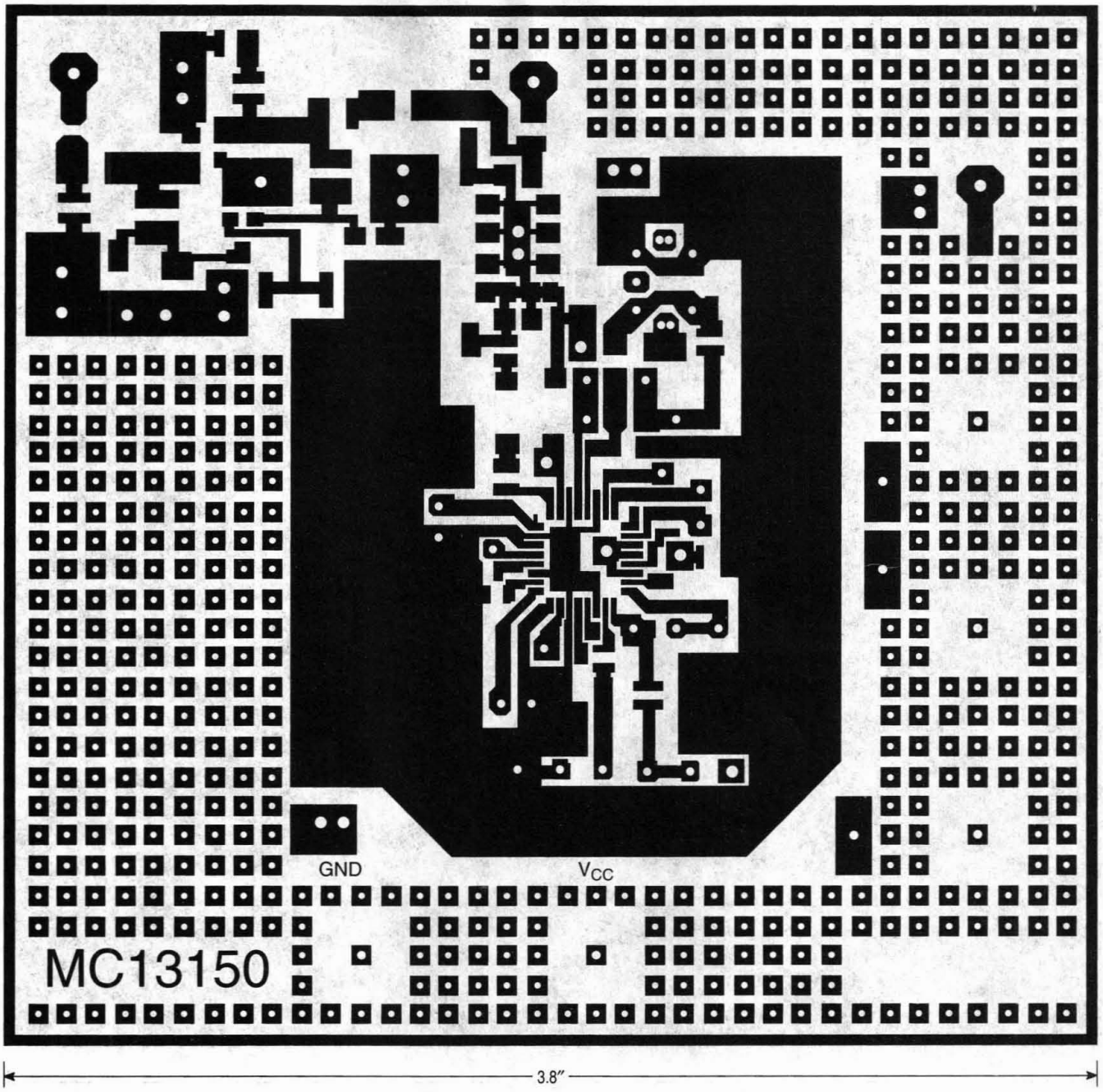
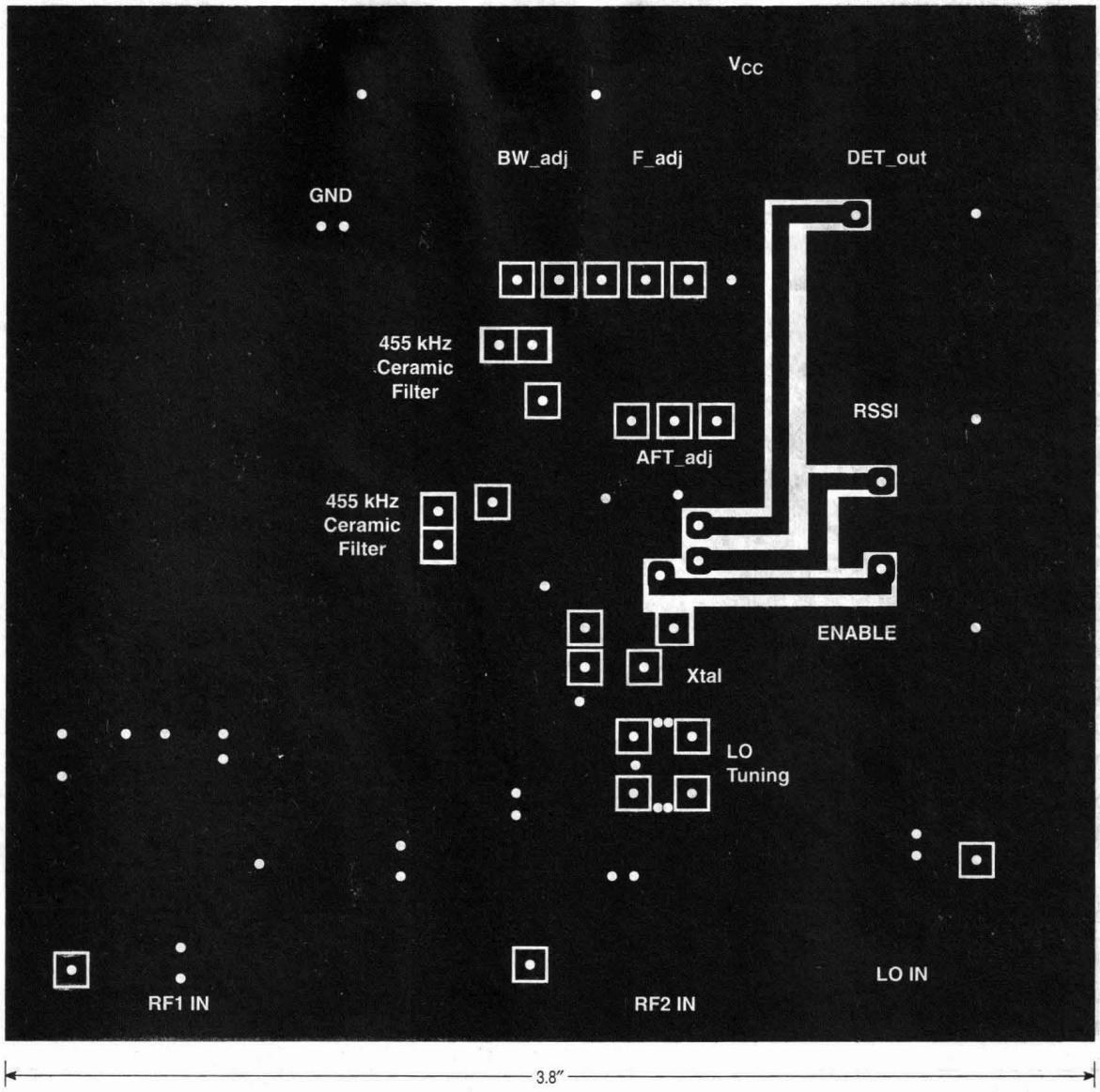


Figure 30. PCB Ground Side View



MOTOROLA

Wideband FM IF

The MC13155 is a complete wideband FM detector designed for satellite TV and other wideband data and analog FM applications. This device may be cascaded for higher IF gain and extended Receive Signal Strength Indicator (RSSI) range.

- 12 MHz Video/Baseband Demodulator
- Ideal for Wideband Data and Analog FM Systems
- Limiter Output for Cascade Operation
- Low Drain Current: 7.0 mA
- Low Supply Voltage: 3.0 to 6.0 V
- Operates to 300 MHz

MC13155

WIDEBAND FM IF

SEMICONDUCTOR TECHNICAL DATA

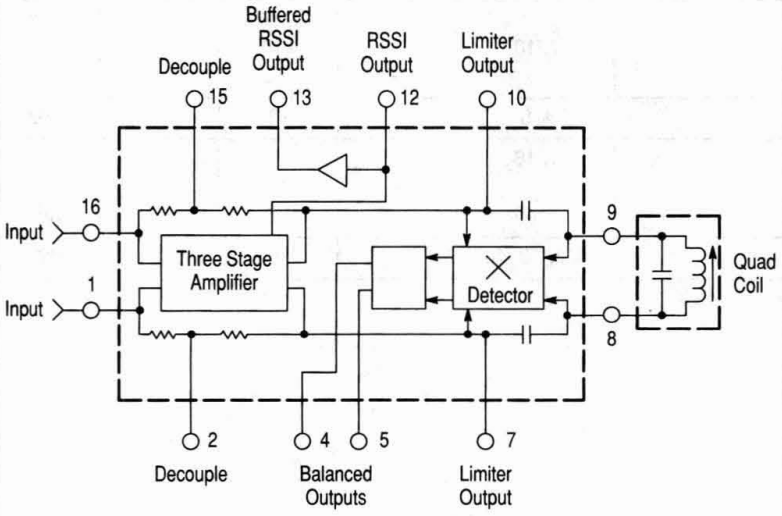
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	11, 14	V_{EE} (max)	6.5	Vdc
Input Voltage	1, 16	V_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

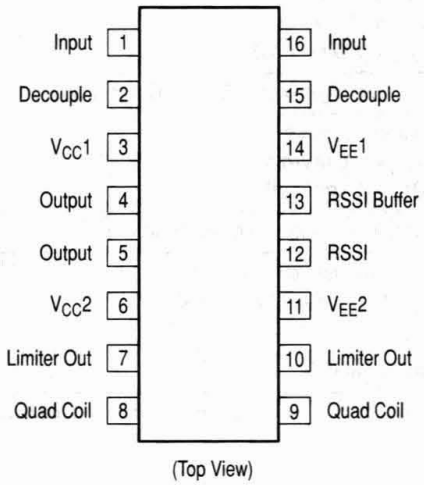
NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

Figure 1. Representative Block Diagram



NOTE: This device requires careful layout and decoupling to ensure stable operation.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13155D	T_A = – 40 to +85°C	SO–16

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (T_A= 25°C) – 40°C ≤ T_A ≤ 85°C	11, 14 3, 6	V_{EE} V_{CC}	– 3.0 to – 6.0 Grounded	Vdc
Maximum Input Frequency	1, 16	f_{in}	300	MHz
Ambient Temperature Range	–	T_J	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (V_{EE} = – 5.0 Vdc) (V_{EE} = – 5.0 Vdc)	11 14 14	I_{11} I_{14} I_{14}	2.0 3.0 3.0	2.8 4.3 4.3	4.0 6.0 6.0	mA
Drain Current Total (see Figure 3) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 3.0 Vdc)	11, 14	I_{Total}	5.0 5.0 5.0 4.7	7.1 7.5 7.5 6.6	10 10.5 10.5 9.5	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, f_{IF} = 70 MHz, V_{EE} = – 5.0 Vdc Figure 2, unless otherwise noted.)

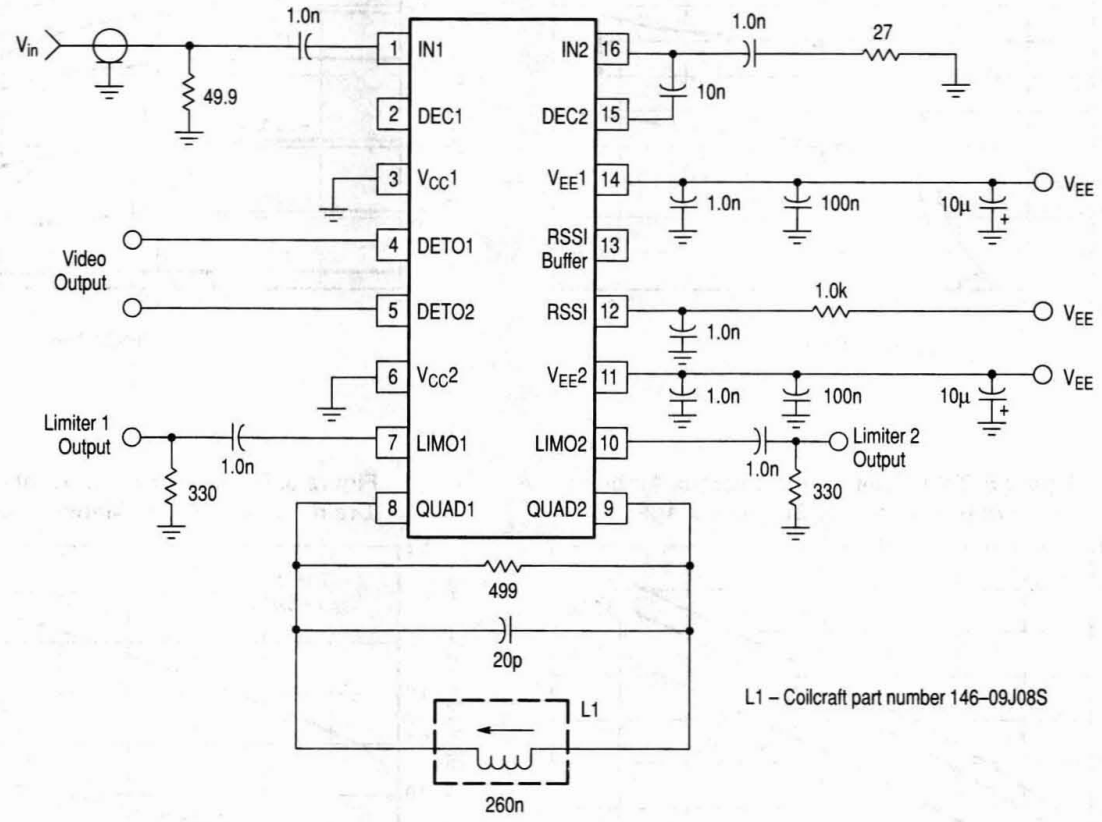
Characteristic	Pin	Min	Typ	Max	Unit
Input for – 3 dB Limiting Sensitivity	1, 16	–	1.0	2.0	mVrms
Differential Detector Output Voltage (V_{in} = 10 mVrms) (f_{dev} = ± 3.0 MHz) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 3.0 Vdc)	4, 5	 470 450 380	 590 570 500	 700 680 620	mV_{p-p}
Detector DC Offset Voltage	4, 5	– 250	–	250	mVdc
RSSI Slope	13	1.4	2.1	2.8	µA/dB
RSSI Dynamic Range	13	31	35	39	dB
RSSI Output (V_{in} = 100 µVrms) (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms) (V_{in} = 100 mVrms) (V_{in} = 500 mVrms)	12	 – – 16 – –	 2.1 2.4 24 65 75	 – – 36 – –	µA
RSSI Buffer Maximum Output Current (V_{in} = 10 mVrms)	13	–	2.3	–	mAdc
Differential Limiter Output (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms)	7, 10	100 –	140 180	– –	mVrms
Demodulator Video 3.0 dB Bandwidth	4, 5	–	12	–	MHz
Input Impedance (Figure 14) @ 70 MHz Rp (V_{EE} = – 5.0 Vdc) Cp (C_2=C_{15} = 100 p)	1, 16	 – –	 450 4.8	 – –	 Ω pF
Differential IF Power Gain	1, 7, 10, 16	–	46	–	dB

NOTE: Positive currents are out of the pins of the device.

CIRCUIT DESCRIPTION

The MC13155 consists of a wideband three–stage limiting amplifier, a wideband quadrature detector which may be operated up to 200 MHz, and a received signal strength indicator (RSSI) circuit which provides a current output linearly proportional to the IF input signal level for approximately 35 dB range of input level.

Figure 2. Test Circuit



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB shown in Figures 19 and 20 is very versatile and is designed to cascade two ICs. The center section of the board provides an area for attaching all surface mount components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 17 and 18). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Limiting Amplifier

Differential input and output ports interfacing the three stage limiting amplifier provide a differential power gain of typically 46 dB and useable frequency range of 300 MHz. The IF gain flatness may be controlled by decoupling of the internal feedback network at Pins 2 and 15.

Scattering parameter (S–parameter) characterization of the IF as a two port linear amplifier is useful to implement maximum stable power gain, input matching, and stability over a desired bandpass response and to ensure stable operation outside the bandpass as well. The MC13155 is unconditionally stable over most of its useful operating frequency range; however, it can be made unconditionally stable over its entire operating range with the proper decoupling of Pins 2 and 15. Relatively small decoupling capacitors of about 100 pF have a significant effect on the wideband response and stability. This is shown in the scattering parameter tables where S–parameters are shown for various values of C2 and C15 and at V_{EE} of – 3.0 and – 5.0 Vdc.

TYPICAL PERFORMANCE AT TEMPERATURE
(See Figure 2. Test Circuit)

Figure 3. Drain Current versus Supply Voltage

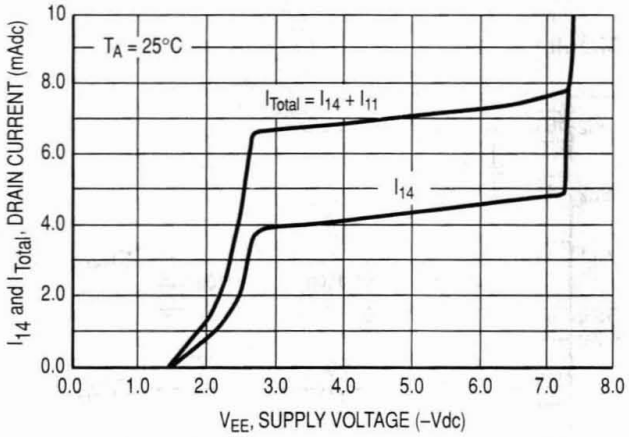


Figure 4. RSSI Output versus Frequency and Input Signal Level

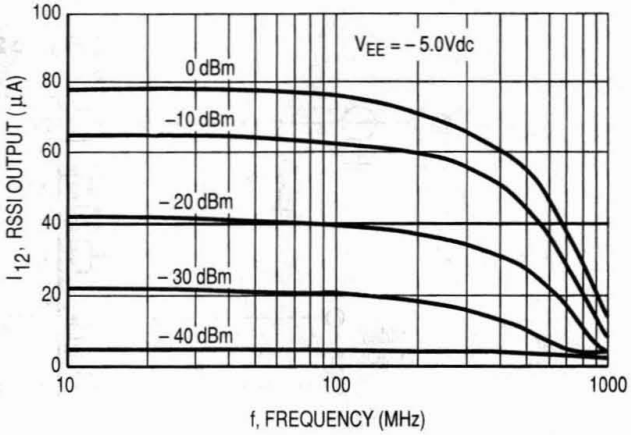


Figure 5. Total Drain Current versus Ambient Temperature and Supply Voltage

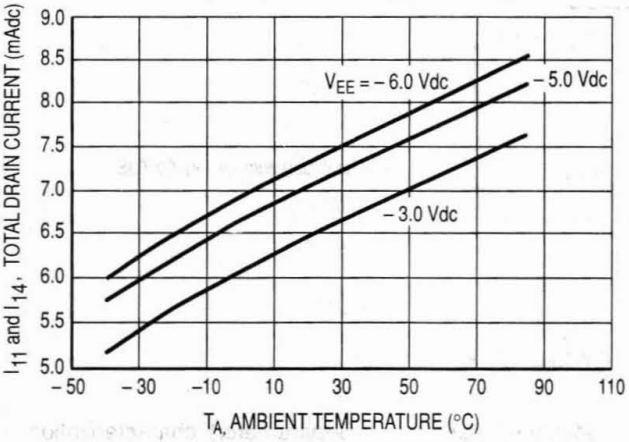


Figure 6. Detector Drain Current and Limiter Drain Current versus Ambient Temperature

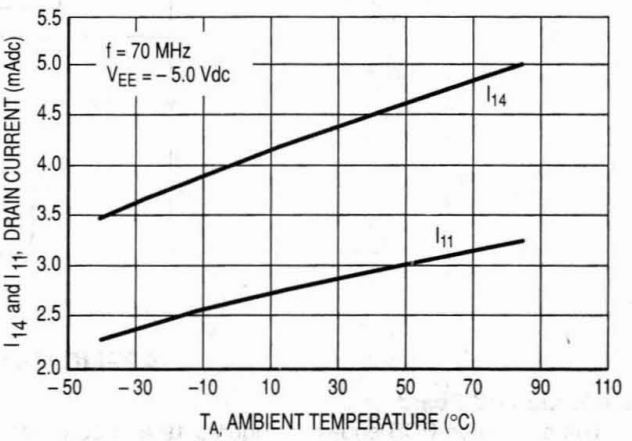


Figure 7. RSSI Output versus Ambient Temperature and Supply Voltage

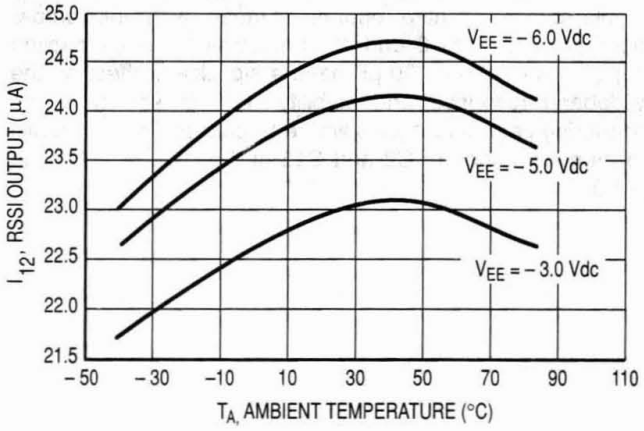


Figure 8. RSSI Output versus Input Signal Voltage (V_{in} at Temperature)

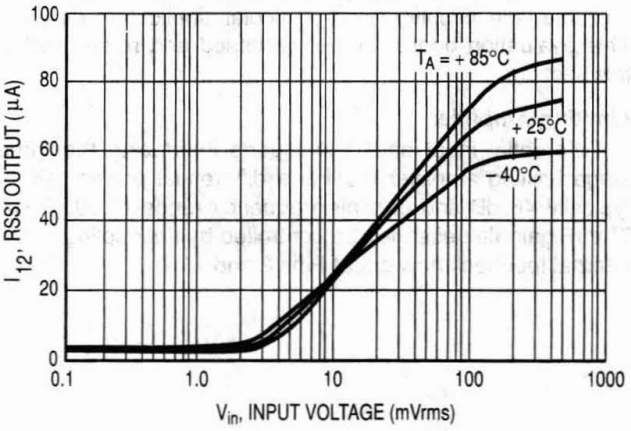


Figure 9. Differential Detector Output Voltage versus Ambient Temperature and Supply Voltage

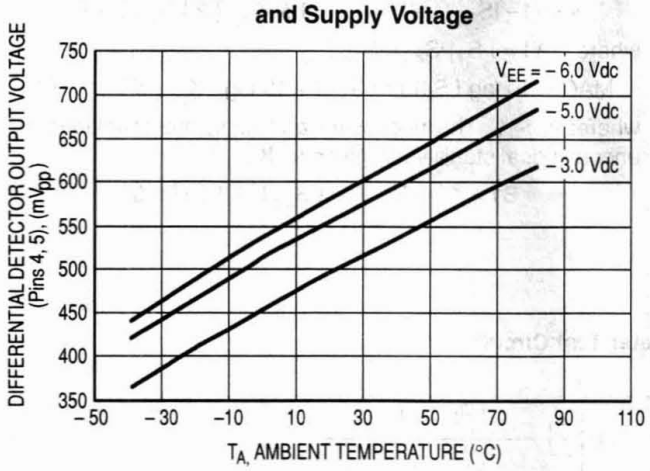


Figure 10. Differential Limiter Output Voltage versus Ambient Temperature
(V_{in} = 1 and 10 mVrms)

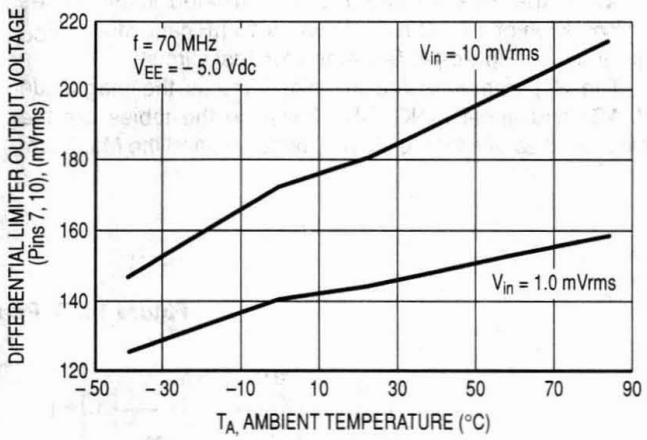


Figure 11A. Differential Detector Output Voltage versus Q of Quadrature LC Tank

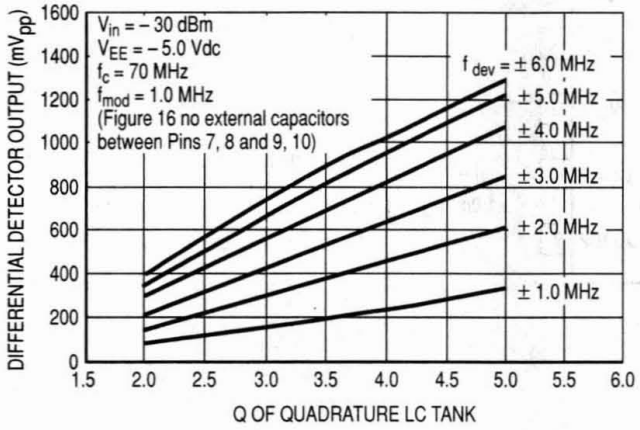


Figure 11B. Differential Detector Output Voltage versus Q of Quadrature LC Tank

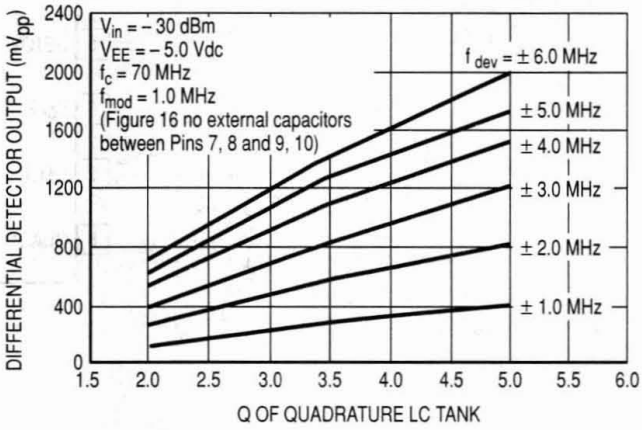


Figure 12. RSSI Output Voltage versus IF Input

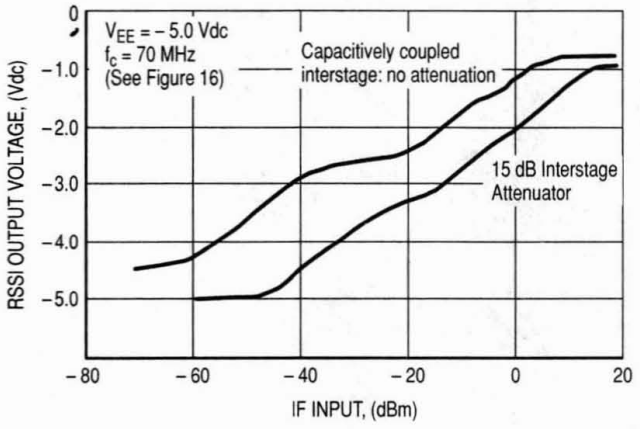
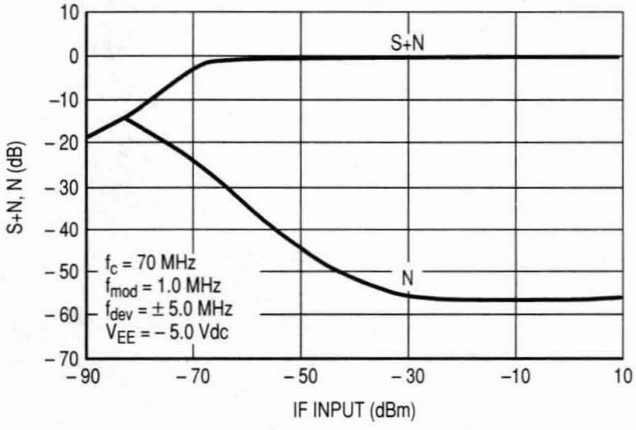


Figure 13. – S+N, N versus IF Input



In the S–parameters measurements, the IF is treated as a two–port linear class A amplifier. The IF amplifier is measured with a single–ended input and output configuration in which the Pins 16 and 7 are terminated in the series combination of a 47 Ω resistor and a 10 nF capacitor to V_{CC} ground (see Figure 14. S–Parameter Test Circuit).

The S–parameters are in polar form as the magnitude (MAG) and angle (ANG). Also listed in the tables are the calculated values for the stability factor (K) and the Maximum Available Gain (MAG). These terms are related in the following equations:

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2) / (2 |S_{12} S_{21}|)$$

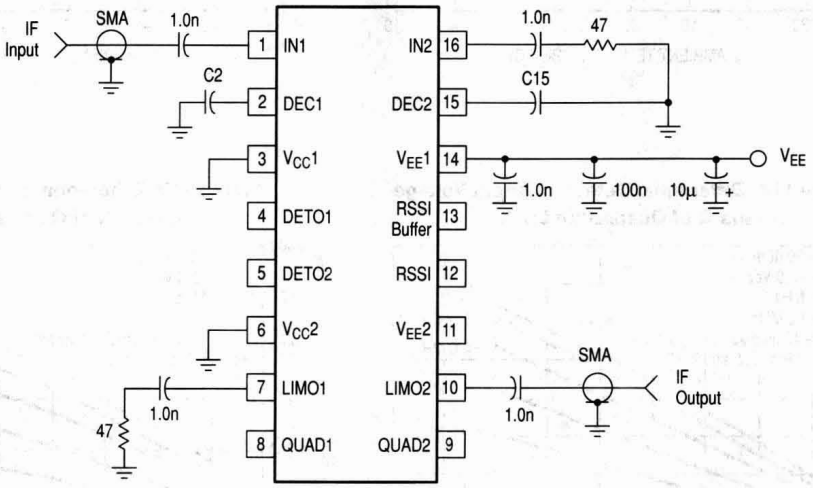
where: $|\Delta| = |S_{11} S_{22} - S_{12} S_{21}|$.

$$MAG = 10 \log |S_{21}| / |S_{12}| + 10 \log |K - (K^2 - 1)^{1/2}|$$

where: K > 1. The necessary and sufficient conditions for unconditional stability are given as K > 1:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$$

Figure 14. S–Parameter Test Circuit



S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.94	–13	8.2	143	0.001	7.0	0.87	– 22	2.2	32
2.0	0.78	– 23	23.5	109	0.001	– 40	0.64	– 31	4.2	33.5
5.0	0.48	1.0	39.2	51	0.001	– 97	0.34	–17	8.7	33.7
7.0	0.59	15	40.3	34	0.001	– 41	0.33	–13	10.6	34.6
10	0.75	17	40.9	19	0.001	– 82	0.41	–1.0	5.7	36.7
20	0.95	7.0	42.9	– 6.0	0.001	– 42	0.45	0	1.05	46.4
50	0.98	–10	42.2	– 48	0.001	– 9.0	0.52	– 3.0	0.29	–
70	0.95	–16	39.8	– 68	0.001	112	0.54	–16	1.05	46.4
100	0.93	– 23	44.2	– 93	0.001	80	0.53	– 22	0.76	–
150	0.91	– 34	39.5	–139	0.001	106	0.50	– 34	0.94	–
200	0.87	– 47	34.9	–179	0.002	77	0.42	– 44	0.97	–
500	0.89	–103	11.1	– 58	0.022	57	0.40	–117	0.75	–
700	0.61	–156	3.5	–164	0.03	0	0.52	179	2.6	13.7
900	0.56	162	1.2	92	0.048	– 44	0.47	112	4.7	4.5
1000	0.54	131	0.8	42	0.072	– 48	0.44	76	5.1	0.4

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.98	–15	11.7	174	0.001	–14	0.84	– 27	1.2	37.4
2.0	0.50	– 2.0	39.2	85.5	0.001	–108	0.62	– 35	6.0	35.5
5.0	0.87	8.0	39.9	19	0.001	100	0.47	– 9.0	4.2	39.2
7.0	0.90	5.0	40.4	9.0	0.001	– 40	0.45	– 8.0	3.1	40.3
10	0.92	3.0	41	1.0	0.001	– 40	0.44	– 5.0	2.4	41.8
20	0.92	– 2.0	42.4	–14	0.001	– 87	0.49	– 6.0	2.4	41.9
50	0.91	– 8.0	41.2	– 45	0.001	85	0.50	– 5.0	2.3	42
70	0.91	–11	39.1	– 63	0.001	76	0.52	– 4.0	2.2	41.6
100	0.91	–15	43.4	– 84	0.001	85	0.50	–11	1.3	43.6
150	0.90	– 22	38.2	–126	0.001	96	0.43	– 22	1.4	41.8
200	0.86	– 33	35.5	–160	0.002	78	0.43	– 21	1.3	39.4
500	0.80	– 66	8.3	– 9.0	0.012	75	0.57	– 63	1.7	23.5
700	0.62	– 96	2.9	– 95	0.013	50	0.49	–111	6.3	12.5
900	0.56	–120	1.0	–171	0.020	53	0.44	–150	13.3	2.8
1000	0.54	–136	0.69	154	0.034	65	0.44	–179	12.5	– 0.8

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.74	4.0	53.6	110	0.001	101	0.97	– 35	0.58	–
2.0	0.90	3.0	70.8	55	0.001	60	0.68	– 34	1.4	45.6
5.0	0.91	0	87.1	21	0.001	–121	0.33	– 60	1.1	49
7.0	0.91	0	90.3	11	0.001	–18	0.25	– 67	1.2	48.4
10	0.91	– 2.0	92.4	2.0	0.001	33	0.14	– 67	1.5	47.5
20	0.91	– 4.0	95.5	–16	0.001	63	0.12	–15	1.3	48.2
50	0.90	– 8.0	89.7	– 50	0.001	– 43	0.24	26	1.8	46.5
70	0.90	–10	82.6	–70	0.001	92	0.33	21	1.4	47.4
100	0.91	–14	77.12	–93	0.001	23	0.42	–1.0	1.05	49
150	0.94	– 20	62.0	–122	0.001	96	0.42	– 22	0.54	–
200	0.95	– 33	56.9	–148	0.003	146	0.33	– 62	0.75	–
500	0.82	– 63	12.3	–12	0.007	79	0.44	– 67	1.8	26.9
700	0.66	– 98	3.8	–107	0.014	84	0.40	–115	4.8	14.6
900	0.56	–122	1.3	177	0.028	78	0.39	–166	8.0	4.7
1000	0.54	–139	0.87	141	0.048	76	0.41	165	7.4	0.96

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.89	–14	9.3	136	0.001	2.0	0.84	– 27	3.2	30.7
2.0	0.76	– 22	24.2	105	0.001	– 90	0.67	– 37	3.5	34.3
5.0	0.52	5.0	35.7	46	0.001	– 32	0.40	–13	10.6	33.3
7.0	0.59	12	38.1	34	0.001	– 41	0.40	–10	9.1	34.6
10	0.78	15	37.2	16	0.001	– 92	0.40	–1.0	5.7	36.3
20	0.95	5.0	38.2	– 9.0	0.001	47	0.51	– 4.0	0.94	–
50	0.96	–11	39.1	– 50	0.001	–103	0.48	– 6.0	1.4	43.7
70	0.93	–17	36.8	– 71	0.001	– 76	0.52	–13	2.2	41.4
100	0.91	– 25	34.7	– 99	0.001	–152	0.51	–19	3.0	39.0
150	0.86	– 37	33.8	–143	0.001	53	0.49	– 34	1.7	39.1
200	0.81	– 49	27.8	86	0.003	76	0.55	– 56	2.4	35.1
500	0.70	– 93	6.2	– 41	0.015	93	0.40	–110	2.4	19.5
700	0.62	–144	1.9	–133	0.049	56	0.40	–150	3.0	8.25
900	0.39	–176	0.72	125	0.11	–18	0.25	163	5.1	–1.9
1000	0.44	166	0.49	80	0.10	– 52	0.33	127	7.5	– 4.8

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.97	–15	11.7	171	0.001	– 4.0	0.84	– 27	1.4	36.8
2.0	0.53	2.0	37.1	80	0.001	– 91	0.57	– 31	6.0	34.8
5.0	0.88	7.0	37.7	18	0.001	– 9.0	0.48	– 7.0	3.4	39.7
7.0	0.90	5.0	37.7	8.0	0.001	–11	0.49	– 7.0	2.3	41
10	0.92	2.0	38.3	1.0	0.001	– 59	0.51	– 9.0	2.0	41.8
20	0.92	– 2.0	39.6	–15	0.001	29	0.48	– 3.0	1.9	42.5
50	0.91	– 8.0	38.5	– 46	0.001	– 21	0.51	– 7.0	2.3	41.4
70	0.91	–11	36.1	– 64	0.001	49	0.50	– 8.0	2.3	40.8
100	0.91	–15	39.6	– 85	0.001	114	0.52	–13	1.7	37.8
150	0.89	– 22	34.4	–128	0.001	120	0.48	– 23	1.6	40.1
200	0.86	– 33	32	–163	0.002	86	0.40	– 26	1.7	37.8
500	0.78	– 64	7.6	–12	0.013	94	0.46	– 71	1.9	22.1
700	0.64	– 98	2.3	–102	0.027	58	0.42	–109	4.1	10.1
900	0.54	–122	0.78	179	0.040	38.6	0.35	–147	10.0	– 0.14
1000	0.53	–136	0.47	144	0.043	23	0.38	–171	15.4	– 4.52

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.81	3.0	37	101	0.001	–19	0.90	– 32	1.1	43.5
2.0	0.90	2.0	47.8	52.7	0.001	– 82	0.66	– 39	0.72	–
5.0	0.91	0	58.9	20	0.001	104	0.37	– 56	2.3	44
7.0	0.90	–1	60.3	11	0.001	– 76	0.26	– 55	2.04	44
10	0.91	– 2.0	61.8	3.0	0.001	105	0.18	– 52	2.2	43.9
20	0.91	– 4.0	63.8	– 15	0.001	59	0.11	–13	2.0	44.1
50	0.90	– 8.0	60.0	– 48	0.001	96	0.22	33	2.3	43.7
70	0.90	–11	56.5	– 67	0.001	113	0.29	15	2.3	43.2
100	0.91	–14	52.7	– 91	0.001	177	0.36	5.0	2.0	43
150	0.93	– 21	44.5	–126	0.001	155	0.35	–17	1.8	42.7
200	0.90	– 43	41.2	–162	0.003	144	0.17	– 31	1.6	34.1
500	0.79	– 65	7.3	–13	0.008	80	0.44	– 75	3.0	22
700	0.65	– 97	2.3	–107	0.016	86	0.38	–124	7.1	10.2
900	0.56	–122	0.80	174	0.031	73	0.38	–174	12	0.37
1000	0.55	–139	0.52	137	0.50	71	0.41	157	11.3	– 3.4

DC Biasing Considerations

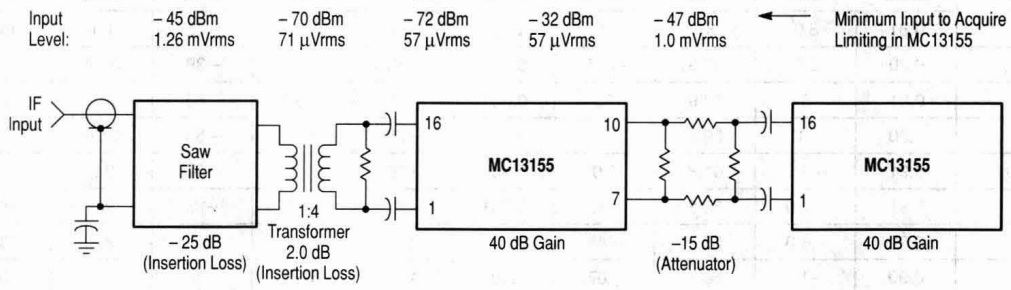
The DC biasing scheme utilizes two V_{CC} connections (Pins 3 and 6) and two V_{EE} connections (Pins 14 and 11). $V_{EE}1$ (Pin 14) is connected internally to the IF and RSSI circuits' negative supply bus while $V_{EE}2$ (Pin 11) is connected internally to the quadrature detector's negative bus. Under positive ground operation, this unique configuration offers the ability to bias the RSSI and IF separately from the quadrature detector. When two ICs are cascaded as shown in the 70 MHz application circuit and provided by the PCB (see Figures 17 and 18), the first MC13155 is used without biasing its quadrature detector, thereby saving approximately 3.0 mA. A total current of 7.0 mA is used to fully bias each IC, thus the total current in the application circuit is approximately 11 mA. Both V_{CC} pins are biased by the same supply. $V_{CC}1$ (Pin 3) is connected internally to the positive bus of the first half of the IF limiting amplifier, while $V_{CC}2$ is internally connected to the positive bus of the RSSI, the quadrature detector circuit, and the second half of the IF limiting amplifier (see Figure 15). This distribution of the V_{CC} enhances the stability of the IC.

RSSI Circuitry

The RSSI circuitry provides typically 35 dB of linear dynamic range and its output voltage swing is adjusted by selection of the resistor from Pin 12 to V_{EE}. The RSSI slope is typically 2.1 μA/dB ; thus, for a dynamic range of 35 dB, the current output is approximately 74 μA. A 47 k resistor will yield an RSSI output voltage swing of 3.5 Vdc. The RSSI buffer output at Pin 13 is an emitter–follower and needs an external emitter resistor of 10 k to V_{EE}.

In a cascaded configuration (see circuit application in Figure 16), only one of the RSSI Buffer outputs (Pin 13) is used; the RSSI outputs (Pin 12 of each IC) are tied together and the one closest to the V_{EE} supply trace is decoupled to V_{CC} ground. The two pins are connected to V_{EE} through a 47 k resistor. This resistor sources a RSSI current which is proportional to the signal level at the IF input; typically, 1.0 mVrms (– 47 dBm) is required to place the MC13155 into limiting. The measured RSSI output voltage response of the application circuit is shown in Figure 12. Since the RSSI current output is dependent upon the input signal level at the IF input, a careful accounting of filter losses, matching and other losses and gains must be made in the entire receiver system. In the block diagram of the application circuit shown below, an accounting of the signal levels at points throughout the system shows how the RSSI response in Figure 12 is justified.

Block Diagram of 70 MHz Video Receiver Application Circuit

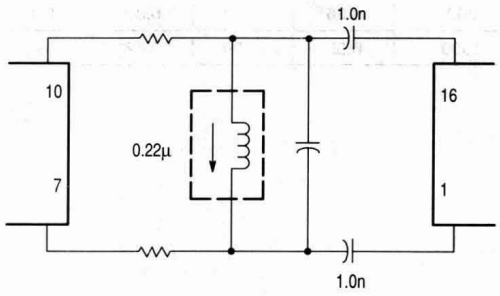


Cascading Stages

The limiting IF output is pinned–out differentially, cascading is easily achieved by AC coupling stage to stage. In the evaluation PCB, AC coupling is shown, however, interstage filtering may be desirable in some applications. In which case, the S–parameters provide a means to implement a low loss interstage match and better receiver sensitivity.

Where a linear response of the RSSI output is desired when cascading the ICs, it is necessary to provide at least 10 dB of interstage loss. Figure 12 shows the RSSI response with and without interstage loss. A 15 dB resistive attenuator is an inexpensive way to linearize the RSSI response. This has its drawbacks since it is a wideband noise source that is dependent upon the source and load impedance and the amount of attenuation that it provides. A better, although more costly, solution would be a bandpass filter designed to the desired center frequency and bandpass response while carefully selecting the insertion loss. A network topology shown below may be used to provide a bandpass response with the desired insertion loss.

Network Topology



Quadrature Detector

The quadrature detector is coupled to the IF with internal 2.0 pF capacitors between Pins 7 and 8 and Pins 9 and 10. For wideband data applications, such as FM video and satellite receivers, the drive to the detector can be increased with additional external capacitors between these pins, thus, the recovered video signal level output is increased for a given bandwidth (see Figure 11A and Figure 11B).

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \quad (1)$$

where: R_T is the equivalent shunt resistance across the LC Tank and X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC Tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by:

$$fc = (2\pi \sqrt{(LC_p)})^{-1} \quad (2)$$

where: L is the parallel tank inductor and C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 70 MHz and a loaded Q of 5. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 70 MHz and an IF bandpass of 10.9 MHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 20 pF. (The minimum value here should be greater than 15 pF making it greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF).

$$C_p = Cint + Cext = 23\ pF$$

Rewrite Equation 2 and solve for L:

$L = (0.159)^2 /(C_p\ fc^2)$

L = 198 nH, thus, a standard value is chosen.

L = 0.22 μH (tunable shielded inductor).

The value of the total damping resistor to obtain the required loaded Q of 5 can be calculated by rearranging Equation 1:

$$R_T = Q(2\pi fL)$$

$R_T = 5\ (2\pi)(70)(0.22) = 483.8\ \Omega.$

The internal resistance, Rint between the quadrature tank Pins 8 and 9 is approximately 3200 Ω and is considered in determining the external resistance, Rext which is calculated from:

Rext = $((R_T)(Rint))/\ (Rint - R_T)$

Rext = 570, thus, choose the standard value.

Rext = 560 Ω.

SAW Filter

In wideband video data applications, the IF occupied bandwidth may be several MHz wide. A good rule of thumb is to choose the IF frequency about 10 or more times greater than the IF occupied bandwidth. The IF bandpass filter is a SAW filter in video data applications where a very selective response is needed (i.e., very sharp bandpass response). The evaluation PCB is laid out to accommodate two SAW filter package types: 1) A five–leaded plastic SIP package. Recommended part numbers are Siemens X6950M which operates at 70 MHz; 10.4 MHz 3 dB passband, X6951M (X252.8) which operates at 70 MHz; 9.2 MHz 3 dB passband; and X6958M which operates at 70 MHz, 6.3 MHz 3 dB passband, and 2) A four–leaded TO–39 metal can package. Typical insertion loss in a wide bandpass SAW filter is 25 dB.

The above SAW filters require source and load impedances of 50 Ω to assure stable operation. On the PC board layout, space is provided to add a matching network, such as a 1:4 surface mount transformer between the SAW filter output and the input to the MC13155. A 1:4 transformer, made by Coilcraft and Mini Circuits, provides a suitable interface (see Figures 16, 17 and 18). In the circuit and layout, the SAW filter and the MC13155 are differentially configured with interconnect traces which are equal in length and symmetrical. This balanced feed enhances RF stability, phase linearity, and noise performance.

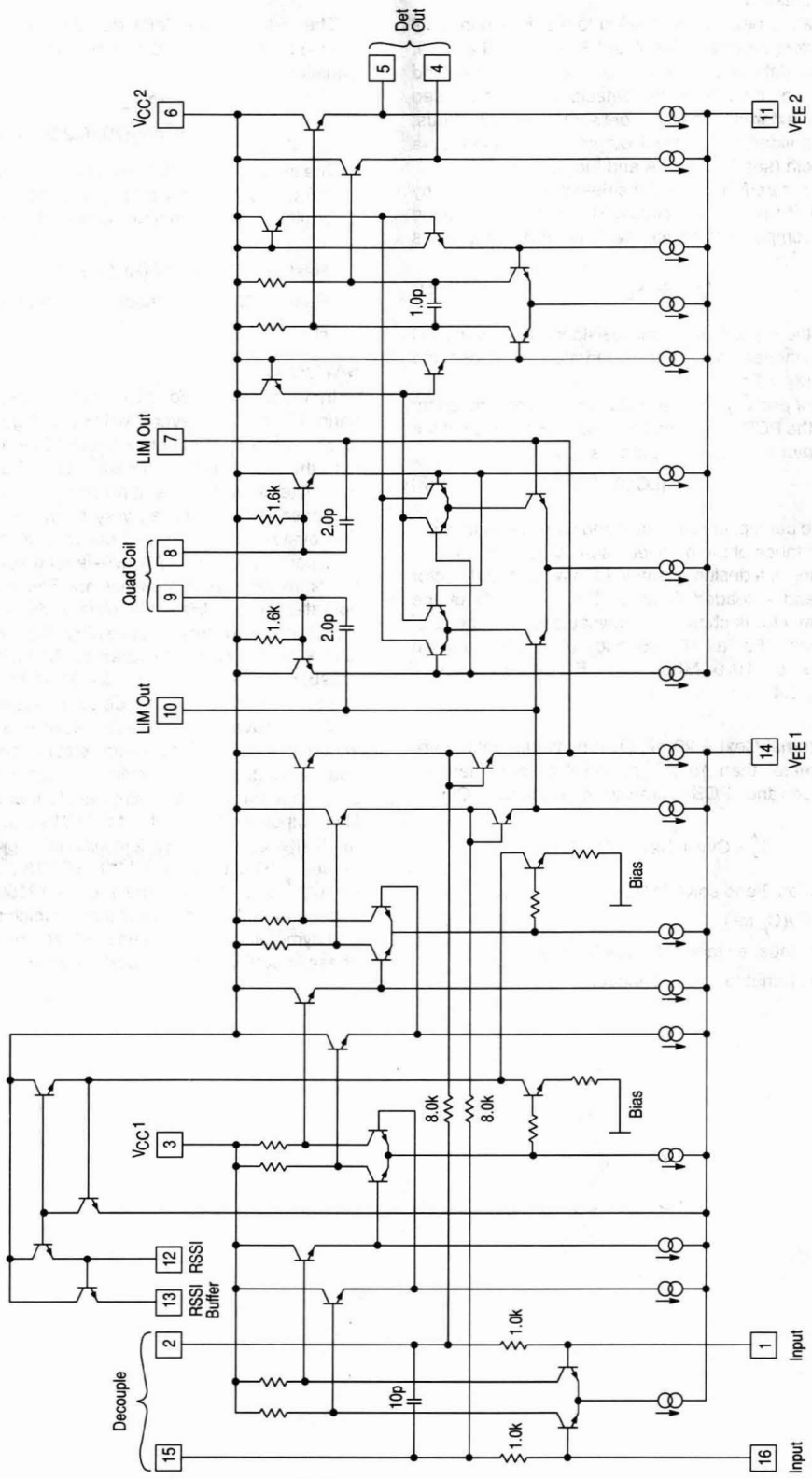


Figure 15. Simplified Internal Circuit Schematic

Figure 16. 70 MHz Video Receiver Application Circuit

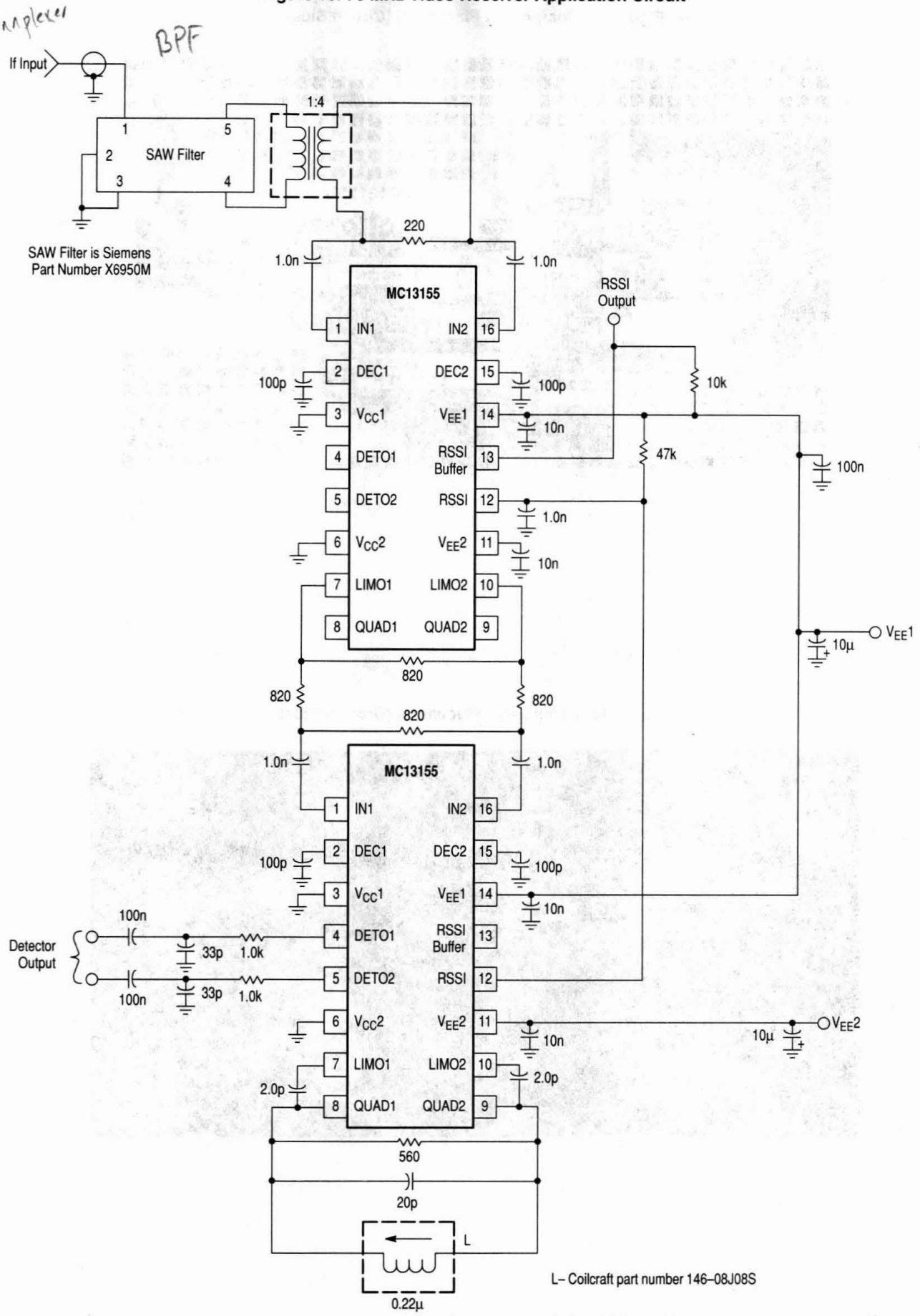


Figure 17. Component Placement (Circuit Side)

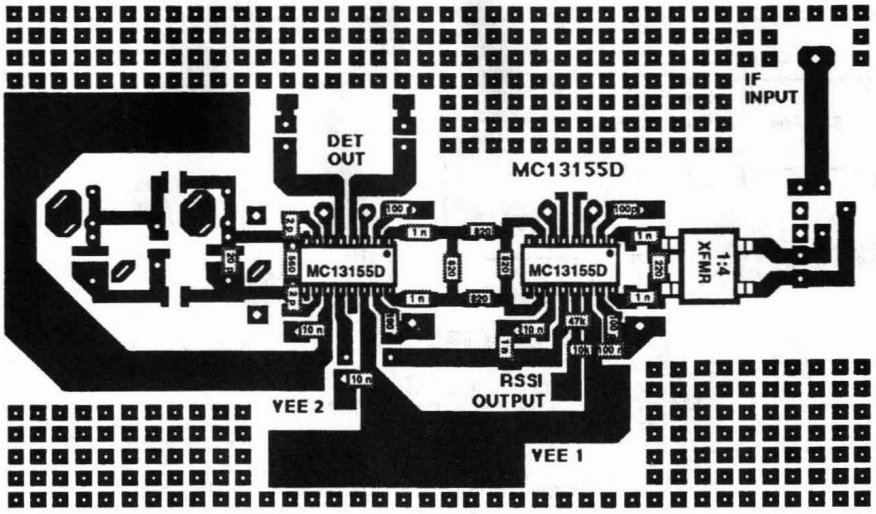


Figure 18. Component Placement (Ground Side)

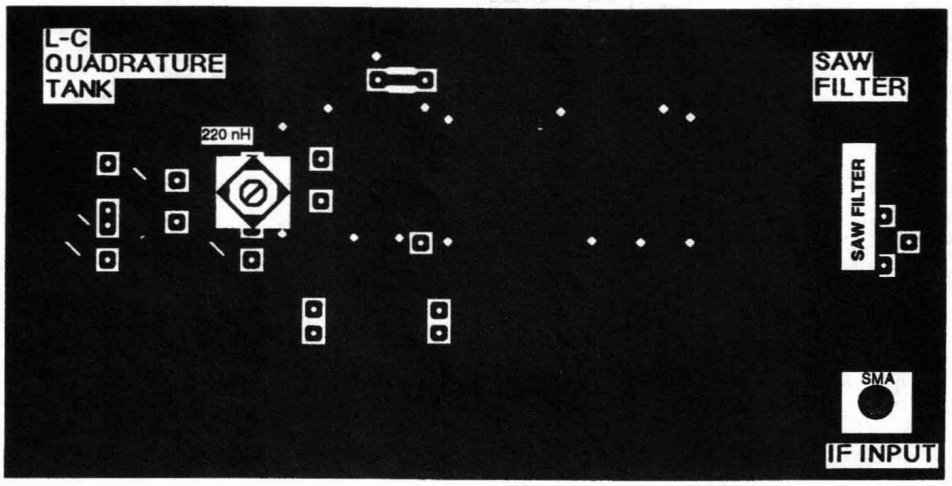


Figure 19. Circuit Side View

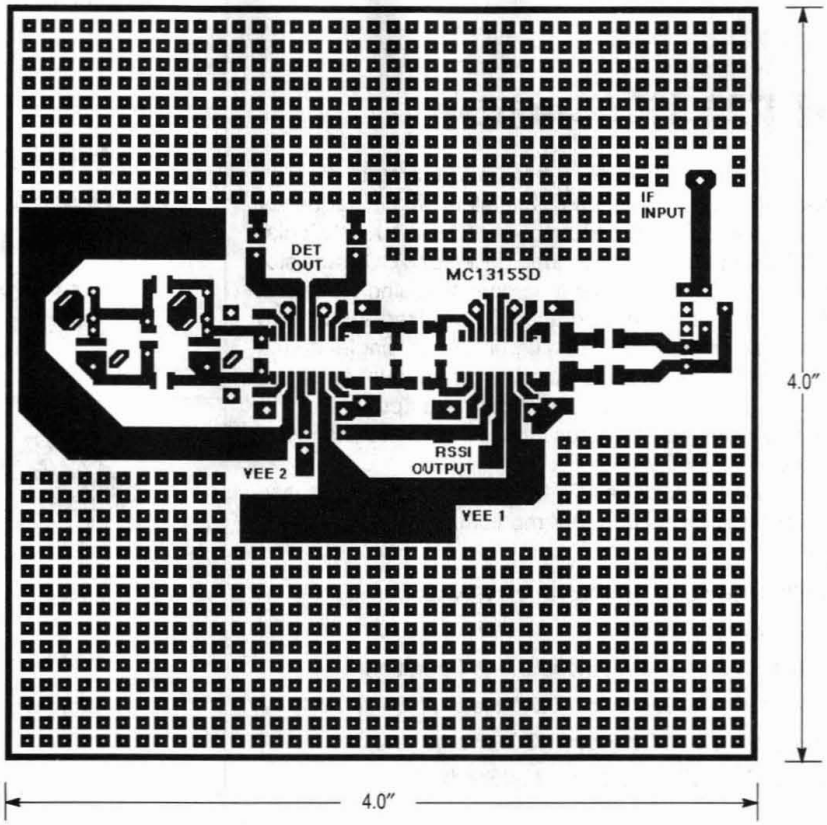
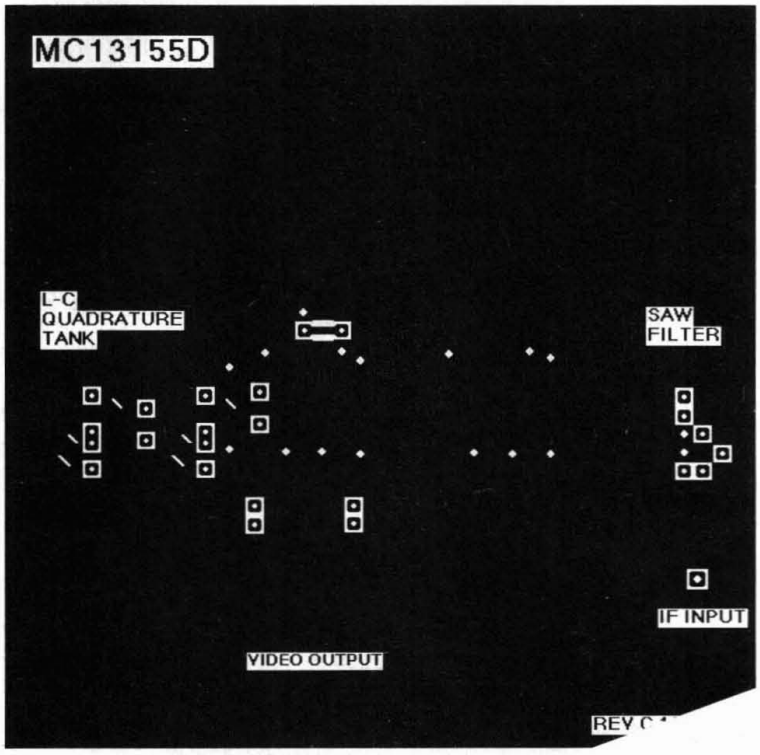


Figure 20. Ground Side View



MOTOROLA

MC13156

Wideband FM IF System

WIDEBAND FM IF SYSTEM FOR DIGITAL AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved at low cost using Motorola's MOSAIC 1.5™ bipolar process. The MC13156 has an onboard grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multichannel operation. The mixer is useful to 500 MHz and may be used in a balanced–differential, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

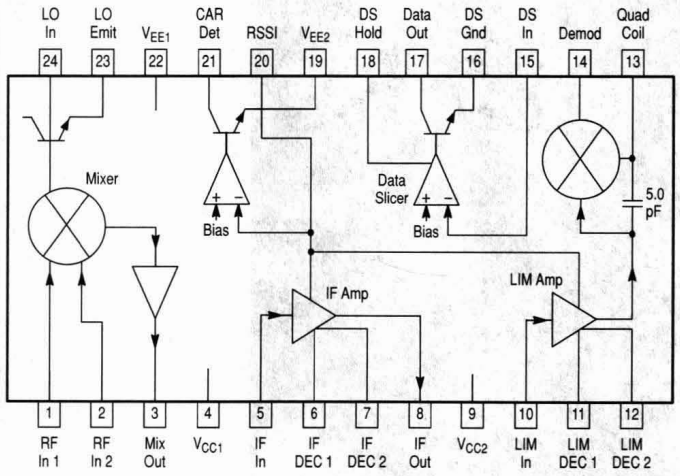
Applications for the MC13156 include CT–2, wideband data links and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity at 200 MHz of 2.0 μV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 330 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range
- 3rd Order Intercept (Input) of –25 dBm (Input Matched)

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

FB SUFFIX
PLASTIC QFP PACKAGE
CASE 873

Simplified Block Diagram



NOTE: Pin Numbers shown for SOIC package only. Refer to Pin Assignments Table.

This device contains 197 active transistors.

PIN CONNECTIONS

Function	SO–24L	QFP
RF Input 1	1	31
RF Input 2	2	32
Mixer Output	3	1
V_{CC1}	4	2
IF Amp Input	5	3
IF Amp Decoupling 1	6	4
IF Amp Decoupling 2	7	5
V_{CC} Connect (N/C Internal)	–	6
IF Amp Output	8	7
V_{CC2}	9	8
Limiter IF Input	10	9
Limiter Decoupling 1	11	10
Limiter Decoupling 2	12	11
V_{CC} Connect (N/C Internal)	–	12, 13, 14
Quad Coil	13	15
Demodulator Output	14	16
Data Slicer Input	15	17
V_{CC} Connect (N/C Internal)	–	18
Data Slicer Ground	16	19
Data Slicer Output	17	20
Data Slicer Hold	18	21
V_{EE2}	19	22
RSSI Output/Carrier Detect In	20	23
Carrier Detect Output	21	24
V_{EE1} and Substrate	22	25
LO Emitter	23	26
LO Base	24	27
V_{CC} Connect (N/C Internal)	–	28, 29, 30

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13156DW	T_A = –40 to +85°C	SO–24L
MC13156FB		QFP

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 19, 22	$V_{EE(max)}$	–6.5	Vdc
Junction Temperature	–	$T_{J(max)}$	150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" table provides for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage @ T_A = 25°C –40°C ≤ T_A ≤ +85°C	4, 9 16, 19, 22	V_{CC} V_{EE}	0 (Ground) –2.0 to –6.0	Vdc
Input Frequency	1, 2	f_{in}	500	MHz
Ambient Temperature Range	–	T_A	–40 to +85	°C
Input Signal Level	1, 2	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 0, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	19, 22	I_{Total}				mA
V_{EE} = –2.0 Vdc			–	4.8	–	
V_{EE} = –3.0 Vdc			3.0	5.0	8.0	
V_{EE} = –5.0 Vdc			–	5.2	–	
V_{EE} = –6.0 Vdc			–	5.4	–	
Drain Current, I_{22} (See Figure 3)	22	I_{22}				mA
V_{EE} = –2.0 Vdc			–	3.0	–	
V_{EE} = –3.0 Vdc			–	3.1	–	
V_{EE} = –5.0 Vdc			–	3.3	–	
V_{EE} = –6.0 Vdc			–	3.4	–	
Drain Current, I_{19} (See Figure 3)	19	I_{19}				mA
V_{EE} = –2.0 Vdc			–	1.8	–	
V_{EE} = –3.0 Vdc			–	1.9	–	
V_{EE} = –5.0 Vdc			–	1.9	–	
V_{EE} = –6.0 Vdc			–	2.0	–	

DATA SLICER (Input Voltage Referenced to V_{EE} = –3.0 Vdc, no input signal; See Figure 15.)

Input Threshold Voltage (High V_{in})	15	V_{15}	1.0	1.1	1.2	Vdc
Output Current (Low V_{in}) Data Slicer Enabled (No Hold) V_{15} > 1.1 Vdc V_{18} = 0 Vdc	17	I_{17}	–	1.7	–	mA

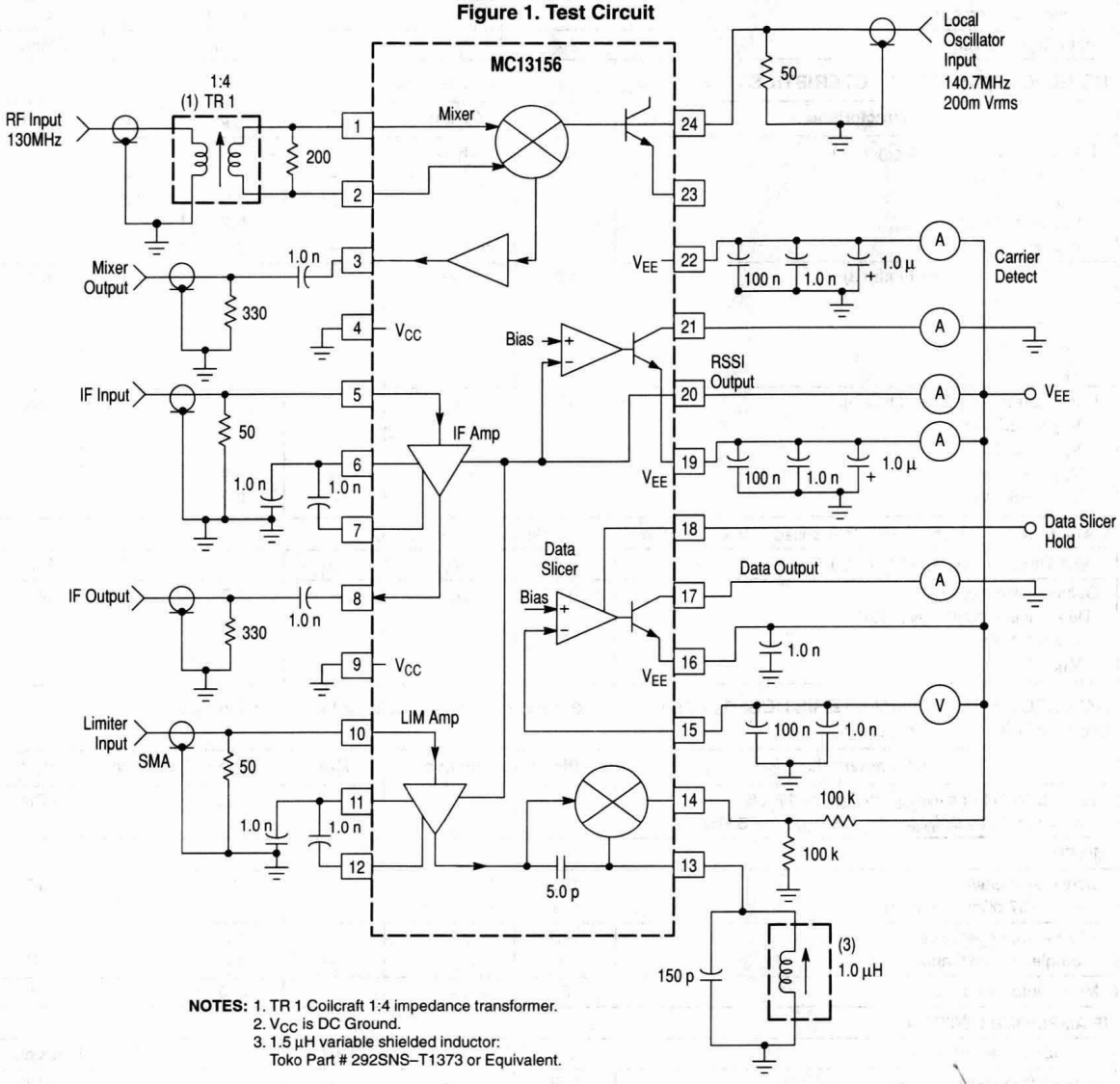
AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figures 17, 25) f_{in} = 144.45 MHz; f_{mod} = 1.0 kHz; f_{dev} = ±75 kHz	1, 14	–	–	–100	–	dBm
MIXER						
Conversion Gain P_{in} = –37 dBm (Figure 4)	1, 3	–	–	22	–	dB
Mixer Input Impedance Single–Ended (Table 1)	1, 2	R_p C_p	– –	1.0 4.0	– –	kΩ pF
Mixer Output Impedance	3	–	–	330	–	Ω
IF AMPLIFIER SECTION						
IF RSSI Slope (Figure 6)	20	–	0.2	0.4	0.6	μA/dB
IF Gain (Figure 5)	5, 8	–	–	39	–	dB
Input Impedance	5	–	–	1.4	–	kΩ
Output Impedance	8	–	–	290	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
LIMITING AMPLIFIER SECTION						
Limiter RSSI Slope (Figure 7)	20	–	0.2	0.4	0.6	µA/dB
Limiter Gain	–	–	–	55	–	dB
Input Impedance	10	–	–	1.4	–	kΩ
CARRIER DETECT						
Output Current – Carrier Detect (High V_{in})	21	–	–	0	–	µA
Output Current – Carrier Detect (Low V_{in})	21	–	–	3.0	–	mA
Input Threshold Voltage – Carrier Detect Input Voltage Referenced to V_{EE} = –3.0 Vdc	20	–	0.9	1.2	1.4	Vdc

Figure 1. Test Circuit



NOTES: 1. TR 1 Coilcraft 1:4 impedance transformer.
2. V_{CC} is DC Ground.
3. 1.5 µH variable shielded inductor:
Toko Part # 292SNS–T1373 or Equivalent.

Figure 2. Total Drain Current versus Supply Voltage and Temperature

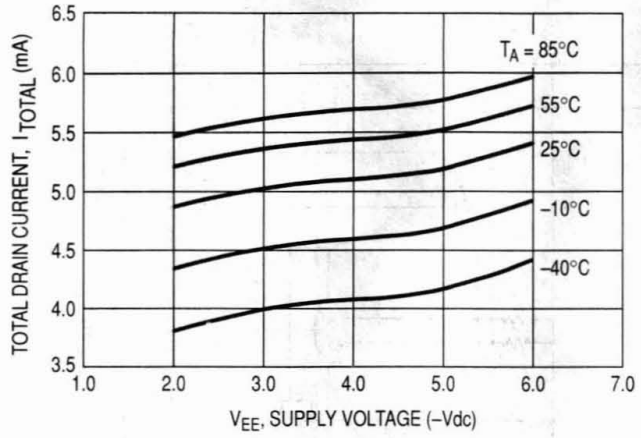


Figure 3. Drain Currents versus Supply Voltage

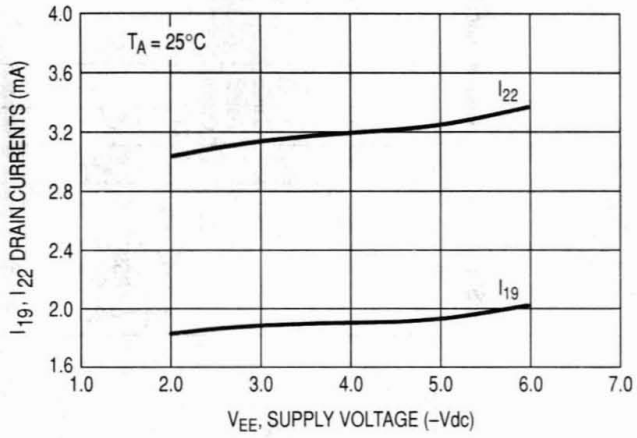


Figure 4. Mixer Gain versus Input Signal Level

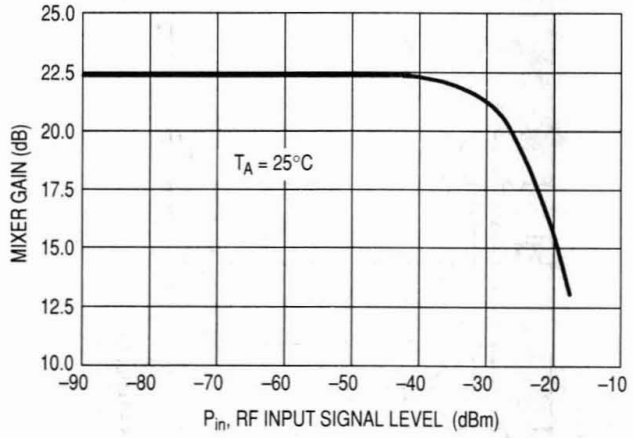


Figure 5. IF Amplifier Gain versus Input Signal Level and Ambient Temperature

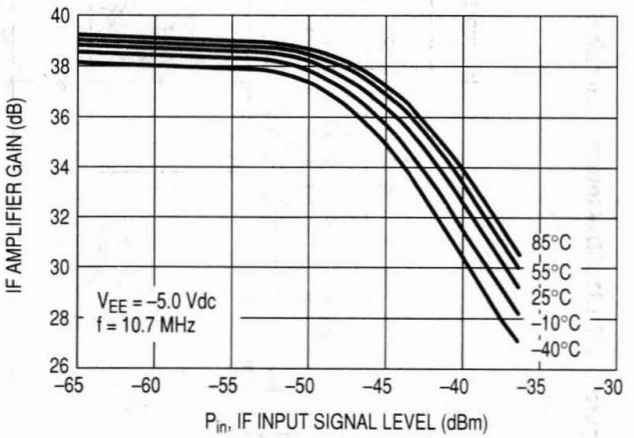


Figure 6. IF Amplifier RSSI Output Current versus Input Signal Level and Ambient Temperature

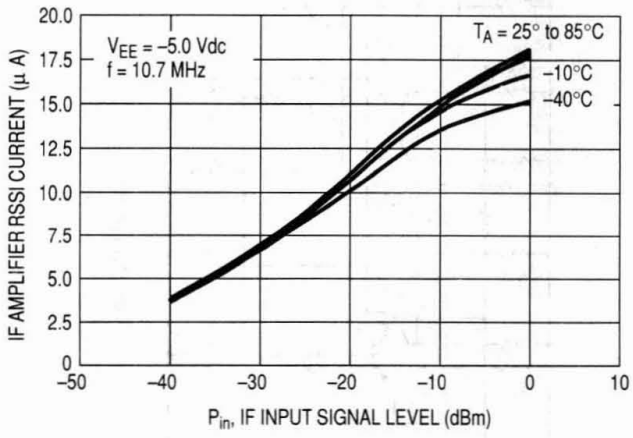


Figure 7. Limiter Amplifier RSSI Output Current versus Input Signal Level and Temperature

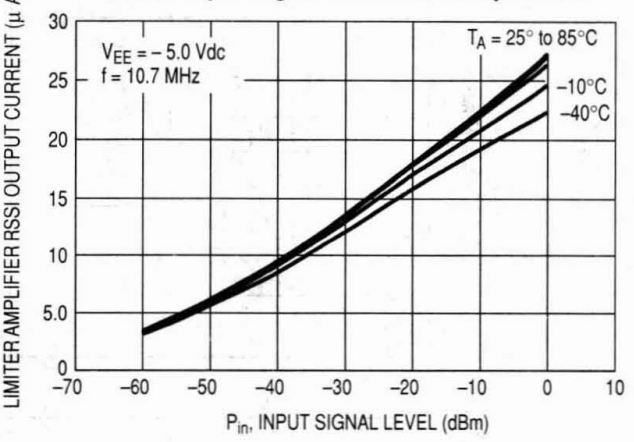
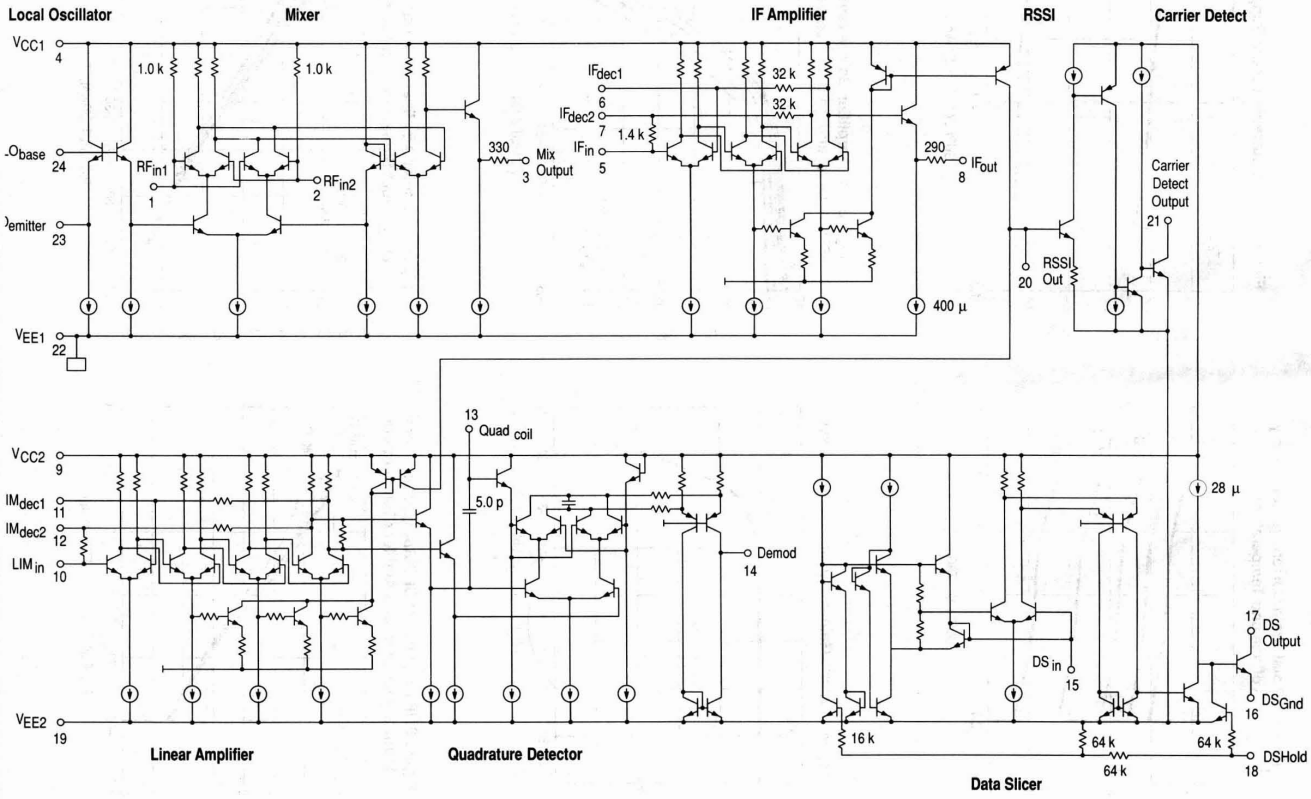


Figure 8. MC13156DW Internal Circuit Schematic



CIRCUIT DESCRIPTION

General

The MC13156 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as CT–2 and wideband data links with data rates up to 500 kbaud. It contains a mixer, oscillator, signal strength meter drive, IF amplifier, limiting IF, quadrature detector and a data slicer with a hold function (refer to Figure 8, Simplified Internal Circuit Schematic).

Current Regulation

Temperature compensating voltage independent current regulators are used throughout.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single–ended mode by connecting the other input to the positive supply rail.

Figure 4 shows the mixer gain and saturated output response as a function of input signal drive. The circuit used to measure this is shown in Figure 1. The linear gain of the mixer is approximately 22 dB. Figure 9 shows the mixer gain versus the IF output frequency with the local oscillator of 150 MHz at 100 mVrms LO drive level. The RF frequency is swept. The sensitivity of the IF output of the mixer is shown in Figure 10 for an RF input drive of 10 mVrms at 140 MHz and IF at 10 MHz.

The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 4.0 pF (see Table 1 for details). The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 23 to V_{EE}. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 10).

The oscillator configurations specified above, and two others using an external transistor, are described in the application section:

1) A 133 MHz oscillator multiplier using a 3rd overtone crystal, and
2) A 307.8 to 309.3 MHz manually tuned, varactor controlled local oscillator.

RSSI

The Received Signal Strength Indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 20 sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic or crystal bandpass filters which have an insertion loss of 8.0 dB. The RSSI circuit is designed to provide 70+ dB of dynamic range with temperature compensation (see Figures 6 and 7 which show RSSI responses of the IF and Limiter amplifiers). Variation in the RSSI output current with supply voltage is small (see Figure 11).

Carrier Detect

When the meter current flowing through the meter load resistance reaches 1.2 Vdc above ground, the comparator flips, causing the carrier detect output to go high. Hysteresis can be accomplished by adding a very large resistor for positive feedback between the output and the input of the comparator.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 39 dB at 10.7 MHz. Figure 5 shows the gain and saturated output response of the IF amplifier over temperature, while Figure 12 shows the IF amplifier gain as a function of the IF frequency.

The fixed internal input impedance is 1.4 kΩ. It is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.4 kΩ source and load impedance.

For 10.7 MHz ceramic filter applications, an external 430 Ω resistor must be added in parallel to provide the equivalent load impedance of 330 Ω that is required by the filter; however, no external matching is necessary at the input since the mixer output matches the 330 Ω source impedance of the filter. For 455 kHz applications, an external 1.1 kΩ resistor must be added in series with the mixer output to obtain the required matching impedance of 1.4 kΩ of the filter input resistance. Overall RSSI linearity is dependent on having total midband attenuation of 12 dB (6.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 290 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that four stages are used with the last three contributing to the RSSI. The fixed internal input impedance is 1.4 kΩ. The total gain of the limiting amplifier section is approximately 55 dB. This IF limiting amplifier section internally drives the quadrature detector section.

Figure 9. Mixer Gain versus IF Frequency

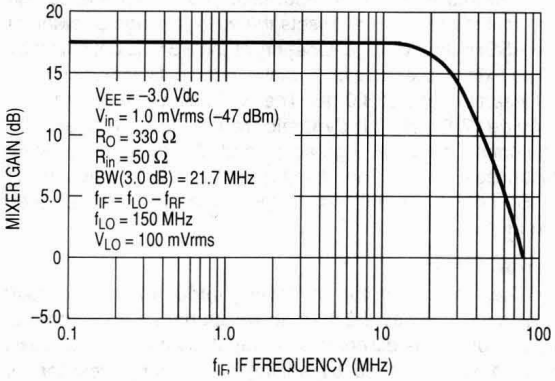


Figure 10. Mixer IF Output Level versus Local Oscillator Input Level

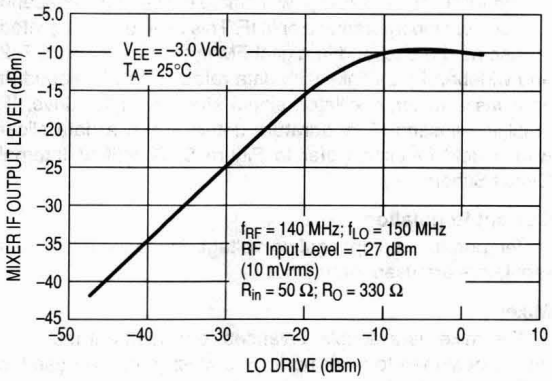


Figure 11. RSSI Output Current versus Supply Voltage and RF Input Signal Level

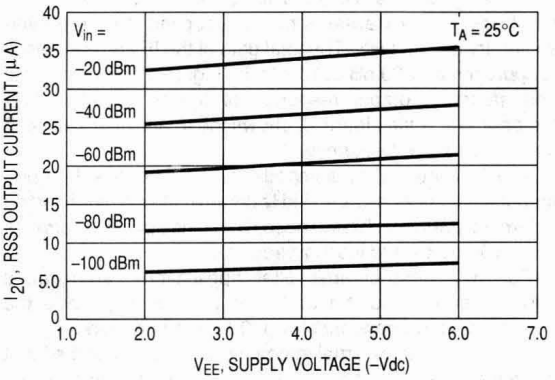


Figure 12. IF Amplifier Gain versus IF Frequency

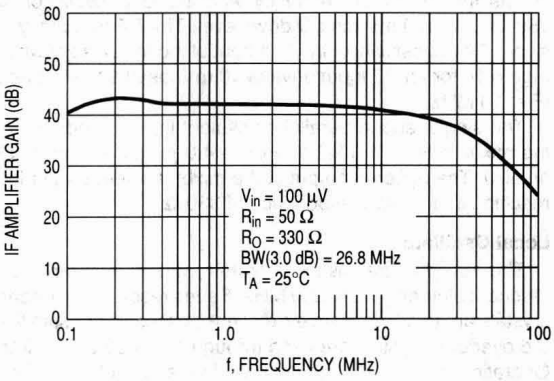
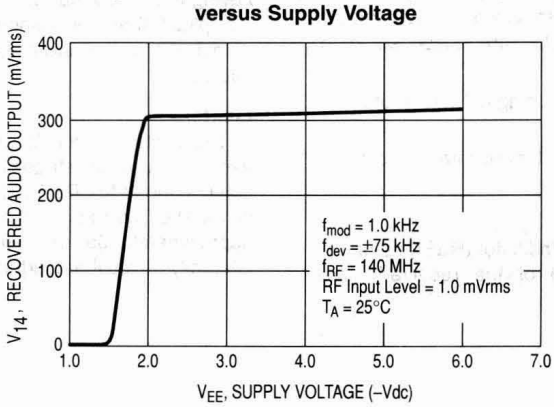


Figure 13. Recovered Audio Output Voltage versus Supply Voltage



Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor to couple the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

The bandwidth of the detector allows for recovery of relatively high data rate modulation. The recovered signal is converted from differential to single ended through a push–pull NPN/PNP output stage. Variation in recovered audio output voltage with supply voltage is very small (see Figure 13). The output drive capability is approximately ±9.0 μA for a frequency deviation of ±75 kHz and 1.0 kHz modulating frequency (see Application Circuit).

Data Slicer

The data slicer input (Pin 15) is self centering around 1.1 V with clamping occurring at 1.1 ± 0.5 V_{be} Vdc. It is designed to square up the data signal. Figure 14 shows a detailed schematic of the data slicer.

The Voltage Regulator sets up 1.1 Vdc on the base of Q12, the Differential Input Amplifier. There is a potential of 1.0 V_{be} on the base–collector of transistor diode Q11 and 2.0 V_{be} on the base–collector of Q10. This sets up a 1.5 V_{be} (~ 1.1 Vdc) on the node between the 36 kΩ resistors which is connected to the base of Q12. The differential output of the data slicer Q12 and Q13 is converted to a single–ended output by the Driver Circuit. Additional circuitry, not shown in Figure 14, tends to keep the data slicer input centered at 1.1 Vdc as input signal levels vary.

The Input Diode Clamp Circuit provides the clamping at 1.0 V_{be} (0.75 Vdc) and 2.0 V_{be} (1.45 Vdc). Transistor diodes Q7 and Q8 are on, thus, providing a 2.0 V_{be} potential at the base of Q1. Also, the voltage regulator circuit provides a potential of 2.0 Vbe on the base of Q3 and 1.0 V_{be} on the emitter of Q3 and Q2. When the data slicer input (Pin 15) is pulled up, Q1 turns off; Q2 turns on, thereby clamping the input at 2.0 V_{be}. On the other hand, when Pin 15 is pulled down, Q1 turns on; Q2 turns off, thereby clamping the input at 1.0 V_{be}.

The recovered data signal from the quadrature detector is ac coupled to the data slicer via an input coupling capacitor. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in dc level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer. When centered there is no input current allowed, which is to say, that the input looks high in impedance.

Another unique feature of the data slicer is that it responds to various logic levels applied to the Data Slicer Hold Control pin (Pin 18). Figure 15 illustrates how the input and output currents under "no hold" condition relate to the input voltage. Figure 16 shows how the input current and input voltage relate for both the "no hold" and "hold" condition.

The hold control (Pin18) does three separate tasks:

1) With Pin 18 at 1.0 V_{be} or greater, the output is shut off (sets high). Q19 turns on which shunts the base drive from Q20, thereby turning the output off.
2) With Pin 18 at 2.0 V_{be} or greater, internal clamping diodes are open circuited and the comparator input is shut off and effectively open circuited. This is accomplished by turning off the current source to emitters of the input differential amplifier, thus, the input differential amplifier is shut off.
3) When the input is shut off, it allows the input capacitor to hold its charge during transmit to improve recovery at the beginning of the next receive period. When it is turned on, it allows for very fast charging of the input capacitor for quick recovery of new tuning or data average. The above features are very desirable in a TDD digital FM system.

Figure 14. Data Slicer Circuit

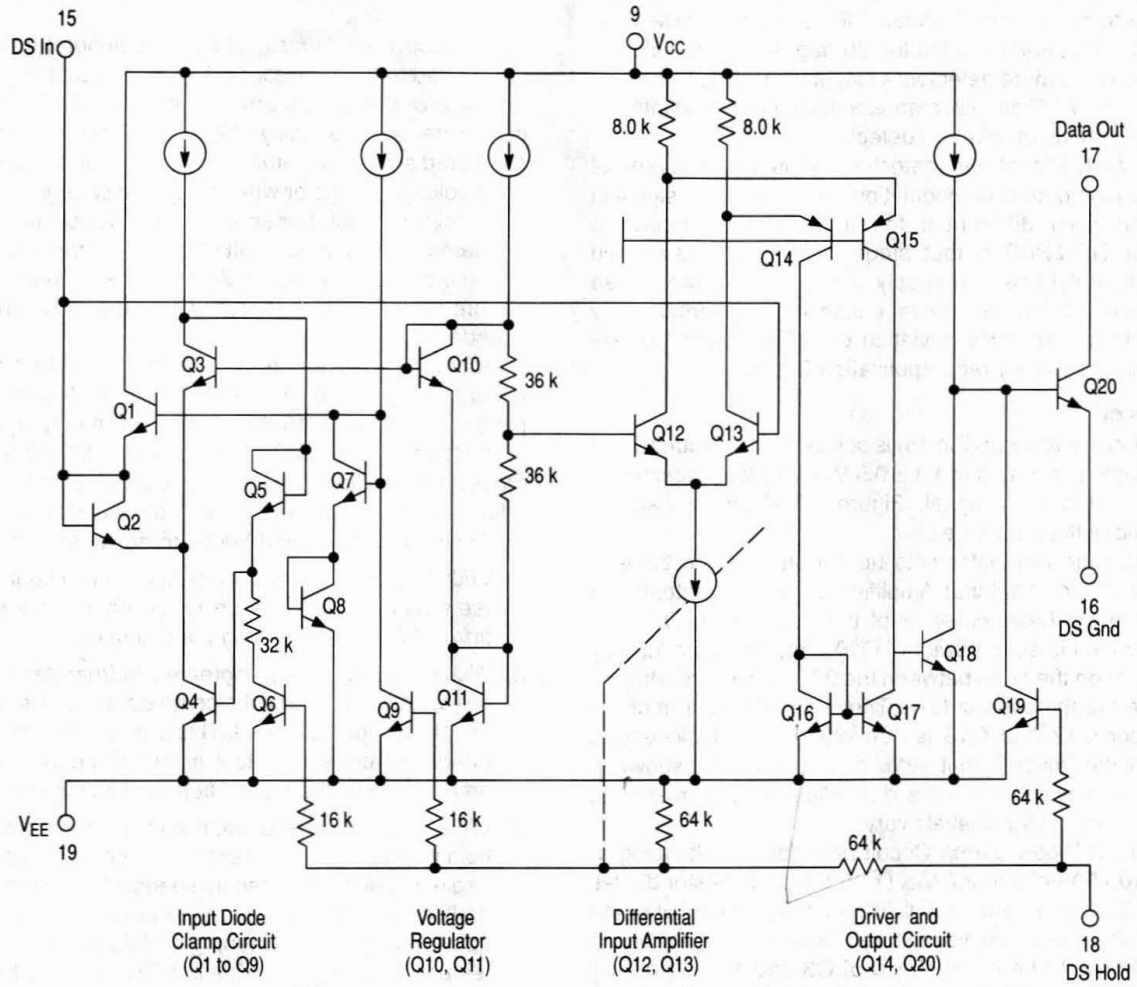


Figure 15. Data Slicer Input/Output Currents versus Input Voltage

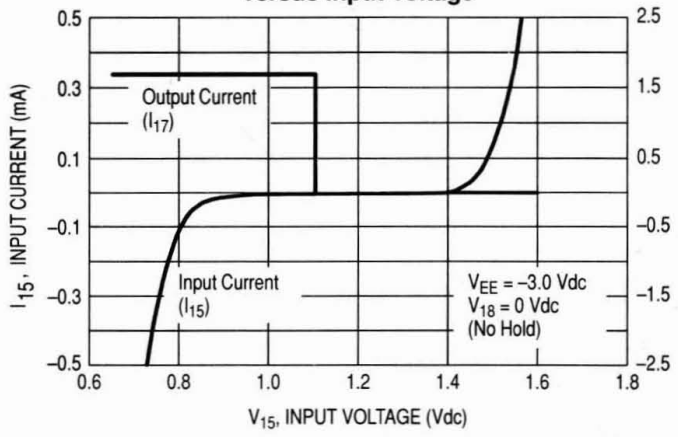


Figure 16. Data Slicer Input Current versus Input Voltage

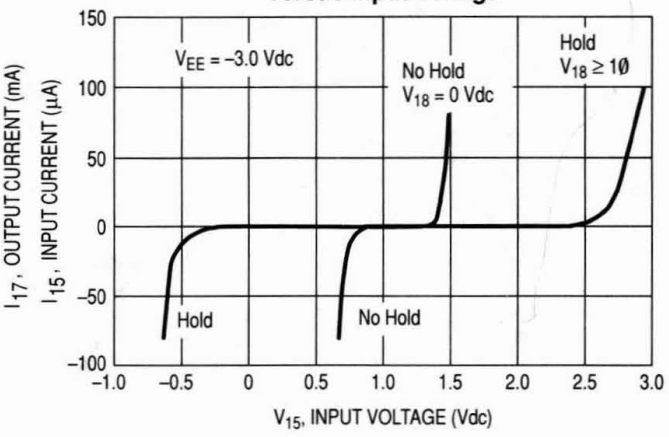
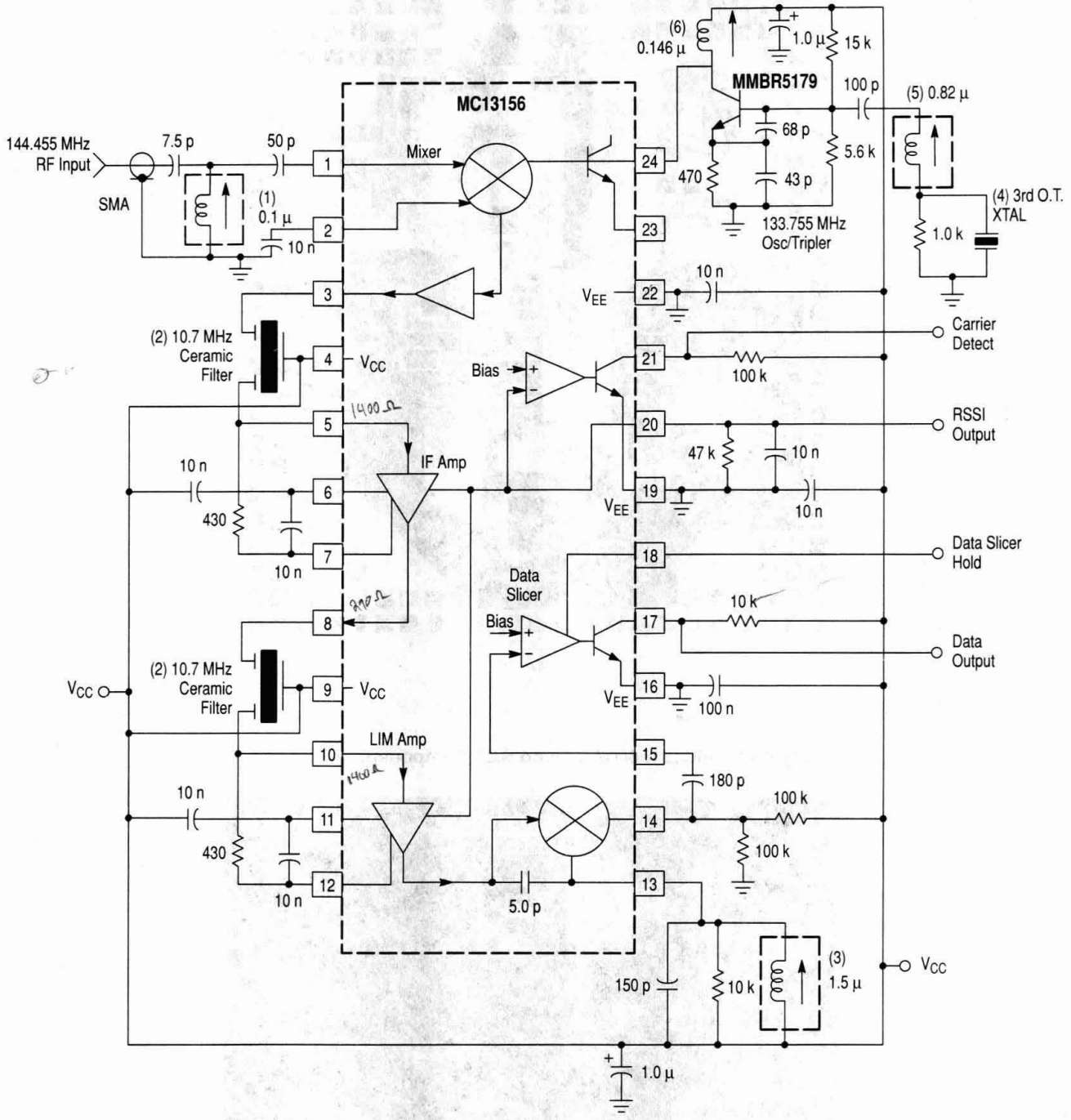


Figure 17. MC13156DW Application Circuit



NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. 10.7 MHz Ceramic Filter: Toko part # SK107M5–A0–10X or Murata Erie part # SFE10.7MHY–A.
3. 1.5 µH Variable Shielded Inductor: Toko part # 292SNS–T1373.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.585 MHz.
5. 0.814 µH Variable Shielded Inductor: Coilcraft part # 143–18J12S.
6. 0.146 µH Variable Inductor: Coilcraft part # 146–04J08.

Figure 18. MC13156DW Circuit Side Component Placement

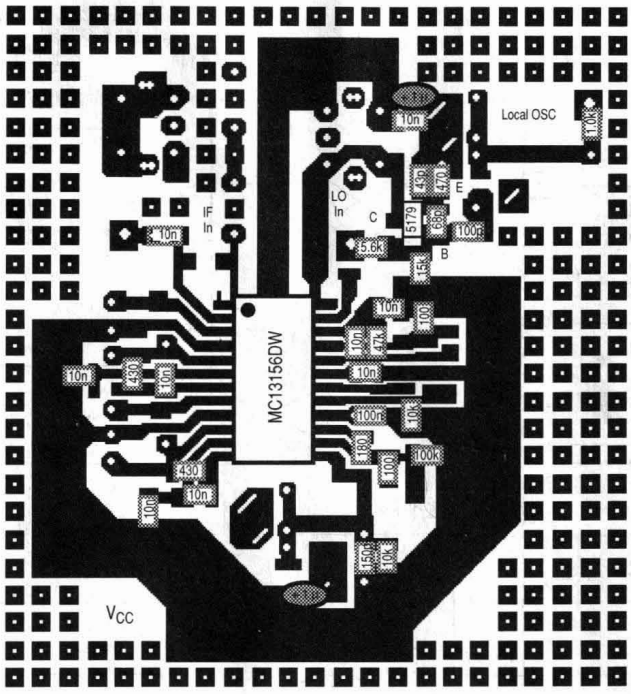
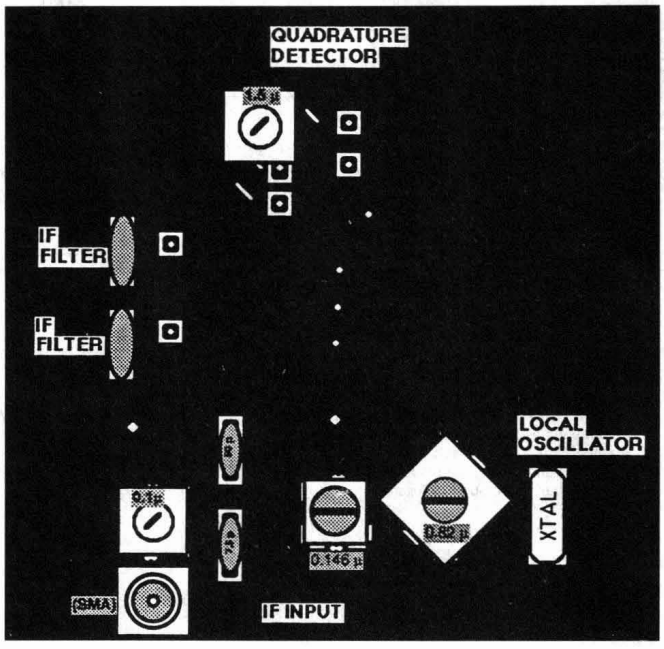


Figure 19. MC13156DW Ground Side Component Placement



APPLICATIONS INFORMATION

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 18 and 19 show the placement for the components specified in the application circuit (Figure 17). The applications circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but equivalent components should give similar results.

Input Matching Networks/Components

The input matching circuit shown in the application circuit schematic is passive high pass network which offers effective image rejection when the local oscillator is below the RF input frequency. Silver mica capacitors are used for their high Q and tight tolerance. The PC board is not dedicated to any particular input matching network topology; space is provided for the designer to breadboard as desired.

Alternate matching networks using 4:1 surface mount transformers or BALUNs provide satisfactory performance. The 12 dB SINAD sensitivity using the above matching networks is typically −100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±75 kHz at f_{IN} = 144.45 MHz and f_{OSC} = 133.75 MHz (see Figure 25).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. The SAW filter should be designed to interface with the mixer input impedance of approximately 1.0 kΩ. Table 1 displays the series equivalent single–ended mixer input impedance.

Local Oscillators

VHF Applications – The local oscillator circuit shown in the application schematic utilizes a third overtone crystal and an RF transistor. Selecting a transistor having good phase noise performance is important; a mandatory criteria is for the device to have good linearity of beta over several decades of collector current. In other words, if the low current beta is suppressed, it will not offer good 1/f noise performance. A third overtone series resonant crystal having at least 25 ppm tolerance over the operating temperature is recommended. The local oscillator is an impedance inversion third overtone Colpitts network and harmonic generator. In this circuit a 560 to 1.0 kΩ resistor shunts the crystal to ensure that it operates in its overtone mode; thus, a blocking capacitor is needed to eliminate the dc path to ground. The resulting parallel LC network should "free–run" near the crystal frequency if a short to ground is placed across the crystal. To provide sufficient output loading at the collector, a high Q variable inductor is used that is tuned to self resonate at the 3rd harmonic of the overtone crystal frequency.

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. Figure 20 shows a 5th overtone oscillator at 93.3 MHz and Figure 21 shows a 7th overtone oscillator at 148.3 MHz. Both circuits use a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have good tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and startup of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high, the performance of the oscillator may be impacted by lower gain margins.

Table 1. Mixer Input Impedance Data
(Single–ended configuration, V_{CC} = 3.0 Vdc, local oscillator drive = 100 mVrms)

Frequency (MHz)	Series Equivalent Complex Impedance (R + jX) (Ω)	Parallel Resistance Rp (Ω)	Parallel Capacitance Cp (pF)
90	190 – j380	950	4.7
100	160 – j360	970	4.4
110	130 – j340	1020	4.2
120	110 – j320	1040	4.2
130	97 – j300	1030	4.0
140	82 – j280	1040	4.0
150	71 – j270	1100	4.0
160	59 – j260	1200	3.9
170	52 – j240	1160	3.9
180	44 – j230	1250	3.8
190	38 – j220	1300	3.8

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 24) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_o, provides a feedback path that is low enough in reactance at frequencies of 5th overtone or higher to cause trouble. C_o has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor (L_o) is placed in parallel with the crystal. L_o is chosen to resonant with the crystal parallel capacitance (C_o) at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

UHF Application

Figure 22 shows a 318.5 to 320 MHz receiver which drives the mixer with an external varactor controlled (307.8 to 309.3 MHz) LC oscillator using an MPS901 (RF low power transistor in a TO–92 plastic package; also MMBR901 is available in a SOT–23 surface mount package). With the 50 kΩ 10 turn potentiometer this oscillator is tunable over a range of approximately 1.5 MHz. The MMBV909L is a low voltage varactor suitable for UHF applications; it is a dual back–to–back varactor in a SOT–23 package. The input matching network uses a 1:4 impedance matching transformer (Recommended sources are Mini–Circuits and Coilcraft).

Using the same IF ceramic filters and quadrature detector circuit as specified in the applications circuit in Figure 17, the 12 dB SINAD performance is –95 dBm for a f_{mod} = 1.0 kHz sinusoidal waveform and f_{dev} ±40 kHz.

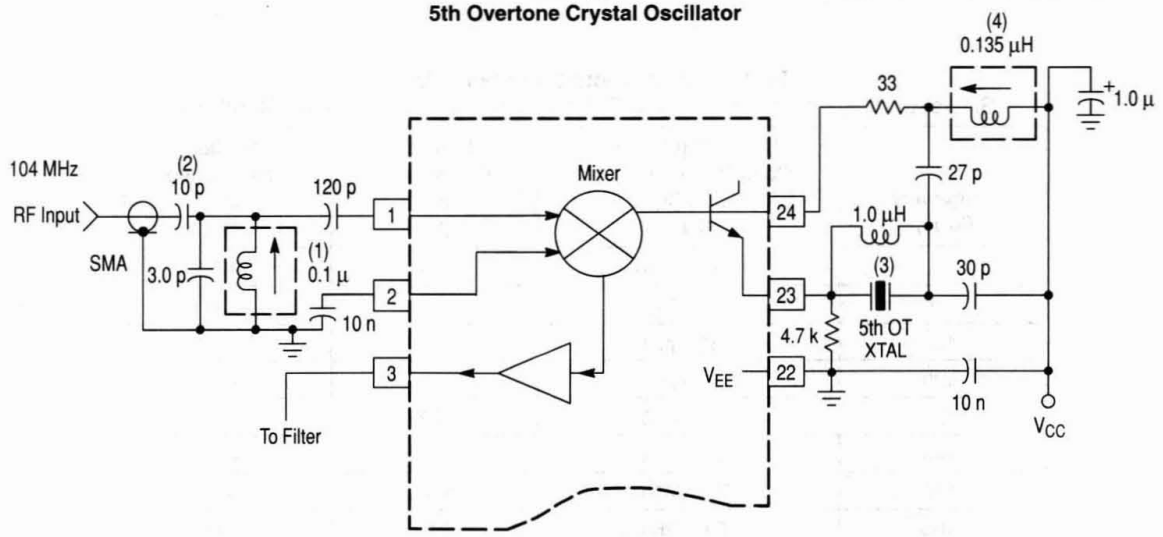
This circuit is breadboarded using the evaluation PC board shown in Figures 32 and 33. The RF ground is V_{CC} and path lengths are minimized. High quality surface mount components were used except where specified. The absolute values of the components used will vary with layout placement and component parasitics.

RSSI Response

Figure 26 shows the full RSSI response in the application circuit. The 10.7 MHz, 110 kHz wide bandpass ceramic filters (recommended sources are TOKO part # SK107M5–AO–10X or Murata Erie SFE10.7MHY–A) provide the correct bandpass insertion loss to linearize the curve between the limiter and IF portions of RSSI. Figure 25 shows that limiting occurs at an input of –100 dBm. As shown in Figure 26, the RSSI output linear from –100 dBm to –30 dBm.

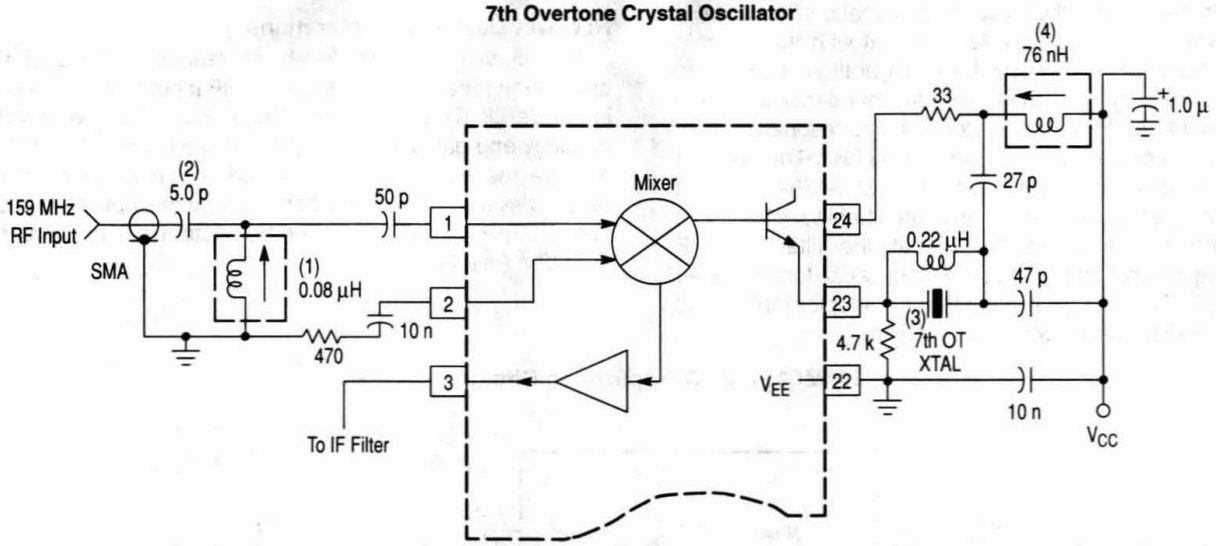
The RSSI rise and fall times for various RF input signal levels and R20 values are measured at Pin 20 without 10 nF filter capacitor. A 10 kHz square wave pulses the RF input signal on and off. Figure 27 shows that the rise and fall times are short enough to recover greater than 10 kHz ASK data; with a wider IF bandpass filters data rates up to 50 kHz may be achieved. The circuit used is the application circuit in Figure 17 with no RSSI output filter capacitor.

Figure 20. MC13156DW Application Circuit
f_{RF} = 104 MHz; f_{LO} = 93.30 MHz
5th Overtone Crystal Oscillator



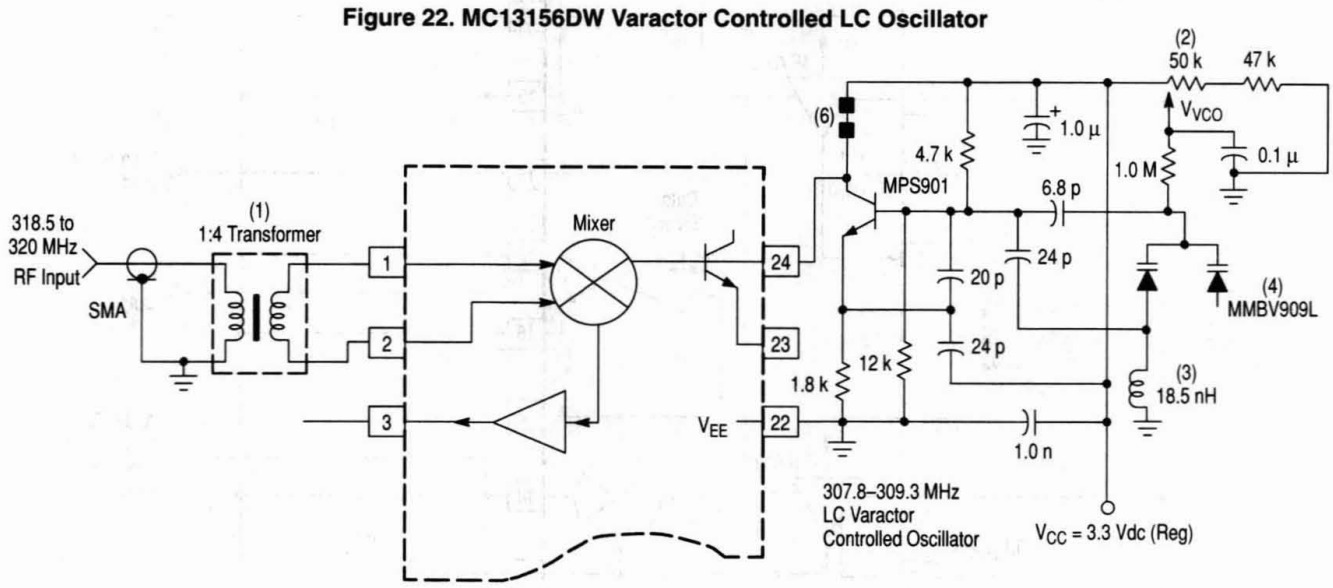
NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. Capacitors are Silver Mica.
3. 5th Overtone, Series Resonant, 25 PPM Crystal at 93.300 MHz.
4. 0.135 µH Variable Shielded Inductor: Coilcraft part # 146–05J08S or equivalent.

Figure 21. MC13156DW Application Circuit
f_{RF} = 159 MHz; f_{LO} = 148.30 MHz
7th Overtone Crystal Oscillator



NOTES: 1. 0.08 µH Variable Shielded Inductor: Toko part # 292SNS–T1365Z or equivalent.
2. Capacitors are Silver Mica.
3. 7th Overtone, Series Resonant, 25 PPM Crystal at 148.300 MHz.
4. 76 nH Variable Shielded Inductor: Coilcraft part # 150–03J08S or equivalent.

Figure 22. MC13156DW Varactor Controlled LC Oscillator



NOTES: 1. 1:4 Impedance Transformer: Mini–Circuits.
2. 50 k Potentiometer, 10 turns.
3. Spring Coil; Coilcraft A05T.
4. Dual Varactor in SOT–23 Package.
5. All other components are surface mount components.
6. Ferrite beads through loop of 24 AWG wire.

45 MHz Narrowband Receiver

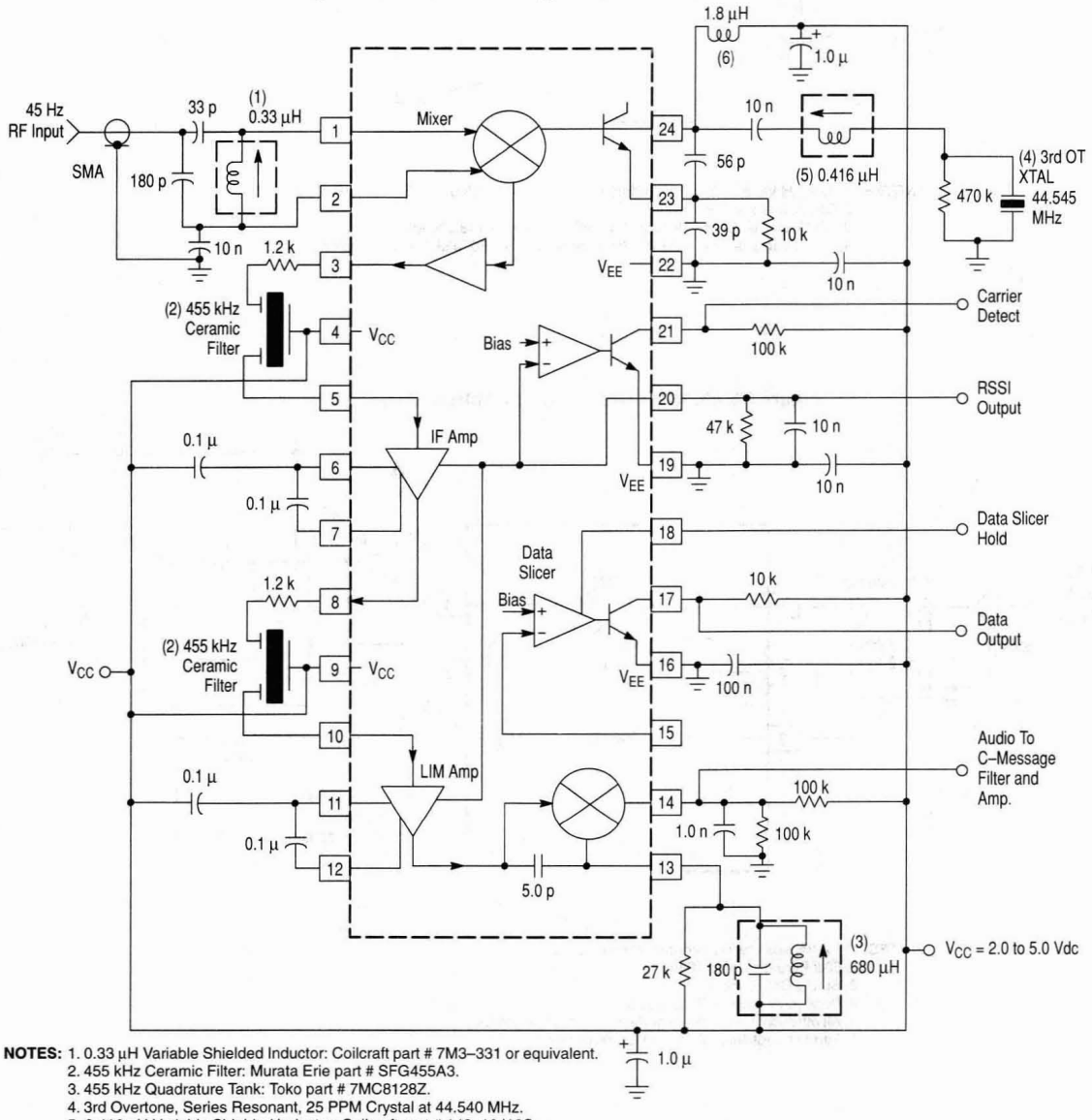
The above application examples utilize a 10.7 MHz IF. In this section a narrowband receiver with a 455 kHz IF will be described. Figure 23 shows a full schematic of a 45 MHz receiver that uses a 3rd overtone crystal with the on–chip oscillator transistor. The oscillator configuration is similar to the one used in Figure 17; it is called an impedance inversion Colpitts. A 44.545 MHz 3rd overtone, series resonant crystal is used to achieve an IF frequency at 455 kHz. The ceramic IF filters selected are Murata Erie part # SFG455A3. 1.2 kΩ chip resistors are used in series with the filters to achieve the terminating resistance of 1.4 kΩ to the filter. The IF decoupling is very important; 0.1 µF chip capacitors are used at Pins 6, 7, 11 and 12. The quadrature detector tank circuit uses a 455 kHz quadrature tank from Toko.

The 12 dB SINAD performance is –109 dBm for a f_{mod} = 1.0 kHz and a f_{dev} = ±4.0 kHz. The RSSI dynamic range is approximately 80 dB of linear range (see Figure 24).

Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 28. This information helps determine the network topology and gain blocks required ahead of the MC13156 to achieve the desired sensitivity and dynamic range of the receiver system. In the application circuit the input third order intercept (IP3) performance of the system is approximately –25 dBm (see Figure 29).

Figure 23. MC13156DW Application Circuit at 45 MHz



NOTES: 1. 0.33 µH Variable Shielded Inductor: Coilcraft part # 7M3–331 or equivalent.
2. 455 kHz Ceramic Filter: Murata Erie part # SFG455A3.
3. 455 kHz Quadrature Tank: Toko part # 7MC8128Z.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.540 MHz.
5. 0.416 µH Variable Shielded Inductor: Coilcraft part # 143–10J12S.
6. 1.8 µH Molded Inductor.

Figure 24. RSSI Output Voltage versus Input Signal Level

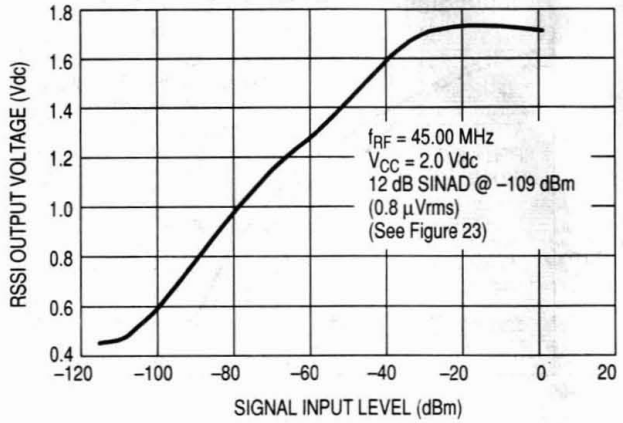


Figure 25. S + N/N versus RF Input Signal Level

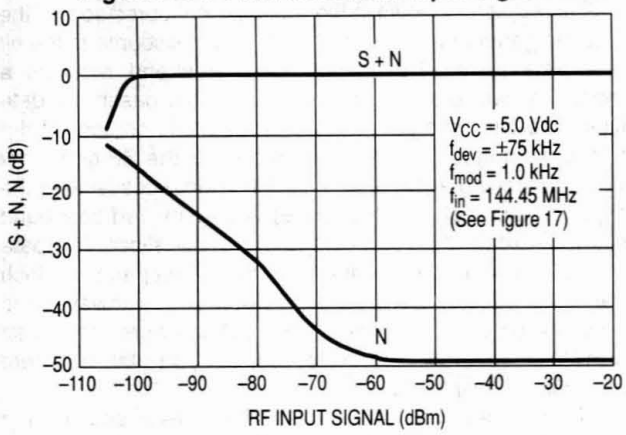


Figure 26. RSSI Output Voltage versus Input Signal Level

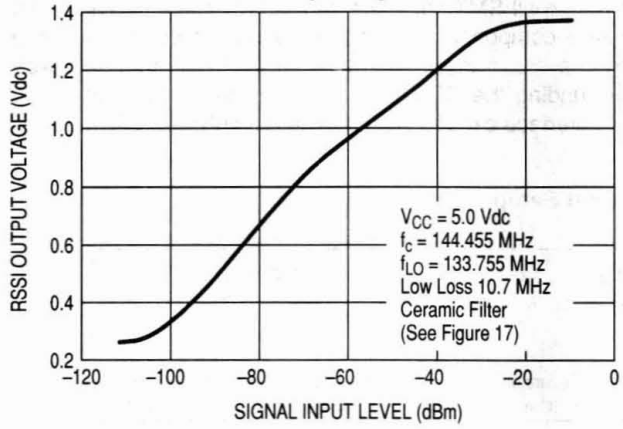


Figure 27. RSSI Output Rise and Fall Times versus RF Input Signal Level

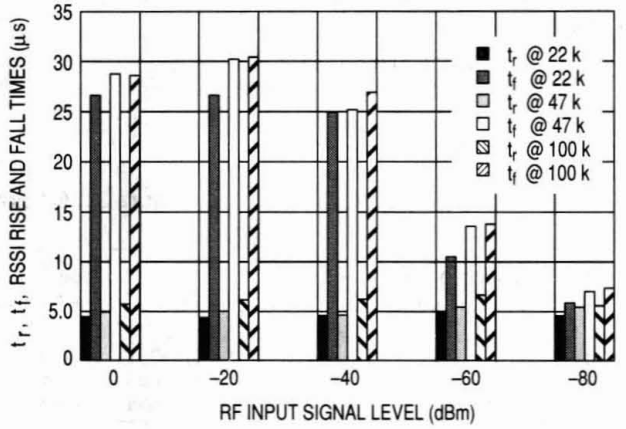


Figure 28. Signal Levels versus RF Input Signal Level

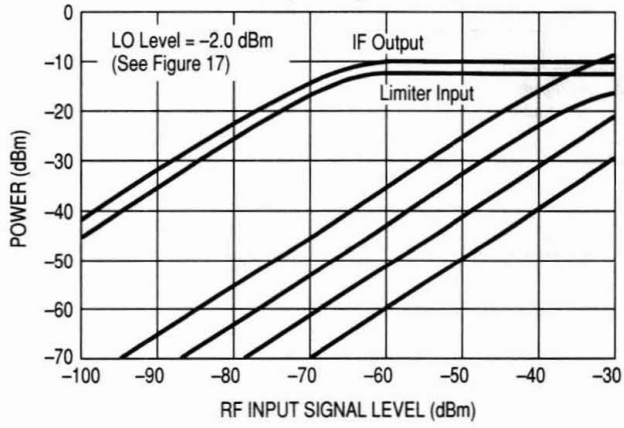
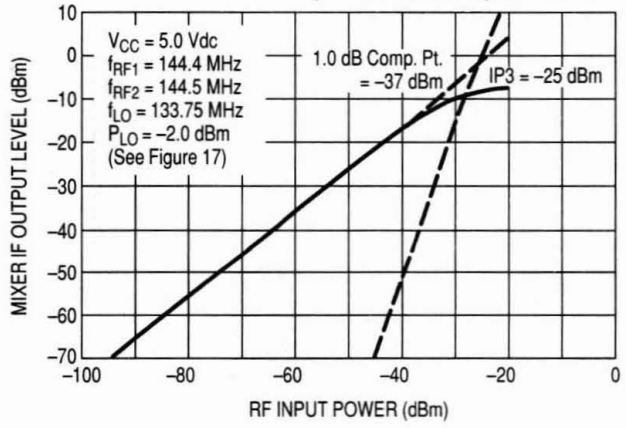


Figure 29. 1.0 dB Compression Pt. and Input Third Order Intercept Pt. versus Input Power



BER TESTING AND PERFORMANCE

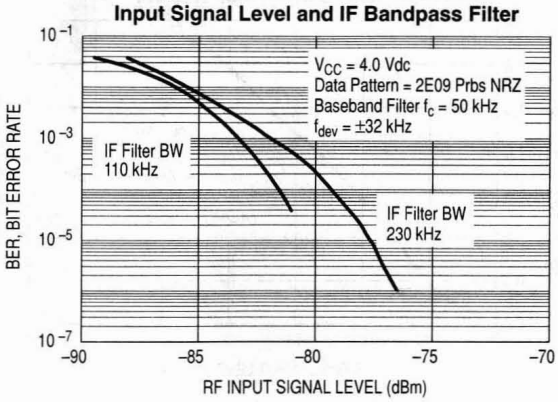
Description

The test setup shown in Figure 31 is configured so that the function generator supplies a 100 kHz clock source to the bit error rate tester. This device generates and receives a repeating data pattern and drives a 5 pole baseband data filter. The filter effectively reduces harmonic content of the baseband data which is used to modulate the RF generator which is running at 144.45 MHz. Following processing of the signal by the receiver (MC13156), the recovered baseband sinewave (data) is AC coupled to the data slicer. The data slicer is essentially an auto–threshold comparator which tracks the zero crossing of the incoming sinewave and provides logic level data at its ouput. Data errors associated with the recovered data are collected by the bit error rate receiver and displayed.

Bit error rate versus RF signal input level and IF filter bandwidth are shown in Figure 30. The bit error rate data was taken under the following test conditions:

- Data rate = 100 kbps
- Filter cutoff frequency set to 39% of the data rate or 39 kHz.
- Filter type is a 5 pole equal–ripple with 0.5° phase error.
- V_{CC} = 4.0 Vdc
- Frequency deviation = ±32 kHz.

Figure 30. Bit Error Rate versus RF Input Signal Level and IF Bandpass Filter



Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 32 and 33). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates.

Figure 31. Bit Error Rate Test Setup

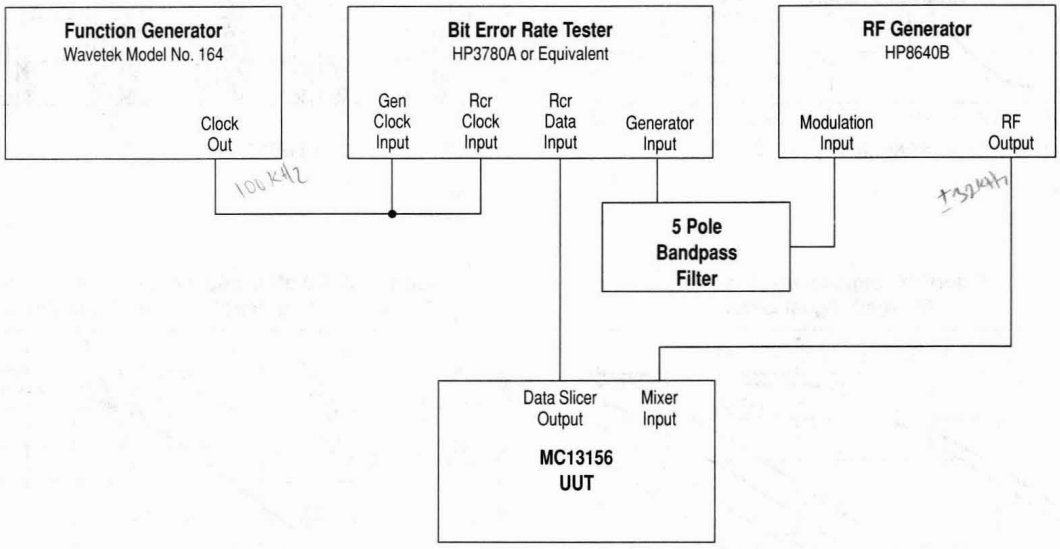


Figure 32. Circuit Side View

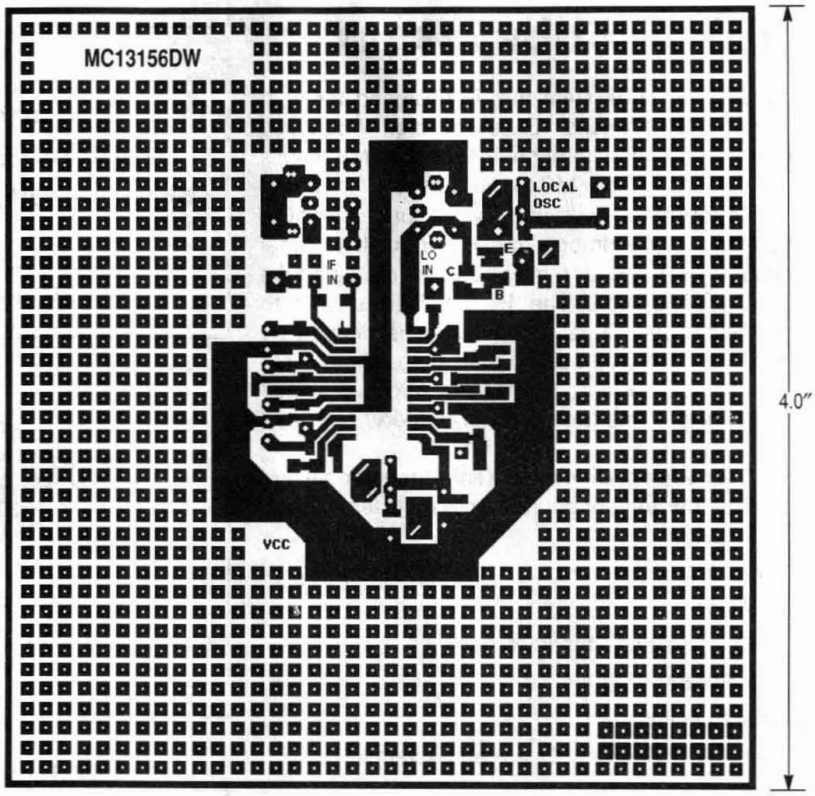
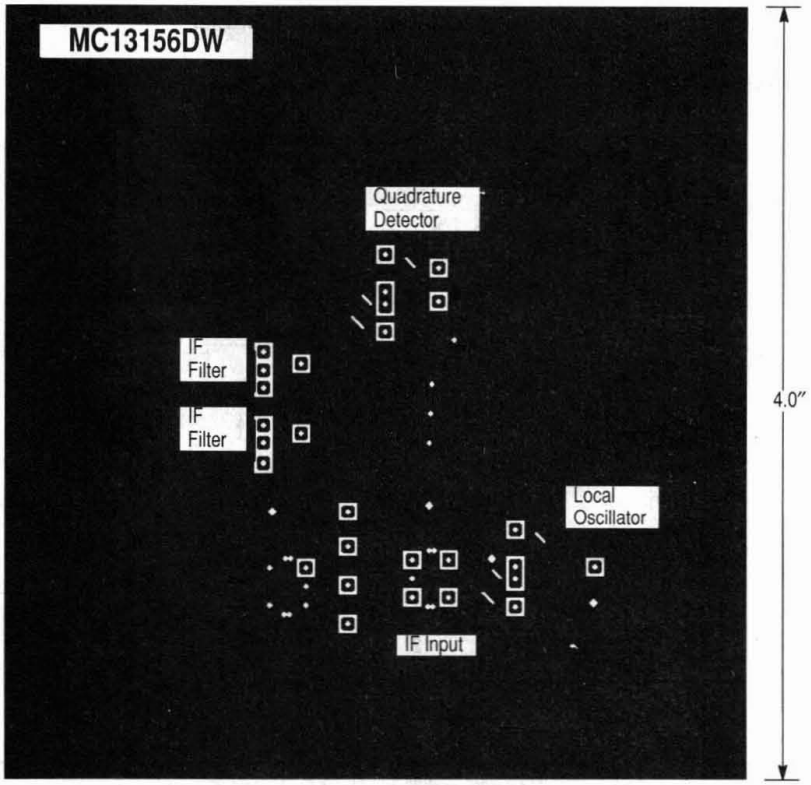


Figure 33. Ground Side View



MOTOROLA

MC13158

Wideband FM IF Subsystem

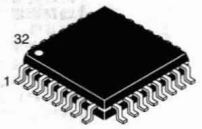
WIDEBAND FM IF SUBSYSTEM FOR DECT AND DIGITAL APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output off to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count

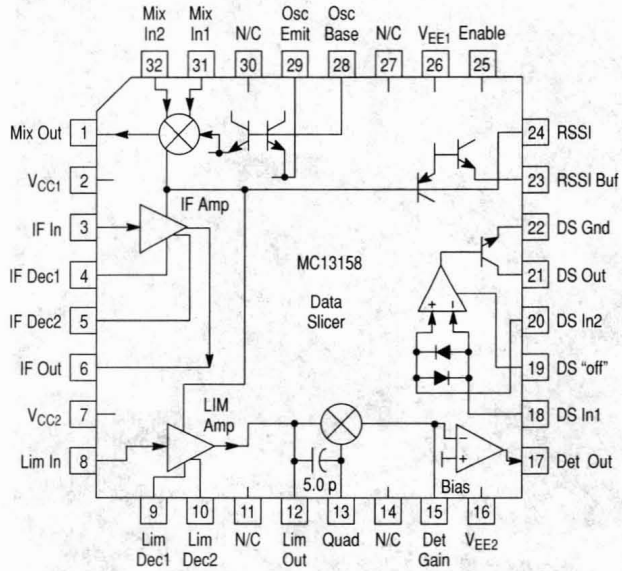


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13158FTB	T_A = – 40 to +85°C	TQFP–32

Representative Block Diagram



This device contains 234 active transistors.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 26	$V_{S(max)}$	6.5	Vdc
Junction Temperature		T_{JMAX}	+150	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

NOTE: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = V_2 = V_7$; $V_{EE} = V_{16} = V_{22} = V_{26}$; $V_S = V_{CC} - V_{EE}$)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25°C −40°C ≤ T_A ≤ 85°C	2, 7 16, 26	V_S	2.0 to 6.0	Vdc
Input Frequency	31, 32	F_{in}	10 to 500	MHz
Ambient Temperature Range		T_A	−40 to +85	°C
Input Signal Level	31, 32	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; No Input Signal; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current	V_S = 2.0 Vdc V_S = 3.0 Vdc V_S = 6.0 Vdc See Figure 2	16, 26	I_{TOTAL}	2.5 3.5 3.5	5.5 5.7 6.0	8.5 8.5 9.5	mA
DATA SLICER (Input Voltage Referenced to V_{EE}; V_S = 3.0 Vdc; No Input Signal)							
Output Current; V_{18} LO; Data Slicer Enabled (DS "on")	$V_{19} = V_{EE}$ $V_{18} < V_{20}$ $V_{20} = V_S/2$ See Figure 3	21	I_{21}	2.0	5.9	–	mA
Output Current; V_{18} HI; Data Slicer Enabled (DS "on")	$V_{19} = V_{EE}$ $V_{18} > V_{20}$ $V_{20} = V_S/2$ See Figure 4	21	I_{21}	–	0.1	1.0	µA
Output Current; Data Slicer Disabled (DS "off")	$V_{19} = V_{CC}$ $V_{20} = V_S/2$	21	I_{21}	–	0.1	1.0	µA

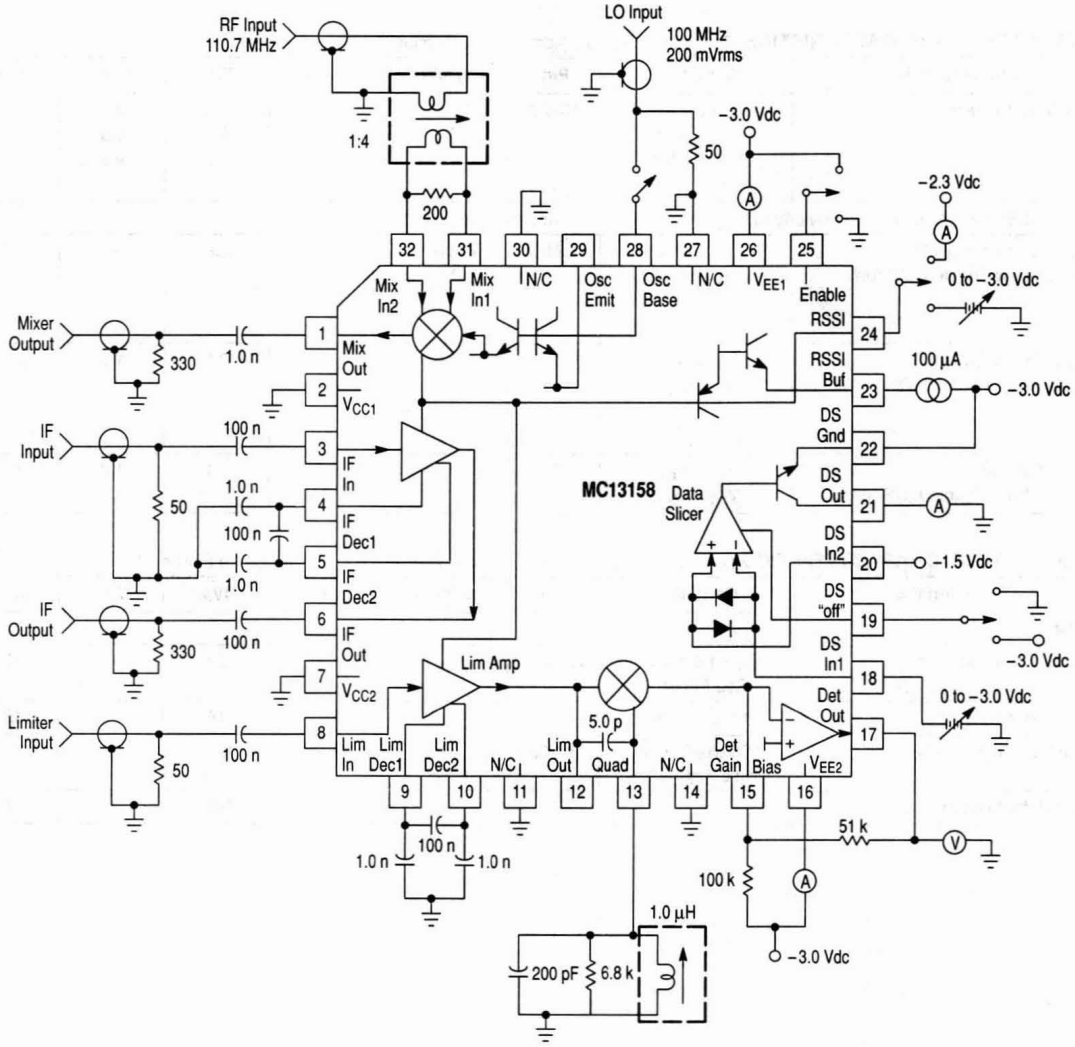
AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 110.7 MHz; f_{LO} = 100 MHz; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
MIXER							
Mixer Conversion Gain	V_{in} = 1.0 mVrms See Figure 5	31, 32, 1	–	–	22	–	dB
Noise Figure	Input Matched	31, 32, 1	NF	–	14	–	dB
Mixer Input Impedance	Single–Ended See Figure 15	31, 32	Rp Cp	– –	865 1.6	– –	Ω pF
Mixer Output Impedance		1	–	–	330	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 110.7 MHz; f_{LO} = 100 MHz; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER SECTION							
IF RSSI Slope	See Figure 8	23	–	0.15	0.3	0.4	μA/dB
IF Gain	f = 10.7 MHz See Figure 7	3, 6	–	–	36	–	dB
Input Impedance		3	–	–	330	–	Ω
Output Impedance		6	–	–	330	–	Ω
LIMITING AMPLIFIER SECTION							
Limiter RSSI Slope	See Figure 9	23	–	0.15	0.3	0.4	μA/dB
Limiter Gain	f = 10.7 MHz	8, 12	–	–	70	–	dB
Input Impedance		8	–	–	330	–	Ω

Figure 1. Test Circuit



Typical Performance Over Temperature

(per Figure 1)

Figure 2. Total Supply Current versus Ambient Temperature, Supply Voltage

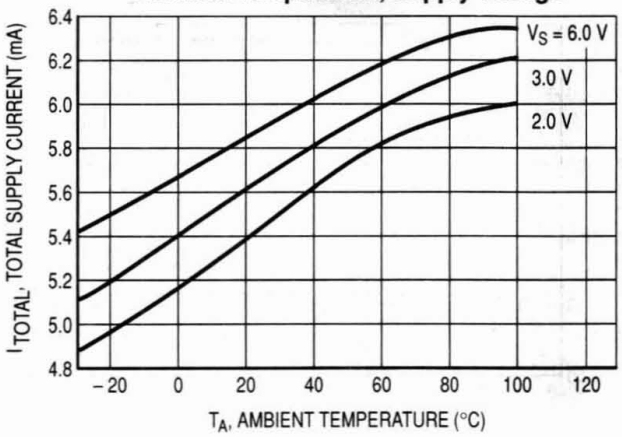


Figure 3. Data Slicer On Output Current versus Ambient Temperature

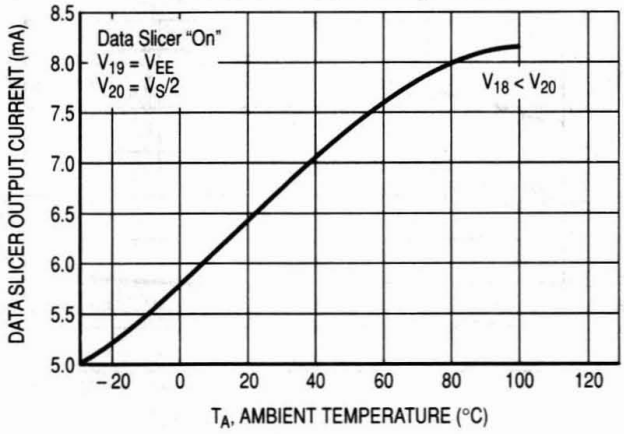


Figure 4. Data Slicer On Output Current versus Ambient Temperature

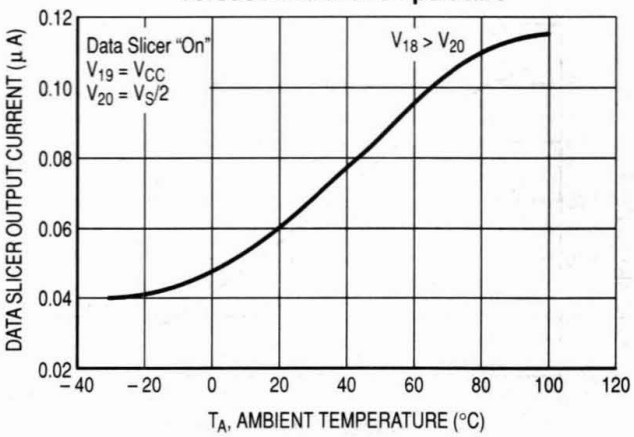


Figure 5. Normalized Mixer Gain versus Ambient Temperature

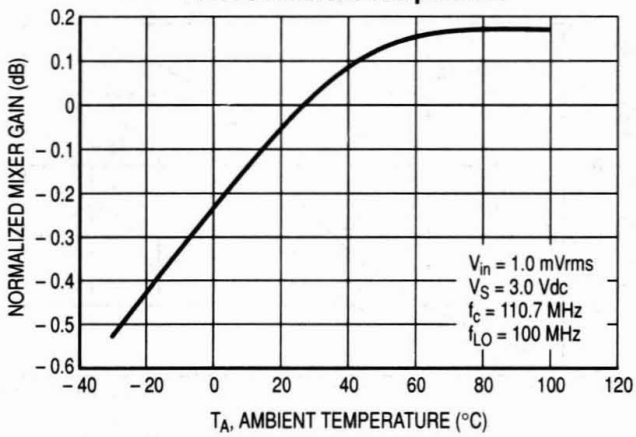


Figure 6. Mixer RSSI Output Current versus Ambient Temperature, Mixer Input Level

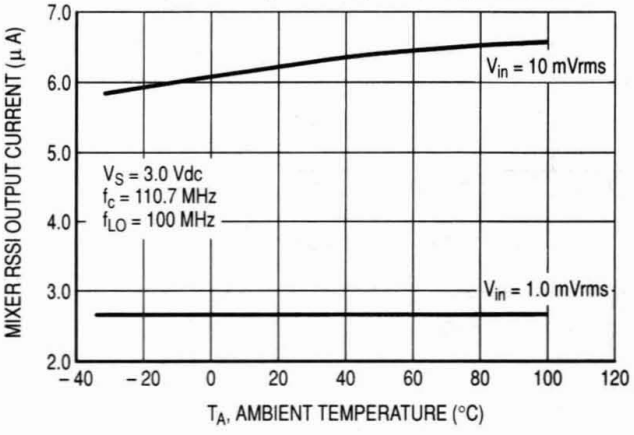
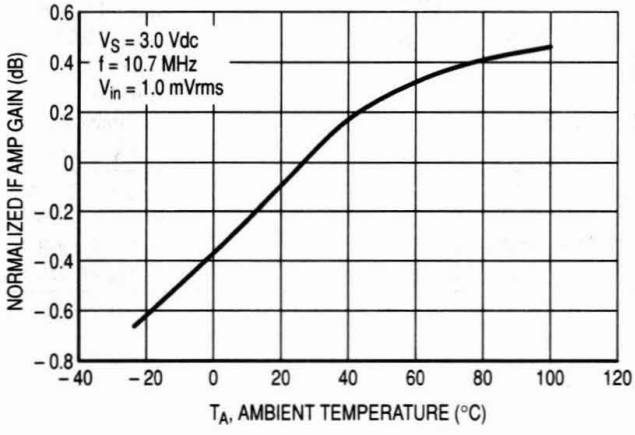


Figure 7. Normalized IF Amp Gain versus Ambient Temperature



tTypical Performance Over Temperature

(per Figure 1)

Figure 8. IF Amp RSSI Output Current versus Ambient Temperature, IF Input Level

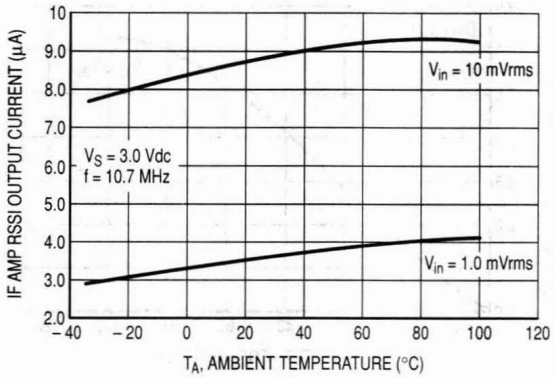


Figure 9. Limiter Amp RSSI Output Current versus Ambient Temperature, Input Signal Level

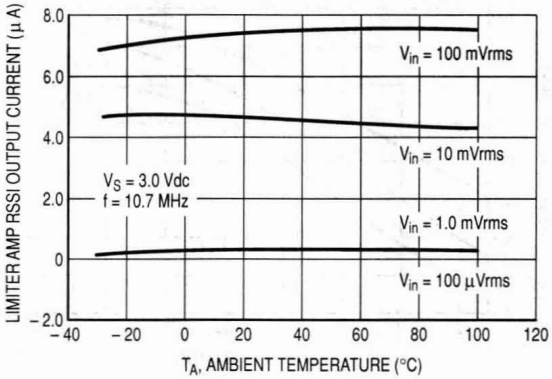


Figure 10. Total RSSI Output Current versus Ambient Temperature (No Signal)

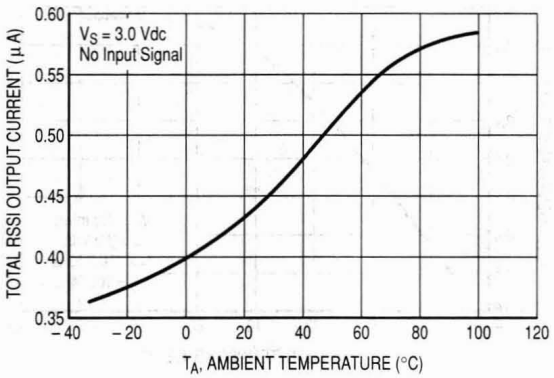
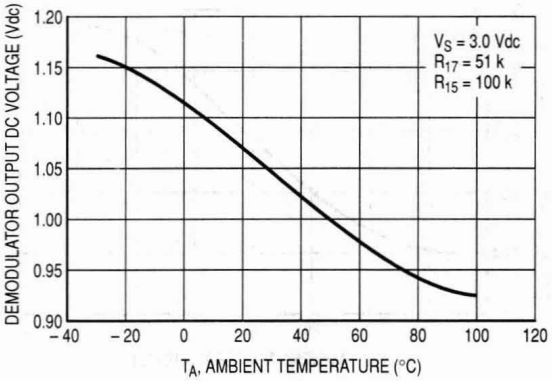


Figure 11. Demodulator DC Voltage versus Ambient Temperature



SYSTEM LEVEL AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 112 MHz; f_{LO} = 122.7 MHz)

Characteristic	Condition	Notes	Symbol	Typ	Unit
12 dB SINAD Sensitivity: Narrowband Application	f_{RF} = 112 MHz f_{mod} = 1.0 kHz f_{dev} = ±125 kHz SINAD Curve	1	–		dBm
Without Preamp	Figure 25			−101	
With Preamp	Figure 26			−113	
Third Order Intercept Point	f_{RF1} = 112 MHz f_{RF2} = 112.1 MHz	2	IIP3	−32	dBm
1.0 dB Comp. Point	V_S = 3.5 Vdc Figure 28		1.0 dB C.Pt.	−39	

NOTES: 1. Test Circuit & Test Set per Figure 24.
2. Test Circuit & Test Set per Figure 27.

CIRCUIT DESCRIPTION

General

The MC13158 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as Digital European Cordless Telephone (DECT) and wideband data links with data rates up to 2.0 Mbps. It contains a mixer, oscillator, Received Signal Strength Indicator (RSSI), IF amplifier, limiting IF, quadrature detector, power down or enable function, and a data slicer with output off function. Further details are covered in the Pin Function Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators which are controlled by the enable pin (Pin 25) where "low" powers up and "high" powers down the entire circuit.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single ended mode by connecting the other input to the positive supply rail. The linear gain of the mixer is approximately 22 dB at 100 mVrms LO drive level. The mixer gain and noise figure have been emphasized at the expense of intermodulation performance. RSSI measurements are added in the mixer to extend the range to higher signal levels. The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 2.0 pF. The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. Third overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor bias is increased by adding an external resistor from Pin 29 to V_{EE}; however, with an external resistor the oscillator stays on during power down. Typically, –10 dBm of local oscillator drive is needed to adequately drive the mixer. With an external oscillator source, the IC can be operated up to 500 MHz.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the mixer, IF and limiting amplifier stages. An increase in RSSI dynamic range, particularly at higher input signal levels is achieved. The RSSI circuit is designed to provide typically 85 dB of dynamic range with temperature compensation.

Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB and 330 Ω source and load impedance. For higher data rates used in DECT and related applications, LC bandpass filtering is necessary to acquire the desired bandpass response; however, the RSSI linearity will require the same insertion loss.

RSSI Buffer

The RSSI output current creates a voltage across an external resistor. A unity voltage–gain amplifier is used to buffer this voltage. The output of this buffer has an active pull–up but no pull–down, so it can also be used as a peak detector. The negative slew rate is determined by external capacitance and resistance to the negative supply.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB at 10.7 MHz.

The fixed internal input impedance is 330 Ω. When using ceramic filters requiring source and loss impedances of 330 Ω, no external matching is necessary. Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that five differential stages are used. The fixed internal input impedance is 330 Ω. The total gain of the limiting amplifier section is approximately 70 dB. This IF limiting amplifier section internally drives the quadrature detector section and it is also brought out on Pin 12.

Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor between Pins 12 and 13. An external capacitor may be added between these pins to increase the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

Internal low pass filter capacitors have been selected to control the bandwidth of the detector. The recovered signal is brought out by the inverting amplifier buffer. An external feedback resistor from the output (Pin 17) to the input of the inverting amplifier (Pin 15) controls the output amplitude; it is combined with another external resistor from the input to the negative supply (Pin 16) to set the output dc level. For a resistor ratio of 1, the DC level at the detector output is 2.0 V_{BE} (see Figure 12). A small capacitor C_{17} across the first resistor (from Pin 17 to 15) can be used to reduce the bandwidth.

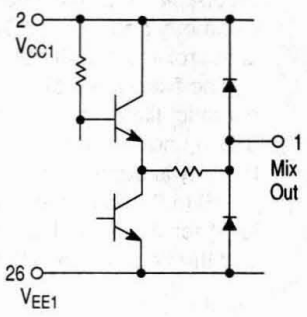
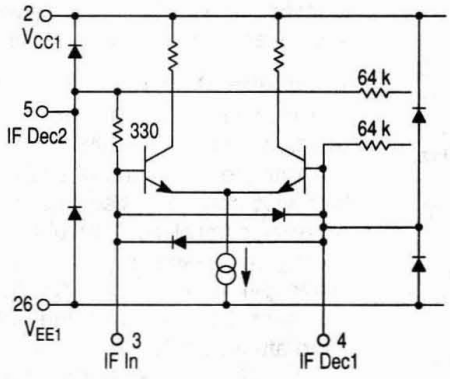
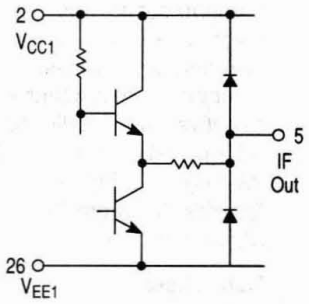
Data Slicer

The data slicer is a comparator that is designed to square up the data signal. Across the data slicer inputs (Pins 18 and 20) are back to back diodes.

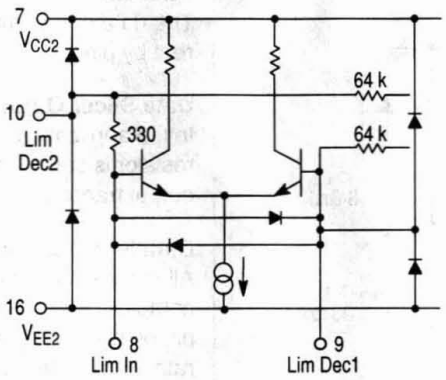
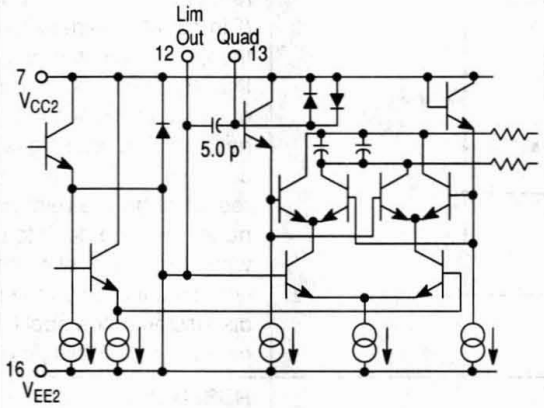
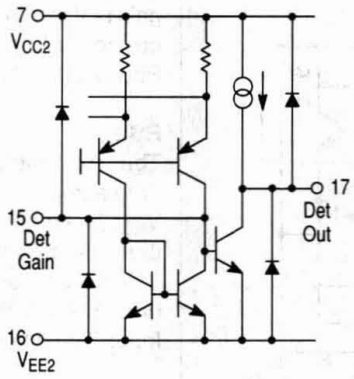
The recovered data signal from the quadrature detector can be DC coupled to the data slicer DS IN1 (Pin 18). In the application circuit shown in Figure 1 it will be centered at 2.0 V_{BE} and allowed to swing ± V_{BE}. A capacitor is placed from DS IN2 (Pin 20) to V_{EE}. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in DC level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer.

A unique feature of the data slicer is that the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22 – DS Gnd) to V_{EE} rather than internally to V_{EE}. This is provided in order to reduce switching feedback to the front end. A control pin is provided to shut the data slicer output off (DS "off" – Pin 19). With DS "off" pin at V_{CC} the data slicer output is shut off by shutting down the base drive to the output transistor. When a channel is being monitored to make an RSSI measurement, but not to collect data, the data output may be shut off to save current.

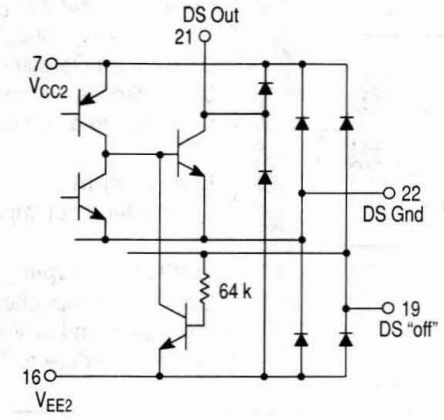
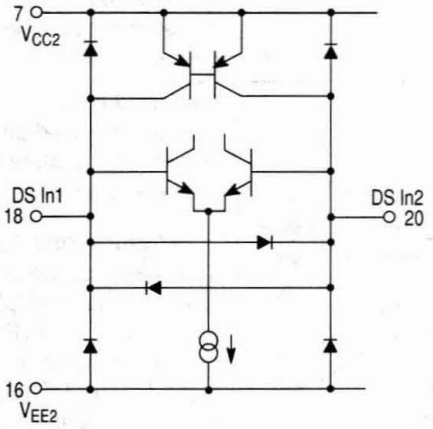
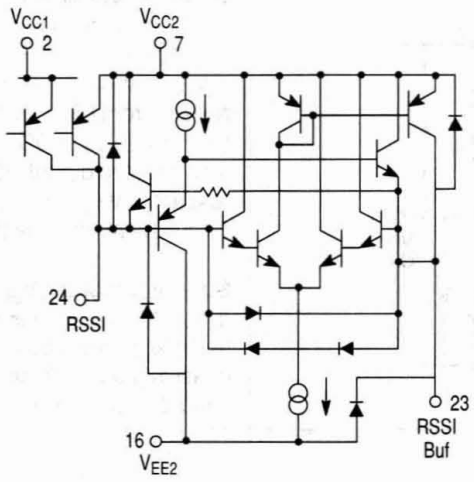
PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1	Mix Out		**Mixer Output** The mixer output impedance is 330 Ω; it matches to 10.7 MHz ceramic filters with 330 Ω input impedance.
2	V_{CC1}		**Supply Voltage (V_{CC1})** This pin is the V_{CC} pin for the Mixer, Local Oscillator, and IF Amplifer. The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
3	IF In		**IF Input** The input impedance at Pin 3 is 330 Ω. It matches the 330 Ω load impedance of a 10.7 MHz ceramic filter. Thus, no external matching is required.
4	IF Dec1		**IF DEC1 & DEC2** IF decoupling pins. Decoupling capacitors should be placed directly at the pins to enhance stability. Two capacitors are decoupled to the RF ground V_{CC1}; one is placed between DEC1 & DEC2.
5	IF Dec2		
6	IF Out		**IF Output** The output impedance is 330 Ω; it matches the 330 input resistance of a 10.7 MHz ceramic filter.

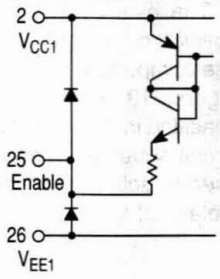
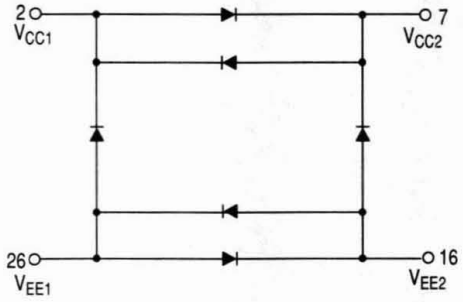
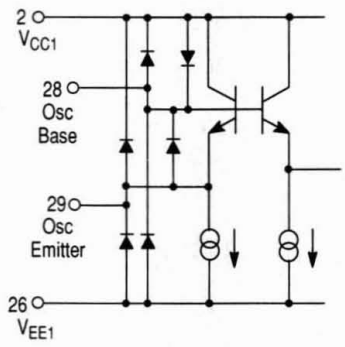
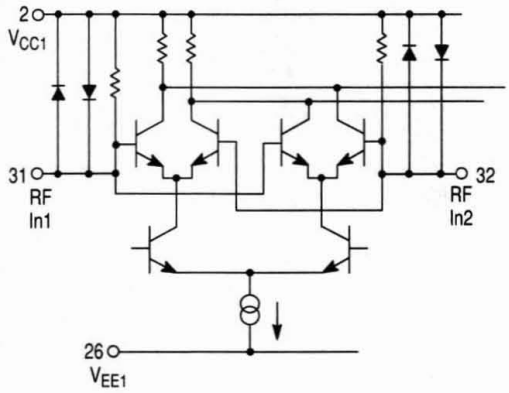
PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
7	V_{CC2}		**Supply Voltage (V_{CC2})** This pin is V_{CC} supply for the Limiter, Quadrature Detector, data slicer and RSSI buffer circuits. In the application PC board this pin is tied to a common V_{CC} trace with V_{CC1}.
8	Lim In		**Limiter Input** The limiter input impedance is 330 Ω.
9	Lim Dec1		**Limiter Decoupling** Decoupling capacitors are placed directly at these pins and to V_{CC} (RF ground). Use the same procedure as in the IF decoupling.
10	Lim Dec2		
11,14, 27 & 28	N/C		**No Connects** There is no internal connection to these pins; however it is recommended that these pins be connected externally to V_{CC} (RF ground).
12	Lim Out		**Limiter Output** The output impedance is low. The limiter drives a quadrature detector circuit with in–phase and quadrature phase signals.
13	Quad		**Quadrature Detector Circuit** The quadrature detector is a doubly balanced four–quadrant multiplier with an internal 5.0 pF capacitor between Pins 12 and 13. An external capacitor may be added to increase the IF signal to Pin 13. The quadrature detector pin is provided to connect the external RLC parallel resonant network which provides the 90 degree phase shift and drives the quadrature detector.
15	Det Gain		**Detector Buffer Amplifier** This is an inverting amplifier. An external feedback resistor from Pin 17 to 15, (the inverting input) controls the output amplitude; another resistor from Pin 15 to the negative supply (Pin 16) sets the DC output level. A 1:1 resistor ratio sets the output DC level at two V_{BE} with respect to V_{EE}. A small capacitor from Pin 17 to 15 can be used to set the bandwidth.
17	Det Out		
16	V_{EE2}		**Supply Ground (V_{EE2})** In the PCB layout, the ground pins (also applies to Pin 26) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground pins.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
19 21 22	DS "off" DS Out DS Gnd		**Data Slicer Off** The data output may be shut off to save current by placing DS "off" (Pin 19) at V_{CC}. **Data Slicer Output** In the application example a 10 kΩ pull–up resistor is connected to the collector of the output transistor at Pin 21. **Data Slicer Ground** All the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22) to ground rather than internally to V_{EE} in order to reduce switching feedback to the front end.
18 20	DS In1 DS In2		**Data Slicer Inputs** The data slicer has differential inputs with back to back diodes across them. The recovered signal is DC coupled to DS IN1 (Pin 18) at nominally V_{18} with respect to V_{EE}; thus, it will maintain $V_{18} \pm V_{BE}$ at Pin 18. DS IN2 (Pin 20) is AC coupled to V_{EE}. The choice of coupling capacitor is dependent on the nature of the data signal. For small signal or continuous bits of the same polarity, the response time is relatively large. On the other hand, for large peak to peak voltage swings or when the DC level at the detector output changes, the response time is short. See the discussion in the application section for external circuit design details.
23 24	RSSI Buf RSSI		**RSSI Buffer** A unity gain amplifier is used to buffer the voltage at Pin 24 to 23.The output of the unity gain buffer (Pin 23) has an active pull up but no pull down. An external resistor is placed from Pin 23 to V_{EE} to provide the pull down. **RSSI** The RSSI output current creates a voltage drop across an external resistor from Pin 24 to V_{EE}. The maximum RSSI current is 26 μA; thus, the maximum RSSI voltage using a 100 kΩ resistor is approximately 2.6 Vdc. Figure 22 shows the RSSI Output Voltage versus Input Signal Level in the application circuit. The negative slew rate is determined by an external capacitor and resistor to V_{EE} (negative supply). The RSSI rise and fall times for various RF input signal levels and R_{24} values without the capacitor, C_{24} are displayed in Figure 24. This is the maximum response time of the RSSI.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
25 26	Enable V_{EE1}		**Enable** The IC regulators are enabled by placing this pin at V_{EE}.
			**V_{CC} and V_{EE} ESD Protection** ESD protection diodes exist between the V_{CC} and V_{EE} pins. It is important to note that significant differences in potential (> 0.5 V_{BE}) between the two V_{CC} pins or between the V_{EE} pins can cause these structures to start to conduct, thus compromising isolation between the supply busses. V_{CC1} & V_{CC2} should be maintained at the same DC potential, as should V_{EE1} & V_{EE2}.
28 29	Osc Base Osc Emitter		**Oscillator Base** This pin is connected to the base lead of the common collector transistor. Since there is no internal bias resistor to the base, V_{CC} is applied through an external choke or coil. **Oscillator Emitter** This pin is connected to the emitter lead; the emitter is connected internally to a current source of about 200 μA. Additional emitter current may be obtained by connecting an external resistor to V_{EE}; $I_E = V_{29}/R_{29}$. Details of circuits using overtone crystal and LC varactor controlled oscillators are discussed in the application section.
31 32	Mix In1 Mix In2		**Mixer Inputs** The parallel equivalent differential input impedance of the mixer is approximately 2.0 kΩ in parallel with 1.0 pF. This equates to a single ended input impedance of 1.0 kΩ in parallel with 2.0 pF. The application circuit utilizes a SAW filter having a differential output that requires a 2.0 kΩ II 2.0 pF load. Therefore, little matching is required between the SAW filter and the mixer inputs. This and alternative circuits are discussed in more detail in the application section.

APPLICATIONS INFORMATION

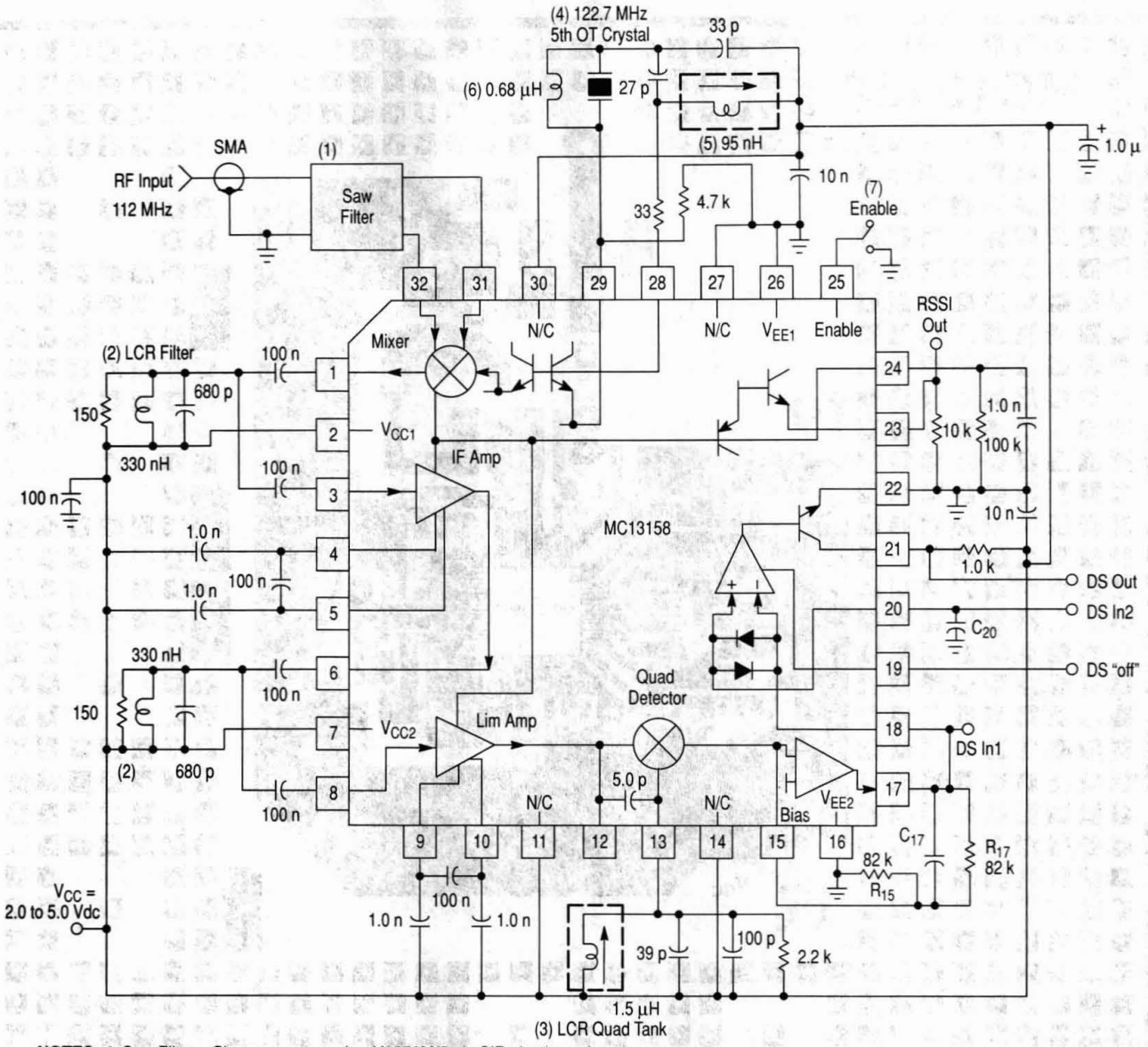
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 13 and 14 show the placement for the components specified in the application circuit (Figure 12). The application circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but alternate components should give similar results.

Figure 12. Application Circuit



NOTES: 1. Saw Filter – Siemens part number Y6970M(5 pin SIP plastic package).

2. An LCR filter reduces the broadband noise in the IF; ceramic filters may be used for data rates under 500 kHz. 4.0 dB insertion loss filters optimize the linearity of RSSI.
3. The quadrature tank components are chosen to optimize linearity of the recovered signal while maintaining adequate recovered signal level. 1.5 µH 7.0 mm variable shielded inductor: Toko part # 292SNS–T1373Z. The shunt resistor is approximately equal to Q(2πfL), where Q ~ 18 (3.0 dB BW = 600 kHz).
4. The local oscillator circuit utilizes a 122.7 MHz, 5th overtone, series resonant crystal specified with a frequency tolerance of 25 PPM, ESR of 120 Ω max. The oscillator configuration is an emitter coupled butler.
5. The 95 NH (Nominal) inductor is a 7.0 mm variable shielded inductor: Coilcraft part # 150–04J08S or equivalent.
6. 0.68 µH axial lead chokes (molded inductor): Coilcraft part # 90–11.
7. To enable the IC, Pin 25 is taken to V_{EE}. The external pull down resistor at Pin 29 could be linked to the enable function; otherwise if it is taken to V_{EE} as shown, it will keep the oscillator biased at about 500 µA depending on the V_{CC} level.
8. The other resistors and capacitors are surface mount components.

Figure 13. Circuit Side Component Placement

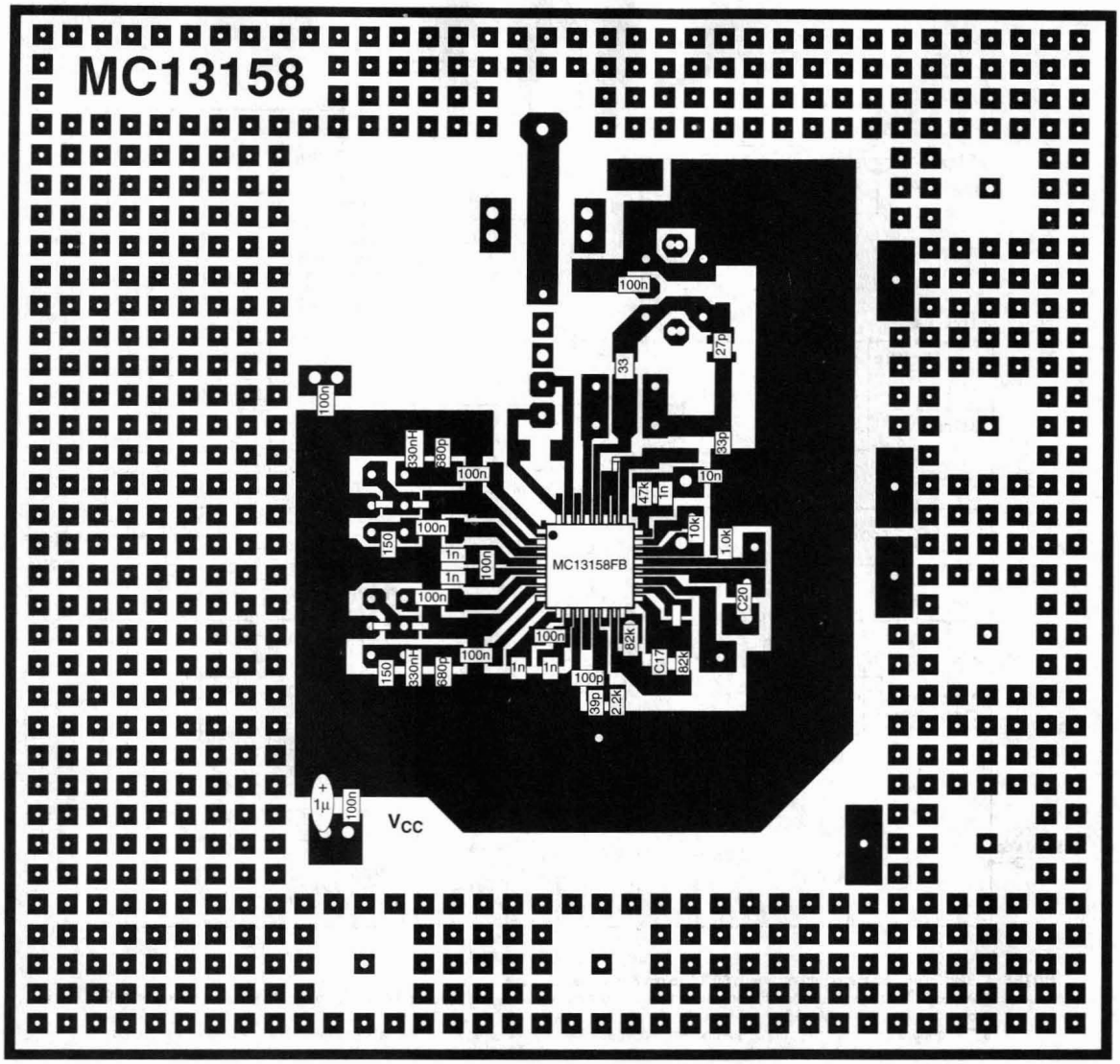
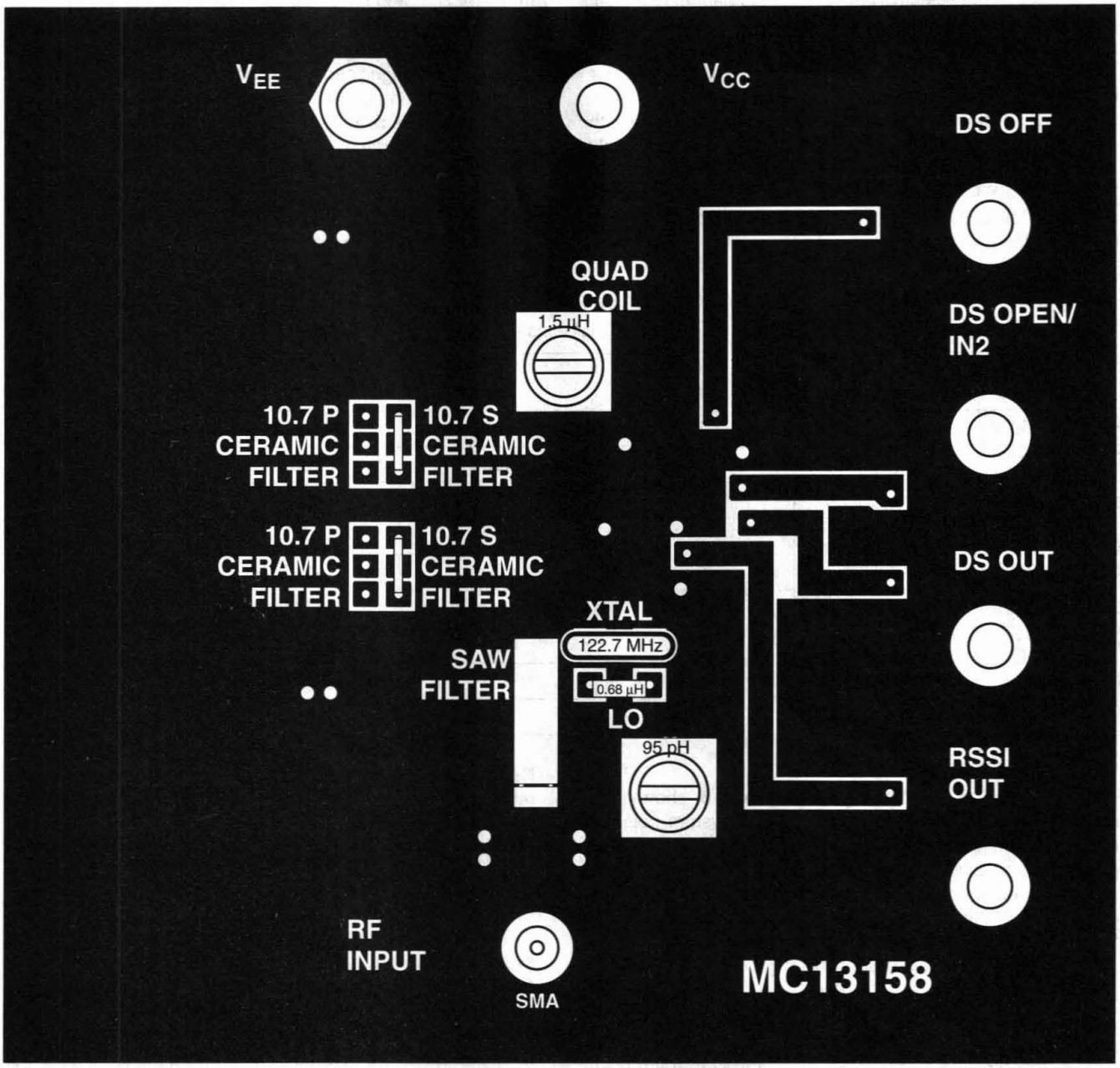


Figure 14. Ground Side Component Placement



Input Matching/Components

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection. In a wideband system the primary sensitivity of the receiver backend may be achieved before the last mixer. Bandpass filtering in the limiting IF is costly and difficult to achieve for bandwidths greater than 280 kHz.

The SAW filter should be selected to easily interface with the mixer differential input impedance of approximately 2.0 kΩ in parallel with 1.0 pF. The PC board is dedicated to the Siemens SAW filter (part number Y6970M); the part is designed for DECT at 112 MHz 1st IF frequency. It is designed for a load impedance of 2.0 kΩ in parallel with 2.0 pF; thus, no or little input matching is required between the SAW filter and the mixer.

The Siemens SAW filter has an insertion loss of typically 10 dB and a 3.0 dB bandwidth of 1.0 MHz. The relatively high insertion loss significantly contributes to the system noise and a filter having lower insertion loss would be desirable. In existing low loss SAW filters, the required load impedance is 50 Ω; thus, interface matching between the filter and the mixer will be required. Figure 15 is a table of the single–ended mixer input impedance. A careful noise analysis is necessary to determine the secondary contribution to system noise.

Figure 15. Mixer Input Impedance
(Single–ended)

f (MHz)	Rs (Ω)	Xs (Ω)	Rp (Ω)	Xp (Ω)	Cp (pF)
50	930	–350	1060	–2820	1.1
100	480	–430	865	–966	1.6
150	270	–400	860	–580	1.8
200	170	–320	770	–410	1.9
250	130	–270	690	–330	1.85
300	110	–250	680	–300	1.8
400	71	–190	580	–220	1.8
500	63	–140	370	–170	1.9
600	49	–110	300	–130	2.0

System Noise Considerations

The system block diagram in Figure 16 shows the cascaded noise stages contributing to the system noise; it represents the application circuit in Figure 12 and a low noise preamp using a MRF941 transistor (see Figure 17). The preamp is designed for a conjugately matched input and output at 2.0 Vdc V_{CE} and 3.0 mAdc I_c. S–parameters at 2.0 V, 3.0 mA and 100 MHz are:

S11 = 0.86, –20
S21 = 9.0, 164
S12 = 0.02, 79
S22 = 0.96, –12

The bias network sets V_{CE} at 2.0 V and I_c at 3.0 mA for V_{CC} = 3.0 to 3.5 Vdc. The preamp operates with 18 dB gain and 2.7 dB noise figure.

In the cascaded noise analysis the system noise equation is:

$$Fsystem = F1 + [(F2–1)/G1] + [(F3–1)]/[(G1)(G2)]$$

where:

F1 = the Noise Factor of the Preamp
G1 = the Gain of the Preamp
F2 = the Noise factor of the SAW Filter
G2 = the Gain of the SAW Filter
F3 = the Noise factor of the Mixer

Note: the proceeding terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

$F = \log^{-1}[(NF \text{ in dB})/10]$ and similarly

$G = \log^{-1}[(Gain \text{ in dB})/10]$

The noise figure and gain measured in dB are shown in the system block diagram. The mixer noise figure is typically 14 dB and the SAW filter adds typically 10 dB insertion loss. Addition of a low noise preamp having a 18 dB gain and 2.7 dB noise figure not only improves the system noise figure but it increases the reverse isolation from the local oscillator to the antenna input at the receiver. Calculating in terms of gain and noise factor yields the following:

F1 = 1.86; G1 = 63.1
F2 = 10; G2 = 0.1
F3 = 25.12

Thus, substituting in the equation for system noise factor:

Fsystem = 5.82; NFsystem = 7.7 dB

Figure 16. System Block Diagram for Noise Analysis

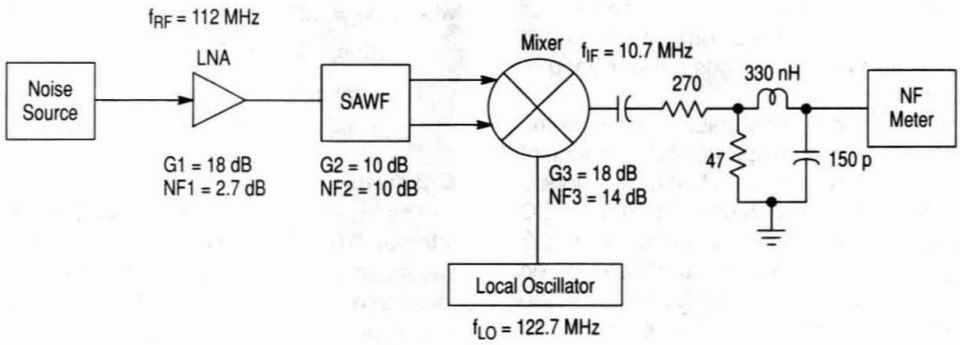
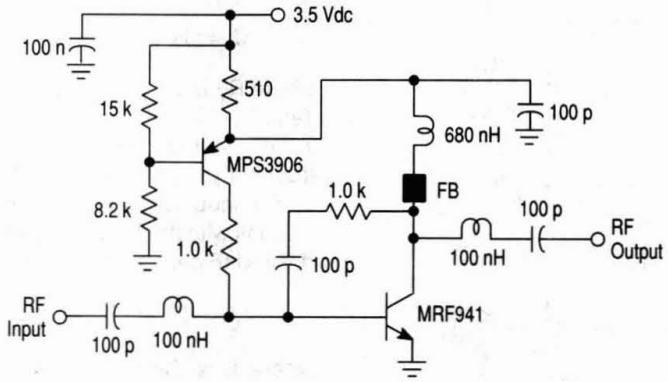


Figure 17. 112 MHz LNA



LOCAL OSCILLATORS

VHF Applications

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. The local oscillator in the application circuit (Figure 12) shows a 5th overtone oscillator at 122.7 MHz. This circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_o, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_o has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned "off" the crystal resonant frequency it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_o, is placed in parallel with the crystal. L_o is chosen to be resonant with the crystal parallel capacitance, C_o, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

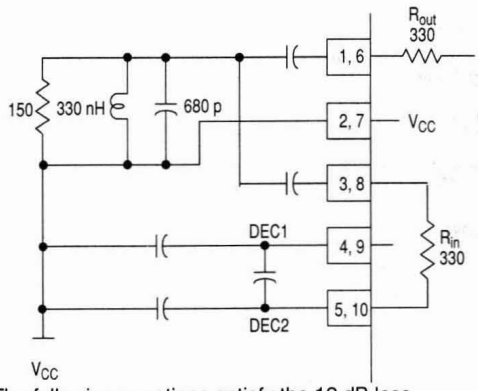
IF Filtering/Matching

In wideband data systems the IF bandpass needed is greater than can be found in low cost ceramic filters operating at 10.7 MHz. It is necessary to bandpass limit with LC networks or series–parallel ceramic filter networks. Murata offers a series–parallel resonator pair (part number

KMFC545) with a 3.0 dB bandwidth of ± 325 kHz and a maximum insertion loss of 5.0 dB. The application PC board is laid out to accommodate this filter pair (a filter pair is used at both locations of the split IF). However, even using a series parallel ceramic filter network yields only a maximum bandpass of 650 kHz. In some applications a wider band IF bandpass is necessary.

A simple LC network yields a bandpass wider than the SAW filter but it does reduce an appreciable amount of wideband IF noise. In the application circuit an LC network is specified using surface mount components. The parallel LC components are placed from the outputs of the mixer and IF amplifier to the V_{CC} trace; internal 330 loads are connected from the mixer and IF amplifier outputs to DEC2 (Pin 5 and 10 respectively).This loads the outputs with the optimal load impedance but creates a low insertion loss filter. An external shunt resistor may be used to widen the bandpass and to acquire the 10 dB composite loss necessary to linearize the RSSI output. The equivalent circuit is shown in Figure 18.

Figure 18. IF LCR Filter



The following equations satisfy the 12 dB loss (1:4 resistive ratio):

$$(Rext)(330)/(Rext + 330) = Requivalent$$
$$Requivalent/(Requivalent + 330) = 1/4$$

Solve for Requivalent:

$$4(Requivalent) = Requivalent + 330$$
$$3(Requivalent) = 330$$
$$Requivalent = 110$$

Substitute for Requivalent and solve for Rext:

$$330(Rext) = 110(Rext) + (330)(110)$$
$$Rext = (330)(110)/220$$
$$Rext = 165\ \Omega$$

The IF is 10.7 MHz although any IF between 10 to 20 MHz could be used. The value of the coil is lowered from that used in the quadrature circuit because the unloaded Q must be maintained in a surface mount component. A standard value component having an unloaded Q = 100 at 10.7 MHz is 330 nH; therefore the capacitor is 669 pF. Standard values have been chosen for these components;

$$Rext = 150\ \Omega$$
$$C = 680\ pF$$
$$L = 330\ nH$$

Computation of the loaded Q of this LCR network is

$$Q = Requivalent/X_L$$

where: $X_L = 2\pi fL$ and Requivalent is 103 Ω

Thus, $Q = 4.65$

The total system loss is

$$20 \log (103/433) = -12.5\ dB$$

Quadrature Detector

The quadrature detector is coupled to the IF with an internal 5.0 pF capacitor between Pins 12 and 13. For wideband data applications, the drive to the detector can be increased with an additional external capacitor between these pins; thus, the recovered signal level output is increased for a given bandwidth

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \qquad [1]$$

where R_T is the equivalent shunt resistance across the LC Tank

X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by

$$f_c = [2\pi\ (LC_p)^{1/2}]^{-1} \qquad [2]$$

where L is the parallel tank inductor C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 10.7 MHz and a loaded Q of 18. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 10.7 MHz and an IF bandpass of 600 kHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 139 pF. (The minimum value here should be much greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF). Thus, C_p = Cint + Cext = 142 pF.

Rewrite equation (2) and solve for L:

$$L = (0.159)^2/(C_p fc^2)$$

L = 1.56 µH; Thus, a standard value is choosen:

L = 1.56 µH (tunable shielded inductor)

The value of the total damping resistor to obtain the required loaded Q of 18 can be calculated by rearranging equation (1):

$$R_T = Q(2\pi fL)$$
$$R_T = 18(2\pi)(10.7)(1.5) = 1815\ \Omega$$

The internal resistance, Rint at the quadrature tank Pin 13 is approximately 13 kΩ and is considered in determining the external resistance, Rext which is calculated from

$$Rext = ((R_T)(Rint))/(Rint - R_T)$$
$$Rext = 2110; \text{ Thus, choose the standard value:}$$
$$Rext = 2.2\ k\Omega$$

It is important to set the DC level of the detector output at Pin 17 to center the peak to peak swing of the recovered signal. In the equivalent internal circuit shown in the Pin Function Description, the reference voltage at the positive terminal of the inverting op amp buffer amplifier is set at 1.0 V_{BE}. The detector DC level, V_{17} is determined by the following equation:

$$V_{17} = [((R_{15}/R_{17}) + 1)/(R_{15}/R_{17})]\ V_{BE}$$

Thus, for a 1:1 ratio of R_{15}/R_{17}, V_{17} = 2.0 V_{BE} = 1.4 Vdc. Similarly for a 2:1, V_{17} = 1.5 V_{BE} = 1.05 Vdc; and for 3:1, V_{17} = 1.33 V_{BE} = 0.93 Vdc.

Figure 19 shows the detector "S–Curves", in which the resistor ratio is varied while maintaining a constant gain (R_{17} is held at 62 k). R_{15} is 62 k for a 1:1 ratio; while R_{15} = 120 k and 180 k to produce the 2:1 and 3:1 ratios. The IF signal into the detector is swept ± 500 kHz about the 10.7 MHz IF center frequency. The resulting curve show how the resistor ratio and the supply voltage effects the symmetry of the "S–curve" (Figure 21 Test Setup). For the 3:1 and 2:1 ratio, symmetry is maintained with V_S from 2.0 to 5.0 Vdc; however, for the 1:1 ratio, symmetry is lost at 2.0 Vdc.

Figure 19. Detector Output Voltage versus Frequency Deviation

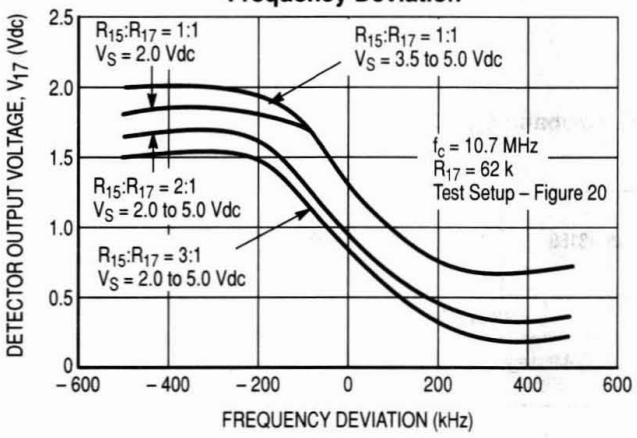
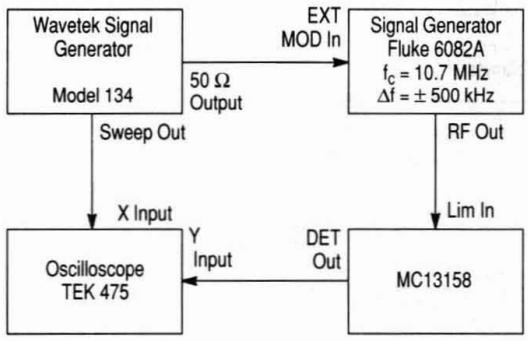


Figure 20. Demodulator "S–Curve" Test Setup



Data Slicer Circuit

C_{20} at the input of the data slicer is chosen to maintain a time constant long enough to hold the charge on the capacitor for the longest strings of bits at the same polarity. For a data rate at 576 kHz a bit stream of 15 bits at the same polarity would equate to an apparent data rate of approximately 77 kbps or 38 kHz. The time constant would be approximately 26 μs. The following expression equates the time constant, t, to the external components:

$$t = 2\pi\ (R_{18})(C_{20})$$

Solve for C_{20}:

$$C_{20} = t/2\pi\ (R_{18})$$

where the effective resistance R_{18} is a complex function of the demodulator feedback resistance and the data slicer input circuit. In the data input network the back to back diodes form a charge and discharge path for the capacitor at Pin 20; however, the diodes create a non–linear response. This resistance is loaded by the ß, beta of the detector output transistor; beta =100 is a typical value (see Figure 21). Thus, the apparent value of the resistance at Pin 18 (DS IN1) is approximately equal to:

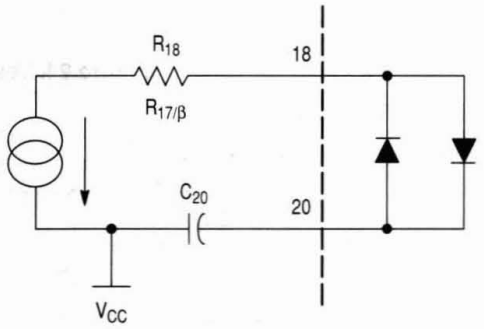
$$R_{18} \sim R_{17}/100$$

where R_{17} is 82 kΩ, the feedback resistor from Pin 17 to 15. Therefore, substituting for R_{18} and solving for C_{20}:

$$C_{20} = 15.9\ (t)/R_{17} = 5.04\ nF$$

The closest standard value is 4.7 nF.

Figure 21. Data Slicer Equivalent Input Circuit



RSSI

In Figure 22, the RSSI versus RF Input Level shows the linear response of RSSI over a 65 dB range but it has extended capability over 80 dB from –80 dBm to +10 dBm. The RSSI is measured in the application circuit (Figure 12) in which a SAW filter is used before the mixer; thus, the overall sensitivity is compromised for the sake of selectivity. The curves are shown for three filters having different bandwidths:

1) LCR Filter with 2.3 MHz 3.0 dB BW (Circuit and Component Placement is shown in Figure 12)
2) Series–Parallel Ceramic Filter with 650 kHz 3.0 dB BW (Murata Part # KMFC–545)
3) Ceramic Filter with 280 kHz 3.0 dB BW.

Figure 22. RSSI Output Voltage versus Signal Input Level

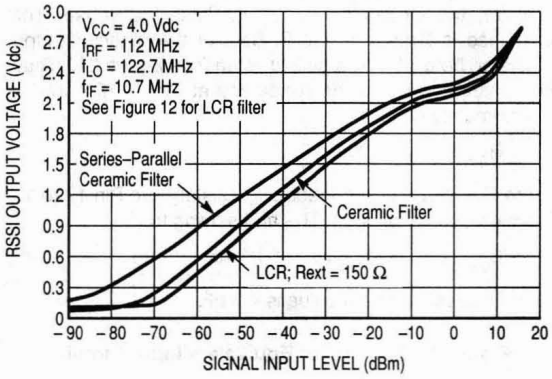
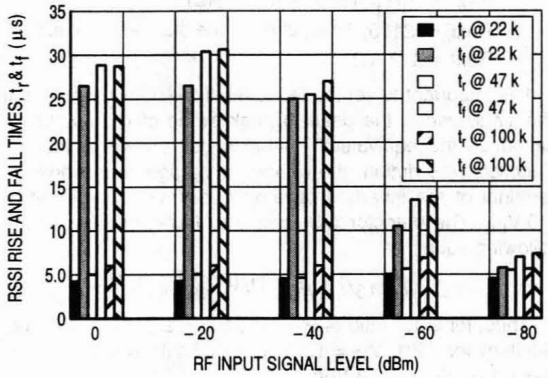


Figure 23. RSSI Output Rise and Fall Times versus RF Input Signal Level



SINAD Performance

Figure 24 shows a test setup for a narrowband demodulator output response in which a C–message filter and an active de–emphasis filter is used following the demodulator. The input is matched using a 1:4 impedance transformer. The SINAD performance is shown in Figure 25 with no preamp and in Figure 26 with a preamp (Preamp – Figure 16). The 12 dB SINAD sensitivity is –101 dBm with no preamp and –113 dBm with the preamp.

Figure 24. Test Setup for Narrowband SINAD

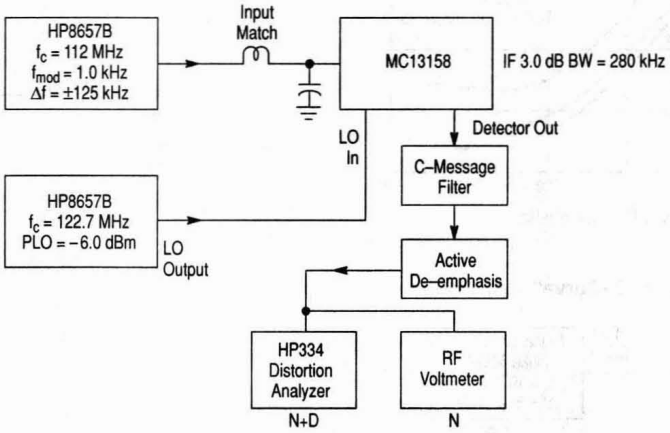


Figure 25. S+N+D, N+D, N versus Input Signal Level (without preamp)

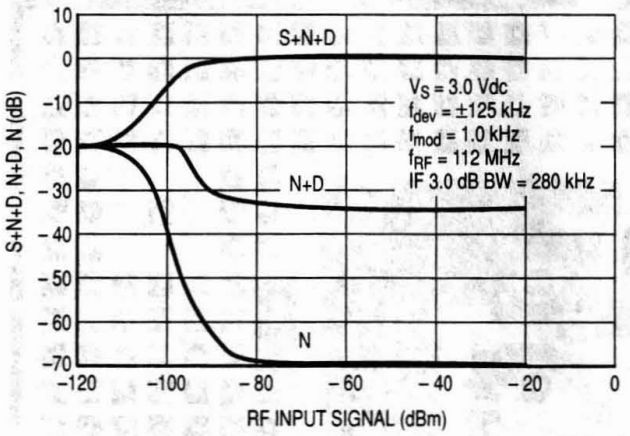


Figure 26. S+N+D, N+D, N versus Input Signal Level (with preamp)

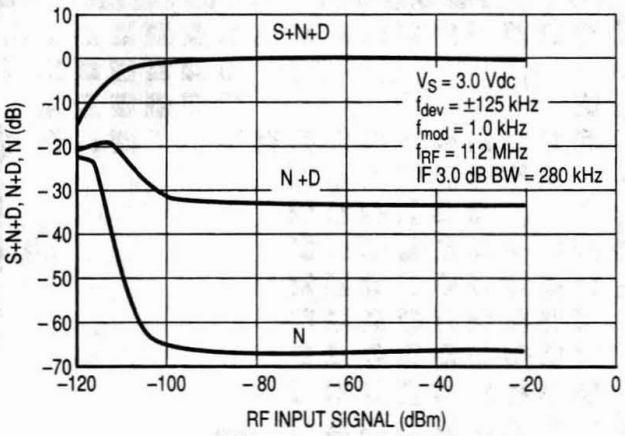


Figure 27. Input IP3, 1.0 dB Compression Pt. Test Setup

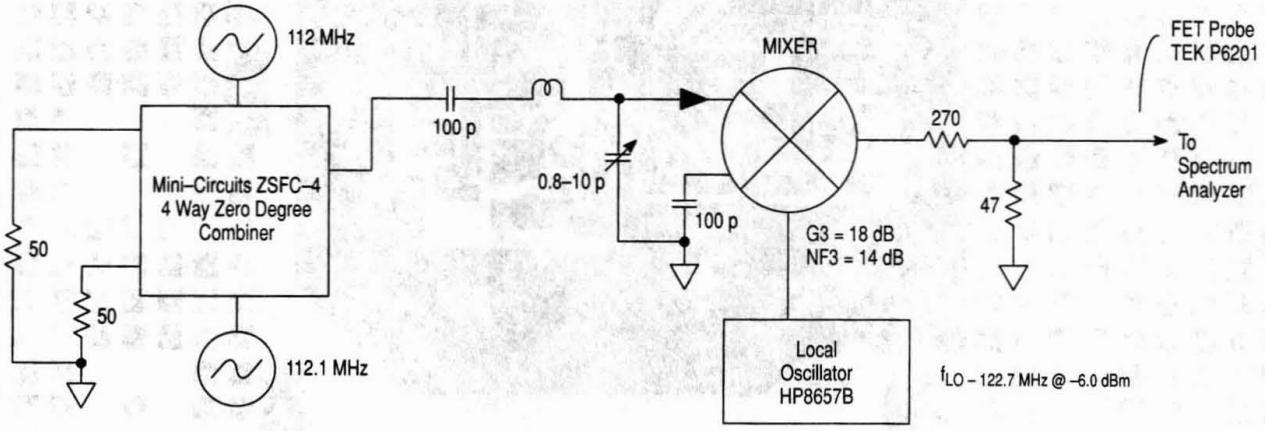


Figure 28. –1.0 dB Compression Pt. and Input Third Order Intercept

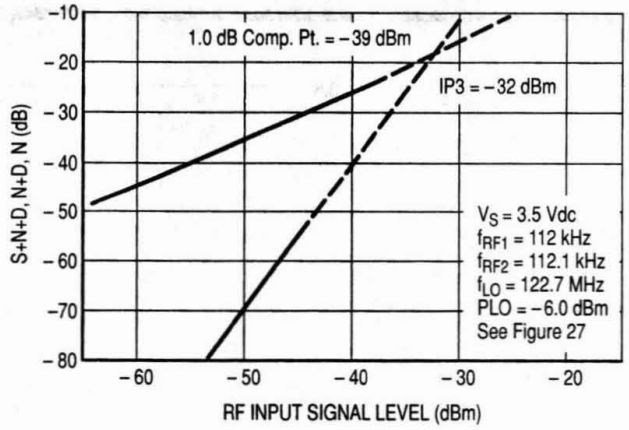

1.0 dB Comp. Pt. = –39 dBm
IP3 = –32 dBm
V_S = 3.5 Vdc
f_{RF1} = 112 kHz
f_{RF2} = 112.1 kHz
f_{LO} = 122.7 MHz
PLO = –6.0 dBm
See Figure 27
S+N+D, N+D, N (dB)
RF INPUT SIGNAL LEVEL (dBm)

Figure 29. Circuit Side View

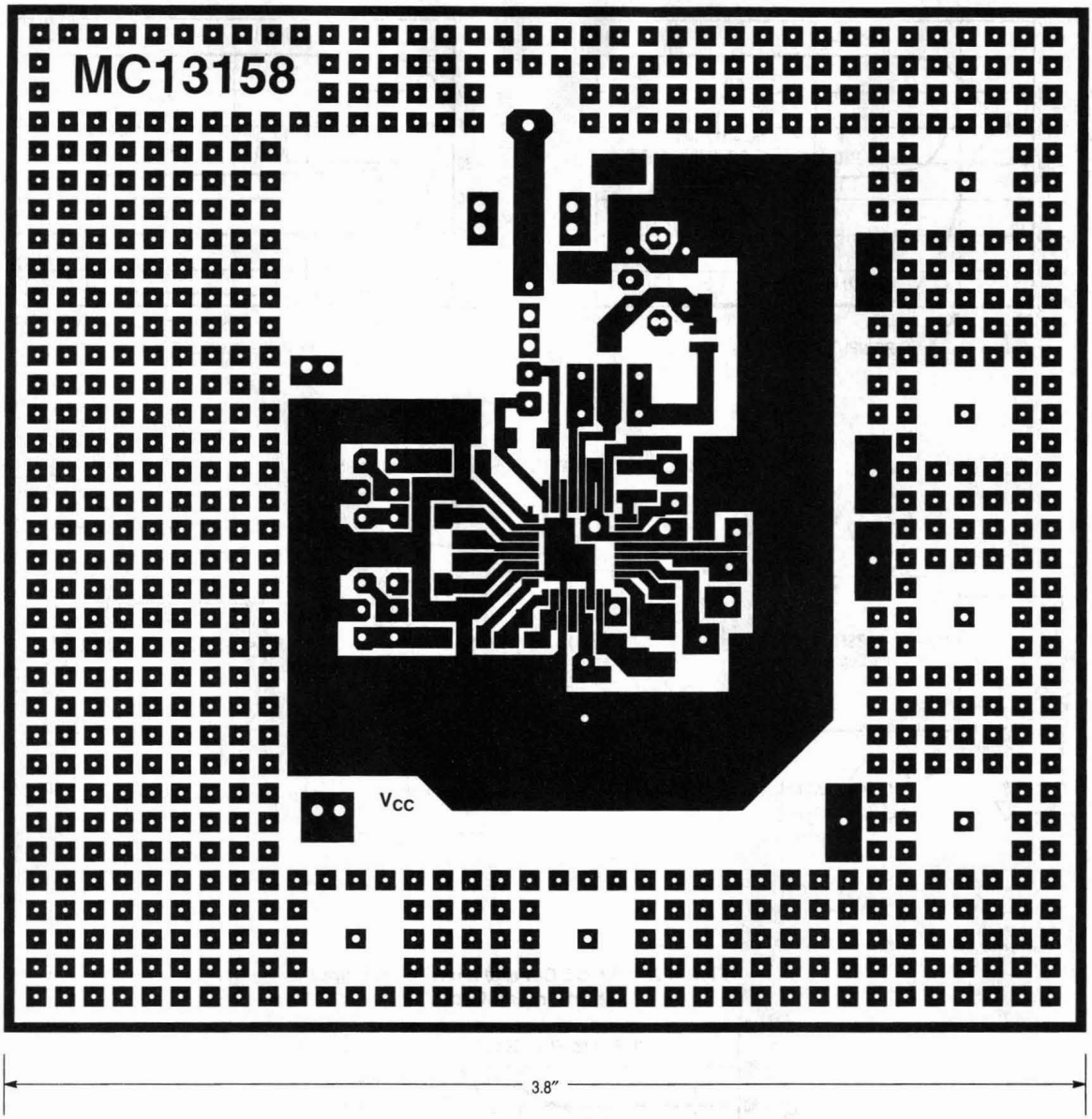
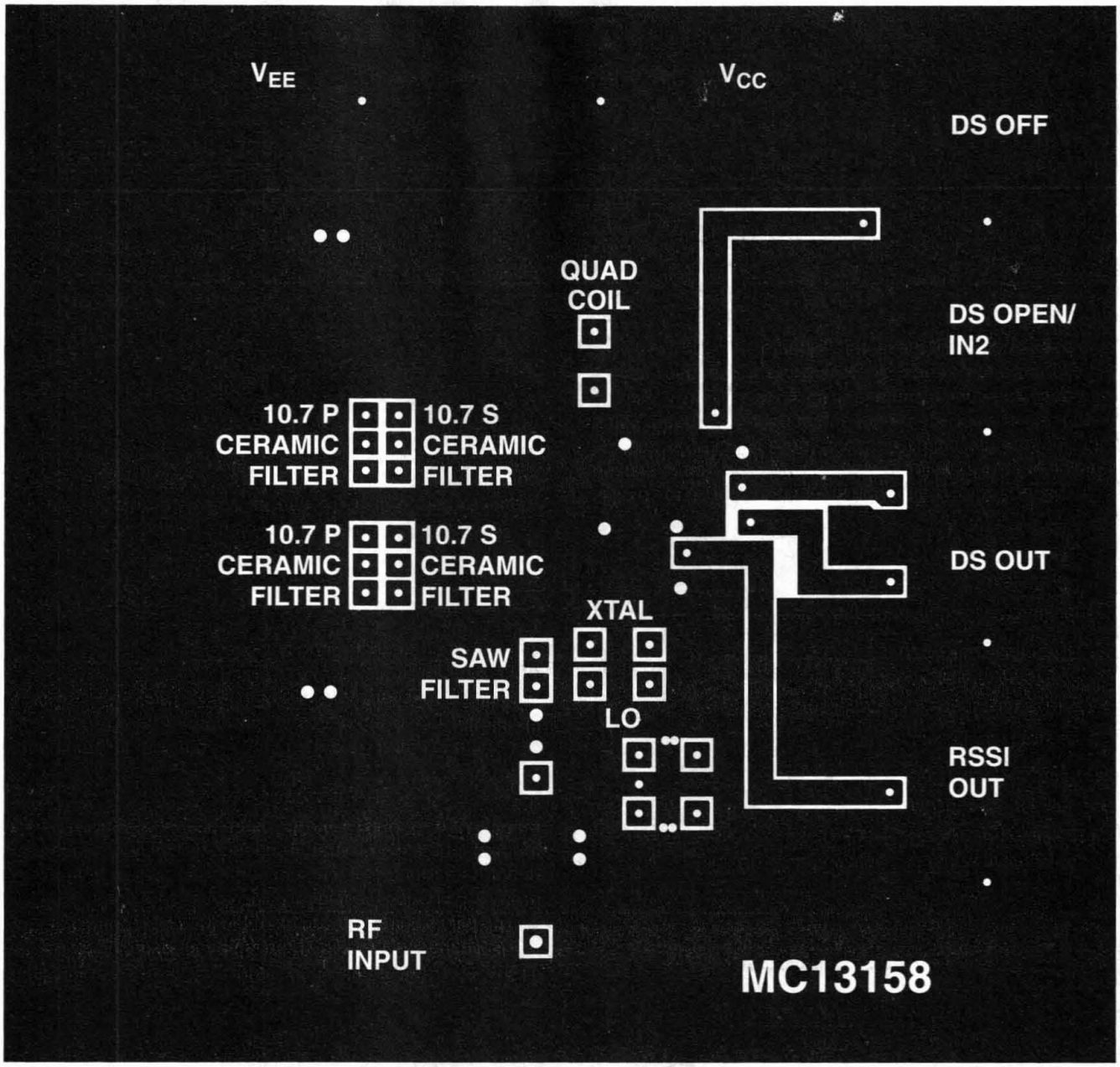


Figure 30. Ground Side View



MOTOROLA

MC13159

Advance Information

Wideband FM IF Subsystem

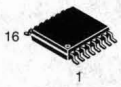
WIDEBAND FM IF SUBSYSTEM FOR PHS AND DIGITAL APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

The MC13159 is a wideband FM IF subsystem that is designed for high performance data and digital applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's RF bipolar process. The MC13159 includes a mixer, local oscillator buffer amplifier, IF amplifier, limiter amplifier and RSSI functions. The mixer is useful for a 240 MHz input used in a single–ended/balanced differential configuration. The IF and limiter amplifier are separated so that an external filter can be used in series, or connected directly with an external capacitor. The RSSI output is derived by summing the output of both the IF and Limiter sections. An enable control is provided to power down the IC for power management in battery powered applications.

Suitable applications include PHS, DECT, PDC, and PCS telephones, wideband wireless data links, and other battery powered radio systems.

- Designed for PHS Applications
- 2.7 to 5.5 V Operating Voltage
- Low Drain Current: 5.5 mA (Typ)
- Wide Input Dynamic Range of Mixer (Maximum –16 dBm Input)
- Enable Function for Power Down Mode
- Over 80 dB of RSSI Dynamic Range (AC Coupling between IF Amplifier and Limiter Amplifier)
- Few External Components Required

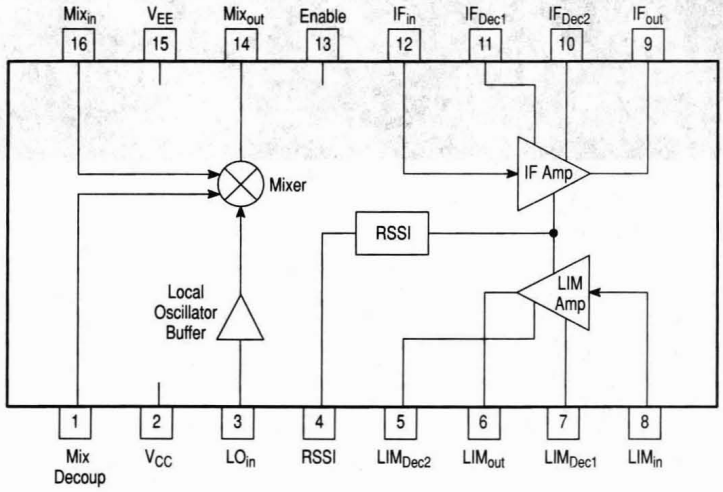


DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13159DTB	T_A = –30° to +85°C	TSSOP–16

Simplified Block Diagram



This device contains 164 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{S(max)}$	6.0	Vdc
Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_S	2.7 to 5.5	Vdc
Input Frequency	f_{in}	10 to 600	MHz
Ambient Temperature Range	T_A	–30 to +85	°C
Input Signal Level at Local Input	V_{in}	–10	dBm

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = 3.0 V; No Input Signal)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Total Drain Current 1	Active Mode	I_{CC1}	4.5	5.5	7.5	mA
Total Drain Current 2	Disable Mode	I_{CC2}	–	0.1	10	μA

AC ELECTRICAL CHARACTERISTICS

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
MIXER (T_A = 25°C; V_S = 3.0; f_{RF} = 240 MHz, f_{LO} = 229.3 MHz)						
Mixer Conversion Gain	50 Ω Termination Input Matched	–	11 –	14 21	17 –	dB
Noise Figure	Input Matched	NF	–	14	–	dB
Mixer Input Impedance	Single–Ended	Rp Cp	– –	400 4.0	– –	Ω pF
Mixer Output Impendance	–	–	–	330	–	Ω
1.0 dB Gain Compression	@Mix_{in}	Vicp	–	–16	–	dBm
3rd Order Input Intercept	50 Ω Termination	IIP3	–	–8.0	–	dBm
IF AMPLIFIER SECTION (T_A = 25°C; V_S = 3.0 V; f_{IF} = 10.7 MHz)						
IF Gain	f = 10.7 MHz	–	32	36	45	dB
Input Impedance	–	–	–	330	–	Ω
Output Impedance	–	–	–	330	–	Ω
LIMITING AMPLIFIER SECTION (T_A = 25°C; V_S = 3.0 V; f_{IF} = 10.7 MHz)						
Limiter Gain	f = 10.7 MHz	–	–	70	–	dB
Input Impedance	–	–	–	330	–	Ω
Output Swing	–	–	400	500	600	mVpp
Output Rise Time	–	–	–	10	–	ns
Output Fall Time	–	–	–	20	–	ns
RSSI SECTION (T_A= 25°C; V_S = 3.0 V; f_{IF} = 10.7 MHz)						
RSSI Slope	–	–	10	14	18	mV/dB
RSSI Output DC Voltage 1	No Input Signal	–	0.8	0.9	1.0	V
RSSI Output DC Voltage 2	V_{IF} = –85 dBm	–	0.82	0.95	1.02	V
RSSI Output DC Voltage 3	V_{IF} = –80 dBm	–	0.85	1.0	1.15	V
RSSI Output DC Voltage 4	V_{IF} = –40 dBm	–	1.4	1.5	1.6	V
RSSI Output DC Voltage 5	V_{in} = 0 dBm	–	1.95	2.1	2.25	V

Figure 1. Test Circuit

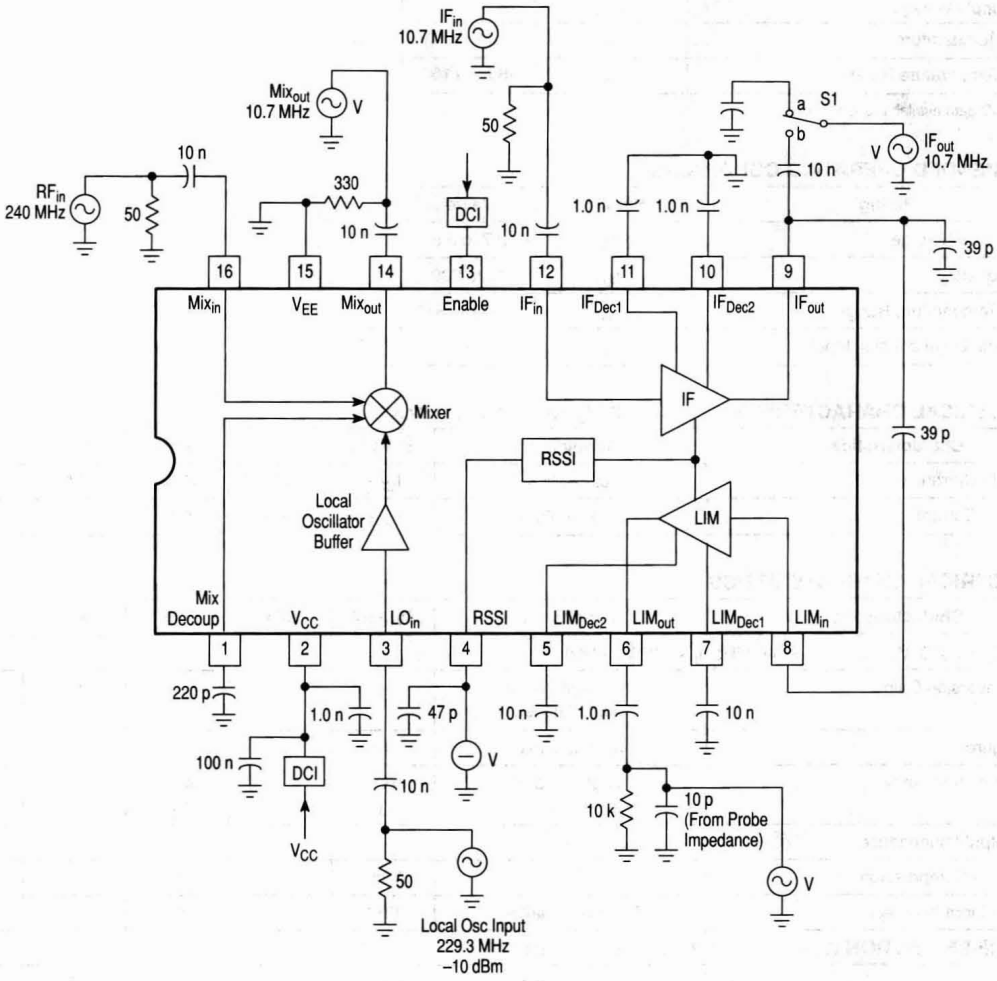
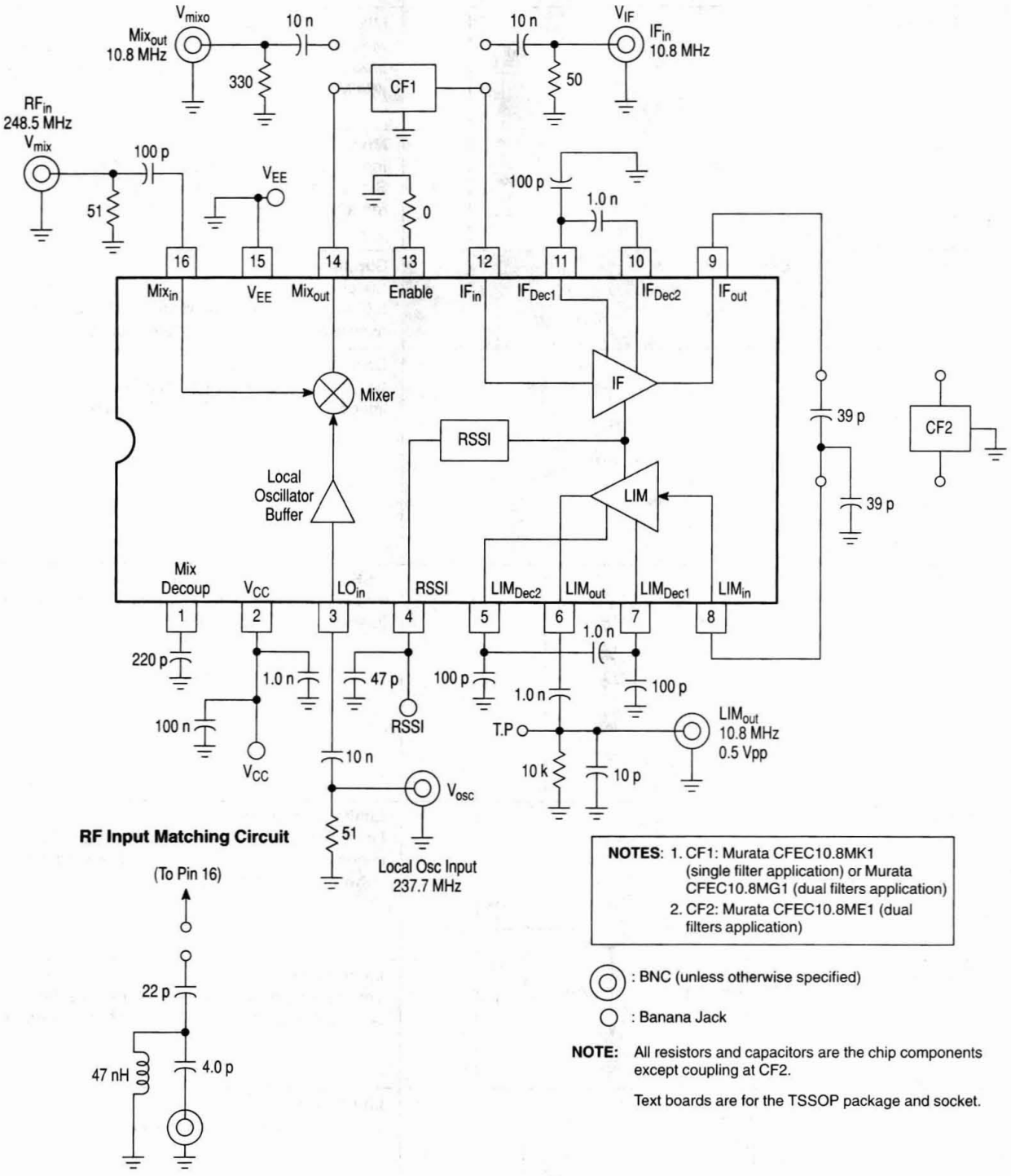


Figure 2. Test Circuit for Evaluation



RF Input Matching Circuit

NOTES: 1. CF1: Murata CFEC10.8MK1 (single filter application) or Murata CFEC10.8MG1 (dual filters application)
2. CF2: Murata CFEC10.8ME1 (dual filters application)

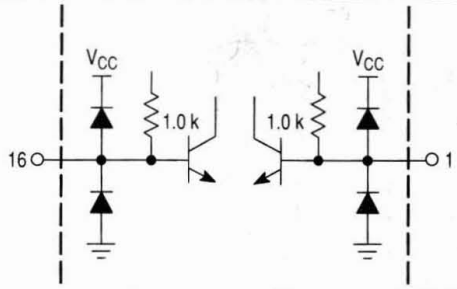
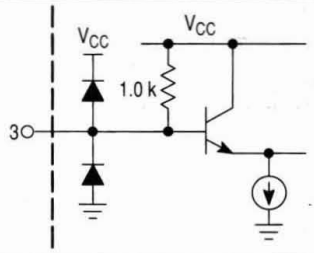
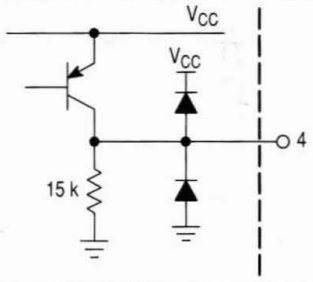
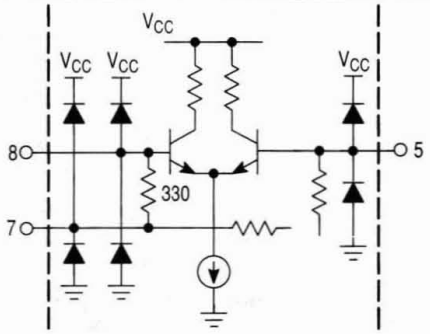
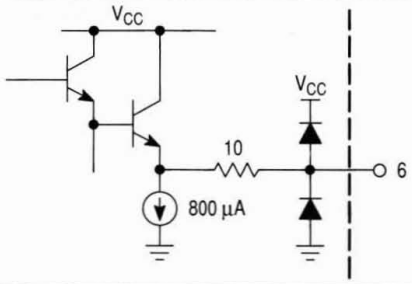
: BNC (unless otherwise specified)

: Banana Jack

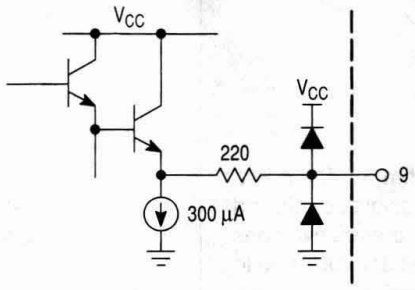
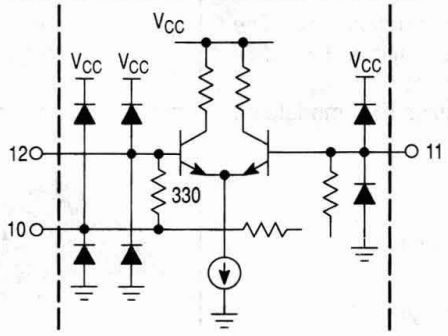
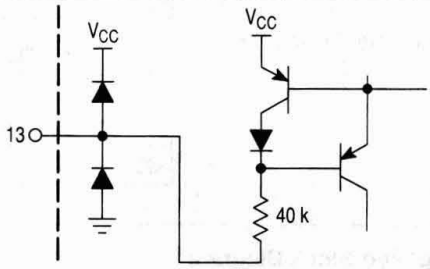
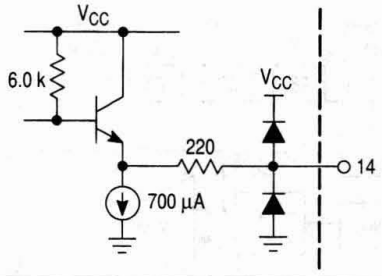
NOTE: All resistors and capacitors are the chip components except coupling at CF2.

Text boards are for the TSSOP package and socket.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description
1	Mix Decoup		**Mixer Decoupling** Mixer decoupling pin. 220 pF is decoupled to the RF ground. This pin also can be used for differential input with Mix_{in}.
16	Mix_{in}		**Mixer Input** Input impedance is about 400 Ω at 240 MHz. Single–ended matching section at 240 MHz is referenced at application circuit.
2	V_{CC}		**Supply Voltage** Supply voltage range range is from 2.7 Vdc to 5.5 Vdc. 1.0 nF of decoupling capacitor is placed directly at this pin to reduce the floor noise.
3	LO_{in}		**Local Oscillator Input** Connected to external local oscillator. Input impedance is about 900 Ω at 230 MHz.
4	RSSI		**RSSI** The RSSI current creates a voltage drop across an internal 15 kΩ resistor.
5 7	LIM_{Dec2} LIM_{Dec1}		**Limiter Decoupling** Limiter decoupling pins. Decoupling capacitors are connected to the RF ground, and one is placed between Dec1 and Dec2.
8	LIM_{in}		**Limiter Input** The input impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
6	LIM_{out}		**Limiter Output** The output level is about 0.5 Vpp.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description
9	IF_{out}		**IF Output** The output impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
10 11	IF_{Dec2} IF_{Dec1}		**IF Decoupling** IF decoupling pins. Decoupling capacitor is connected from Dec1 to the RF ground, and one is placed between Dec1 and Dec2.
12	IF_{in}		**IF Input** The input impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
13	Enable		**Enable** The IC regulators are enabled by placing this pin at V_{EE}.
14	Mix_{out}		**Mixer Output** The mixer output impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
15	V_{EE}		**Supply Ground**

MOTOROLA

MC13173

Infrared Integrated Transceiver IC

INFRARED TRANSCEIVER

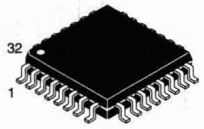
SEMICONDUCTOR TECHNICAL DATA

The MC13173 is a low power infrared integrated system (IRIS). It is a unique blend of a split IF wideband FM receiver and a specialized infrared LED transmitter. This device was designed to provide communications between portable computers via a half duplex infrared link at data rates up to 200 kbps.

The receiver includes a mixer, IF amplifier and limiter and data slicer. The IF amplifier is split to accommodate two low cost cascaded filters. The RSSI output is derived by summing the output of both IF sections.

The transmitter section includes a frequency synthesizer, FSK modulator, harmonic low pass filter and an IR LED driver.

- Transmitter Operates in Two Modes:
  - On/Off Pulsing for Remote Control
  - FSK Modulation at 1.4 MHz for Data Communications
- Over 70 dB of RSSI Range
- Split IF for Improved Filtering and Extended RSSI Range
- Digitally controlled Via a Six Line Interface Bus
- Individual Circuit Blocks Can Be Powered Down When Not In Use for Power Conservation

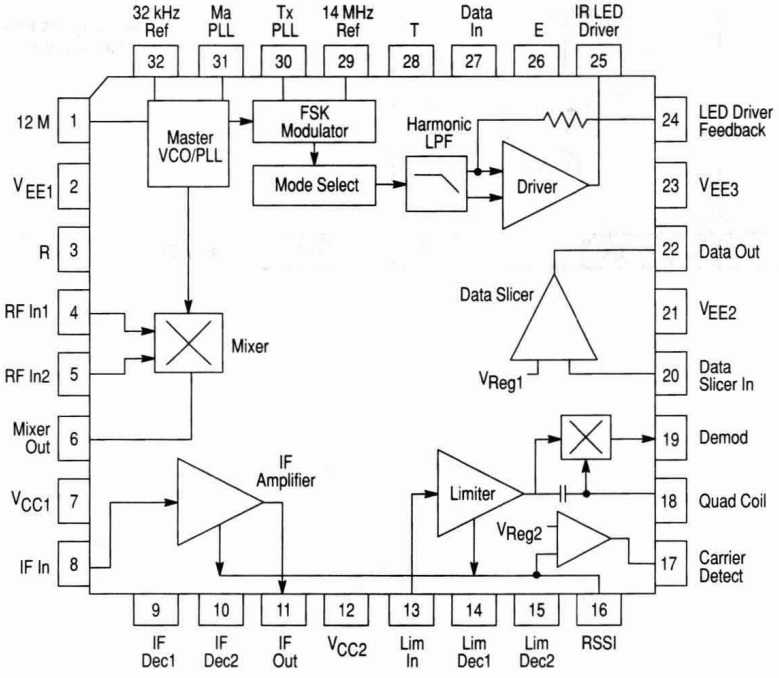


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13173FTB	T_A = – 40° to +85°C	TQFP–32

Simplified Block Diagram



This device contains 914 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC} - V_{EE}$	6.0	Vdc
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	$V_{CC} - V_{EE}$	2.7 to 5.5	Vdc
Ambient Temperature Range	T_A	– 40 to +85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Control Pin Logic State T	R	E	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (See Table 2)				7, 12	I_{CC}				
Receive Mode	0	1	0			–	6.5	9.0	mA
Communications Mode	1	0	0			–	4.75	8.0	
A/V Mode	1	0	1			–	1.5	–	
Standby Mode	0	0	0			–	<10	–	nA
Master PLL Charge Current				31	I_{MA}	–	±25	–	µA
DATA SLICER									
Data Slicer Threshold Voltage				20	V_{TH1}	0.85	1.1	1.4	Vdc
Maximum Pull–Down Current				22	I_{DS}	1.0	1.8	–	mA
CARRIER DETECT									
Carrier Detect Threshold Voltage				16	V_{TH2}	1.0	1.15	1.3	Vdc
Maximum Pull–Down Current				17	I_{CD}	1.1	3.0	–	mA
TRANSMITTER									
Maximum Pull–Up Current				25	I_{OH}	5.8	7.0	–	mA
Maximum Pull–Down Current				25	I_{OL}	–	150	700	µA
DC Output Voltage				24	V_O	–	200	–	mV
Transmit PLL Charge Current				30	I_{TX}	–	±25	–	µA

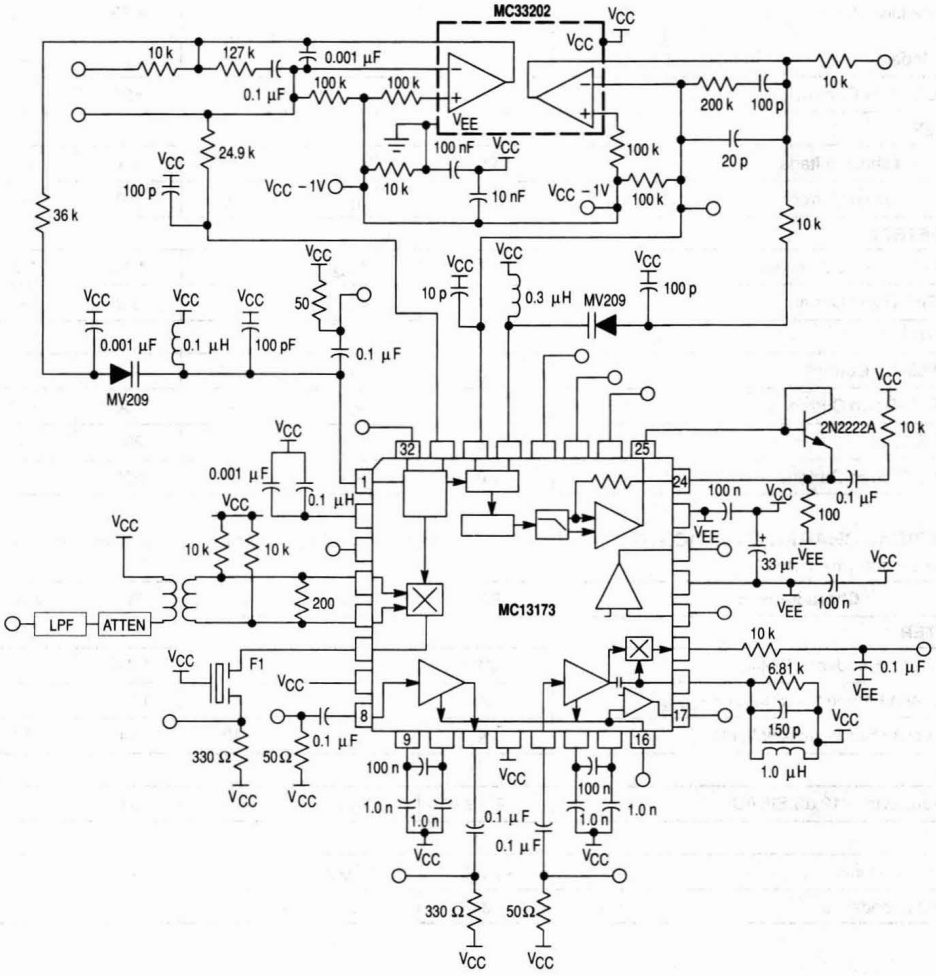
AC ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
TRANSMITTER						
Upper Sideband Frequency (Mark)	24	f_{HI}	–	1.427	–	MHz
Lower Sideband Frequency (Space)	24	f_{LO}	–	1.317	–	MHz
Upper and Lower Sideband Amplitude	24	V_{SB}	40	54	70	mVrms
RECEIVER						
Receiver Sensitivity – 12 dB SINAD	4, 19	V_{SIN}	–	5.0	–	µV
MIXER						
Mixer Conversion Gain	4, 5, 6	$AV_{(Mix)}$	–	23.5	–	dB
Mixer Output Impedance	6	Z_O	–	330	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER						
IF Amplifier Gain	8, 11	–	–	54	–	dB
IF Amplifier RSSI Slope	16	–	–	275	–	nA/dB
Input Impedance	8	Z_{IN}	–	330	–	Ω
Output Impedance	11	Z_O	–	330	–	Ω
RSSI Current Range	16	–	–	20	–	µA
RSSI Dynamic Range	16	–	–	70	–	dB
LIMITING AMPLIFIER						
Input Impedance	13	Z_{IN}	–	330	–	Ω
Limiter RSSI Slope	16	–	–	360	–	nA/dB
RSSI Current Range	16	–	–	20	–	µA
RSSI Dynamic Range	16	–	–	58	–	dB

Figure 1. Test Circuit



CIRCUIT DESCRIPTION

General

The MC13173 infrared transceiver integrates a split IF wideband FM receiver and an IR LED transmitter into a single IC. The transmitter is comprised of an FSK modulator, harmonic low pass filter, and IR LED driver. The receiver consists of a mixer, IF amplifier and limiting IF, detector, and data slicer. It includes RSSI and carrier detect functions.

The transmitter is capable of two modes of operation. It was primarily designed for use in the Communications Mode, which enables point–to–point data links, such as the communication from keyboard to computer, or for the exchange of data between portable computers. In this mode it is capable of 200 kbps half duplex FSK operation.

The transmitter can also operate in an "A/V" Mode, which pulses the LED on and off with no carrier. (See Figure 11).

Digital Interface Bus

The MC13173 is controlled via a six line 3.3 V digital interface bus. That includes three control pins, data in and out pins, and a carrier detect pin. Listed below is a brief description of each pin and its function.

Table 1. Digital Interface Pin Descriptions

Pin	Pin Name	Symbol	I/O	Description
28	Transmit Enable	T	I	High – Transmitter is enabled Low – Transmitter is disabled
27	Data In	DI	I	Data Input – 38.2 kbps Communication Mode
3	Receive Enable	R	I	High – Receiver is enabled Low – Receiver is disabled
22	Data Out	DO	O	Demodulated Output Signal
17	Carrier Detect	CD	O	High – Carrier is present Low – Carrier is not present
26	Transmit Modulation Enable	E	I	High – Transmitter is in A/V Mode Low – Transmitter is in Communications Mode

This transceiver was designed for use in battery powered, hand–held consumer products. To minimize power consumption, the digital interface enables individual system blocks to be powered down while not in use. The following diagram shows the mode of the IC and the power state of each circuit block for a given set of control levels.

Table 2. Power State Table

Control Pins*				Circuit Block Power States (See Figures 2 and 3)				Supply Current (Typical)
T	R	E	Mode	Master VCO	FSK Modulator	Receiver	LED Driver	
0	0	0	OFF	Off	Off	Off	Off	10 nA
0	0	1	OFF	Off	Off	Off	Off	70 µA
0	1	X	Receive	On	Off	On	Off	6.5 mA
1	1	1	Receive	On	Off	On	On	7.5 mA
1	1	0	Transmit – Comm Mode	On	On	On	On	9.0 mA
1	0	0	Transmit – Comm Mode	On	On	Off	On	4.75 mA
1	0	1	Transmit – A/V Mode	Off	Off	Off	On	1.5 mA

* With Data In Pin Low

Master VCO/PLL

The master VCO provides the reference frequency for the FSK modulator and the LO frequency for the receiver downconverter. With a 32.768 kHz input frequency to the master VCO on Pin 1, the LO frequency for the receiver will be at 12.075 MHz. The reference frequency for the FSK modulator will be at approximately 1.1 MHz. The master VCO and FSK modulator are not used when the transmitter is used in A/V mode, and both are powered down.

Receiver Description

The single conversion receiver portion of the MC13173 is low power and wideband, and incorporates a split IF. This section includes a mixer, IF amplifier, limiting IF, quadrature detector and data slicer.

Mixer

The mixer is a double balanced four quadrant multiplier. It can be driven either differentially or single–ended by connecting the unused input to the positive supply rail.

The buffered output is internally loaded for an output impedance of 330 Ω for use with a standard ceramic filter.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB. The fixed internal input impedance is 330 Ω for use with a 10.7 MHz ceramic filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

Limiter

The limiter section is similar to the IF amplifier section, except that four stages are used with the last three contributing to the RSSI. This IF limiting amplifier section drives the quadrature detector internally.

RSSI/Carrier Detect

The received signal strength indicator (RSSI) outputs a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor sets the output voltage range.

The carrier detect threshold is set at approximately 1.2 Vdc. When the RSSI level exceeds that threshold, the carrier detect output will go high. A large resistor may be added externally between the comparator output and the positive input for hysteresis.

Quadrature Detector

The demodulator is a conventional quadrature type with an external LC tank driven through an internal 5 pF capacitor. The output is buffered to give an output impedance of less than 1.0 kΩ at an average DC level of around 1.1 V.

Data Slicer

The data slicer is designed to square up the data signal. It is self centering at about 1.1 V, and clips at about 0.75 V and 1.45 V. There is a short time constant for large peak–to–peak voltage swings or when there is a change in DC level at the detector output. The time constant is longer for small signals or for continuous bits of the same polarity which drift close to the threshold voltage.

Transmission Description

The MC13173 uses a dual modulus PLL to frequency shift key (FSK) modulate the baseband digital input signal, producing the necessary logic high and low frequencies for transmission. The transmit frequency for a logic high is 1.427 MHz, and the frequency for a low is 1.317 MHz with a 32.768 kHz reference frequency.

FSK Modulator

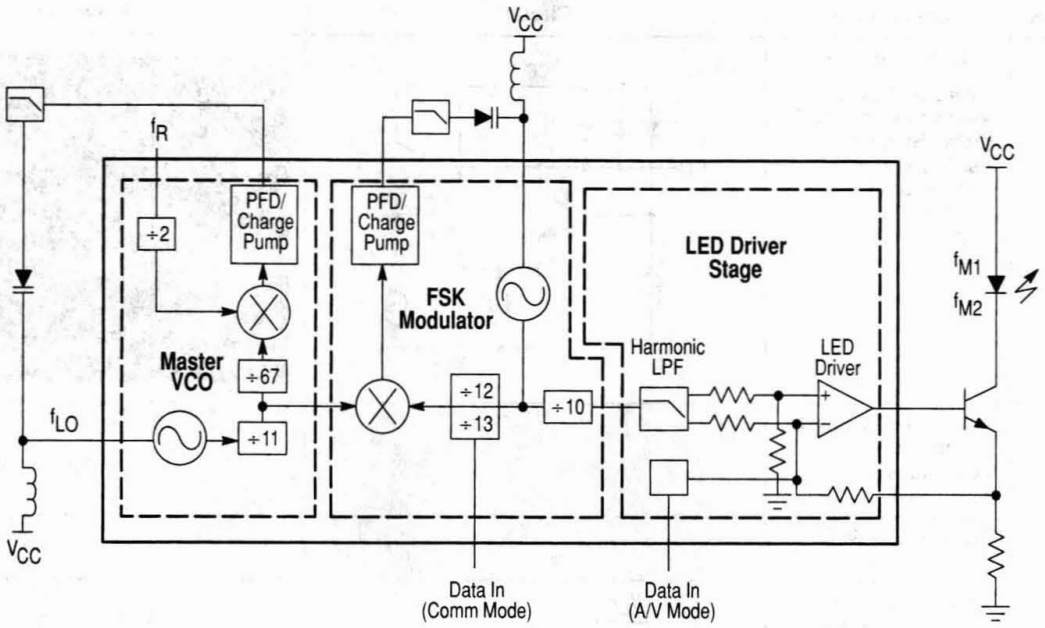
In the communications mode, the FSK modulator uses the reference frequency from the Master VCO to produce the two frequencies required for a logic high and a logic low. In the A/V mode, the FSK modulator is not used and is powered down.

LED Driver Stage

A low pass filter following the FSK modulator removes the undesired harmonic frequencies from the square–wave output of the divider circuits in PLLs. The resulting sinusoidal waveforms are fed into a unity gain difference amplifier, which drives the base of an external transistor, modulating the IR LED.

In A/V mode, the data is input directly into the inverting input of the op amp, and the low pass filter is not used.

Figure 2. Transmitter Block Diagram



f_R = 32.768 kHz

$f_{LO} = \frac{67 \times 11}{2} f_R$

Data High: $f_{M1} = \frac{13}{11 \times 10} f_{LO}$

Data Low: $f_{M2} = \frac{12}{11 \times 10} f_{LO}$

Figure 3. Receiver Block Diagram

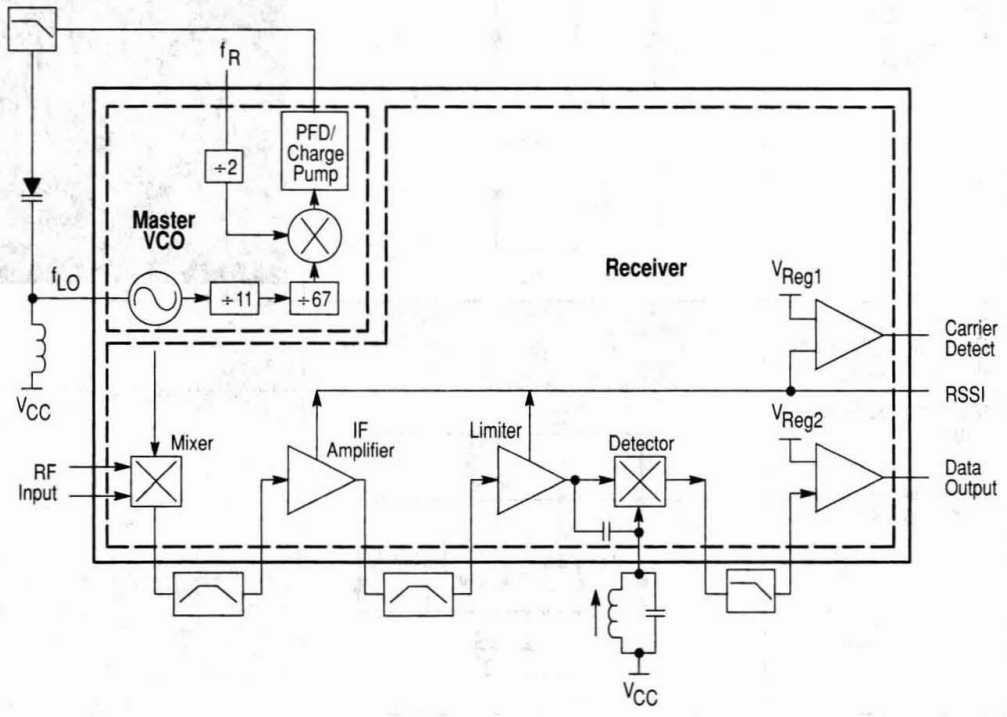


Table 3. PIN FUNCTION DESCRIPTION (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

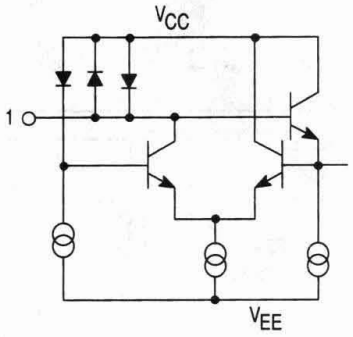
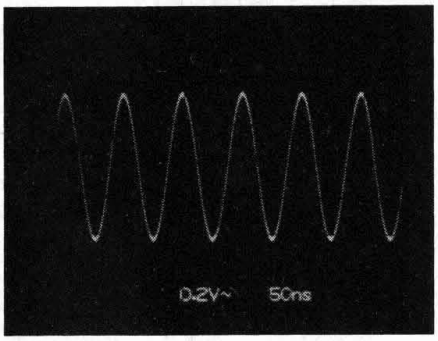
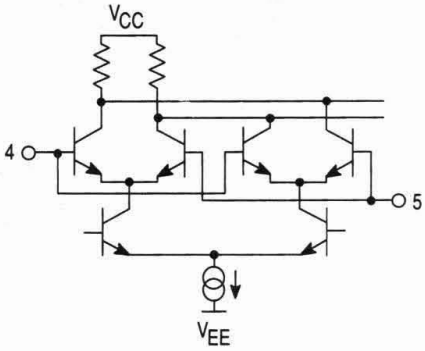
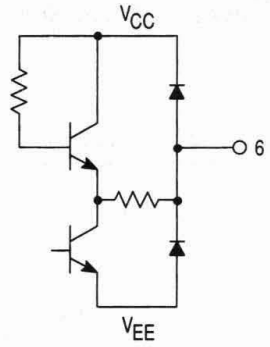
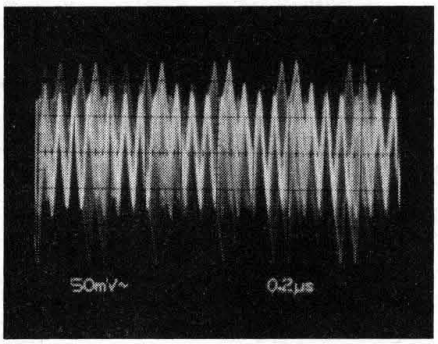
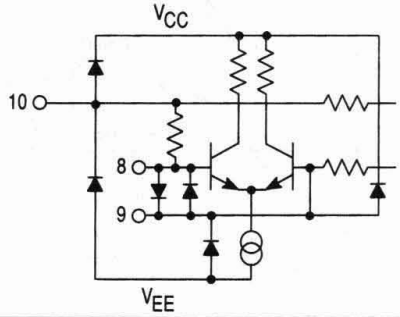
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
1	12 M	VCO for Master PLL. (Measured using a low capacitance FET probe. Standard oscilloscope probes can pull oscillator off frequency. See Figure 14.)		
2, 21, 23	V_{EE}	DC ground. Should be connected to a continuous ground plane on the PCB.		
3	R	Receive Enable Pin. See Tables 1 & 2.		
4, 5	RF In1 RF In2	RF Input to the mixer. 1.375 MHz average carrier frequency with ± 50 kHz deviation.		
6	Mixer Out	10.7 MHz IF Z_O = 330 Ω RF In = – 20 dBm Modulation = 32.768 kHz		
7, 12	V_{CC}	Supply voltage and RF ground, should be decoupled to V_{EE}.		
8	IF In	IF input impedance is 330 Ω. RF In = – 20 dBm Modulation = 32.768 kHz		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

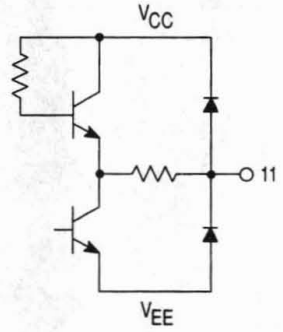
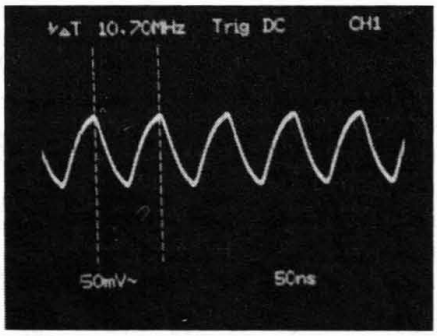
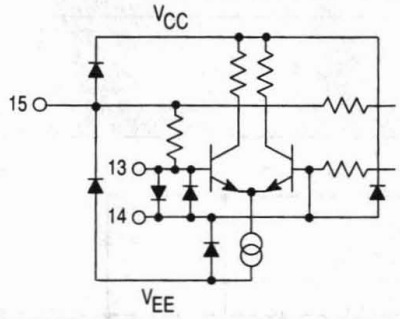
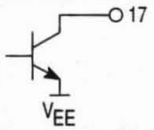
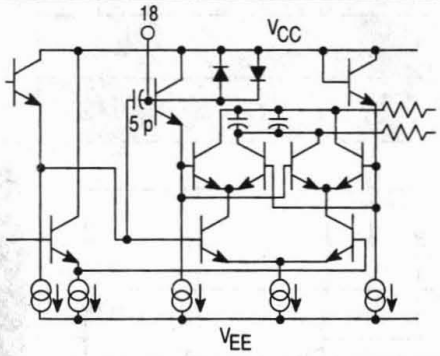
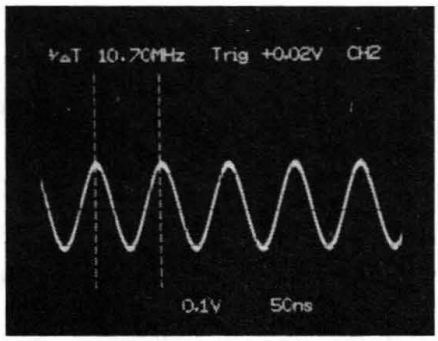
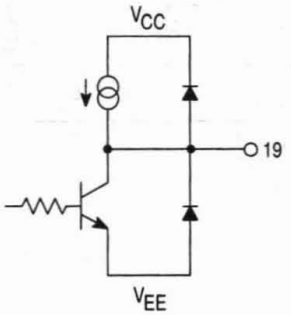
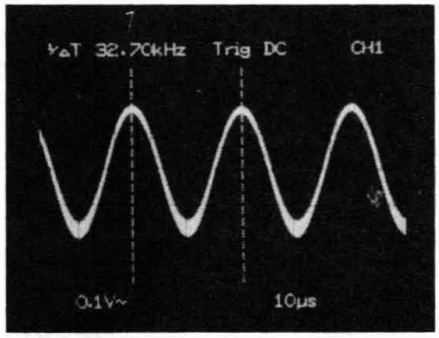
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
9, 10	IF Dec	IF decoupling as shown in Figure 15.	See Circuit for Pin 8.	
11	IF Out	IF Output. Z_O = 330 Ω. –20 dBm RF input level. Output is sinusoidal with lower drive levels.		
13	Lim In	Limiter input. Z_{In} = 330 Ω.		
14, 15	Lim Dec	External limiter decoupling as shown in application circuit.		
16	RSSI	Received Signal Strength Indicator Output. (See Figure 13)		
17	Carrier Detect	Logic output of the carrier detect comparator.		
18	Quad Coil	Quadrature tuning circuit. Modulated 10.7 MHz IF. Measured with a low capacitance FET probe.		
19	Demod	Demodulated signal output measured at the pin (before filtering). Modulation = 32.768 kHz sine wave.		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

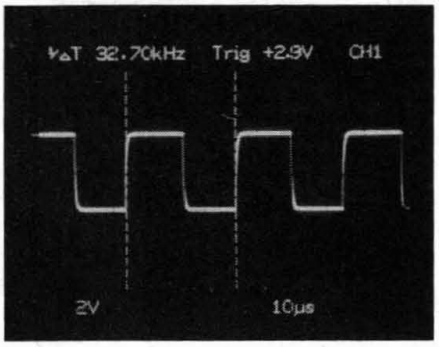
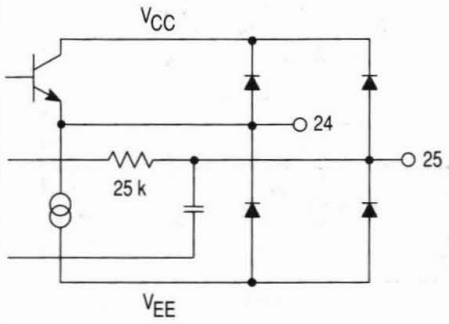
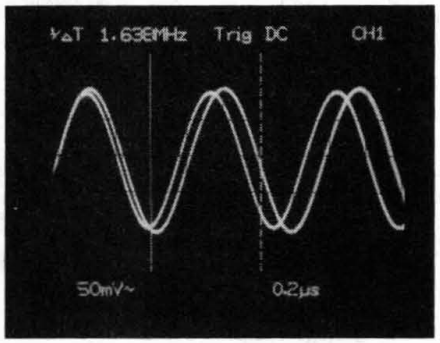
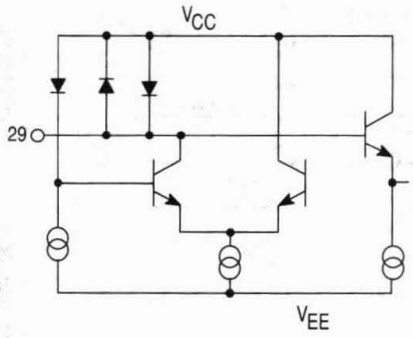
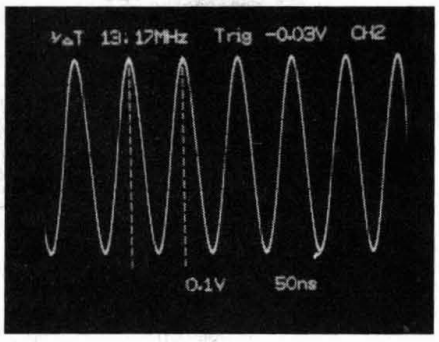
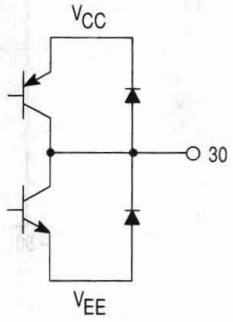
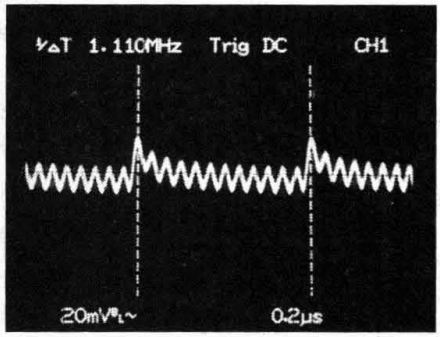
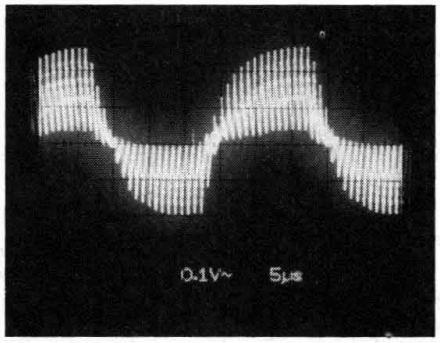
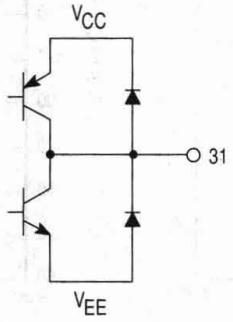
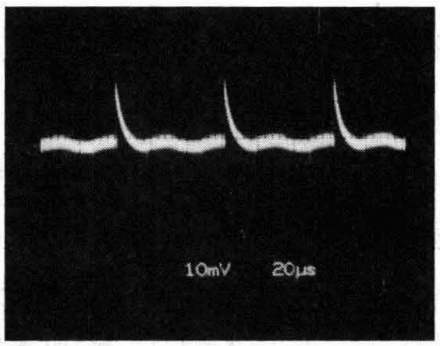
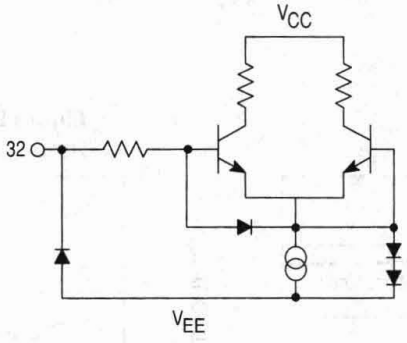
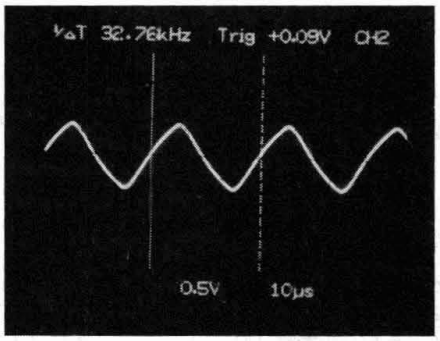
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
20	Data Slicer In	Input from the receiver demodulated output.		
22	Data Out	Output from the receiver data slicer. Modulation = 32.768 kHz sine wave. RF input driven by frequency generator. See also Figure 10.		
24	LED Driver Feed-back	Feedback for the LED driver op amp.		
25	IR LED Driver	Output of the unity gain output buffer in Communications Mode. See Figure 11 for transmit output in A/V mode. Modulation = 32.768 kHz square wave.		
26	E	Transmit Modulation Enable. See Tables 1 & 2.		
27	Data In	Modulation input for transmit data.		
28	T	Transmit Enable pin. See Tables 1 & 2.		
29	14 MHz Ref	VCO for FSK Modulator phase locked loop. (Measured using a low capacitance FET probe. Standard oscilloscope probes can pull oscillator off frequency. See Figure 14.) No modulation (Data In low).		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
30	Tx PLL	Phase detector output for the FSK Modulator. (With loop closed and locked.) No modulation (Data In low).		
		With 32.768 kHz square wave modulation. Note: Probing the output of the phase detectors directly may disturb the loop. It is best to probe the output of the op amp when evaluating loop response.		
31	Ma PLL	Output of the phase detector charge pump for the Master PLL. (With loop closed and locked.)		
32	32 kHz Ref	Input to 32.768 kHz reference. Filtered from TTL oscillator using application circuit in Figure 15. Approximately 1.0 Vp–p triangle wave at 32.768 kHz.		

Typical Performance Over Temperature

(Measured using test circuit in Figure 1)

Figure 4. Normalized Mixer Gain versus Temperature

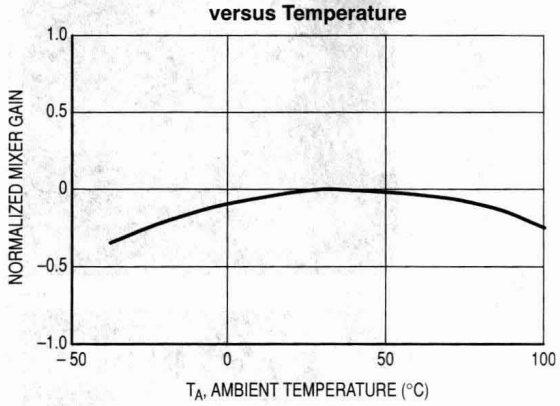


Figure 5. Normalized IF Amp Gain versus Temperature

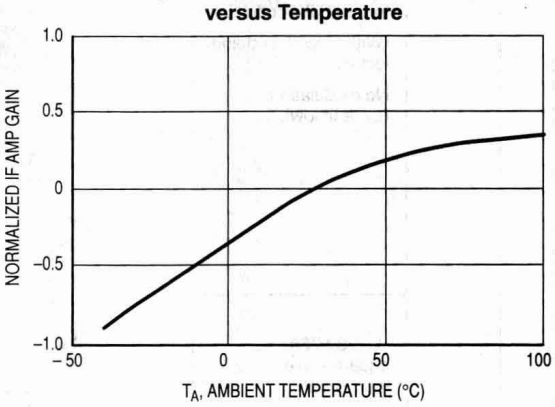


Figure 6. Maximum Pull–Up Current versus Temperature (Pin 25)

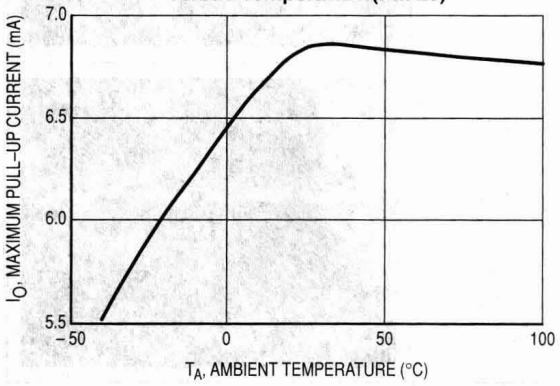


Figure 7. Maximum Pull–Down Current versus Temperature (Pin 25)

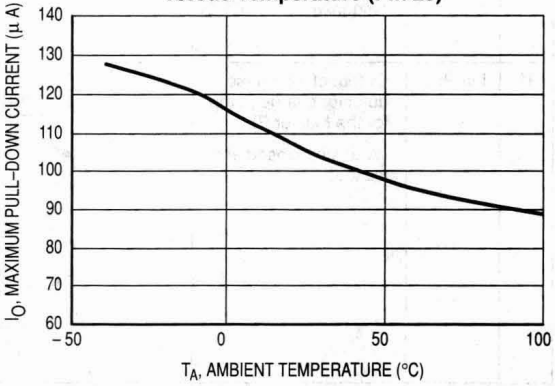


Figure 8. Supply Current versus Temperature

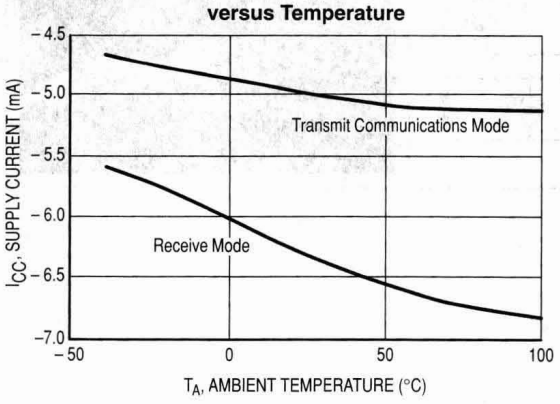
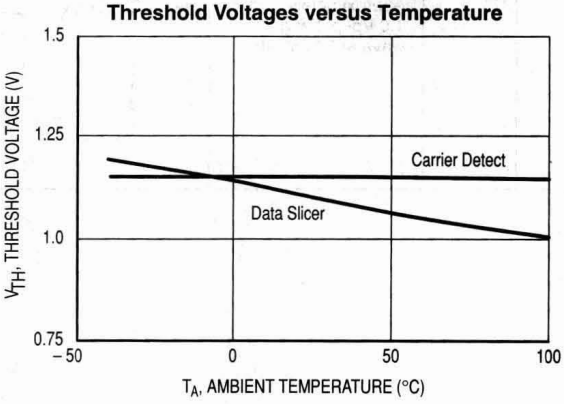


Figure 9. Data Slicer and Carrier Detect Threshold Voltages versus Temperature



APPLICATIONS INFORMATION

The MC13173 transceiver is specially designed to operate from a 32.768 kHz reference which is readily available in most computer applications. The frequency synthesizer on chip generates a receiver local oscillator frequency and the transmit mark and space frequencies from this fixed reference frequency, eliminating the need for additional crystals or manual tuning.

Large divide ratios are needed to generate these frequencies, however. For example, the receiver LO frequency is 368.5 times the 32.768 kHz reference frequency. This requires that the reference frequency be both accurate and stable. A two percent error in the reference frequency would pull the LO off frequency by over 240 kHz, putting the IF frequency out of the usable bandwidth of the filters and discriminator. For this reason, a 32.768 kHz oscillator circuit has been included on the demonstration board design. Although TTL crystal oscillators are available, this oscillator circuit uses an inexpensive tuning fork crystal and a hex inverter to generate a square wave reference frequency, which is then filtered and level adjusted to a 1.0 Vp–p triangle wave to drive pin 32. A TTL Clock Oscillator could also be used with the filter circuit as shown.

Frequency Synthesizer

The recommended op amp for the external loop filter is the MC33202. For low voltage operation, ($V_{CC} \leq 3.3$ V) an op amp that is rail–to–rail on both the input and output is advisable to obtain the widest possible output voltage range without distortion. Sufficient distortion from the op amp such as phase reversal on the output caused by overdriving the inputs could prevent the loop from locking to the reference.

In debugging the loop filter, it is important to note that the FSK Modulator phase locked loop will not lock until the Master VCO is locked to the reference. If the application circuit in Figure 15 is used, both loops should lock without the need for any additional tweaking. Since the VCO has ±2.0 MHz of range using the MV209 varactor diode (see Figure 11), neither precision components nor tuning should be required. To ensure both loops are operating properly, first evaluate each VCO with the loop open and a voltage equal to $V_{CC}/2$ applied to the resistor in series with the varactor. Since there is a relatively small capacitance (<40 pF) in series with the LC tank circuit, the VCO pin is sensitive to any parasitic capacitance. Thus when using a standard oscilloscope probe having 10 to 20 pF capacitance it is difficult to measure the VCO frequency without shifting its frequency. A low capacitance FET probe used with a frequency counter will enable you to accurately measure the VCO frequency without altering it in the process.

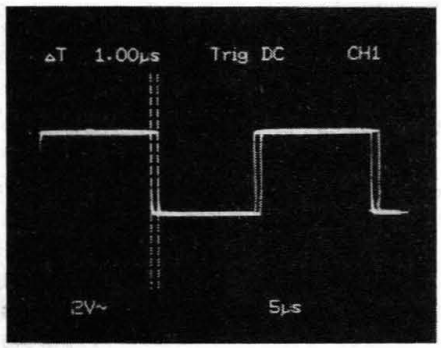
The free running frequency of the VCO should be approximately on frequency when the loop is open and the varactor is biased at mid–supply. The VCO for the Master PLL should run at 12.05 MHz. The free running frequency of the FSK Modulator should be at 13.72 MHz, midway between the two VCO frequencies needed to generate the transmit mark and space frequencies. The FSK Modulator loop is only active when the transmitter is enabled and the device is in the communications mode (see Tables 1 & 2). **If either the "T" pin is low or the "E" pin is high, the VCO will be off and you will see no oscillation on Pin 29.**

Once the loops are closed, the VCO frequencies should track the reference frequency within the hold–in range of the loop. Although the FSK Modulator loop is dependent on the Master VCO, the Master VCO is completely independent of the FSK Modulator. In fact, the FSK Modulator can be powered down (see Table 2) without affecting the Master VCO operation. In the application circuit in Figure 15 a single reference voltage for both op amps in the loop filters is provided by two diodes to V_{CC}. If the Master VCO is affected by the FSK Modulator loop, this generally indicates a problem with the common reference voltage to the op amp, and may mean the diodes are in backwards.

Once the loops are closed you should see a phase detector output such as is shown in the Pin Function Description in Table 3. If the VCO was on frequency when the loop was open, the phase detector outputs should swing around mid supply and not hit against either the positive or negative rail. Latching to V_{CC} or V_{EE} may indicate the loop filter circuitry is not implemented correctly.

Due to the digital design of the phase detectors, the transmitter can only transition between mark and space frequencies on a clock edge. On the receive side this may be seen as a double image on the detector output, with a discrete time delay which does not vary with the frequency of the data input (see Figure 10). This is a normal consequence of using a digital phase detector and should not be confused with jitter from the data slicer.

Figure 10. Receive Data Output
(Data Transmitted from Companion MC13173)



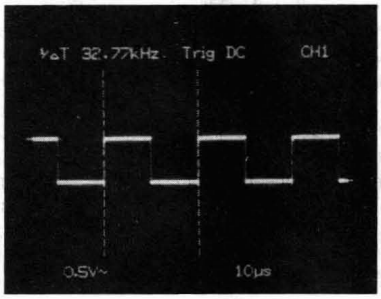
Transmitter

The light emitting diode (LED) driver in the transmitter is capable of 6.0 to 10 mA of pull–up current. Selection of the external transistor and biasing resistor will depend on the LEDs used. Typical infrared LEDs require 50 to 100 mA of current and have a forward voltage of 1.5V. Sufficient current is needed to obtain the maximum power output without distorting the output by overdriving the LED. Key specifications include rise and fall time, wavelength, beam width (generally given in half–angle), maximum power output and efficiency. Choice of wavelengths is generally determined by cost and power efficiency, which may vary between vendors. The LEDs used in this application are at 880 nm and were chosen for best efficiency. However LEDs in general are very inefficient, converting only 1 or 2 percent of the electrical power into optical power. Multiple LEDs can be used to increase transceiver range.

Disabling the transmitter via the data bus turns off the output of the LED driver, removing the base current from the external transistor and thereby turning off the IR LED. Because of the high current drawn by the LED, this offers considerable power savings when the transmitter is not in use and can be easily controlled by a microcontroller with no additional circuitry.

In the "A/V" transmit mode, the data output is on/off keyed, with the LED on for a data high, and off for a data low. It is a baseband signal, with no carrier present (see Figure 11).

Figure 11. LED Driver Output in A/V Mode



Receiver

The receiver portion of the MC13173 is similar to the design of Motorola's MC13156 Wideband FM Receiver. Instead of using the mixer to downconvert from a higher RF frequency, this application is designed to upconvert the 1.372 MHz input to a 10.7 MHz IF. The wide deviation, relative to the RF input frequency, requires a low Q tuned circuit to recover this bandwidth:

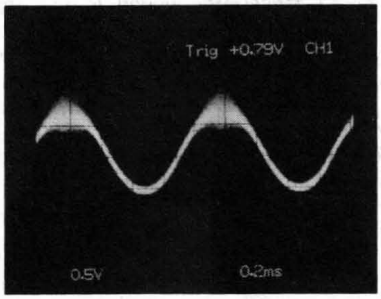
$$Q \approx \frac{f_c}{BW_{3\ dB}}, \text{ where } f_c = 1.372 \text{ MHz}$$

By Carson's Rule, the BW = 2(fdev + fmod). Since for mark/space frequencies of 1.317 MHz and 1.427 MHz the deviation is fixed at ±50 kHz, the bandwidth for a 50 kHz square wave (100 kbps) would be 200 kHz, and the tuned input requires a Q of less than 7. The low Q of the tank circuit reduces both the selectivity and the sensitivity of the receiver. For a Q of 7, the resistor required across the 56 µH inductor can be calculated:

$$R = QX_L = (7) \bullet (2\pi) \bullet (1.372\ E6) \bullet (56\ E{-}6)$$
$$R = 3.3\ k\Omega$$

The 10.7 MHz ceramic filters also need to be wide enough to pass the full frequency range which will include some harmonics. In the application circuit in Figure 15, Toko filters with a bandwidth of 330 kHz or 360 kHz are recommended to accommodate higher data rates. If the IF filters are too narrow, the recovered signal may have noise on the peaks (see Figure 12).

Figure 12. Receive Data Output



The RSSI has over 70 dB of dynamic range and 20 µA of current range. The RSSI output provides the input to the carrier detect comparator (see Figure 13) and a logarithmic output proportional to the input signal level. It can, therefore, be used to recover amplitude shift keyed (ASK) data.

The key specifications for the infrared detectors are response time, sensitivity, acceptance angle, and wavelength. Some vendors offer detectors in a black package with a built–in daylight filter. Although the transparent packages offer better sensitivity, the detectors with the daylight filter offer a much better signal to noise ratio. Response time (or maximum frequency) of the system is generally limited by the capability of the emitters rather than the detectors. For this application, a rise and fall time of 500 ns is sufficient.

Design and Layout Considerations

Although the frequencies in this design are low by RF standards, careful layout and good decoupling are still good practice. The high gain limiter and IF blocks should be decoupled as shown in the application circuit as near the IC as possible for best receiver performance. Also the TTL levels from the reference oscillator and the wide current swing applied to the IR LEDs can easily be picked up on V_{CC}, creating problems for the sensitive phase detector circuits and receiver RF inputs. Avoid long parallel traces and use plenty of decoupling to keep the supply rail clean.

Typical Performance

(Measured using Application Circuit in Figure 15)

Figure 13. RSSI Output Current versus RF Input Level

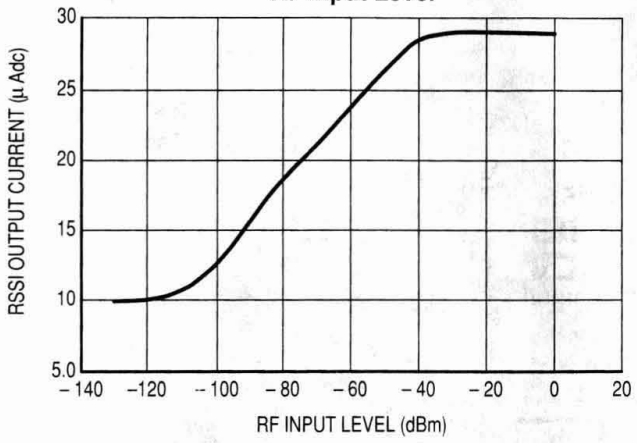


Figure 14. VCO Frequency versus Varactor Voltage

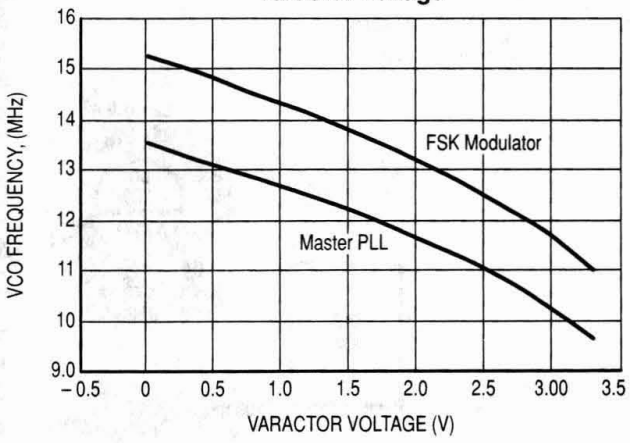
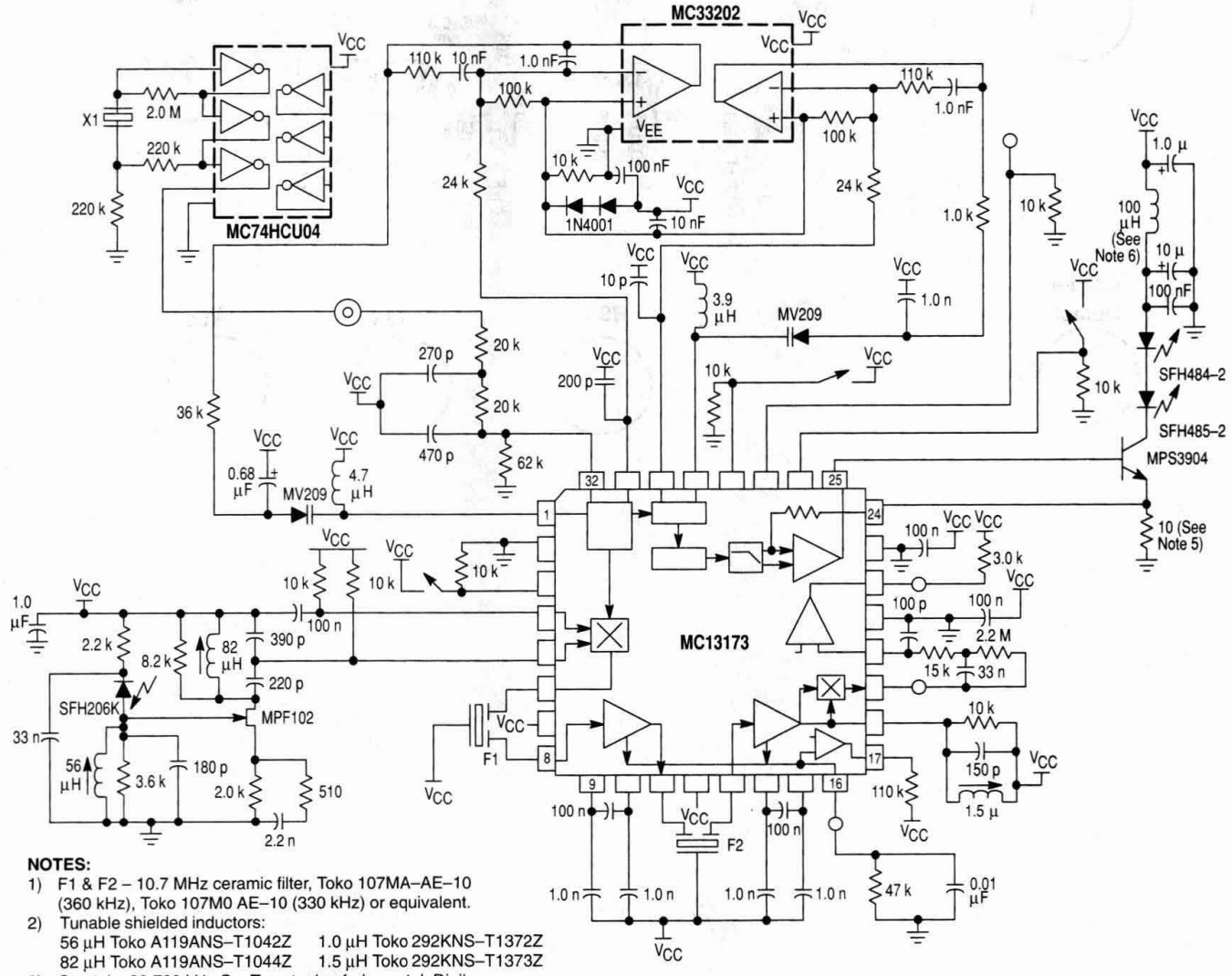


Figure 15. Application Circuit



NOTES:

1) F1 & F2 – 10.7 MHz ceramic filter, Toko 107MA–AE–10 (360 kHz), Toko 107M0 AE–10 (330 kHz) or equivalent.
2) Tunable shielded inductors:
   56 μH Toko A119ANS–T1042Z 1.0 μH Toko 292KNS–T1372Z
   82 μH Toko A119ANS–T1044Z 1.5 μH Toko 292KNS–T1373Z
3) Crystal – 32.768 kHz C – Type tuning fork crystal. Digikey part number SE3201 or equivalent.
4) LEDs and Detectors SFH484–2, SFH485–2 and SFH206K are made by Siemens.
5) Optimum bias resistor depends on the LEDs used.
6) May be fixed or tunable.

Figure 16. Component Placement

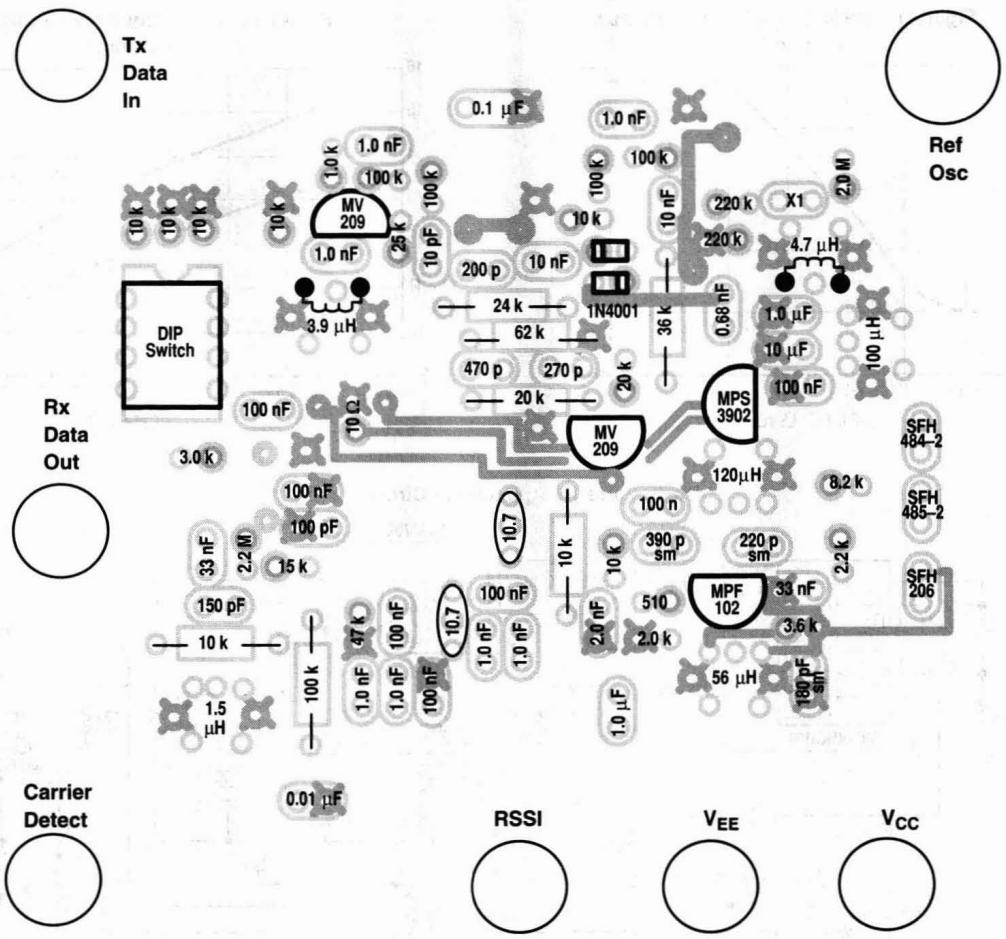


Figure 17. Solder Side View

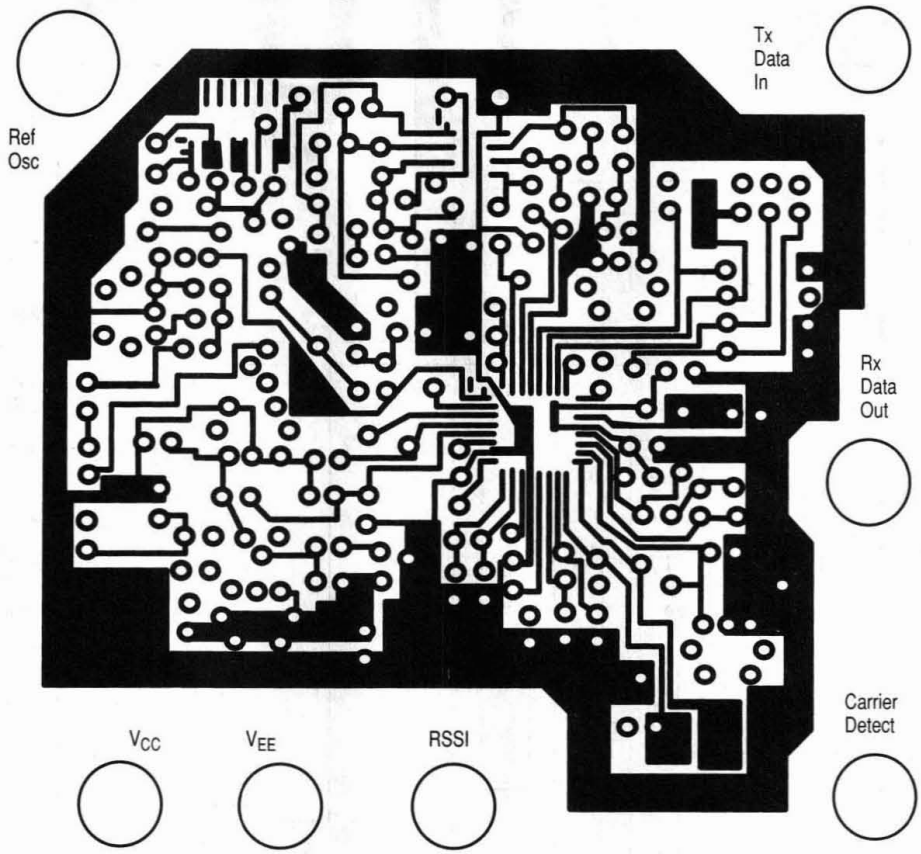


Figure 18. Component Side View

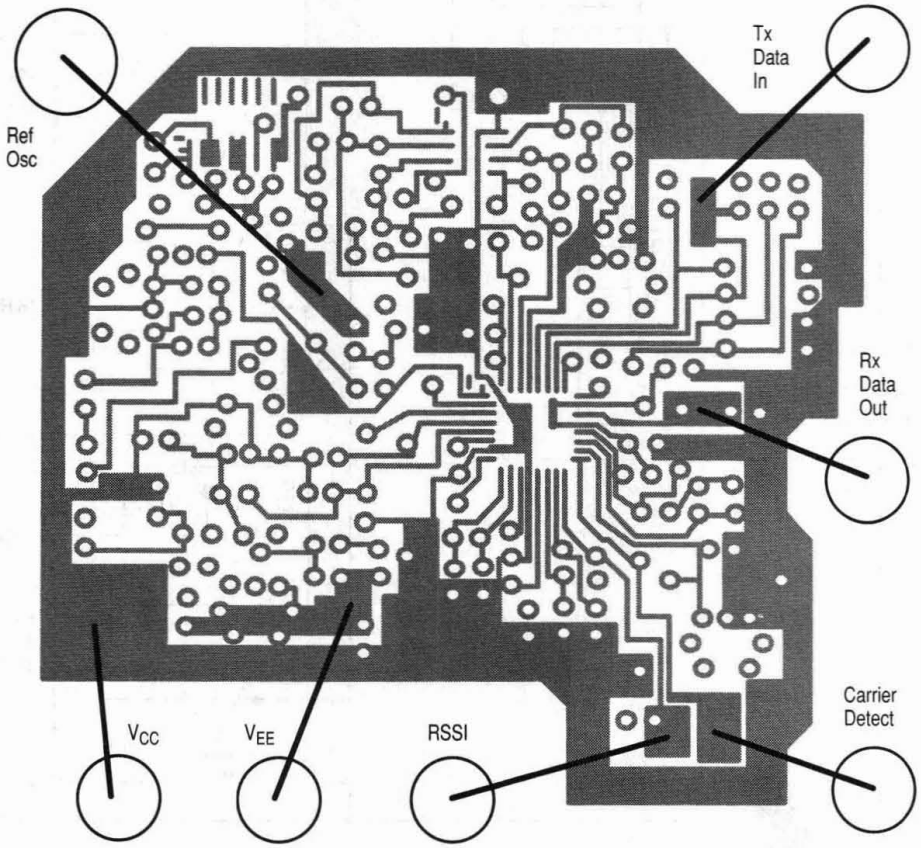
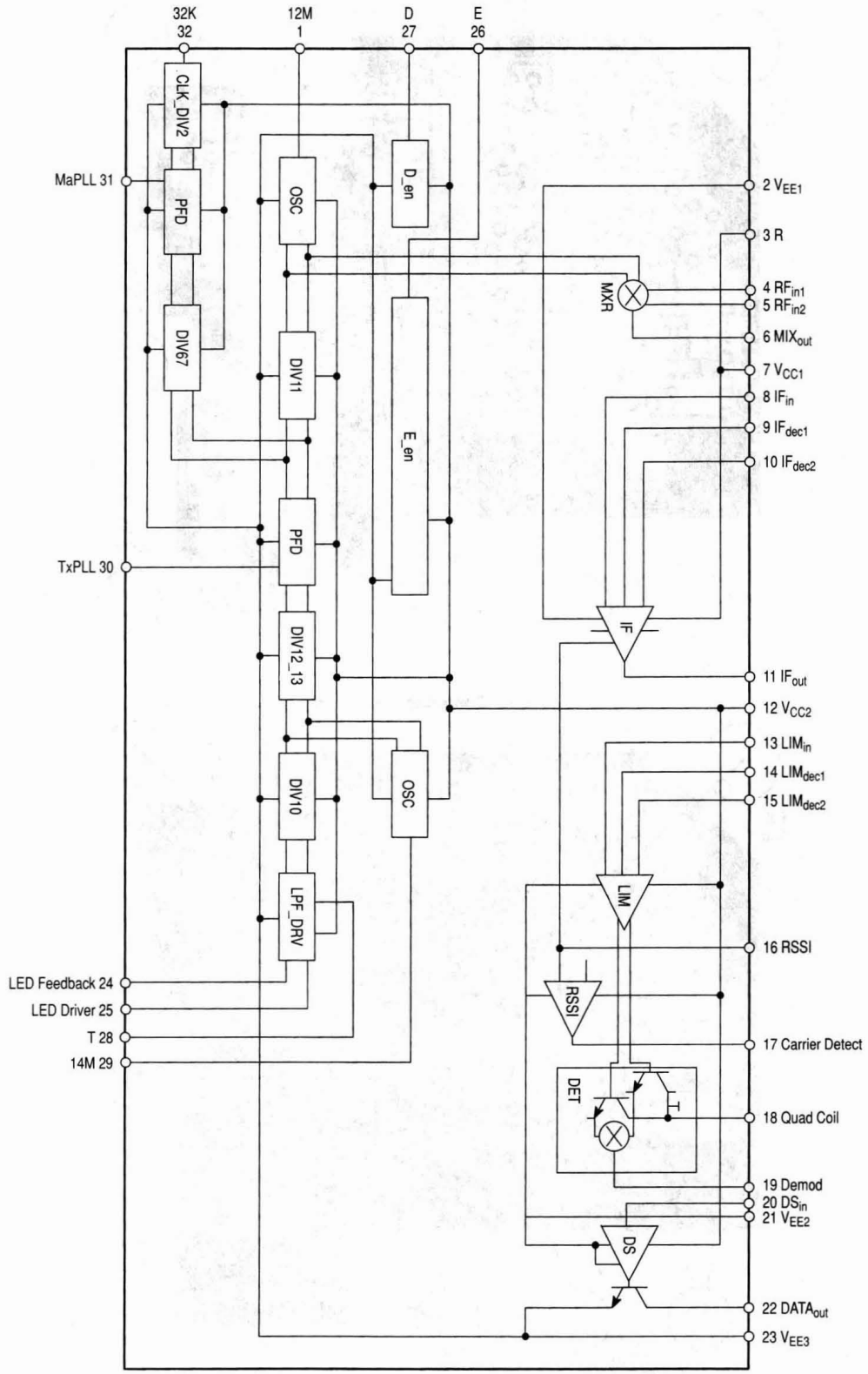


Figure 19. Detailed Internal Block Diagram



MOTOROLA

MC13175
MC13176

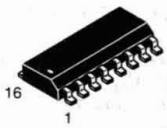
UHF FM/AM Transmitter

UHF FM/AM TRANSMITTER

SEMICONDUCTOR TECHNICAL DATA

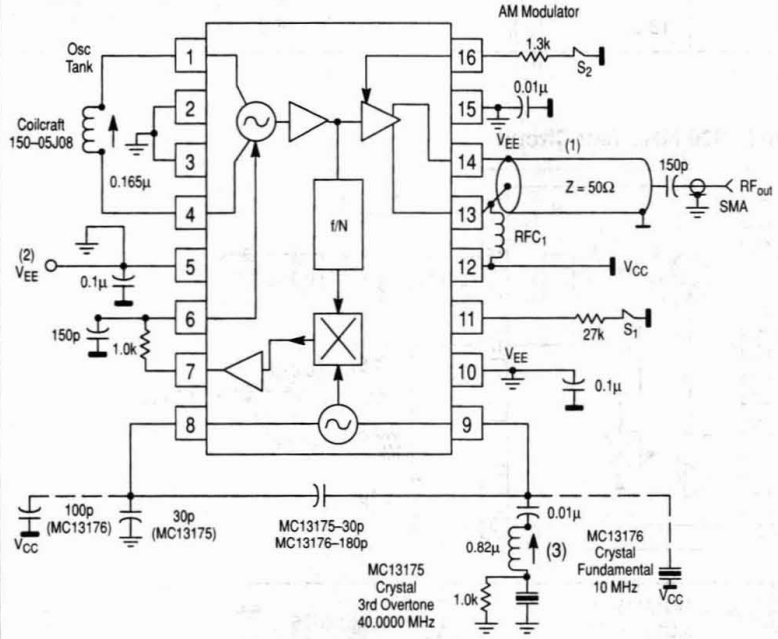
The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷ 8 (MC13175) or ÷ 32 (MC13176) prescaler and phase detector forming a versatile PLL system. Targeted applications are in the 260 to 470 MHz band and 902 to 928 MHz band covered by FCC Title 47; Part 15. Other applications include local oscillator sources in UHF and 900 MHz receivers, UHF and 900 MHz video transmitters, RF Local Area Networks (LANs), and high frequency clock drivers. The MC13175/76 offer the following features:

- UHF Current Controlled Oscillator
- Uses Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Fewer External Parts Required
- Low Operating Supply Voltage (1.8 to 5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output On and Off
- (MC13175) $f_o = 8 \times f_{ref}$; (MC13176) $f_o = 32 \times f_{ref}$



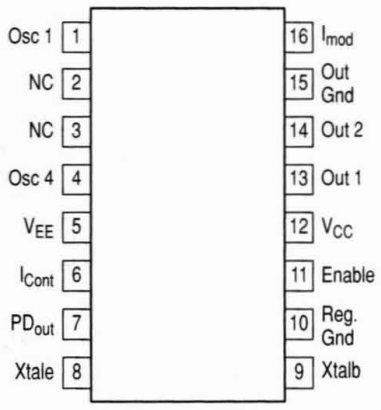
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Figure 1. Typical Application as 320 MHz AM Transmitter



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength at 320 MHz equals 1.5 inches.
2. Pins 5, 10 & 15 are ground and connected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); recommended source is Coilcraft "slot seven" 7mm tuneable inductor, Part #7M3–821. 1.0k resistor. Shunting the crystal prevents it from oscillating in the fundamental mode.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13175D	$T_A = -40°$ to $+85°C$	SO–16
MC13176D		SO–16

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

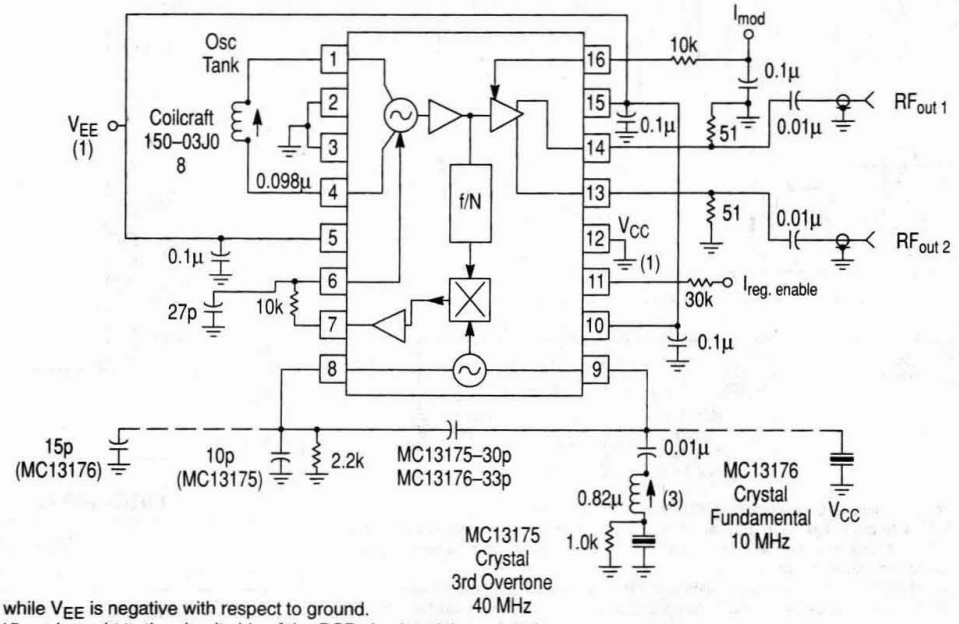
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	1.8 to 5.0	Vdc
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (Figure 2; V_{EE} = – 3.0 Vdc, T_A = 25°C, unless otherwise noted.)*

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (Power down: I_{11} & I_{16} = 0)	–	I_{EE1}	– 0.5	–	–	µA
Supply Current (Enable [Pin 11] to V_{CC} thru 30 k, I_{16} = 0)	–	I_{EE2}	–18	–14	–	mA
Total Supply Current (Transmit Mode) (I_{mod} = 2.0 mA; f_o = 320 MHz)	–	I_{EE3}	– 39	– 34	–	mA
Differential Output Power (f_o = 320 MHz; V_{ref} [Pin 9] = 500 mV_{p-p}; f_o = N x f_{ref}) I_{mod} = 2.0 mA (see Figures 7 and 8) I_{mod} = 0 mA	13 & 14	P_{out}	 2.0 –	 + 4.7 – 45	 – –	dBm
Hold–in Range (± Δf_{ref} x N) MC13175 (see Figure 7) MC13176 (see Figure 8)	13 & 14	± Δf_H	 3.5 4.0	 6.5 8.0	 – –	MHz
Phase Detector Output Error Current MC13175 MC13176	7	I_{error}	 20 22	 25 27	 – –	µA
Oscillator Enable Time (see Figure 27)	11 & 8	t_{enable}	–	4.0	–	ms
Amplitude Modulation Bandwidth (see Figure 29)	16	BW_{AM}	–	25	–	MHz
Spurious Outputs (I_{mod} = 2.0 mA) Spurious Outputs (I_{mod} = 0 mA)	13 & 14 13 & 14	P_{son} P_{soff}	– –	– 50 – 50	– –	dBc
Maximum Divider Input Frequency Maximum Output Frequency	– 13 & 14	f_{div} f_o	– –	950 950	– –	MHz

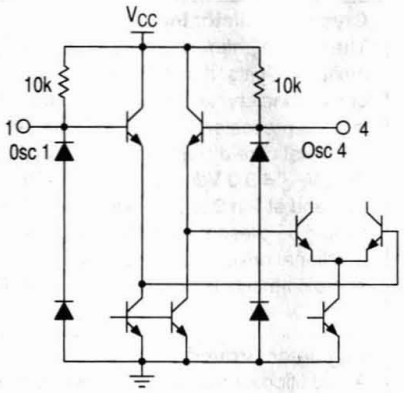
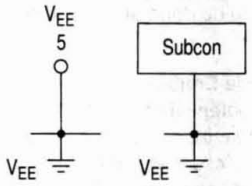
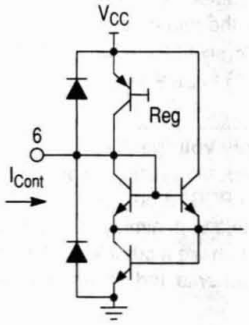
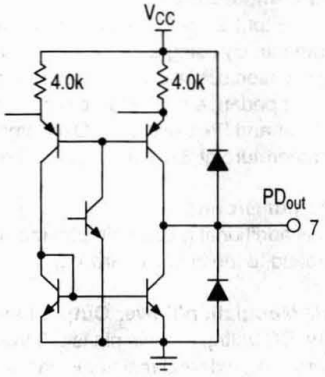
* For testing purposes, V_{CC} is ground (see Figure 2).

Figure 2. 320 MHz Test Circuit



NOTES: 1. V_{CC} is ground; while V_{EE} is negative with respect to ground.
2. Pins 5, 10 and 15 are brought to the circuit side of the PCB via plated through holes. They are connected together with a trace on the PCB and each Pin is decoupled to V_{CC} (ground).
3. Recommended source is Coilcraft "slot seven" inductor, part number 7M3–821.

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1 & 4	Osc 1, Osc 4		**CCO Inputs** The oscillator is a current controlled type. An external oscillator coil is connected to Pins 1 and 4 which forms a parallel resonance LC tank circuit with the internal capacitance of the IC and with parasitic capacitance of the PC board. Three base–emitter capacitances in series configuration form the capacitance for the parallel tank. These are the base–emitters at Pins 1 and 4 and the base–emitter of the differential amplifier. The equivalent series capacitance in the differential amplifier is varied by the modulating current from the frequency control circuit (see Pin 6, internal circuit). A more thorough discussion is found in the Applications Information section.
5	V_{EE}		**Supply Ground (V_{EE})** In the PCB layout, the ground pins (also applies to Pins 10 and 15) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground returns.
6	I_{Cont}		**Frequency Control** For V_{CC} = 3.0 Vdc, the voltage at Pin 6 is approximately 1.55 Vdc. The oscillator is current controlled by the error current from the phase detector. This current is amplified to drive the current source in the oscillator section which controls the frequency of the oscillator. Figures 9 and 10 show the Δf_{osc} versus I_{Cont}, Figure 5 shows the Δf_{osc} versus I_{Cont} at – 40°C, + 25°C and + 85°C for 320 MHz. The CCO may be FM modulated as shown in Figures 18 and 19, MC13176 320 MHz FM Transmitter. A detailed discussion is found in the Applications Information section.
7	PD_{out}		**Phase Detector Output** The phase detector provides ± 30 μA to keep the CCO locked at the desired carrier frequency. The output impedance of the phase detector is approximately 53 kΩ. Under closed loop conditions there is a DC voltage which is dependent upon the free running oscillator and the reference oscillator frequencies. The circuitry between Pins 7 and 6 should be selected for adequate loop filtering necessary to stabilize and filter the loop response. Low pass filtering between Pin 7 and 6 is needed so that the corner frequency is well below the sum of the divider and the reference oscillator frequencies, but high enough to allow for fast response to keep the loop locked. Refer to the Applications Information section regarding loop filtering and FM modulation.

PIN FUNCTION DESCRIPTIONS

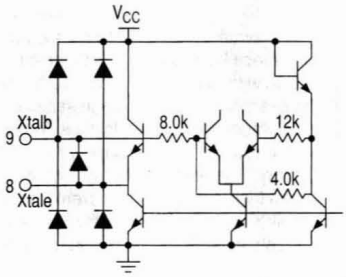
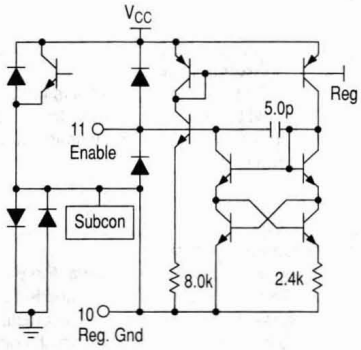
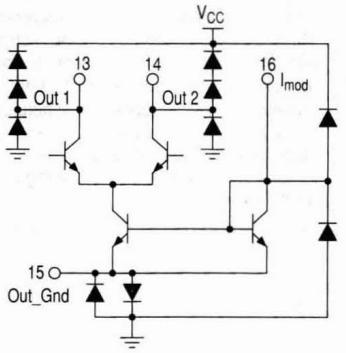
Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
8	Xtale		**Crystal Oscillator Inputs** The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With V_{CC} = 3.0 Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp–p should be present at Pin 9. The Colpitts is biased at 200 μA; additional drive may be acquired by increasing the bias to approximately 500 μA. Use 6.2 k from Pin 8 to ground.
9	Xtalb		
10	Reg. Gnd		**Regulator Ground** An additional ground pin is provided to enhance the stability of the system. Decoupling to the V_{CC} (RF ground) is essential; it should be done at the ground return for Pin 10. **Device Enable** The potential at Pin 11 is approximately 1.25 Vdc. When Pin 11 is open, the transmitter is disabled in a power down mode and draws less than 1.0 μA I_{CC} if the MOD at Pin 16 is also open (i.e., it has no current driving it). To enable the transmitter a current source of 10 μA to 90 μA is provided. Figures 3 and 4 show the relationship between I_{CC}, V_{CC} and $I_{reg.\ enable}$. Note that I_{CC} is flat at approximately 10 mA for $I_{reg.\ enable}$ = 5.0 to 100 μA (I_{mod} = 0).
11	Enable		
12	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
13 & 14	Out 1 and Out 2		**Differential Output** The output is configured differentially to easily drive a loop antenna. By using a transformer or balun, as shown in the application schematic, the device may then drive an unbalanced low impedance load. Figure 6 shows how much the Output Power and Free–Running Oscillator Frequency change with temperature at 3.0 Vdc; I_{mod} = 2.0 mA. **Output Ground** This additional ground pin provides direct access for the output ground to the circuit board V_{EE}. **AM Modulation/Power Output Level** The DC voltage at this pin is 0.8 Vdc with the current source active. An external resistor is chosen to provide a source current of 1.0 to 3.0 mA, depending on the desired output power level at a given V_{CC}. Figure 28 shows the relationship of Power Output to Modulation Current, I_{mod}. At V_{CC} = 3.0 Vdc, 3.5 dBm power output can be acquired with about 35 mA I_{CC}. For FM modulation, Pin 16 is used to set the desired output power level as described above. For AM modulation, the modulation signal must ride on a positive DC bias offset which sets a static (modulation off) modulation current. External circuitry for various schemes is further discussed in the Applications Information section.
15	Out_Gnd		
16	I_{mod}		

Figure 3. Supply Current versus Supply Voltage

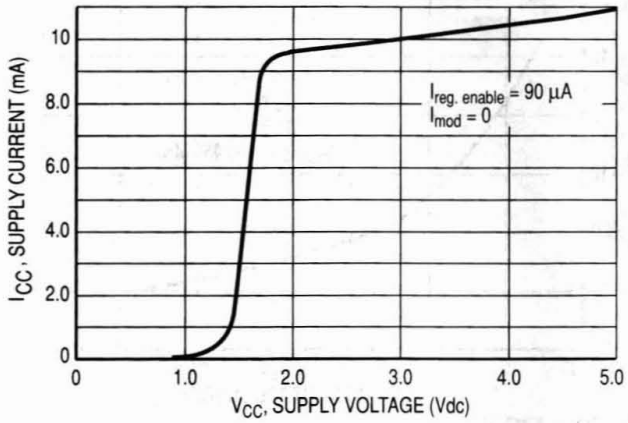


Figure 4. Supply Current versus Regulator Enable Current

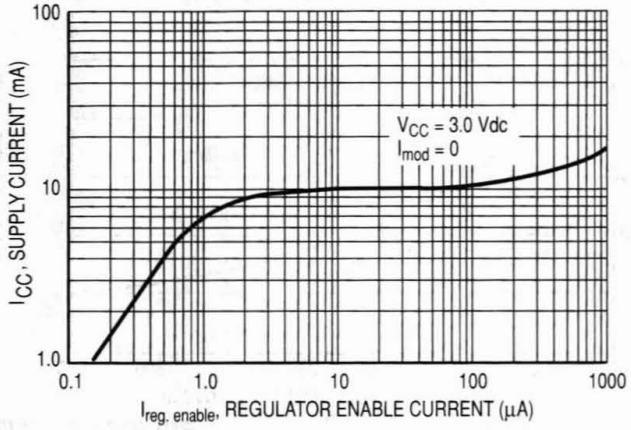


Figure 5. Change Oscillator Frequency versus Oscillator Control Current

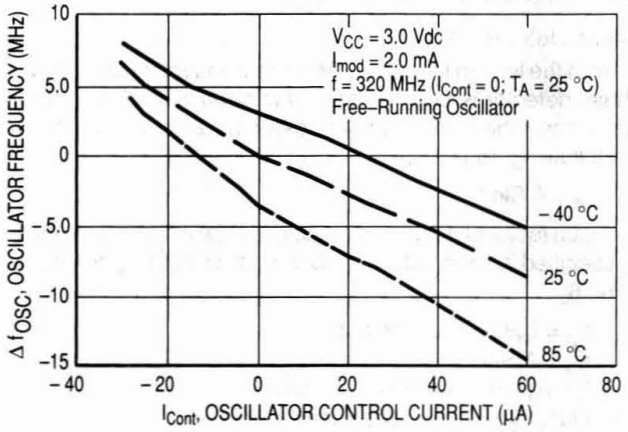

V_{CC} = 3.0 Vdc
I_{mod} = 2.0 mA
f = 320 MHz (I_{Cont} = 0; T_A = 25 °C)
Free–Running Oscillator
– 40 °C
25 °C
85 °C
Δ f_{OSC}, OSCILLATOR FREQUENCY (MHz)
I_{Cont}, OSCILLATOR CONTROL CURRENT (μA)

Figure 6. Change in Oscillator Frequency and Output Power versus Ambient Temperature

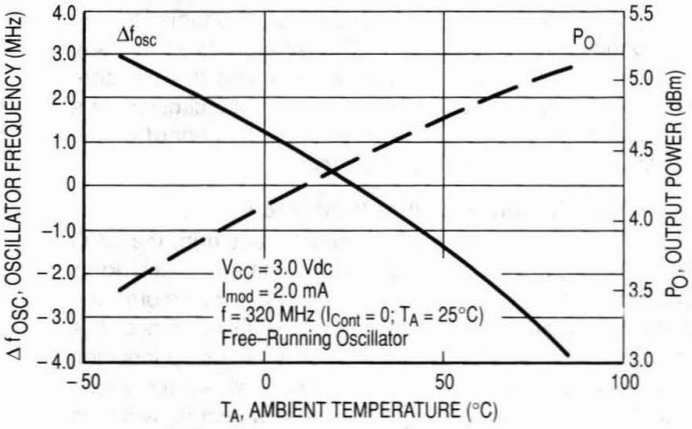


Figure 7. MC13175 Reference Oscillator Frequency versus Phase Detector Current

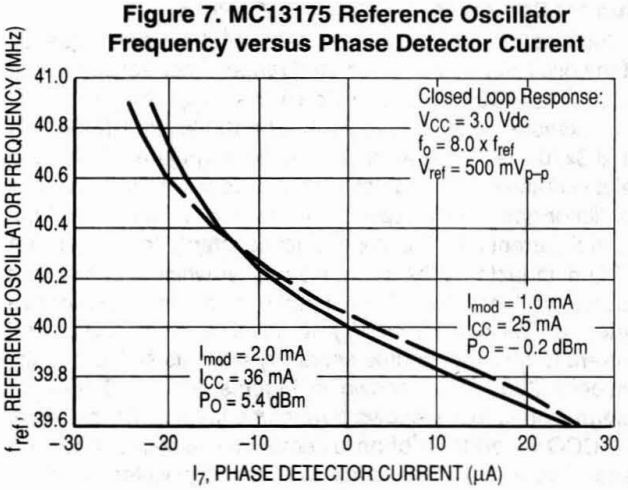

Closed Loop Response:
V_{CC} = 3.0 Vdc
f_o = 8.0 x f_{ref}
V_{ref} = 500 mV_{p-p}
I_{mod} = 1.0 mA
I_{CC} = 25 mA
P_O = – 0.2 dBm
I_{mod} = 2.0 mA
I_{CC} = 36 mA
P_O = 5.4 dBm
f_{ref}, REFERENCE OSCILLATOR FREQUENCY (MHz)
I_7, PHASE DETECTOR CURRENT (μA)

Figure 8. MC13176 Reference Oscillator Frequency versus Phase Detector Current

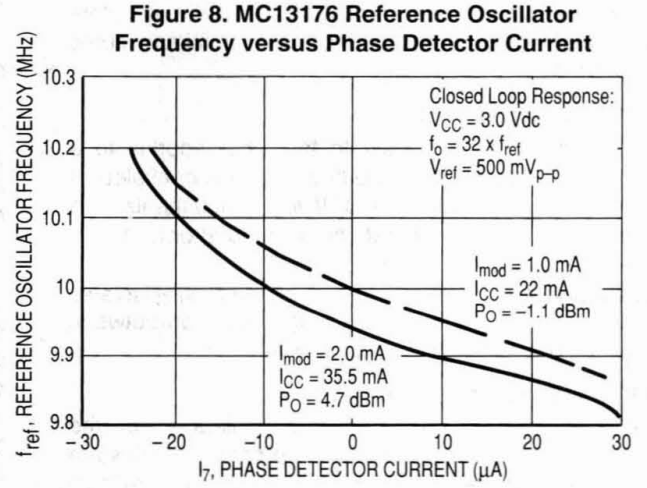

Closed Loop Response:
V_{CC} = 3.0 Vdc
f_o = 32 x f_{ref}
V_{ref} = 500 mV_{p-p}
I_{mod} = 1.0 mA
I_{CC} = 22 mA
P_O = –1.1 dBm
I_{mod} = 2.0 mA
I_{CC} = 35.5 mA
P_O = 4.7 dBm
f_{ref}, REFERENCE OSCILLATOR FREQUENCY (MHz)
I_7, PHASE DETECTOR CURRENT (μA)

Figure 9. Change in Oscillator Frequency versus Oscillator Control Current

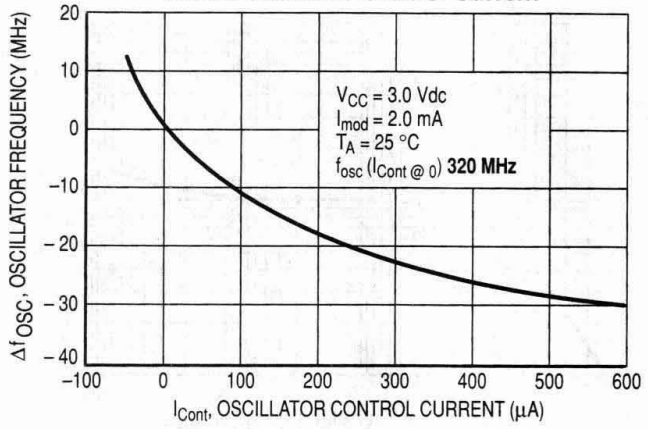
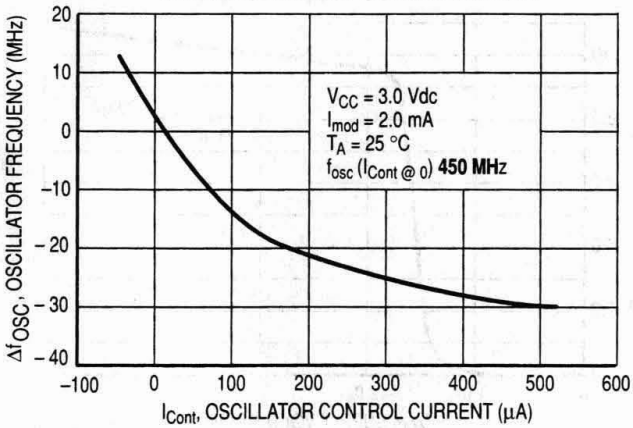


Figure 10. Change in Oscillator Frequency versus Oscillator Control Current



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB, shown in Figures 33 and 34, is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 35 and 36). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Current Controlled Oscillator (Pins 1 to 4)

It is critical to keep the interconnect leads from the CCO (Pins 1 and 4) to the external inductor symmetrical and equal in length. With a minimum inductor, the maximum free running frequency is greater than 1.0 GHz. Since this inductor will be small, it may be either a microstrip inductor, an air wound inductor or a tuneable RF coil. An air wound inductor may be tuned by spreading the windings, whereas tuneable RF coils are tuned by adjusting the position of an aluminum core in a threaded coilform. As the aluminum core coupling to the windings is increased, the inductance is decreased. The temperature coefficient using an aluminum core is better than a ferrite core. The UniCoil™ inductors made by Coilcraft may be obtained with aluminum cores (Part No. 51–129–169).

Ground (Pins 5, 10 and 15)

Ground Returns: It is best to take the grounds to a backside ground plane via plated through holes or eyelets at the pins. The application PCB layout implements this technique. Note that the grounds are located at or less than 100 mils from the devices pins.

Decoupling: Decoupling each ground pin to V_{CC} isolates each section of the device by reducing interaction between sections and by localizing circulating currents.

Loop Characteristics (Pins 6 and 7)

Figure 11 is the component block diagram of the MC1317XD PLL system where the loop characteristics are described by the gain constants. Access to individual components of this PLL system is limited, inasmuch as the loop is only pinned out at the phase detector output and the frequency control input for the CCO. However, this allows for characterization of the gain constants of these loop components. The gain constants K_p, K_o and K_n are well defined in the MC13175 and MC13176.

Phase Detector (Pin 7)

With the loop in lock, the difference frequency output of the phase detector is DC voltage that is a function of the phase difference. The sinusoidal type detector used in this IC has the following transfer characteristic:

$$I_e = A \sin \theta_e$$

The gain factor of the phase detector, K_p (with the loop in lock) is specified as the ratio of DC output current, I_e to phase error, θ_e:

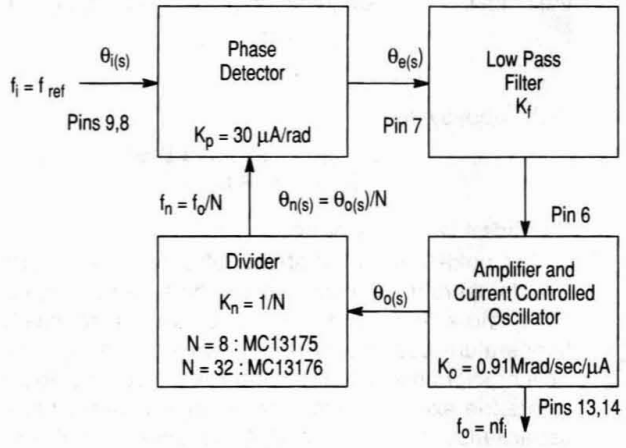
$$K_p = I_e/\theta_e \text{ (Amps/radians)}$$
$$K_p = A \sin \theta_e/\theta_e$$
$$\sin \theta_e \sim \theta_e \text{ for } \theta_e \leq 0.2 \text{ radians;}$$
$$\text{thus, } K_p = A \text{ (Amps/radians)}$$

Figures 7 and 8 show that the detector DC current is approximately 30 μA where the loop loses lock at $\theta_e = \pm \pi/2$ radians; therefore, K_p is 30 μA/radians.

Current Controlled Oscillator, CCO (Pin 6)

Figures 9 and 10 show the non–linear change in frequency of the oscillator over an extended range of control current for 320 and 450 MHz applications. K_o ranges from approximately 6.3×10^5 rad/sec/μA or 100 kHz/μA (Figure 9) to 8.8×10^5 rad/sec/μA or 140 kHz/μA (Figure 10) over a relatively linear response of control current (0 to 100 μA). The oscillator gain factor depends on the operating range of the control current (i.e., the slope is not constant). Included in the CCO gain factor is the internal amplifier which can sink and source at least 30 μA of input current from the phase detector. The internal circuitry at Pin 6 limits the CCO control current to 50 μA of source capability while its sink capability exceeds 200 μA as shown in Figures 9 and 10. Further information to follow shows how to use the full capabilities of the CCO by addition of an external loop amplifier and filter (see Figure 15). This additional circuitry yields at K_o = 0.145 MHz/μA or 9.1×10^5 rad/sec/μA.

Figure 11. Block Diagram of MC1317XD PLL



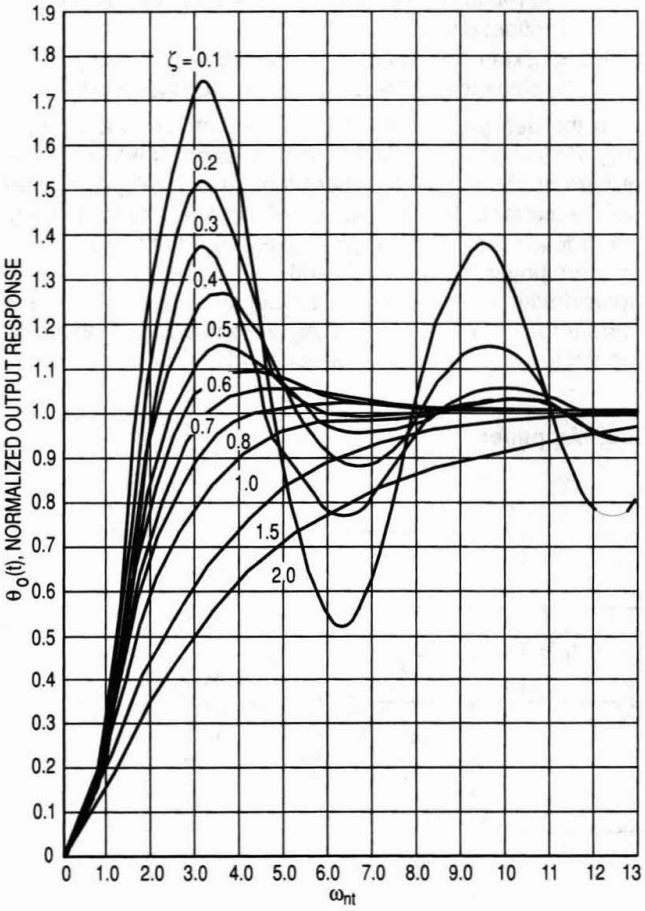
Where: K_p = Phase detector gain constant in µA/rad; K_p = 30 µA/rad
K_f = Filter transfer function
K_n = 1/N; N = 8 for the MC13175 and N = 32 for the MC13176
K_o = CCO gain constant in rad/sec/µA
K_o = 9.1 x 10^5 rad/sec/µA

Loop Filtering

The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time and transient response are controlled externally by loop filtering.

The natural frequency (ω_n) and damping factor (∂) are important in the transient response to a step input of phase or frequency. For a given ∂ and lock time, ω_n can be determined from the plot shown in Figure 12.

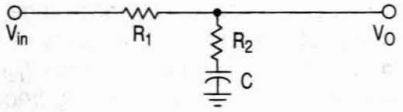
Figure 12. Type 2 Second Order Response



For ∂ = 0.707 and lock time = 1.0 ms;
then ω_n = 5.0/t = 5.0 krad/sec.

The loop filter may take the form of a simple low pass filter or a lag–lead filter which creates an additional pole at origin in the loop transfer function. This additional pole along with that of the CCO provides two pure integrators ($1/s^2$). In the lag–lead low pass network shown in Figure 13, the values of the low pass filtering parameters R_1, R_2 and C determine the loop constants ω_n and ∂. The equations $t_1 = R_1C$ and $t_2 = R_2C$ are related in the loop filter transfer functions $F(s) = 1 + t_2s/1 + (t_1 + t_2)s$.

Figure 13. Lag–Lead Low Pass Filter



The closed loop transfer function takes the form of a 2nd order low pass filter given by,

$$H(s) = K_vF(s)/s + K_vF(s)$$

From control theory, if the loop filter characteristic has F(0) = 1, the DC gain of the closed loop, K_v is defined as,

$$K_v = K_pK_oK_n$$

and the transfer function has a natural frequency,

$$\omega_n = (K_v/t_1 + t_2)^{1/2}$$

and a damping factor,

$$\partial = (\omega_n/2)\,(t_2 + 1/K_v)$$

Rewriting the above equations and solving for the MC13176 with ∂ = 0.707 and ω_n = 5.0 k rad/sec:

$K_v = K_pK_oK_n = (30)\,(0.91 \times 10^6)\,(1/32) = 0.853 \times 10^6$
$t_1 + t_2 = K_v/\omega_n2 = 0.853 \times 10^6/(25 \times 106) = 34.1$ ms
$t_2 = 2\partial/\omega_n = (2)\,(0.707)/(5 \times 10^3) = 0.283$ ms
$t_1 = (K_v/\omega_n2) - t_2 = (34.1 - 0.283) = 33.8$ ms

For C = 0.47 μ;

then, $R_1 = t_1/C = 33.8 \times 10^{-3}/0.47 \times 10^{-6} = 72$ k

dthus, $R_2 = t_2/C = 0.283 \times 10^{-3}/0.47 \times 10^{-6} = 0.60$ k

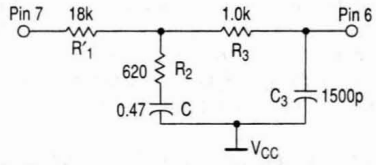
In the above example, the following standard value components are used,

C = 0.47 μ; R_2 = 620 and R'_1 = 72 k – 53 k ~ 18 k

(R'_1 is defined as R_1 – 53 k, the output impedance of the phase detector.)

Since the output of the phase detector is high impedance (~50 k) and serves as a current source, and the input to the frequency control, Pin 6 is low impedance (impedance of the two diode to ground is approximately 500 Ω), it is imperative that the second order low pass filter design above be modified. In order to minimize loading of the R_2C shunt network, a higher impedance must be established to Pin 6. A simple solution is achieved by adding a low pass network between the passive second order network and the input to Pin 6. This helps to minimize the loading effects on the second order low pass while further suppressing the sideband spurs of the crystal oscillator. A low pass filter with R_3 = 1.0 k and C_2 = 1500 p has a corner frequency (f_c) of 106 kHz; the reference sideband spurs are down greater than – 60 dBc.

Figure 14. Modified Low Pass Loop Filter



Hold–In Range

The hold–in range, also called the lock range, tracking range and synchronization range, is the ability of the CCO frequency, f_o to track the input reference signal, $f_{ref} \bullet N$ as it gradually shifted away from the free running frequency, f_f. Assuming that the CCO is capable of sufficient frequency deviation and that the internal loop amplifier and filter are not overdriven, the CCO will track until the phase error, θ_e approaches $\pm\pi/2$ radians. Figures 5 through 8 are a direct measurement of the hold–in range (i.e. $\Delta f_{ref} \times N = \pm\Delta f_H \times 2\pi$). Since sin θ_e cannot exceed ±1.0, as θ_e approaches $\pm\pi/2$ the hold–in range is equal to the DC loop gain, $K_v \times N$.

$$\pm\Delta\omega_H = \pm K_v \times N$$

where, $K_v = K_p K_o K_n$.

In the above example,

$\pm\Delta\omega_H = \pm$ 27.3 Mrad/sec

$\pm\Delta f_H = \pm$ 4.35 MHz

Extended Hold–in Range

The hold–in range of about 3.4% could cause problems over temperature in cases where the free–running oscillator drifts more than 2 to 3% because of relatively high temperature coefficients of the ferrite tuned CCO inductor. This problem might worsen for lower frequency applications where the external tuning coil is large compared to internal capacitance at Pins 1 and 4. To improve hold–in range performance, it is apparent that the gain factors involved must be carefully considered.

K_n = is either 1/8 in the MC13175 or 1/32 in the MC13176.

K_p = is fixed internally and cannot be altered.

K_o = Figures 9 and 10 suggest that there is capability of greater control range with more current swing. However, this swing must be symmetrical about the center of the dynamic response. The suggested zero current operating point for ±100 μA swing of the CCO is at about + 70 μA offset point.

Ka = External loop amplification will be necessary since the phase detector only supplies ± 30 μA.

In the design example in Figure 15, an external resistor (R_5) of 15 k to V_{CC} (3.0 Vdc) provides approximately 100 μA of current boost to supplement the existing 50 μA internal source current. R_4 (1.0 k) is selected for approximately 0.1 Vdc across it with 100 μA. R_1, R_2 and R_3 are selected to set the potential at Pin 7 and the base of 2N4402 at approximately 0.9 Vdc and the emitter at 1.55 Vdc when error current to Pin 6 is approximately zero μA. C_1 is chosen to reduce the level of the crystal sidebands.

Figure 15. External Loop Amplifier

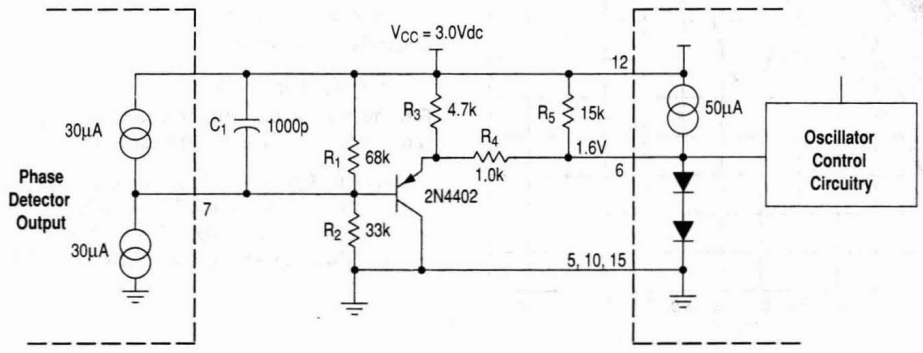
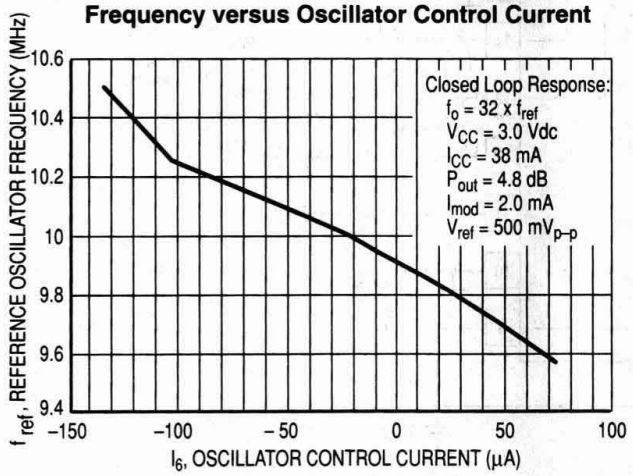


Figure 16 shows the improved hold–in range of the loop. The Δf_{ref} is moved 950 kHz with over 200 μA swing of control current for an improved hold–in range of ±15.2 MHz or ± 95.46 Mrad/sec.

Figure 16. MC13176 Reference Oscillator Frequency versus Oscillator Control Current



Lock–in Range/Capture Range

If a signal is applied to the loop not equal to free running frequency, f_f, then the loop will capture or lock–in the signal by making $f_s = f_o$ (i.e. if the initial frequency difference is not too great). The lock–in range can be expressed as $\Delta\omega_L \sim \pm 2\partial\omega_n$

FM Modulation

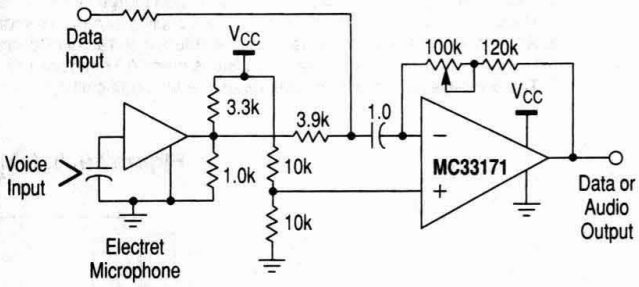
Noise external to the loop (phase detector input) is minimized by narrowing the bandwidth. This noise is minimal in a PLL system since the reference frequency is usually derived from a crystal oscillator. FM can be achieved by applying a modulation current superimposed on the control current of the CCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus, allowing the CCO to deviate in frequency. The loop bandwidth is related to the natural frequency ω_n. In the lag–lead design example where the natural frequency, ω_n = 5.0 krad/sec and a damping factor, ∂ = 0.707, the loop bandwidth = 1.64 kHz. Characterization data of the closed loop responses for both the MC13175 and MC13176 at 320 MHz (Figures 7 and 8, respectively) show satisfactory performance using only a simple low–pass loop filter network. The loop filter response is strongly influenced by the high output impedance of the push–pull current output of the phase detector.

f_c = 0.159/RC;
For R = 1.0 k + R_7 (R_7 = 53 k) and C = 390 pF
f_c = 7.55 kHz or ω_c = 47 krad/sec

The application example in Figure 18 of a 320 MHz FM transmitter demonstrates the FM capabilities of the IC. A high value series resistor (100 k) to Pin 6 sets up the current source to drive the modulation section of the chip. Its value is dependent on the peak to peak level of the encoding data and the maximum desired frequency deviation. The data input is AC coupled with a large coupling capacitor which is selected for the modulating frequency. The component placements on the circuit side and ground side of the PC board are shown in Figures 35 and 36, respectively. Figure 20 illustrates the input data of a 10 kHz modulating signal at 1.6 Vp–p. Figures 21 and 22 depict the deviation and resulting modulation spectrum showing the carrier null at – 40 dBc. Figure 23 shows the unmodulated carrier power output at 3.5 dBm for V_{CC} = 3.0 Vdc.

For voice applications using a dynamic or an electret microphone, an op amp is used to amplify the microphone's low level output. The microphone amplifier circuit is shown in Figure 17. Figure 19 shows an application example for NBFM audio or direct FSK in which the reference crystal oscillator is modulated.

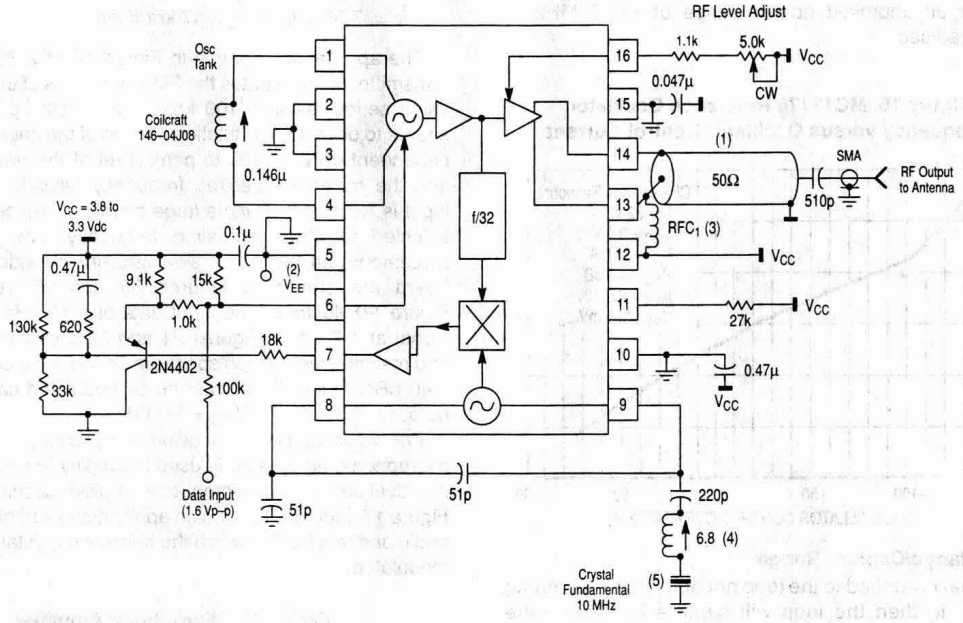
Figure 17. Microphone Amplifier



Local Oscillator Application

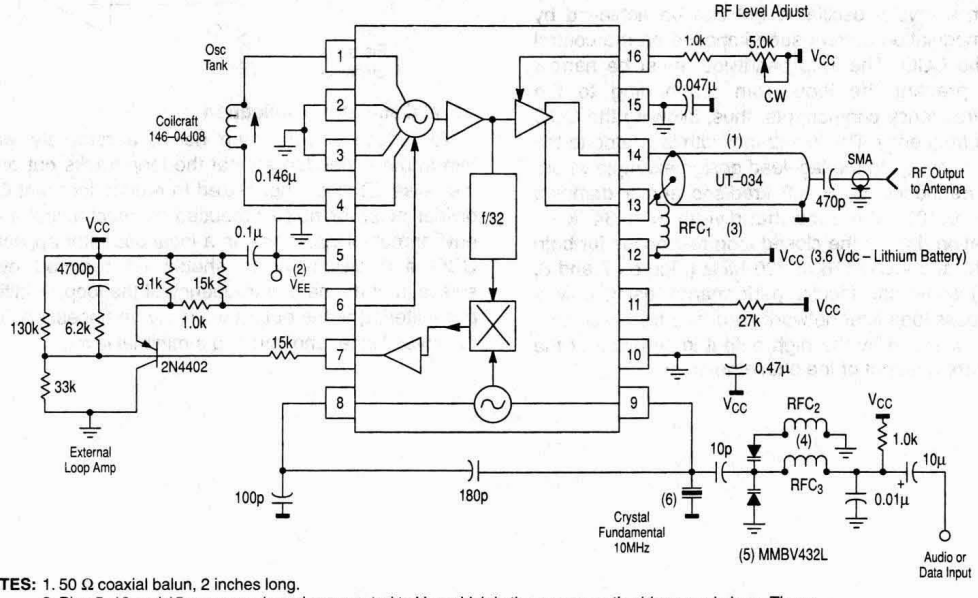
To reduce internal loop noise, a relatively wide loop bandwidth is needed so that the loop tracks out or cancels the noise. This is emphasized to reduce inherent CCO and divider noise or noise produced by mechanical shock and environmental vibrations. In a local oscillator application the CCO and divider noise should be reduced by proper selection of the natural frequency of the loop. Additional low pass filtering of the output will likely be necessary to reduce the crystal sideband spurs to a minimal level.

Figure 18. 320 MHz MC13176D FM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor or 190 nH Coilcraft 146–05J08.
4. Recommended source is a Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3–682.
5. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 19. 320 MHz NBFM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor.
4. RFC_2 and RFC_3 are high impedance crystal frequency of 10 MHz; 8.2 µH molded inductor gives XL > 1000 Ω..
5. A single varactor like the MV2105 may be used whereby RFC_2 is not needed.
6. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 20. Input Data Waveform

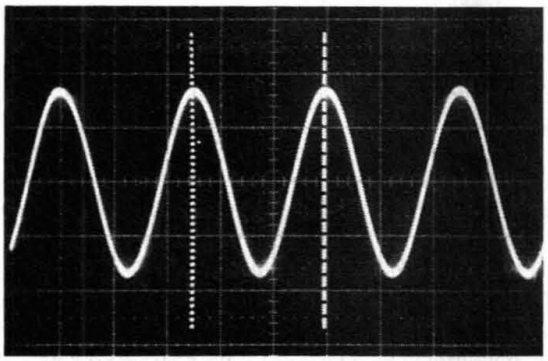


Figure 21. Frequency Deviation

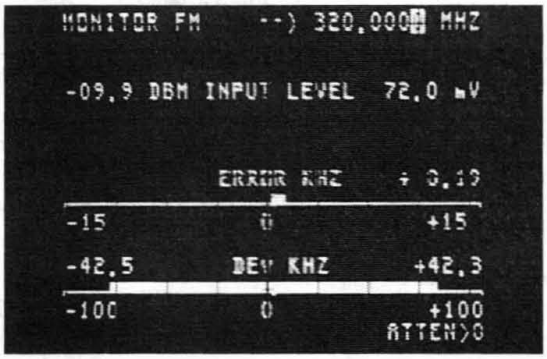


Figure 22. Modulation Spectrum

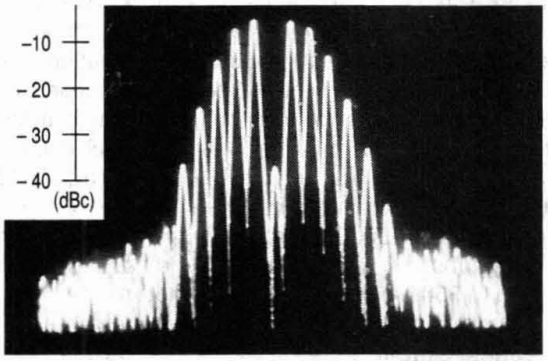
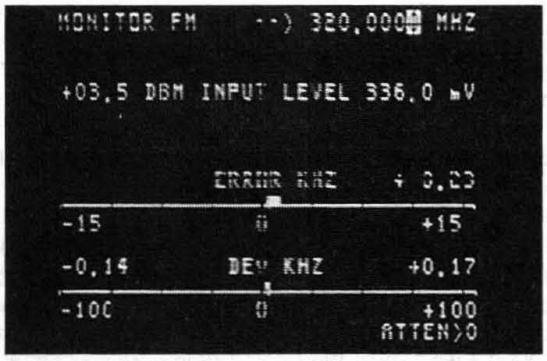


Figure 23. Unmodulated Carrier



Reference Crystal Oscillator (Pins 8 and 9)

Selection of Proper Crystal: A crystal can operate in a number of mechanical modes. The lowest resonant frequency mode is its fundamental while higher order modes are called overtones. At each mechanical resonance, a crystal behaves like a RLC series–tuned circuit having a large inductor and a high Q. The inductor L_s is series resonance with a dynamic capacitor, C_s determined by the elasticity of the crystal lattice and a series resistance R_s, which accounts for the power dissipated in heating the crystal. This series RLC circuit is in parallel with a static capacitance, C_p which is created by the crystal block and by the metal plates and leads that make contact with it.

Figure 24 is the equivalent circuit for a crystal in a single resonant mode. It is assumed that other modes of resonance are so far off frequency that their effects are negligible.

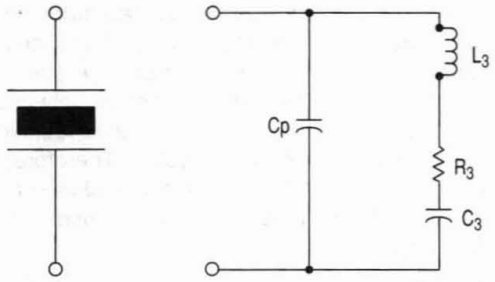
Series resonant frequency, f_s is given by;

$$f_s = 1/2\pi(L_sC_s)^{1/2}$$

and parallel resonant frequency, f_p is given by;

$$f_p = f_s(1 + C_s/C_p)^{1/2}$$

Figure 24. Crystal Equivalent Circuit



the frequency separation at resonance is given by;

$$\Delta f = f_p - f_s = f_s[1 - (1 + C_s/C_p)^{1/2}]$$

Usually f_p is less than 1% higher than f_s, and a crystal exhibits an extremely wide variation of the reactance with frequency between f_p and f_s. A crystal oscillator circuit is very stable with frequency. This high rate of change of impedance with frequency stabilizes the oscillator, because any significant change in oscillator frequency will cause a large phase shift in the feedback loop keeping the oscillator on frequency.

Manufacturers specify crystal for either series or parallel resonant operation. The frequency for the parallel mode is calibrated with a specified shunt capacitance called a "load capacitance." The most common value is 30 to 32 pF. If the load capacitance is placed in series with the crystal, the equivalent circuit will be series resonance at the specified parallel–resonant frequency. Frequencies up to 20 MHz use parallel resonant crystal operating in the fundamental mode, while above 20 MHz to about 60 MHz, a series resonant crystal specified and calibrated for operation in the overtone mode is used.

Application Examples

Two types of crystal oscillator circuits are used in the applications circuits: 1) fundamental mode common emitter Colpitts (Figures 1, 18, 19, and 25), and 2) third overtone impedance inversion Colpitts (also Figures 1 and 25).

The fundamental mode common emitter Colpitts uses a parallel resonant crystal calibrated with a 32 pf load capacitance. The capacitance values are chosen to provide excellent frequency stability and output power of > 500 mVp–p at Pin 9. In Figures 1 and 25, the fundamental mode reference oscillator is fixed tuned relying on the repeatability of the crystal and passive network to maintain the frequency, while in the circuit shown in Figures 18 and 19, the oscillator frequency can be adjusted with the variable inductor for the precise operating frequency.

The third overtone impedance inversion Colpitts uses a series resonance crystal with a 25 ppm tolerance. In the application examples (Figures 1 and 25), the reference oscillator operates with the third overtone crystal at 40.0000 MHz. Thus, the MC13175 is operated at 320 MHz (f_o/8 = crystal; 320/8 = 40.0000 MHz. The resistor across the crystal ensures that the crystal will operate in the series resonant mode. A tuneable inductor is used to adjust the oscillation frequency; it forms a parallel resonant circuit with the series and parallel combination of the external capacitors forming the divider and feedback network and the base–emitter capacitance of the device. If the crystal is shorted, the reference oscillator should free–run at the frequency dictated by the parallel resonant LC network.

The reference oscillator can be operated as high as 60 MHz with a third overtone crystal. Therefore, it is possible to use the MC13175 up to at least 480 MHz and the MC13176 up to 950 MHz (based on the maximum capability of the divider network).

Enable (Pin 11)

The enabling resistor at Pin 11 is calculated by:

$$R_{eg.\ enable} = V_{CC} - 1.0\ Vdc/I_{reg.\ enable}$$

From Figure 4, $I_{reg.\ enable}$ is chosen to be 75 µA. So, for a V_{CC} = 3.0 Vdc $R_{reg.\ enable}$ = 26.6 kΩ, a standard value 27 kΩ resistor is adequate.

Layout Considerations

Supply (Pin 12): In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactance along the trace; it is best that V_{CC} (RF ground) completely fills around the surface mounted components and interconnect traces on the circuit side of the board. This technique is demonstrated in the evaluation PC board.

Battery/Selection/Lithium Types

The device may be operated from a 3.0 V lithium battery. Selection of a suitable battery is important. Because one of the major problems for long life battery powered equipment is oxidation of the battery terminals, a battery mounted in a clip–in socket is not advised. The battery leads or contact post should be isolated from the air to eliminate oxide build–up. The battery should have PC board mounting tabs which can be soldered to the PCB. Consideration should be given for the peak current capability of the battery. Lithium batteries have current handling capabilities based on the composition of the lithium compound, construction and the battery size. A 1300 mA/hr rating can be achieved in the cylindrical cell battery. The Rayovac CR2/3A lithium–manganese dioxide battery is a crimp sealed, spiral wound 3.0 Vdc, 1300 mA/hr cylindrical cell with PC board mounting tabs. It is an excellent choice based on capacity and size (1.358″ long by 0.665″ in diameter).

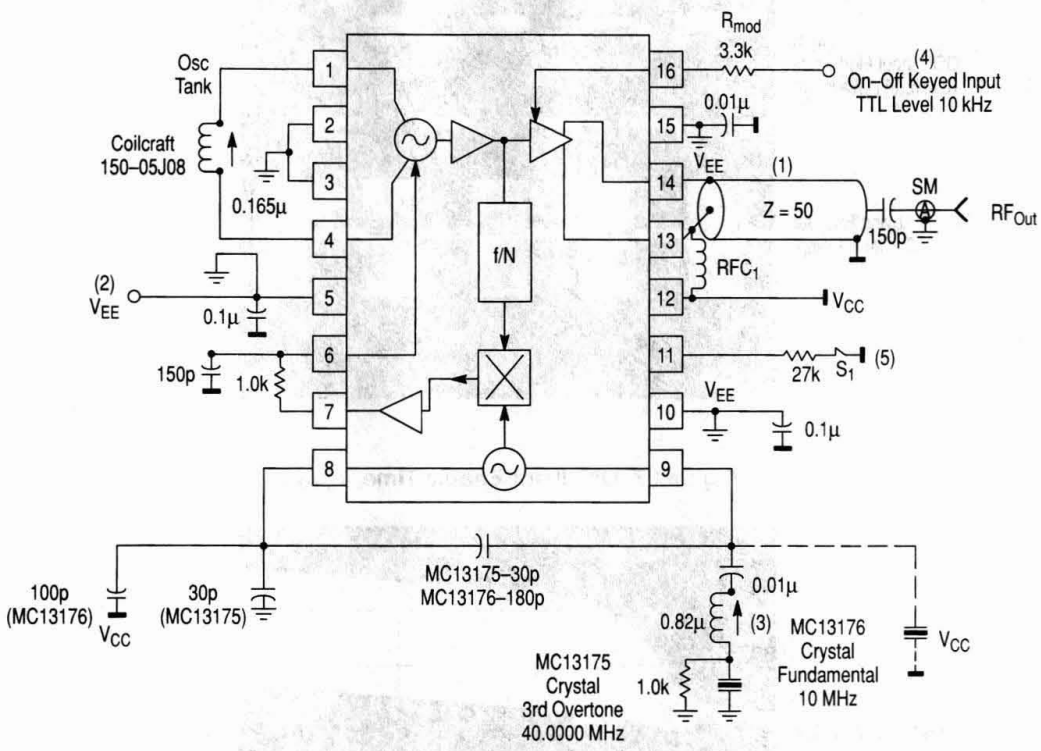
Differential Output (Pins 13, 14)

The availability of micro–coaxial cable and small baluns in surface mount and radial–leaded components allows for simple interface to the output ports. A loop antenna may be directly connected with bias via RFC or 50 Ω resistors. Antenna configuration will vary depending on the space available and the frequency of operation.

AM Modulation (Pin 16)

Amplitude Shift Key: The MC13175 and MC13176 are designed to accommodate Amplitude Shift Keying (ASK). ASK modulation is a form of digital modulation corresponding to AM. The amplitude of the carrier is switched between two or more values in response to the PCM code. For the binary case, the usual choice is On–Off Keying (often abbreviated OOK). The resultant amplitude modulated waveform consists of RF pulses called marks, representing binary 1 and spaces representing binary 0.

Figure 25. ASK 320 MHz Application Circuit



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength line (1.5″) provides the best match to a 50 Ω load.

2. Pins 5, 10 and 15 are ground and connnected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.

3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); 1.0 k resistor shunting the crystal prevents it from oscillating in the fundamental mode. Recommended source is Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3–821.

4. The On–Off keyed signal turns the output of the transmitter off and on with TTL level pulses through R_{mod} at Pin 16. The "On" power and I_{CC} is set by the resistor which sets $I_{mod} = VTTL - 0.8 / R_{mod}$. (see Figure 28).

5. S1 simulates an enable gate pulse from a microprocessor which will enable the transmitter. (see Figure 4 to determine precise value of the enabling resistor based on the potential of the gate pulse and the desired enable.)

Figure 25 shows a typical application in which the output power has been reduced for linearity and current drain. The current draw on the device is 16 mA I_{CC} (average) and – 22.5 dBm (average power output) using a 10 kHz modulating rate for the on–off keying. This equates to 20 mA and – 2.3 dBm "On", 13 mA and – 41 dBm "Off". In Figure 26, the device's modulating waveform and encoded carrier are displayed. The crystal oscillator enable time is needed to set the acquisition timing. It takes typically 4.0 msec to reach full magnitude of the oscillator waveform (see Figure 27, Oscillator Waveform, at Pin 8). A square waveform of 3.0 V peak with a period that is greater than the oscillator enable time is applied to the Enable (Pin 11).

Figure 26. ASK Input Waveform and Modulated Carrier

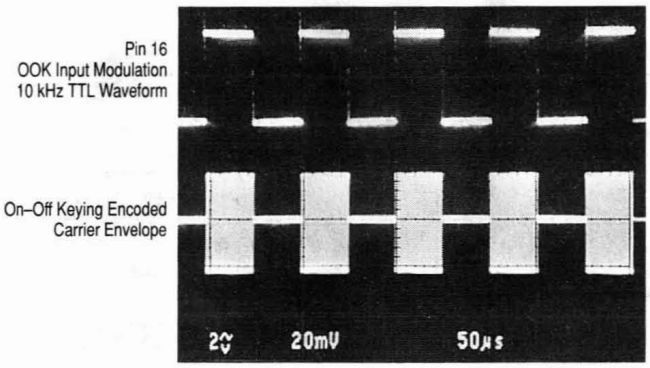


Figure 27. Oscillator Enable Time, T_{enable}

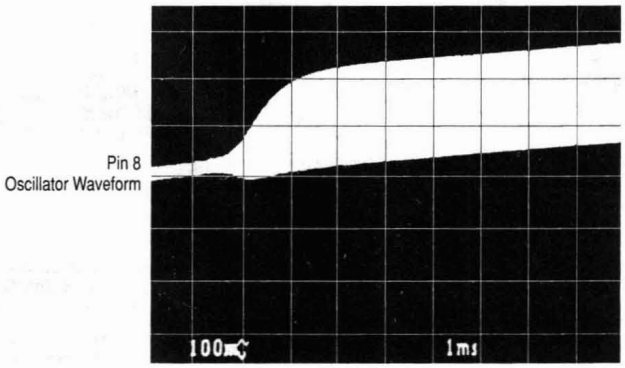
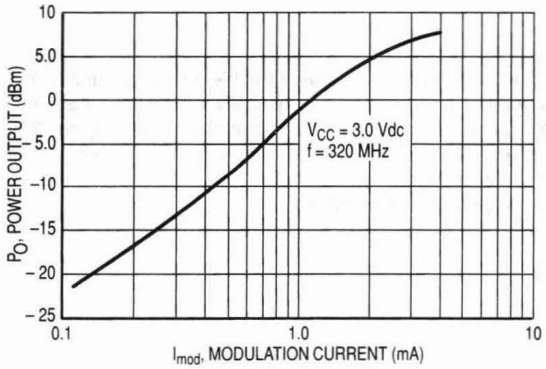


Figure 28. Power Output versus Modulation Current



Analog AM

In analog AM applications, the output amplifier's linearity must be carefully considered. Figure 28 is a plot of Power Output versus Modulation Current at 320 MHz, 3.0 Vdc. In order to achieve a linear encoding of the modulating sinusoidal waveform on the carrier, the modulating signal must amplitude modulate the carrier in the linear portion of its power output response. When using a sinewave modulating signal, the signal rides on a positive DC offset called V_{mod} which sets a static (modulation off) modulation current, I_{mod}. I_{mod} controls the power output of the IC. As the modulating signal moves around this static bias point the modulating current varies causing power output to vary or to be AM modulated. When the IC is operated at modulation current levels greater than 2.0 mAdc the differential output stage starts to saturate.

In the design example, shown in Figure 29, the operating point is selected as a tradeoff between average power output and quality of the AM.

For V_{CC} = 3.0 Vdc; I_{CC} = 18.5 mA and I_{mod} = 0.5 mAdc and a static DC offset of 1.04 Vdc, the circuit shown in Figure 29 completes the design. Figures 30, 31 and 32 show the results of – 6.9 dBm output power and 100% modulation by the 10 kHz and 1.0 MHz modulating sinewave signals. The amplitude of the input signals is approximately 800 mVp–p.

Where R_{mod} = (V_{CC} – 1.04 Vdc)/0.5 mA = 3.92 k, use a standard value resistor of 3.9 k.

Figure 29. Analog AM Transmitter

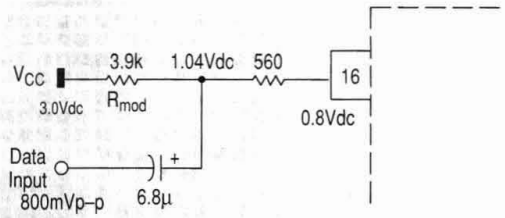


Figure 30. Power Output of Unmodulated Carrier

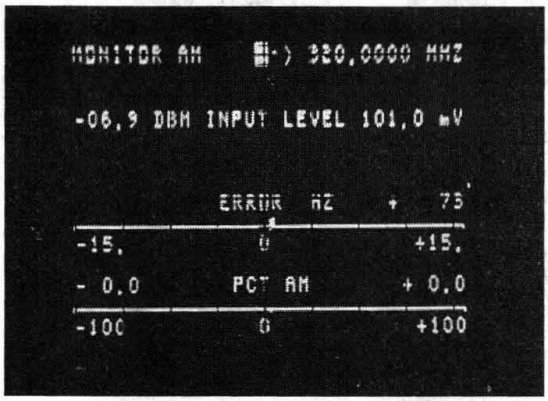


Figure 31. Input Signal and AM Modulated Carrier for f_{mod} = 10 kHz

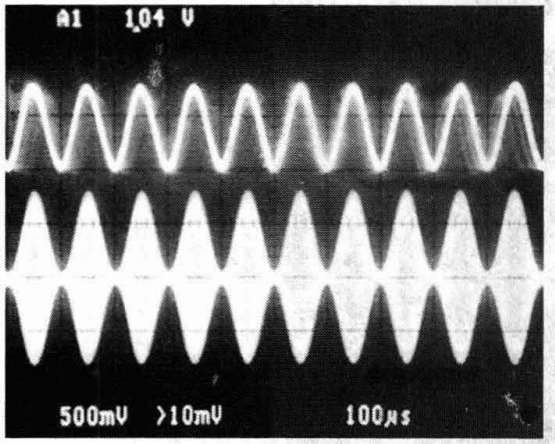


Figure 32. Input Signal and AM Modulated Carrier for f_{mod} = 1.0 MHz

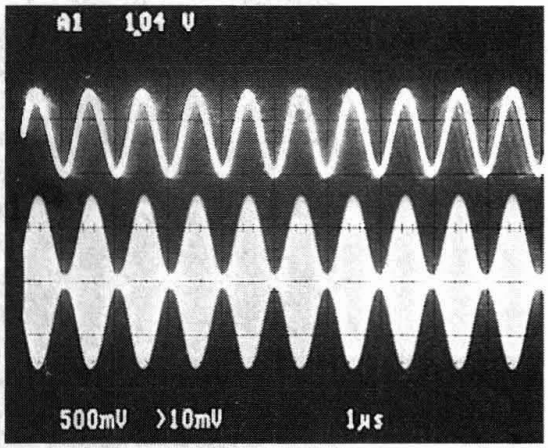


Figure 33. Circuit Side View of MC1317XD

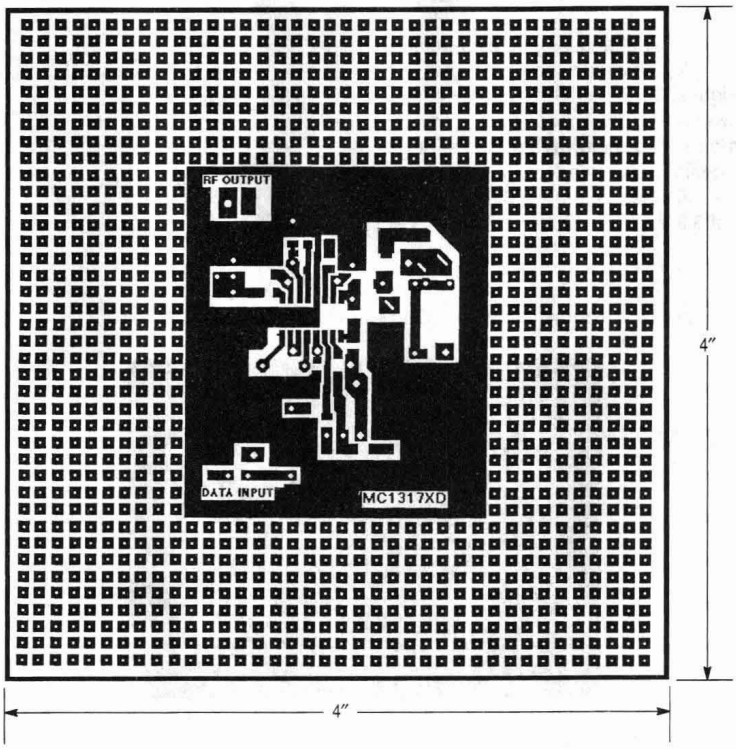


Figure 34. Ground Side View

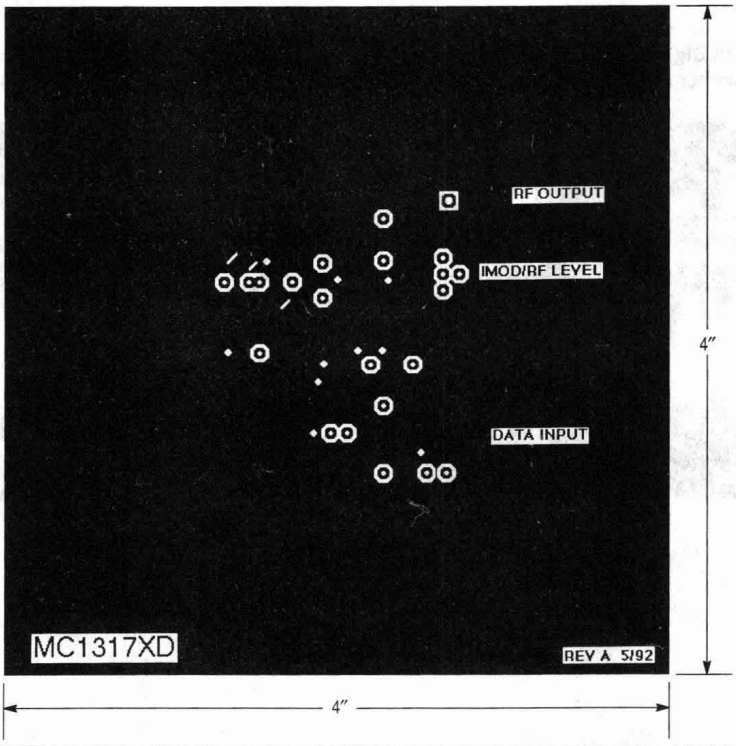


Figure 35. Surface Mounted Components Placement (on Circuit Side)

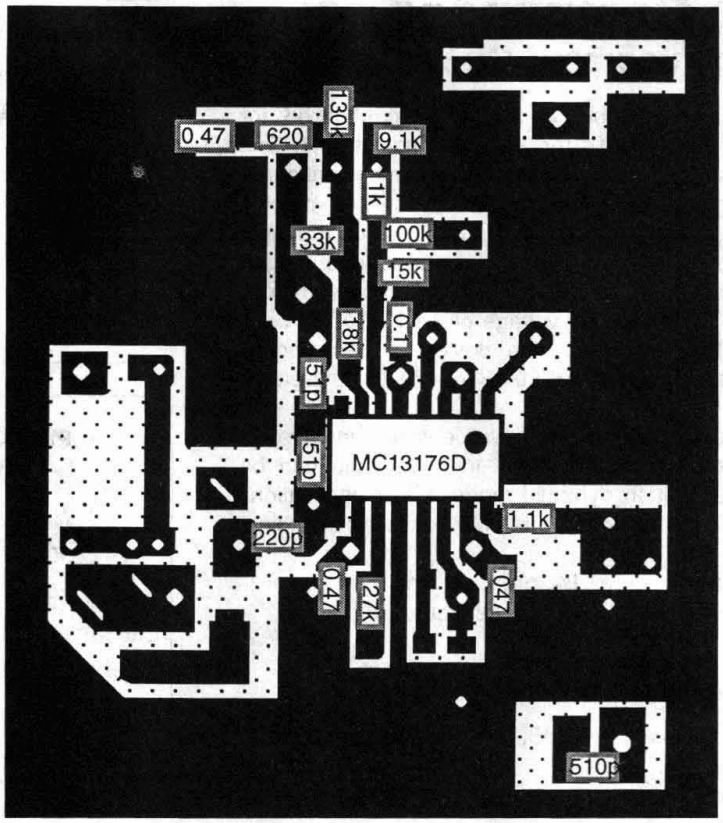
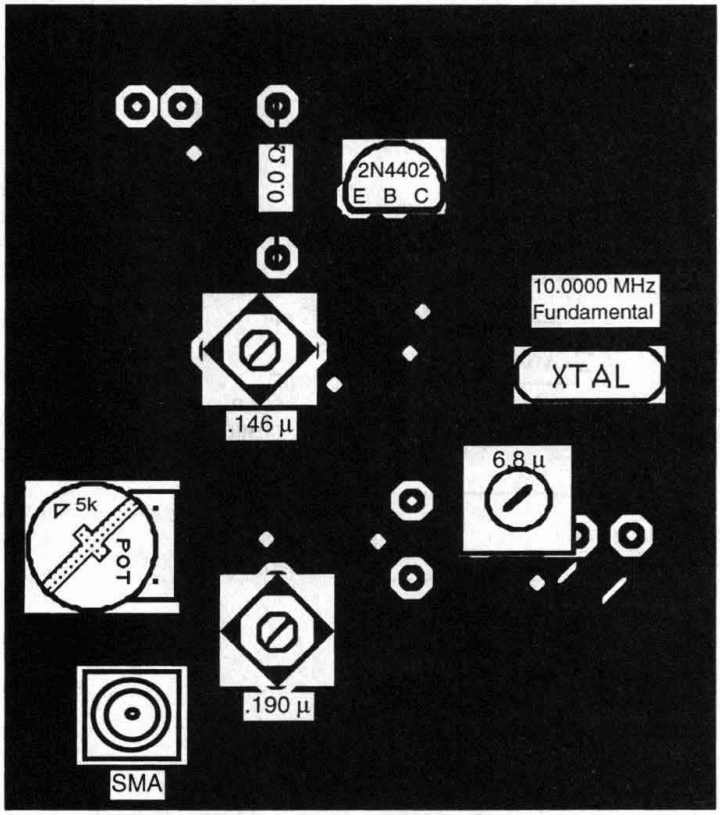


Figure 36. Radial Leaded Components Placement (on Ground Side)



MOTOROLA

Low Voltage Compander

Silicon Monolithic Integrated Circuit

MC33110

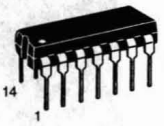
The MC33110 contains two variable gain circuits configured for compressing and expanding the dynamic range of an audio signal. One circuit is configured as an expander, while the other circuit can be configured as a compressor or expander. Each circuit has a full wave rectifier to provide average value information to a variable gain cell located in either the input stage or the feedback path. An internal, temperature stable bandgap reference provides the necessary precision voltages and currents required.

The MC33110 will operate from a supply voltage of 2.1 to 7.0 V, over a temperature range of – 40° to + 85°C. The device is designed to accommodate an 80 dB dynamic range from – 60 dB to + 20 dB, referenced to 100 mVrms.

Applications include cordless telephone, CB, walkie–talkie, most voice RF links, and any application where the signal–to–noise ratio can be improved by reducing the transmitted dynamic range. Other applications include speakerphone and voice activated intercom, dictating machine, standard telephone, etc.

The MC33110 is packaged in a 14 pin DIP for through–the–hole applications and an SO–14 surface mount.

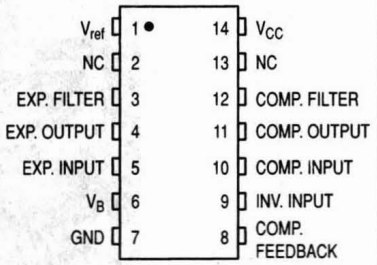
- Operating Supply Voltage: 2.1 to 7.0 V
- No Precision External Components Required
- 80 dB Dynamic Range Compressed to 40 dB, Re–expandable to 80 dB
- Unity Gain Level: 100 mVrms
- Adjustable Response Time
- Ambient Operating Temperature: – 40 to + 85°C
- Temperature Compensated Reference
- Applications Include Cordless Phone, CB Radio, Speakerphone, etc.



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

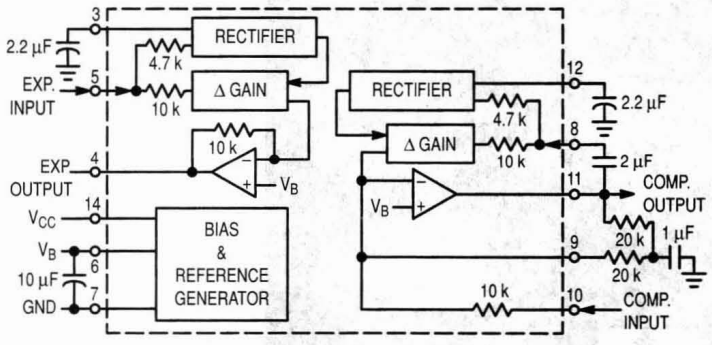
PIN CONNECTIONS
(TOP VIEW)



ORDERING INFORMATION

Device	Temperature Range	Package
MC33110D MC33110P	– 40° to + 85°C	SO–14 Plastic DIP

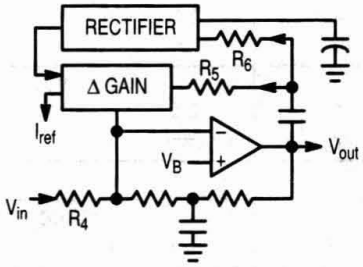
SIMPLIFIED BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin	Description
V_{ref}	1	Normally this pin is not used and is left open. It can be used to make limited adjustments to the 0 dB level. Any noise or leakage at this pin will affect the 0 dB level and gain tracking.
NC	2, 13	No connection. These pins are not internally connected.
Expander Filter	3	Connect to an external capacitor to filter the full wave rectifier's output. This capacitor affects attack and decay times, as well as low frequency accuracy.
Expander Output	4	Output of the expander amplifier.
Expander Input	5	The input impedance is nominally 3.2 kΩ. Nominal signal range is 3.16 mVrms to 316 mVrms. Must be capacitor coupled to the signal source.
V_B	6	An internal reference voltage, nominally $V_{CC}/2$. This is an ac ground and must be well filtered to obtain high power supply rejection and low crosstalk.
Ground	7	Connect to a clean power supply ground.
Compressor Feedback	8	Input to the compressor variable gain stage and rectifier. Normally the signal is supplied by the compressor's output (Pin 11). Input impedance is nominally 3.2 kΩ.
Inverting Input	9	Inverting input to the compressor amplifier. Normally, this is connected to the compressor's output through a filtered DC feedback path.
Compressor Input	10	The input impedance is nominally 10 kΩ. Nominal signal range is 100 μVrms to 1.0 Vrms. Must be capacitor coupled to the signal source.
Compressor Output	11	Output of the compressor amplifier.
Compressor Filter	12	Connect to an external capacitor to filter the full wave rectifier's output. This capacitor affects attack & decay times, and low frequency accuracy.
V_{CC}	14	Power supply pin. Connect to a power supply providing between 2.1 V and 7.0 V. Nominal current consumption is 3.5 mA.

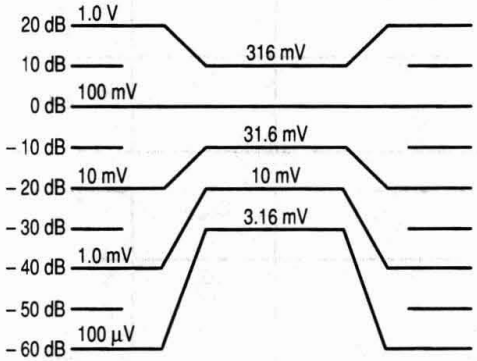
COMPRESSOR



$$V_{out} = \sqrt{\frac{R_5 \times R_6 \times I_{ref} \times V_{in}}{7.2 \times R_4}}$$

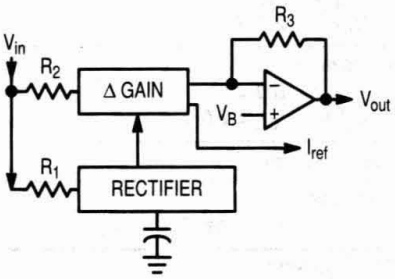
$$= 0.3162 \times \sqrt{V_{in}}$$

TRANSFER FUNCTIONS



(VOLTAGES ARE RMS)

EXPANDER



$$V_{out} = \frac{7.2 \times R_3 \times V_{in}^2}{R_1 \times R_2 \times I_{ref}}$$

$$= 10 \times V_{in}^2$$

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Supply Voltage	V_{CC}	+ 12, – 0.5	Vdc
High Input Voltage (Pin 5 & 10)	V_{IH}	V_{CC} + 0.5	Vdc
Low Input Voltage	V_{IL}	– 0.5	Vdc
Output Source Current (Pin 4 & 11)	I_{O+}	Self–Limiting	
Output Sink Current	I_{O-}	20	mA
Junction Temperature	T_J	– 65, + 150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage	V_{CC}	2.1	—	7.0	Vdc
Input Voltage Range	V_{IR}				Vrms
Compressor, 2.1 V < V_{CC} < 7.0 V		0	—	1.0	
Expander, V_{CC} = 2.1 V		0	—	0.25	
Expander, 3.0 V < V_{CC} < 7.0 V		0	—	0.316	
Input Frequency	F_{in}	100	—	20 k	Hz
Output Load	R_L				Ω
Compressor (Pin 11, V_O = 100 mV)		300	—	∞	
Expander (Pin 4, V_O = 100 mV)		150	—	∞	
Ambient Temperature	T_A	– 40	—	+ 85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, f = 1.0 kHz, unless otherwise noted, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Power Supply Current	I_{CC}				mA
V_{CC} = + 5.0 V		—	3.5	5.5	
V_{CC} = + 2.1 V		—	3.3	—	
V_B Voltage	V_B				Vdc
V_{CC} = + 5.0 V		2.4	2.5	2.6	
2.1 V < V_{CC} < 7.0 V		—	$V_{CC}/2$	—	
COMPRESSOR					
0 dB Gain	$G_{(CO)}$				dB
V_{in} = 100 mVrms, Pin 1 = Open		– 1.5	0	1.5	
Gain Tracking	G_t				dB
@ V_{in} = 1.0 Vrms, output relative to $G_{(CO)}$		+ 9.0	+ 10	+ 11	
@ V_{in} = 10 mVrms, output relative to $G_{(CO)}$		—	– 10	—	
@ V_{in} = 1.0 mVrms, output relative to $G_{(CO)}$		—	– 20	—	
@ V_{in} = 100 µVrms, output relative to $G_{(CO)}$		– 31	– 30	– 29	
Total Harmonic Distortion	THD				%
V_{in} = 100 mVrms, f = 1.0 kHz		0	0.1	1.5	
Power Supply Rejection	PSRR				dB
f = 1.0 kHz, C_{VB} = 10 µF, V_{in} = – 20 dB		—	22	—	
Attack Time (Capacitor @ Pin 12 = 2.2 µF)	$t_{a(C)}$	—	6.0	—	ms
Decay Time (Capacitor @ Pin 12 = 2.2 µF)	$t_{d(C)}$	—	20	—	ms
Input Impedance Pin 10	R_{in}	—	10	—	kΩ
Pin 8		—	3.2	—	
Peak Output Current Pin 11	I_{pk}	—	0.3	—	mA
Output Offset	V_{OO}				mVdc
Pin 11, with respect to Pin 6, NO SIGNAL		– 150	0	+ 150	
Change from NO SIGNAL to 1.0 Vrms at Input		—	50	—	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, f = 1.0 kHz, unless otherwise noted, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
EXPANDER					
0 dB Gain (V_{in} = 100 mVrms, Pin 1 = open)	$G_{(EO)}$	 – 1.5	 0	 1.5	dB
Gain Tracking @ V_{in} = 316 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 31.6 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 10 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 3.16 mVrms, output relative to $G_{(EO)}$	G_t	 + 19 — — – 61	 + 20 – 20 – 40 – 60	 + 21 — — – 59	dB
Total Harmonic Distortion V_{in} = 100 mVrms, f = 1.0 kHz	THD	 0	 0.06	 1.5	%
Power Supply Rejection (f = 1.0 kHz, C_{VB} = 10 µF)	PSRR	—	37	—	dB
Attack Time (Capacitor @ Pin 3 = 2.2 µF)	$t_{a(E)}$	—	19	—	ms
Decay Time (Capacitor @ Pin 3 = 2.2 µF)	$t_{d(E)}$	—	20	—	ms
Input Impedance Pin 5	R_{in}	—	3.2	—	kΩ
Peak Output Current Pin 4	I_{pk}	—	1.0	—	mA
Output Offset Pin 4, with respect to Pin 6, NO SIGNAL Change from NO SIGNAL to 316 mVrms at Input	V_{OO}	 – 150 —	 0 25	 + 150 —	mVdc
MISCELLANEOUS					
Gain (Pin 10 to Pin 4; Pin 11 capacitor coupled to Pin 5) V_{CC} = 7.0 V, V_{in} = 1.0 Vrms V_{CC} = 3.0 V, V_{in} = 1.0 Vrms V_{CC} = 2.1 V, V_{in} = 31.6 mVrms	A_V	 – 2.5 – 2.5 – 2.5	 0 0 0	 + 2.5 + 2.5 + 2.5	dB
Channel Separation Expander to Compressor, output measured at Pin 11 V_{in} @ Pin 5 = 316 mVrms, f = 1.0 kHz V_{in} @ Pin 5 = 316 mVrms, f = 10 kHz	CS	 43 —	 48 68	 — —	dB
Compressor to Expander, output measured at Pin 4 V_{in} @ Pin 10 = 1.0 Vrms, f = 1.0 kHz V_{in} @ Pin 10 = 1.0 Vrms, f = 10 kHz		 65 —	 107 114	 — —	

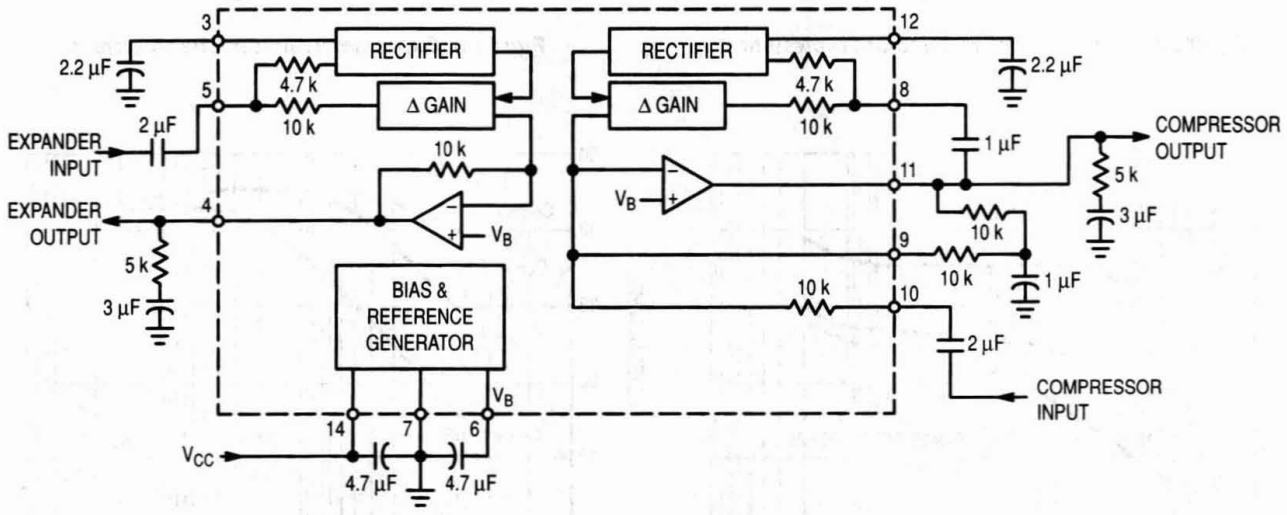


Figure 1. Test Circuit

COMPRESSOR

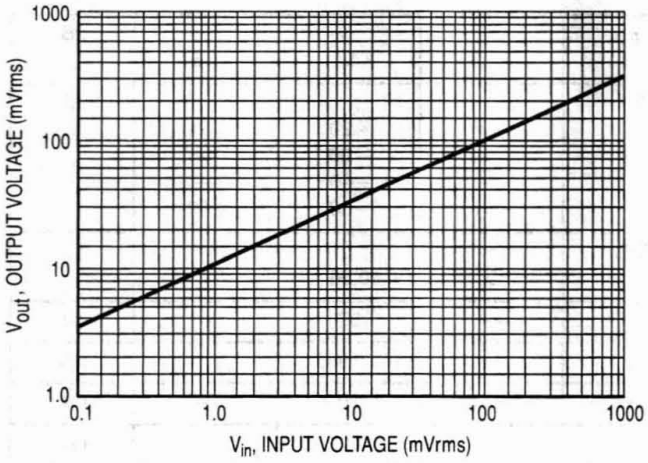


Figure 2. Compressor Transfer Characteristics

EXPANDER

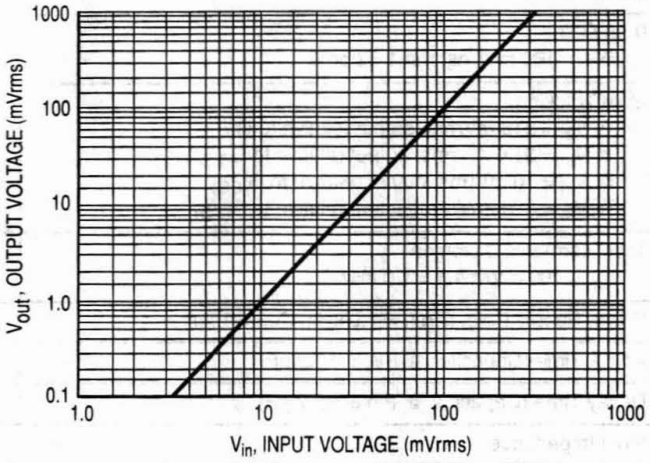


Figure 3. Expander Transfer Characteristics

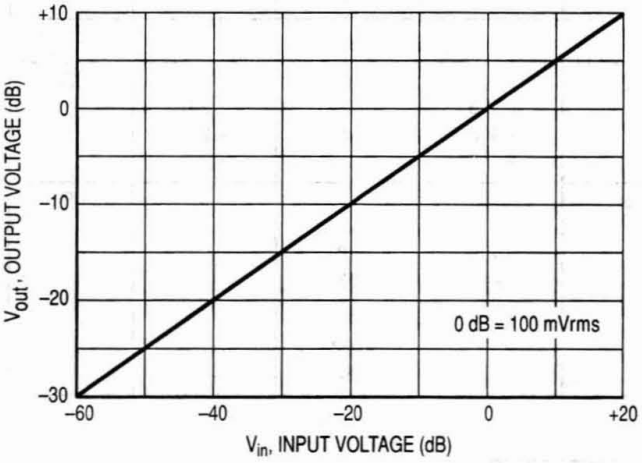


Figure 4. Compressor Transfer Characteristics

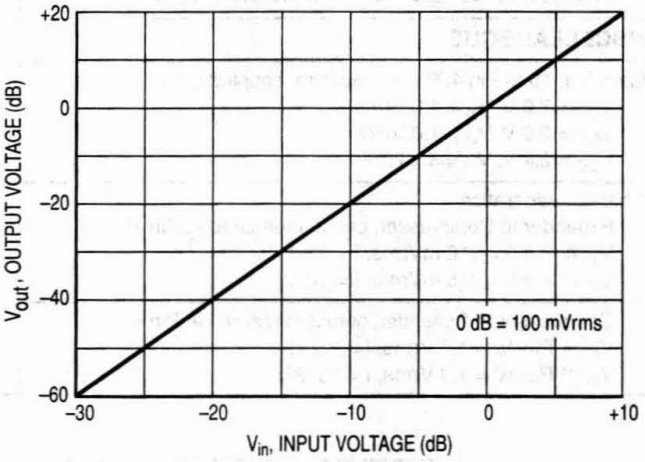


Figure 5. Expander Transfer Characteristics

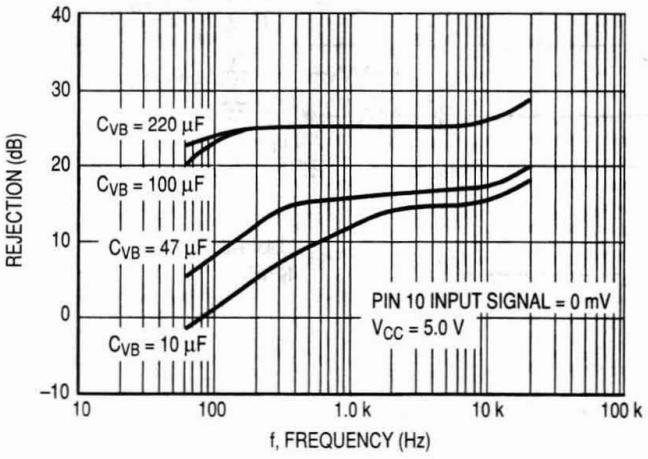


Figure 6. Power Supply Rejection (Compressor)

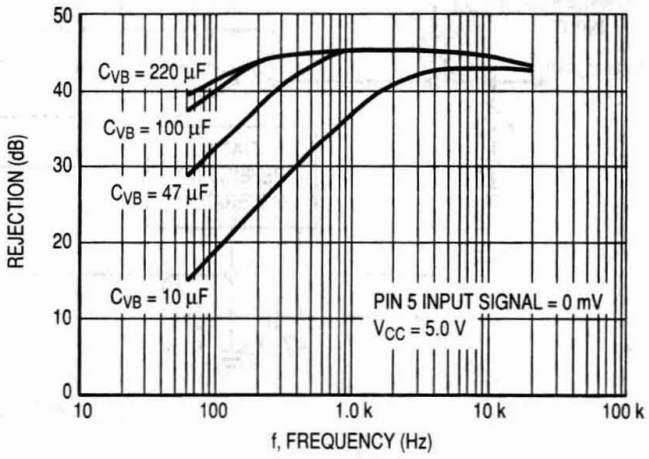


Figure 7. Power Supply Rejection (Expander)

COMPRESSOR

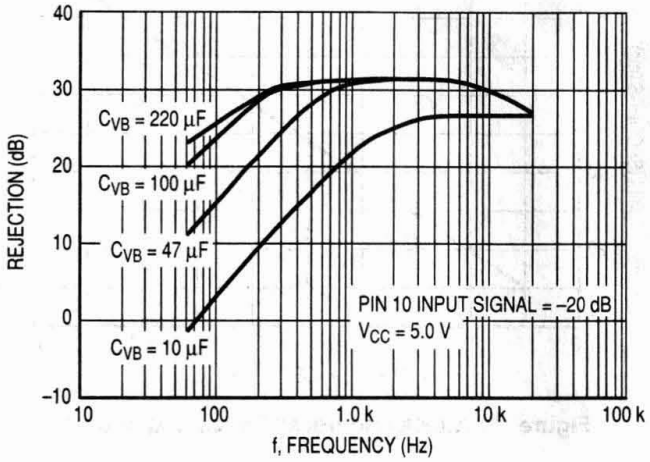


Figure 8. Power Supply Rejection (Compressor)

EXPANDER

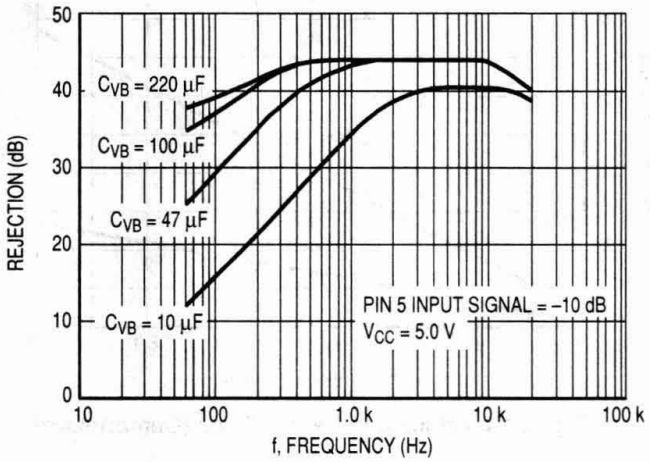


Figure 9. Power Supply Rejection (Expander)

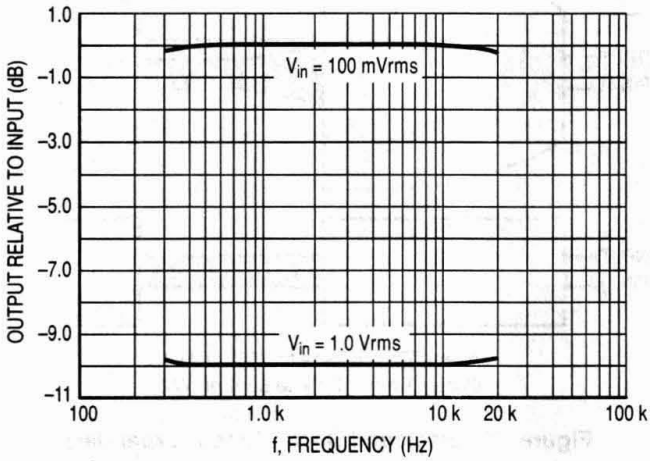


Figure 10. Frequency Response (Compressor)

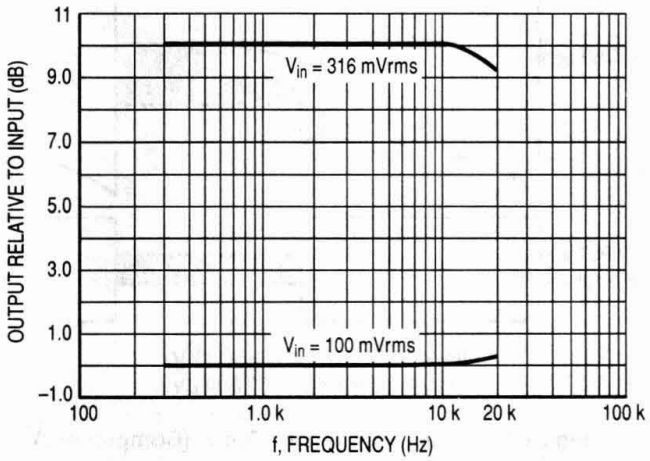


Figure 11. Frequency Response (Expander)

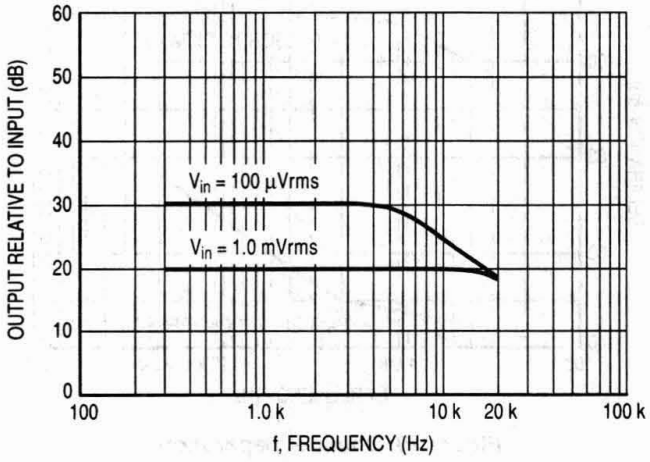


Figure 12. Frequency Response (Compressor)

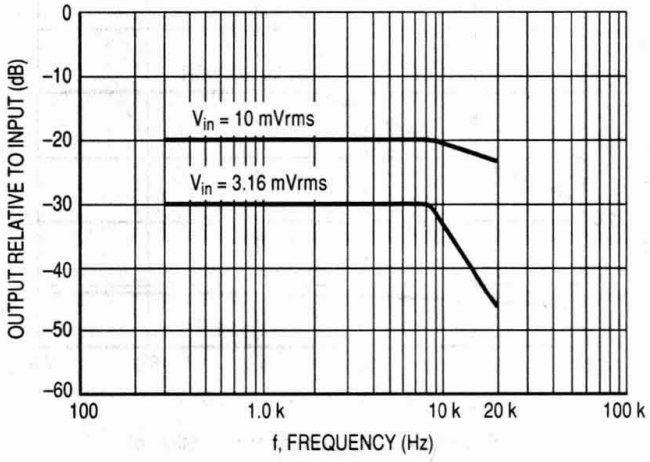


Figure 13. Frequency Response (Expander)

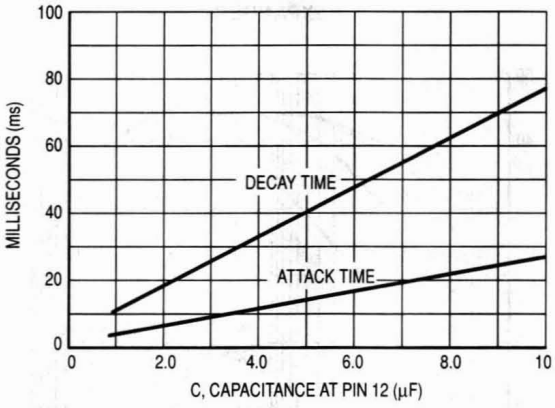


Figure 14. Attack and Decay Times (Compressor)

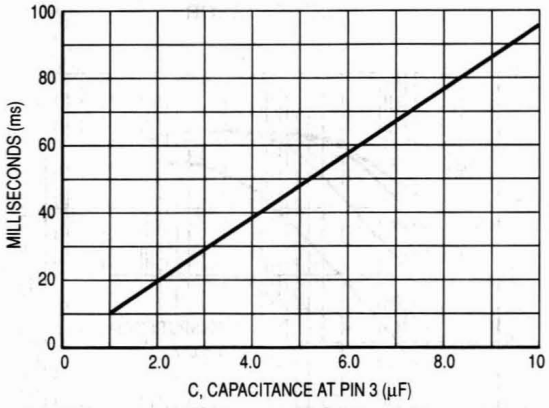
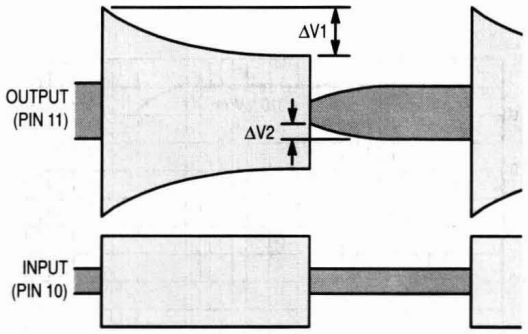
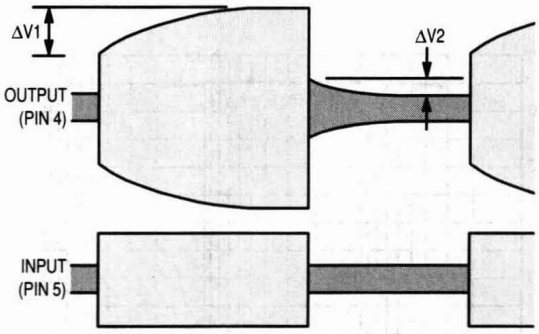


Figure 15. Attack and Decay Times (Expander)



Attack Time = Time to 63% of ΔV1.
Decay Time = Time to 63% of ΔV2.

Figure 16. Attack and Decay Times (Compressor)



Attack Time = Time to 63% of ΔV1.
Decay Time = Time to 63% of ΔV2.

Figure 17. Attack and Decay Times (Expander)

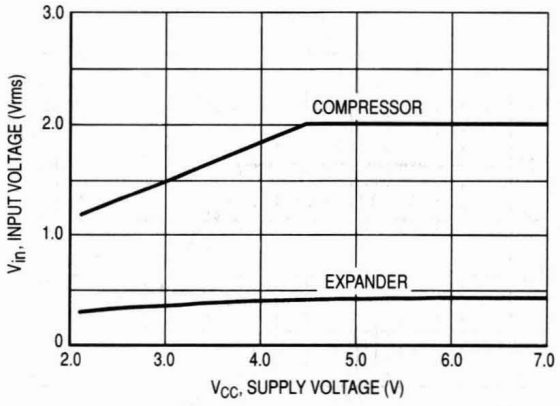


Figure 18. Maximum Input Signal

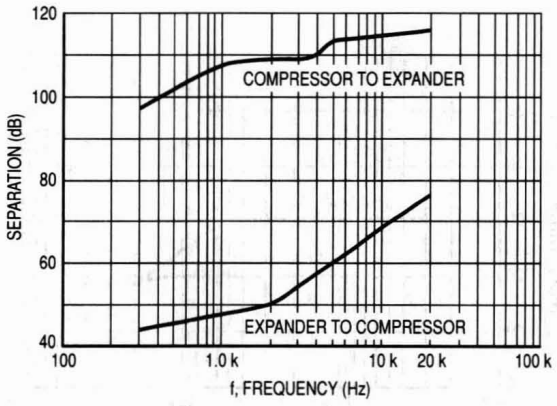


Figure 19. Channel Separation

COMPRESSOR

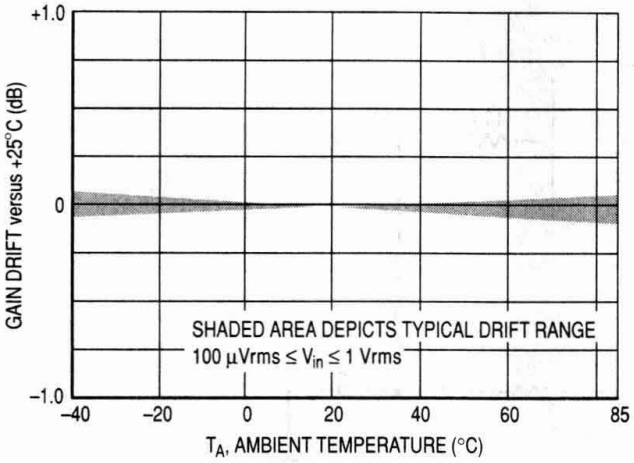


Figure 20. Compressor Gain Tracking versus Temperature

EXPANDER

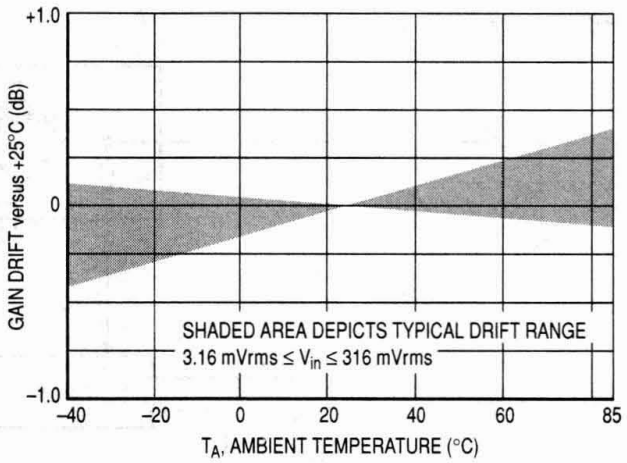


Figure 21. Expander Gain Tracking versus Temperature

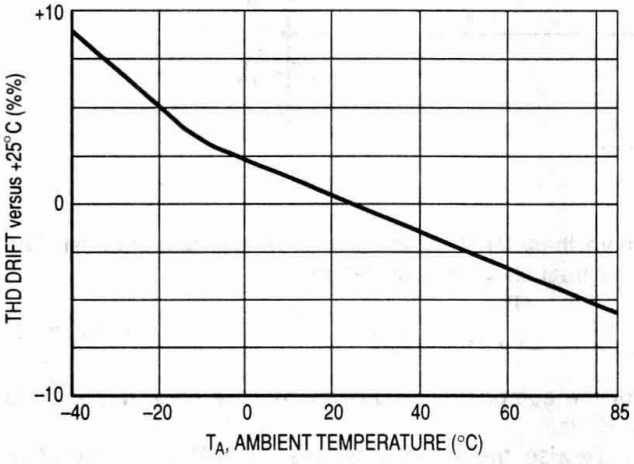


Figure 22. Compressor THD versus Temperature

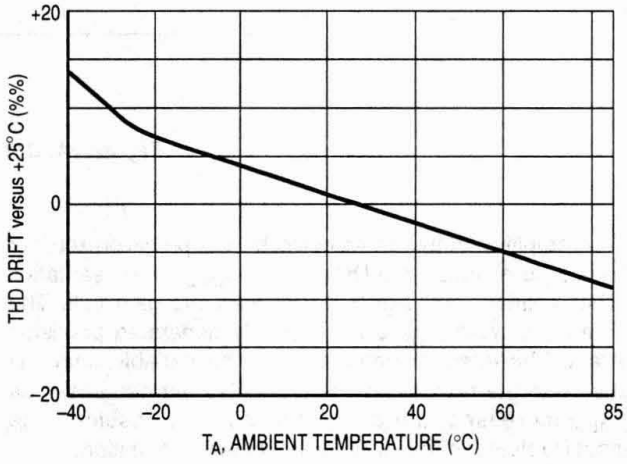


Figure 23. Expander THD versus Temperature

FUNCTIONAL DESCRIPTION

Introduction

The MC33110 compander (COMpressor and exPANDER) is composed of two variable gain circuits which provide compression and expansion of the signal dynamic range. The compressor will take a signal with an 80 dB dynamic range (100 μV to 1.0 Vrms), and reduce that to a 40 dB dynamic range by attenuating strong signals, while amplifying low level signals. The expander does the opposite in that the 40 dB signal range is increased to a dynamic range of 80 dB by amplifying strong signals and attenuating low level signals. The 0 dB level is internally set at 100 mVrms — that is the signal level which is neither amplified nor attenuated. Both circuits contain the necessary precision full wave rectifier, variable gain cell, and temperature compensated references required for accurate and stable performance.

Note: All dB values mentioned in this data sheet, unless otherwise noted, are referred to 100 mVrms.

Compressor

The compressor is an operational amplifier with a fixed input resistor and a variable gain cell in its feedback path as shown in Figure 24.

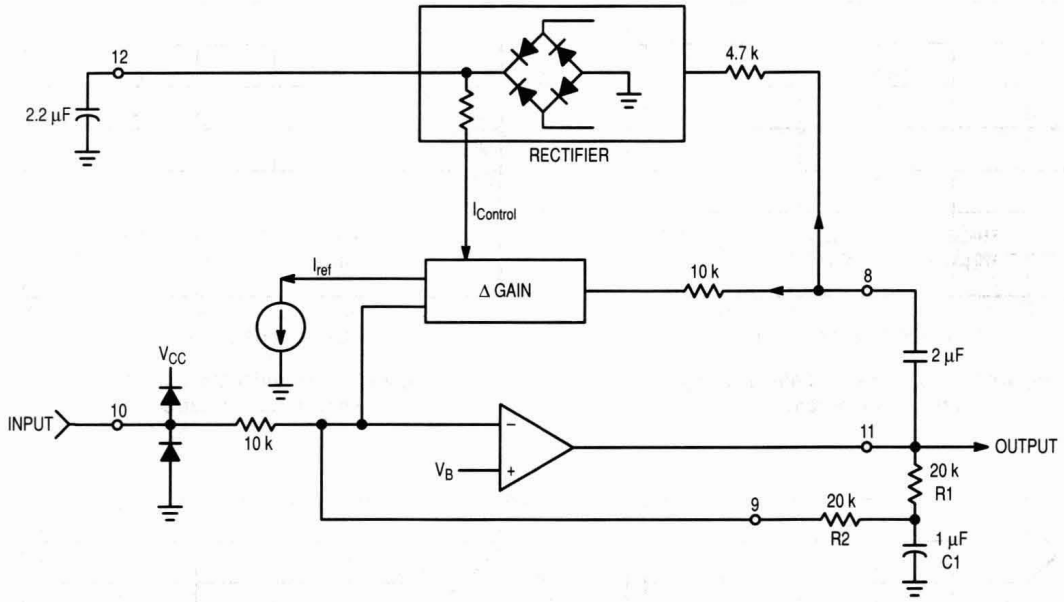


Figure 24. Compressor

The amplifier output is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{Control}$), representative of the rectifier's AC signal, to the variable gain cell. The reference current (I_{ref}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{Control}$ increases, thereby providing compression. The output is related to the input by the following equation:

$$V_{out} = 0.3162 \times \sqrt{V_{in}} \qquad \text{(Equation 1)}$$

In terms of dB levels, the relationship is:

$$V_{out(dB)} = 0.5 \times V_{in(dB)} \qquad \text{(Equation 2)}$$

where 0 dB = 100 mVrms (see Figure 2 and 4).

The inputs and output are internally biased at V_B ($V_{CC/2}$), and must therefore be capacitor coupled to external circuitry. Pin 10 input impedance is nominally 10 kΩ (± 20%), and the maximum functional input signal is shown in Figure 18. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow and distortion will show up at the output.

When no AC signals are present at the input, the variable gain cell will attempt to set such a high gain that the circuit may be come unstable. For this reason resistors R1 and R2, and capacitor C1 are added to provide DC stability. The pole formed by R1, R2 and C1 should have a pole frequency no more than 1/10th of the lowest frequency of interest. The pole frequency is calculated from:

$$f = \frac{R_1 + R_2}{2\pi \times R_1 R_2 C_1} \qquad \text{(Equation 3)}$$

for the component values shown, the pole frequency is ≈ 16 Hz.

Likewise, the capacitor between Pins 11 and 8 should be selected such that, in conjunction with the input impedance at Pin 8 (≈ 3200 Ω, ± 20%), the resulting pole frequency is no more than 1/10 of the lowest frequency of interest. With the components shown, the pole frequency is < 30 Hz. This pole frequency is calculated from:

$$f = \frac{1}{2\pi \times 3.2\ k \times C} \qquad \text{(Equation 4)}$$

The output of the rectifier is filtered by the capacitor at Pin 12, which, in conjunction with an internal 10 k resistor, provides the time constant for the attack and decay times. Figure 14 and 16 indicate how the times vary with the capacitor value. The attack time for the compressor is always faster than the decay time due to the fact that the rectifier is fed from the output rather than the input. Since the output is initially larger than expected (immediately after the input has increased), the external capacitor is charged more quickly during the initial part of the time constant. When the input is decreased, the time constant is closer to that calculated by t = RC. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Expander

The expander is an operational amplifier with a fixed feedback resistor and a variable gain cell in its input path as shown in Figure 25.

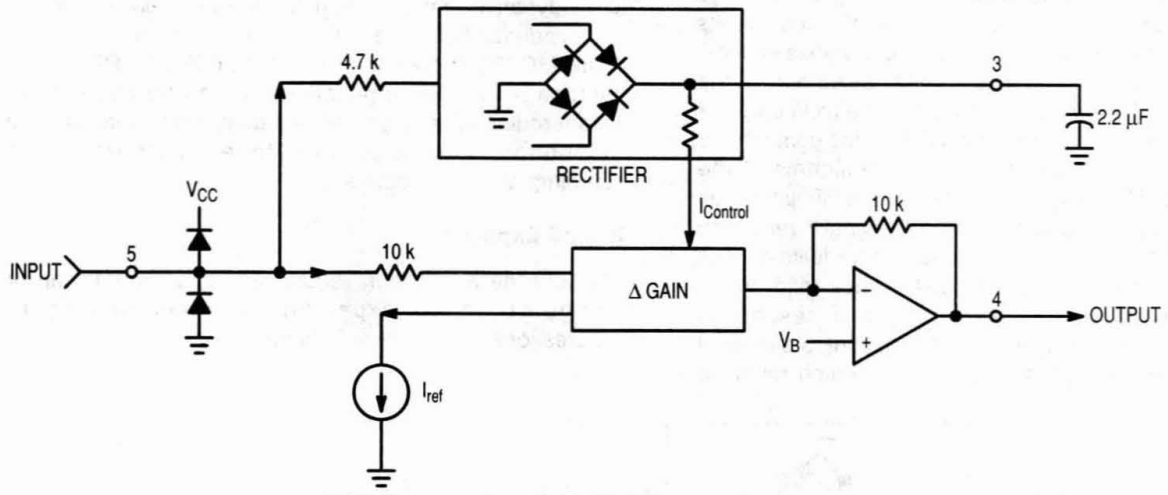


Figure 25. Expander

The input signal is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{Control}$), representative of the AC input signal, to the variable gain cell. The reference current (I_{ref}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{Control}$ increases, thereby providing expansion. The output is related to the input by the following equation:

$$V_{out} = 10 \times (V_{in})^2 \qquad \text{(Equation 5)}$$

In terms of dB levels, the relationship is:

$$V_{out(dB)} = 2.0 \times V_{in(dB)} \qquad \text{(Equation 6)}$$

where 0 dB = 100 mVrms (see Figure 3 and 5).

The inputs and output are internally biased at $V_B(V_{CC/2})$, and must therefore be capacitor coupled to external circuitry. The input impedance at Pin 5 is nominally 3.2 kΩ (± 20%), and the maximum functional input signal is shown in Figure 18. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow, and distortion will show up at the output.

The output of the rectifier is filtered by the capacitor at Pin 3, which, in conjunction with an internal 10 k resistor, provides the time constant for the attack and decay times. Figure 15 and 17 indicate how the times vary with the capacitor value. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Power Supply

The MC33110 requires a power supply voltage between 2.1 V and 7.0 V, and a nominal current of 3.5 mA. The supply voltage should be well filtered and free of ripple. A minimum of 4.7 µF in parallel with a 0.01 µF capacitor is recommended for filtering and RF bypass.

V_B (Pin 6) is an internally generated mid supply reference, and is used internally as an AC ground. The external capacitor at Pin 6 filters this voltage, and its value affects the power supply noise rejection as shown in Figures 6 through 9. This reference voltage may be used to bias external circuitry as long as the current draw is limited to < 10 µA.

Signal–to–Noise Improvement

Among the basic reasons for the original development of compander type circuits was to improve the signal–to–noise ratio of long distance telecom circuits, and of voice circuits which are transmitted over RF links (CBs, walkie–talkies, cordless phones, etc.). Since much of the noise heard at the receiving end of a transmission is due to noise picked up, for example, in the airway portion of the RF link, the compressor was developed to increase the low–level signals at the transmitting end. Then any noise picked in the RF link would be a smaller percentage of the transmitted signal level. At the receiving end, the signal is then expanded back to its original level, retaining the same high signal–to–noise ratio. While the above explanation indicates it is not necessary to attenuate strong signals (at the transmitting end), a benefit of doing this is the reduced dynamic range which must be handled by the system transmitter and receiver. The MC33110 was designed for a two–to–one compression and expansion, i.e. an 80 dB dynamic signal is compressed to a 40 dB dynamic range, transmitted to the receiving end and then expanded back to an 80 dB dynamic range.

The MC33110 compander is not limited to RF or long distance telephony applications. It can be used in any system requiring an improved signal–to–noise ratio such as telephones, speakerphones, tape recorders, digital recording, and many others.

Second Expander

Should the application require it, the MC33110 can be configured as two expanders by reconfiguring the compressor side as shown in Figure 26.

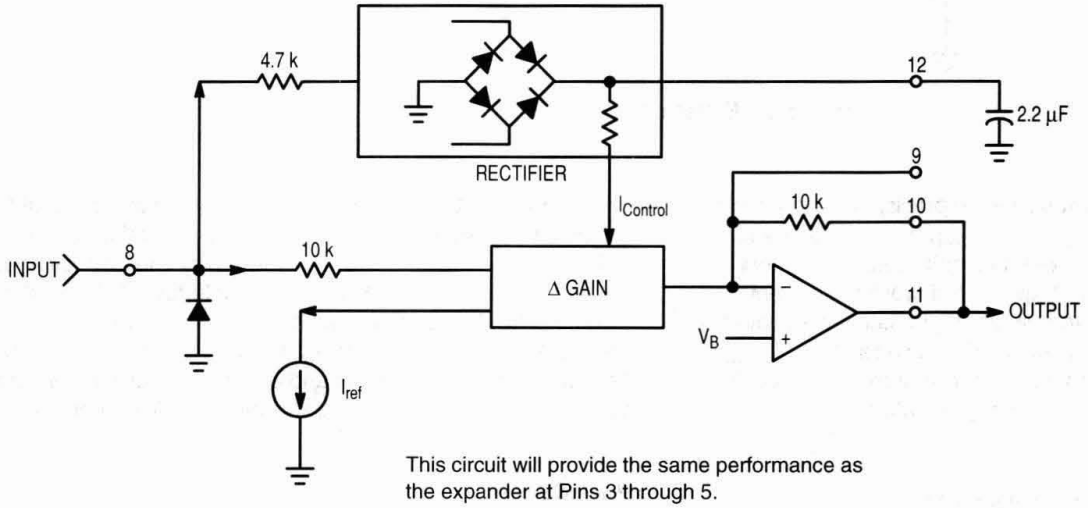


Figure 26. Second Expander

Power Supplies, Grounding

The PC board layout, the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC} or ground, can cause a distorted output, or incorrect gain level.

V_{CC} must be decoupled to the appropriate ground **at the IC** (within 1″ max) with a 4.7 µF capacitor and a 0.01 µF ceramic. A tantalum capacitor is recommended for the larger value if very high frequency noise is present since electrolytic capacitors simply have too much inductance at those frequencies. The quality of the power supply voltage should be checked at the IC with a high frequency scope. Noise spikes (always present if digital circuits are near this IC) can easily exceed 400 mV, and if they get into the IC, the output can have noise or distortion. Noise can be reduced by inserting resistors and/or inductors between the supply and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 V or greater at frequencies of 50 kHz to 1.0 MHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, a three terminal regulator (MC78L05ACP), with appropriate high frequency filtering, should be used and dedicated to the analog portion of the circuit.

The ripple content of the supply should not allow its magnitude to exceed the values in the Recommended Operating Conditions table.

The PC board tracks supplying V_{CC} and ground to the MC33110 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The analog circuitry containing the MC33110 should be close to the power supply, or the connector where the supply voltages enter the board. If V_{CC} is supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC33110 and associated circuitry.

PC Board Layout

Although this device is intended for use in the audio frequency range, the amplifiers have a bandwidth of ≈ 300 kHz, and can therefore oscillate at frequencies outside the voiceband should there be excessive stray capacitance or other unintended feedback loops. A solid ground plane is strongly recommended to minimize coupling of any digital noise into the analog section. Use of wire wrapped boards should definitely be avoided.

Since many applications of the MC33110 compander involve voice transmission over RF links, care must be taken in the design of the product to keep RF signals out of the MC33110 and associated circuitry. This involves proper layout of the PC boards, the physical arrangement of the boards, shielding, proper RF ground, etc.

GLOSSARY

ATTACK TIME — The settling time for a circuit after its input signal has been increased.

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BANDWIDTH — The range of information carrying frequencies of a communication system.

CHANNEL SEPARATION — The ability of one circuit to reject outputting signals which are being processed by another circuit. Also referred to as crosstalk, it is usually expressed in dB.

COMPANDER — A contraction of the words compressor and expander. A compander is composed of two circuits, one of each kind.

COMPRESSOR — A circuit which compresses or reduces the dynamic range of a signal by attenuating strong signals and amplifying low level signals.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P_1/P_2) for power measurements, and

20 x log (V_1/V_2) for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω or 0.775 V rms, is typically defined as 0 dBm for telecom applications. Any voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = – 90 dBm.

dBrnC — Indicates a dBrn measurement using a C–message weighting filter.

DECAY TIME — The settling time for a circuit after its input signal has been decreased.

EXPANDER — A circuit which expands or increases the dynamic range of a signal by amplifying strong signals and attenuating low level signals.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number and a decrease is a negative number.

POWER SUPPLY REJECTION RATIO — The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

SIGNAL–TO–NOISE RATIO — The ratio of the desired signal to unwanted signals (noise) within a defined frequency range. The larger the number, the better.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically, it is 300 to 3400 Hz.

MOTOROLA

Advance Information

Low Voltage Compander

The MC33111 contains two variable gain circuits configured for compressing and expanding the dynamic range of an audio signal. One circuit is configured as an expander, and the other is configured as a compressor. Each circuit has a full wave rectifier to provide average value information to a variable gain cell located in either the input stage or the feedback path. An internal temperature stable bandgap reference provides the necessary precision voltages.

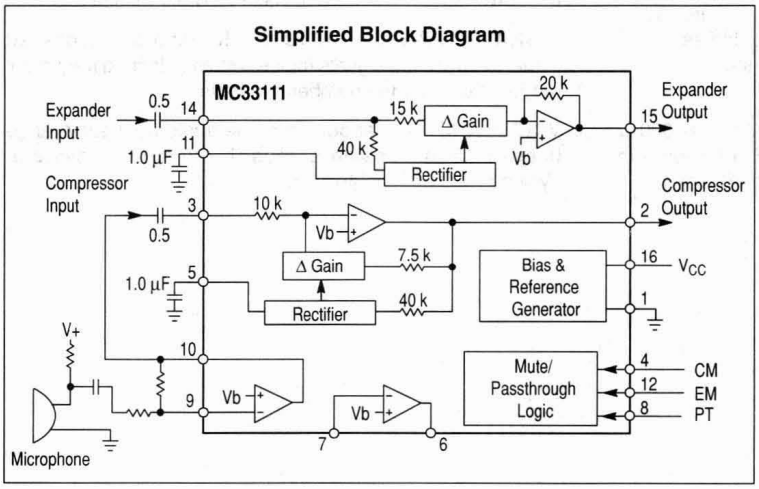
Included in the MC33111 are controls for muting each section independently, and for passthrough of both. Two uncommitted op amps are available for peripheral functions.

The MC33111 will operate from a supply voltage of 3.0 V to 7.0 V, and over a temperature range of – 40° to + 85°C. It is designed to accommodate a 60 dB dynamic range; from – 40 dB to + 20 dB referenced to 100 mVrms.

Applications include cordless telephone, CBs, walkie-talkies, and most voice RF links, and any application where an improvement in the signal to noise ratio is desired. Other applications include speakerphones and voice activated intercoms, dictating machines, etc.

- Operating Supply Voltage: 3.0 V to 7.0 V
- Output Voltage Swing = 2.8 V_{p-p} with V_{CC} = 3.0 V
- No Precision External Components Required
- 60 dB Dynamic Range Compressed to 30 dB, Re-expandable to 60 dB
- Unity Gain Level set at 100 mVrms
- Attack and Decay Times Adjustable
- Mute and Passthrough Controls
- Two Uncommitted Op Amps
- Temperature Compensated Reference
- Available in Standard DIP and Surface Mount Packages

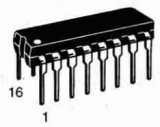
Simplified Block Diagram



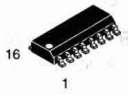
MC33111

LOW VOLTAGE COMPANDER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

TRUTH TABLE

CM	EM	PT	Function
0	0	0	Normal
1	X	X	Comp. Mute
X	1	X	Expander Mute
0	0	1	Passthrough

ORDERING INFORMATION

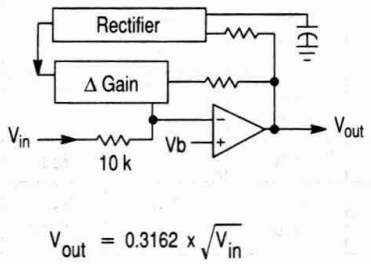
Device	Temperature Range	Package
MC33111D	– 40° to + 85°C	SO-16
MC33111P		Plastic DIP

PIN FUNCTION DESCRIPTION

Name	Pin	Description
Ground	1	Connect to a clean power supply ground.
Compressor Output	2	Output of the compressor section.
Compressor Input	3	Compressor input. The input impedance is nominally 10 kΩ. Nominal signal range is 1.0 mVrms to 1.0 Vrms in normal mode, and up to 0.8 Vrms in passthrough mode. Must be capacitor coupled to the signal source.
Compressor Mute	4	A logic high mutes the compressor. A logic low permits normal operation and passthrough.
Compressor Filter	5	Connect an external capacitor to filter the full wave rectifier's output. This capacitor affects attack and decay times, and low frequency accuracy.
Amplifier #1	6, 7	Inverting input (7) and output (6) of an op amp internally referenced to Vb.
Passthrough	8	A logic high sets the gain of both expander and compressor to ≈ 0 dB, independent of input level.
Amplifier #2	9, 10	Inverting input (9) and output (10) of an op amp internally referenced to Vb.
Expander Filter	11	Connect an external capacitor to filter the full wave rectifier's output. This capacitor affects attack and decay times, and low frequency accuracy.
Expander Mute	12	A logic high mutes the expander. A logic low permits normal operation and passthrough.
No Connect	13	This pin is not internally connected to anything.
Expander Input	14	Expander input. The input impedance is nominally 10.9 kΩ. Nominal signal range is 10 mVrms to 316 mVrms in normal mode, and up to 1.0 Vrms in passthrough mode. Must be capacitor coupled to the signal source.
Expander Output	15	Output of the expander section.
V_{CC}	16	Power supply. Connect to a power supply voltage in the range of 3.0 V to 7.0 V. Bypass capacitor should be provided at this pin.

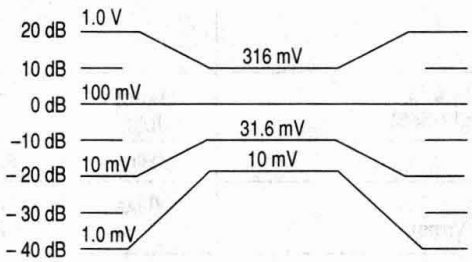
TRANSFER FUNCTIONS

Compressor



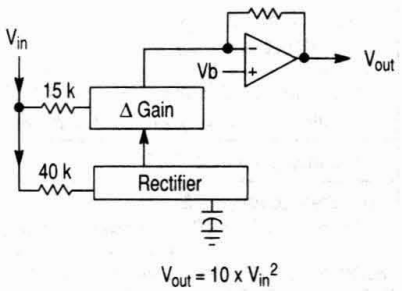
$V_{out} = 0.3162 \times \sqrt{V_{in}}$

Compression **Expansion**



(Voltages are rms)

Expander



$V_{out} = 10 \times V_{in}^2$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Supply Voltage (Pin 16 – Pin 1)	V_{CC}	−0.5, +12	Vdc
High Input Voltage (Pins 3, 4, 8, 12, 14)	V_{IH}	V_{CC} + 0.5	Vdc
Low Input Voltage (Pins 3, 4, 8, 12, 14)	V_{IL}	− 0.5	Vdc
Output Source Current (Pins 2, 6, 10, 15)	IO+	Self-limiting	mA
Output Sink Current (Pins 2, 6, 10, 15)	IO–	Self-limiting	mA
Storage Temperature	T_{stg}	− 65, +150	°C

NOTE: Devices should not be operated at these limits. The "Recommended Operating Conditions" provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage	V_{CC}	3.0	—	7.0	Vdc
Input Signal Voltage Range (3.0 V < V_{CC} < 7.0 V)	V_{in}				
Compressor		0	—	1.3	Vrms
— Normal and Mute Mode					
— Passthrough Mode		0	—	0.8	
Expander		0	—	0.32	
— Normal Mode					
— Mute Mode		0	—	1.3	
— Passthrough Mode		0	—	1.0	
Frequency Range (± 1.0 dB accuracy)	Fin	0.300	—	10	kHz
Logic Input Voltage Range (Pins 4, 8, 12)	V_{in}	0	—	V_{CC}	Vdc
Operating Ambient Temperature	T_A	– 40	—	+ 85	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, f = 1.0 kHz, T_A = + 25°C, unless noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPRESSOR (Pin 4 = Low unless noted)					
0 dB Gain (V_{in} = 100 mVrms)	G_{OC}	–1.5	0	1.5	dB
Gain tracking relative to G_{OC}	G_{TC}				dB
V_{in} = 1.0 Vrms		9.0	10	11	
V_{in} = 1.0 mVrms		– 21	– 20	–19	
Passthrough Gain (Pin 8 = High, Pin 4 = Low, V_{in} = 1.0 Vrms)	G_{PTC}	– 2.0	0	1.0	dB
Muting (Δ Gain) with Pin 4 = High (V_{in} = 1.0 Vrms)	G_{MTC}	55	67	—	dB
Max. Output Swing @ Pin 2 (3.0 V < V_{CC} < 7.0 V)	V_{out}				V_{p-p}
Normal Mode		—	1.1	—	
Passthrough Mode		—	2.3	—	
Peak Output Current (3.0 ≤ V_{CC} ≤ 7.0 V, Normal or Passthrough Modes, V_{in} = Max)	I_{PK}	—	± 4.0	—	mA
Total Harmonic Distortion (V_{in} = 100 mVrms)	THD	—	0.2	1.0	%
Power Supply Rejection @ 1.0 KHz	PSRR				dB
V_{in} (Pin 3) = 0		—	37	—	
V_{in} (Pin 3) = 10 mVrms		—	64	—	
V_{in} (Pin 3) = 1.0 Vrms		—	72	—	
Attack Time (Capacitor @ Pin 5 = 1.0 µF, per EIA-553)	$t_{AT(C)}$	—	3.0	—	ms
Decay Time (Capacitor @ Pin 5 = 1.0 µF, per EIA-553)	$t_{D(C)}$	—	14	—	
Input Impedance at Pin 3	Rin	8.0	10	14	kΩ
DC Bias Level (Pin 2)	Vb_{IAS}	1.4	Vb	1.6	Vdc
Output DC Shift (V_{in} Changed from 0 to 100 mVrms)		– 20	1.6	2.0	mVdc
EXPANDER (Pin 12 = Low, unless noted)					
0 dB Gain (V_{in} = 100 mVrms)	G_{OE}	–1.5	0	1.5	dB
Gain Tracking Relative to G_{OE}	G_{TE}				dB
V_{in} = 316 mVrms		19	20	21	
V_{in} = 10 mVrms		– 41	– 40	– 39	
Passthrough Gain (Pin 8 = High, Pin 12 = Low, V_{in} = 1.0 Vrms)	G_{PTE}	–1.0	0	2.0	dB
Muting (Δ Gain) with Pin 12 = High (V_{in} = 0.316 Vrms)	G_{MTE}	60	76	—	dB
Max. Output Swing @ Pin 15 (3.0 V < V_{CC} , 7.0 V)	V_{out}				V_{p-p}
Normal Mode		—	2.8	—	
Passthrough Mode		—	2.8	—	
Peak Output Current	I_{PK}				mA
V_{CC} = 3.0 V, V_{out} ≤ 2.4 V_{p-p}		—	± 3.5	—	
V_{CC} = 3.0 V, V_{out} = 2.7 V_{p-p}		—	±1.0	—	
V_{CC} ≥ 3.6 V, V_{out} ≤ 2.8 V_{p-p}		—	± 4.0	—	
Total Harmonic Distortion (V_{in} = 100 mVrms)	THD	—	0.2	1.0	%

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, f = 1.0 kHz, T_A = + 25°C, unless noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
EXPANDER (Pin 12 = Low, unless noted)					
Power Supply Rejection @ 1.0 kHz	PSRR				dB
V_{in} (Pin 14) = 0		—	74	—	
V_{in} (Pin 14) = 10 mVrms		—	76	—	
V_{in} (Pin 14) = 316 mVrms		—	62	—	
Attack Time (Capacitor @ Pin 11 = 1.0 µF, per EIA-553)	$t_{AT(E)}$	—	3.0	—	ms
Decay Time (Capacitor @ Pin 11 = 1.0 µF, per EIA-553)	$t_{D(E)}$	—	14	—	
Input Impedance at Pin 14	R_{in}	8.0	10.9	14	kΩ
DC Bias Level (Pin 15)	Vb_{IAS}	1.4	Vb	1.6	Vdc
Output DC Shift (V_{in} changed from 0 to 100 mVrms)		– 20	1.0	20	mVdc
LOGIC INPUTS (Pins 4, 8, 12)					
Switching Threshold (3.0 < V_{CC} < 7.0 V)	V_{ST}	—	1.3	—	Vdc
Input Current	Rin				µA
@ V_{in} = 0 V		—	0	—	
@ V_{in} = 3.6 V		—	55	—	
Timing (V_{in} @ Pins 3 and 14 = 300 mVrms, See Figures 1, 2)					µs
Comp. Mute (Pin 4) to Comp. Output — Low-to-High	t_{CMLH}	—	2.0	—	
High-to-Low	t_{CMHL}	—	3.0	—	
Exp. Mute (Pin 12) to Exp. Output — Low-to-High	t_{EMLH}	—	2.0	—	
High-to-Low	t_{EMHL}	—	3.0	—	
Passthrough (Pin 8) to Comp. Output — Low-to-High	t_{PCLH}	—	2.0	—	
High-to-Low	t_{PCHL}	—	5.0	—	
Passthrough (Pin 8) to Exp. Output — Low-to-High	t_{PELH}	—	6.0	—	
High-to-Low	t_{PEHL}	—	7.0	—	
OP AMPS (Pins 6, 7, 9, 10)					
Open Loop Gain	A_{VOL}	—	100	—	dB
Gain Bandwidth	BW	—	300	—	kHz
Input Bias Current @ Pins 7, 9	I_{IB}	—	8.0	—	nA
Max Output Swing @ Pins 6, 10 (3.0 V < V_{CC} < 7.0 V)	V_{out}	—	2.8	—	V_{p-p}
Peak Output Current	I_{PK}				mA
V_{CC} = 3.0 V, $V_{out} \leq$ 2.4 V_{p-p}		—	± 3.0	—	
V_{CC} = 3.0 V, V_{out} = 2.6 V_{p-p}		—	± 2.0	—	
$V_{CC} \geq$ 3.6 V, $V_{out} \leq$ 2.8 V_{p-p}		—	± 3.7	—	
Total Harmonic Distortion (V_{out} = 1.0 Vrms, Unity Gain)	THD	—	0.02	0.2	%
MISCELLANEOUS					
Power Supply Current	I_{CC}				mA
@ V_{CC} = 3.6 V		—	1.5	2.0	
@ V_{CC} = 7.0 V		—	1.7	—	
Reference Voltage	Vb	—	1.5	—	Vdc
Channel Separation	CS				dB
Expander to Compressor					
(Pin 14 = 316 mVrms @ 1.0 kHz and Pin 3 = 0 mVrms)		40	70	—	
(Pin 14 = 100 mVrms (300 Hz < f < 20 kHz), Pin 3 = 100 mVrms @ 1.2 kHz)		—	96	—	
Compressor to Expander					
(Pin 3 = 1.0 Vrms @ 1.0 kHz and Pin 14 = 0 mVrms)		60	100	—	
(Pin 3 = 100 mVrms (300 Hz < f < 20 kHz), Pin 14 = 100 mVrms @ 1.2 kHz)		—	97	—	

TEMPERATURE PERFORMANCE (Typical performance based on device characterization, not guaranteed.)

Characteristic	– 40°C	+25°C	+ 85°C
Power Supply Current @ V_{CC} = 3.6 V @ V_{CC} = 7.0 V	 1.2 mA 1.4 mA	 1.5 mA 1.7 mA	 1.6 mA 1.9 mA
Reference Voltage (Vb)	1.495 V	1.5 V	1.505 V
0 dB Gain (V_{in} = 100 mVrms) — Compressor	0.08 dB	0 dB	– 0.04 dB
0 dB Gain (V_{in} = 100 mVrms) — Expander	0.04 dB	0 dB	– 0.03 dB
Total Harmonic Distortion (V_{in} = 100 mVrms) — Compressor	0.3%	0.2%	0.2%
Total Harmonic Distortion (V_{in} = 100 mVrms) — Expander	0.3%	0.2%	0.16%
Gain Tracking Relative to 0 dB Gain — Compressor V_{in} = 1.0 Vrms V_{in} = 1.0 mVrms	 10.8 dB –19.95 dB	 10 dB – 20 dB	 10 dB – 20.1 dB
Gain Tracking Relative to 0 dB Gain — Expander V_{in} = 316 mVrms V_{in} = 10 mVrms	 18.6 dB – 40.2 dB	 20 dB – 40 dB	 19.95 dB – 39.9 dB
Muting (Δ Gain) with Pin 4 = High (V_{in} = 1.0 Vrms) — Compressor	68 dB	67 dB	66 dB
Muting (Δ Gain) with Pin 12 = High (V_{in} = 0.316 Vrms) — Expander	76 dB	76 dB	75 dB

Figure 1. Mute Timing

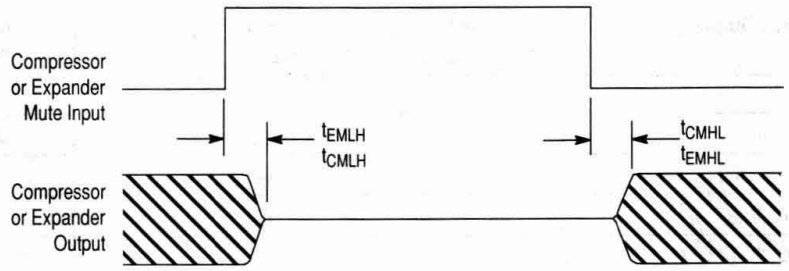


Figure 2. Passthrough Timing

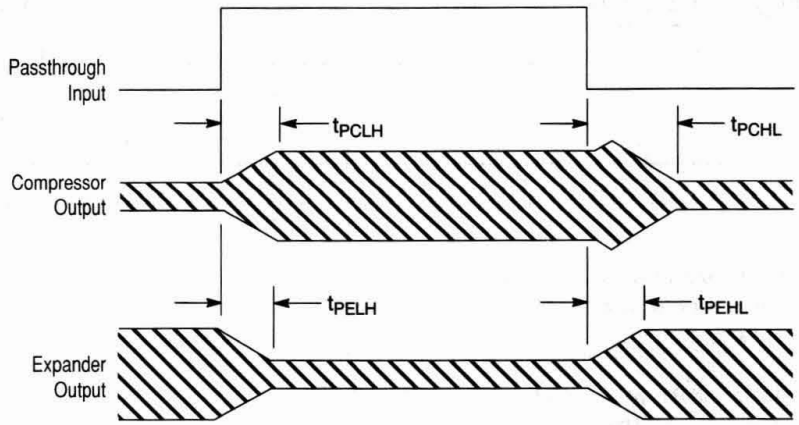


Figure 3. Transfer Characteristics

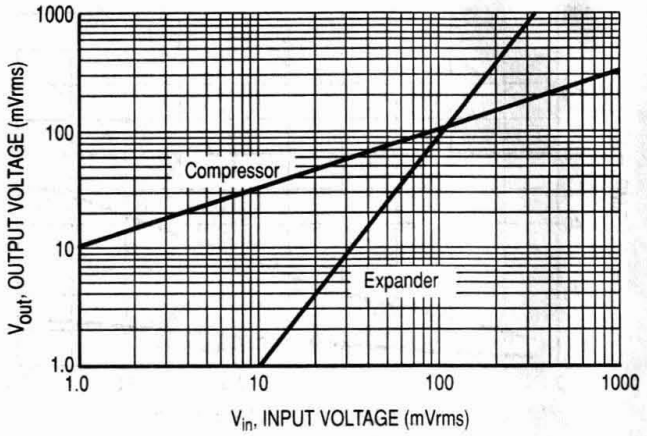


Figure 4. Transfer Characteristics

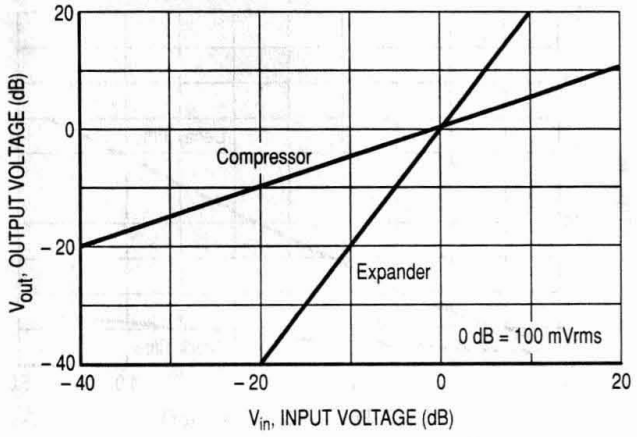


Figure 5. Frequency Response (Compressor)

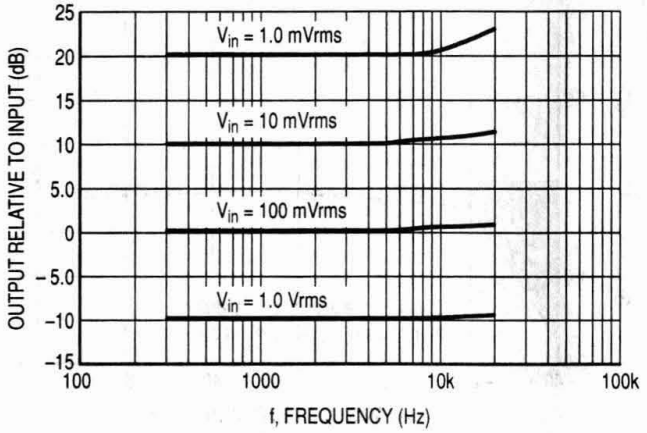


Figure 6. Frequency Response (Expander)

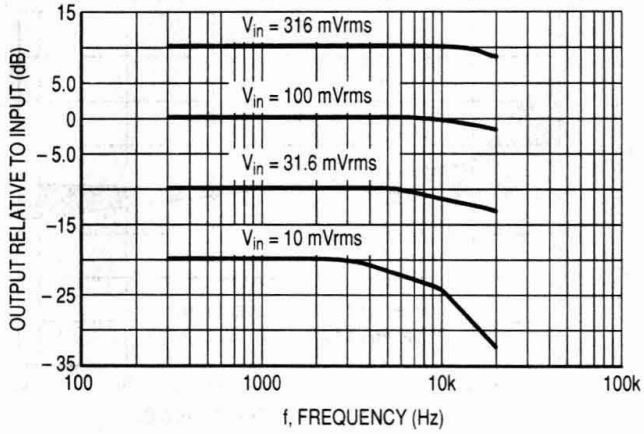
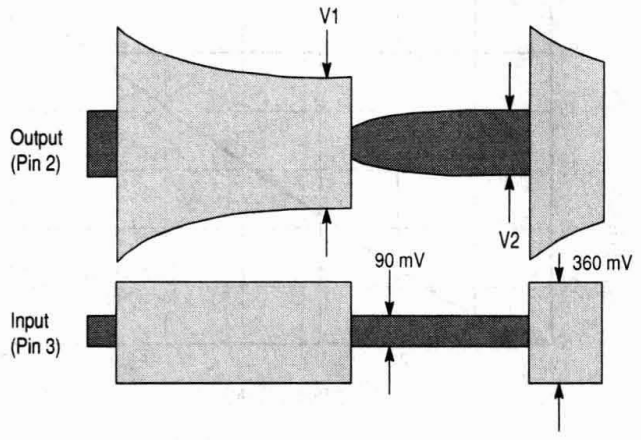
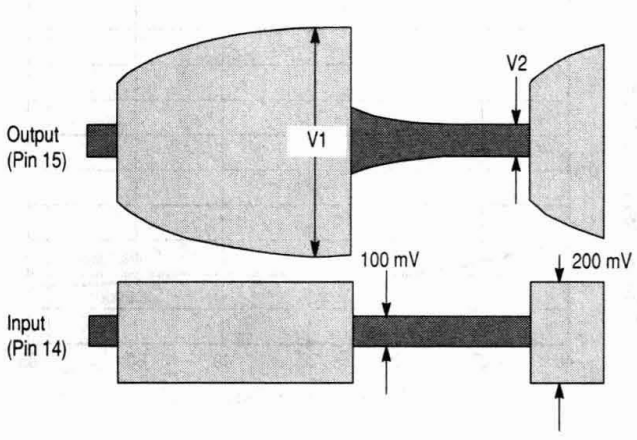


Figure 7. Attack and Decay Times (Compressor)



Attack Time = Time to 1.5 x V1 from input increase.
Decay Time = Time to 0.75 x V2 from input decrease.
Test per EIA-553.

Figure 8. Attack and Decay Times (Expander)



Attack Time = Time to 0.57 x V1 from input increase.
Decay Time = Time to 1.5 x V2 from input decrease.
Test per EIA-553.

Figure 9. Attack and Decay Times (Compressor)

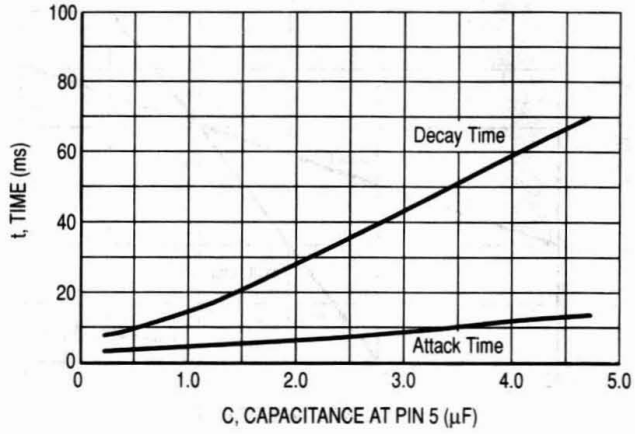


Figure 10. Attack and Decay Times (Expander)

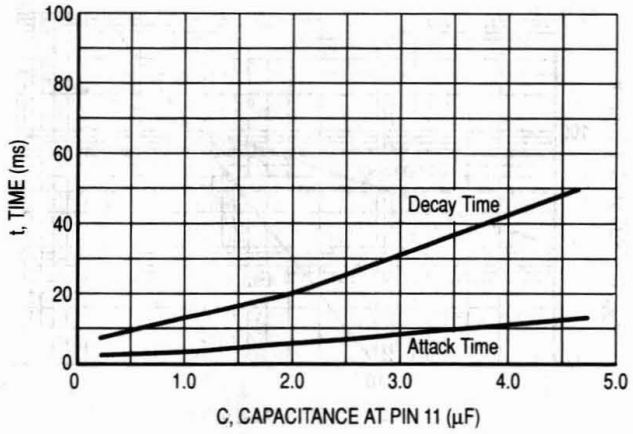


Figure 11. Compressor Gain Tracking versus Temperature

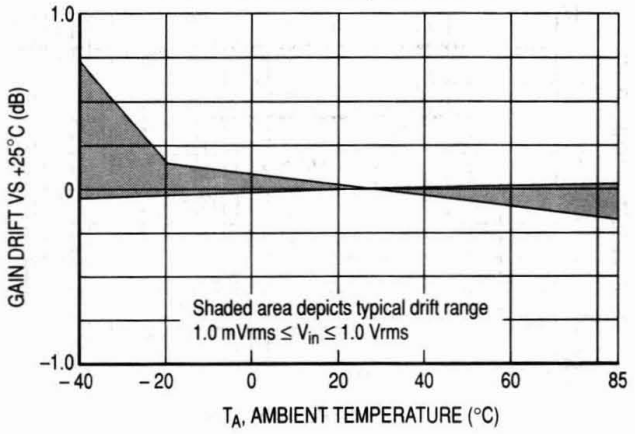


Figure 12. Expander Gain Tracking versus Temperature

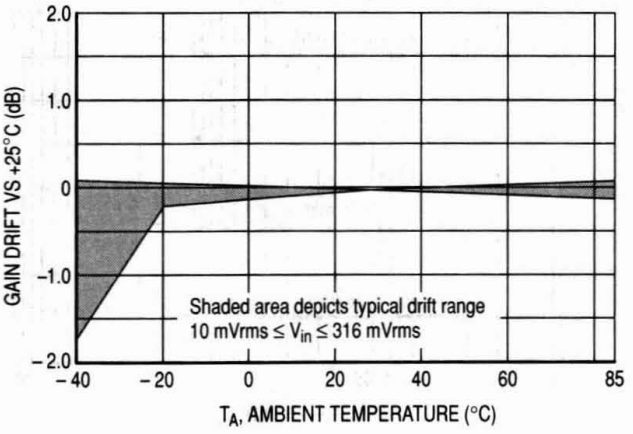


Figure 13. THD versus Temperature

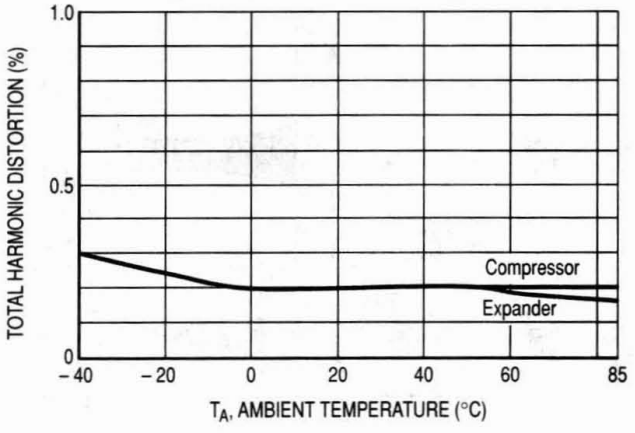
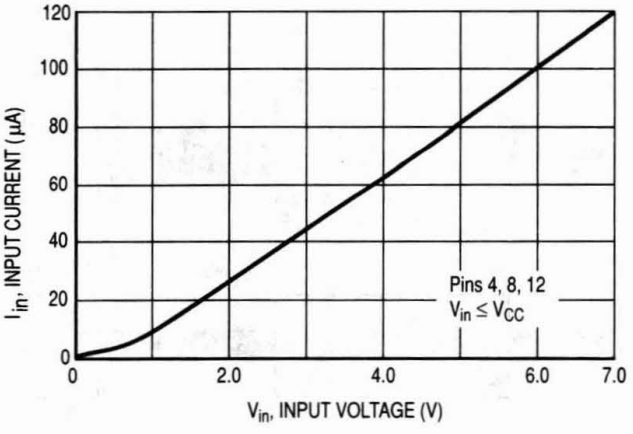


Figure 14. Logic Inputs' Current



FUNCTIONAL DESCRIPTION

Introduction

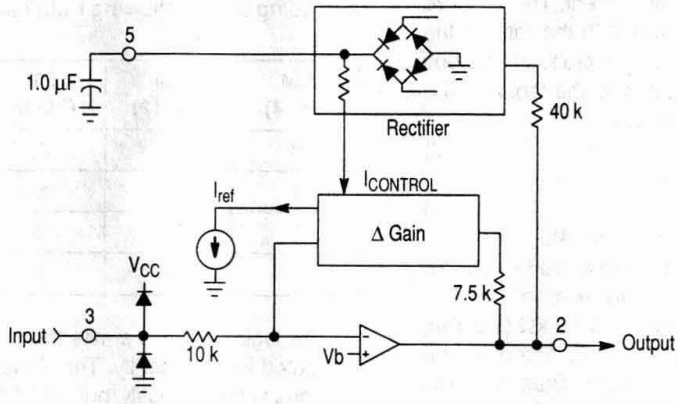
The MC33111 compander (COMpressor and exPANDER) is composed of two variable gain circuits which provide compression and expansion of a signal's dynamic range. The compressor will take a signal with a 60 dB dynamic range (1.0 mV to 1.0 Vrms), and reduce that to a 30 dB dynamic range (10 mV to 316 mV) by attenuating strong signals, while amplifying low level signals. The expander does the opposite in that the 30 dB signal range is increased to a dynamic range of 60 dB by amplifying strong signals and attenuating low level signals. The 0 dB level is internally set at 100 mVrms — that is the signal level which is neither amplified nor attenuated. Both circuits contain the necessary precision full wave rectifier, variable gain cell, and temperature compensated references required for accurate and stable performance.

Both the compressor and expander can be muted independently by the use of Pins 4 and 12, respectively. A minimum of 55 dB of muting is guaranteed for the compressor, and 60 dB for the expander. A passthrough function (Pin 8) is provided which sets both sections to unity gain, regardless of input level.

Two uncommitted op amps are provided which can be used for perpherial functions. Each is internally biased at Vb (≈ +1.5 V), and has a bandwidth of ≈ 300 kHz.

NOTE: All dB values mentioned in this data sheet, unless otherwise noted, are referenced to 100 mVrms.

Figure 15. Compressor



Compressor

The compressor is a noninverting amplifier with a fixed input resistor and a variable gain cell in its feedback path as shown in Figure 15.

The amplifier output is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{CONTROL}$), representative of the rectifier's AC signal, to the variable gain cell. The reference current (I_{REF}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{CONTROL}$ increases, thereby providing compression. The output is related to the input by the following equation (V_{in} and V_{out} are rms volts):

$$V_{out} = 0.3162 \times \sqrt{V_{in}} \quad (1)$$

In terms of dB levels, the relationship is:

$$Vo(dB) = 0.5 \times Vi(dB) \quad (2)$$

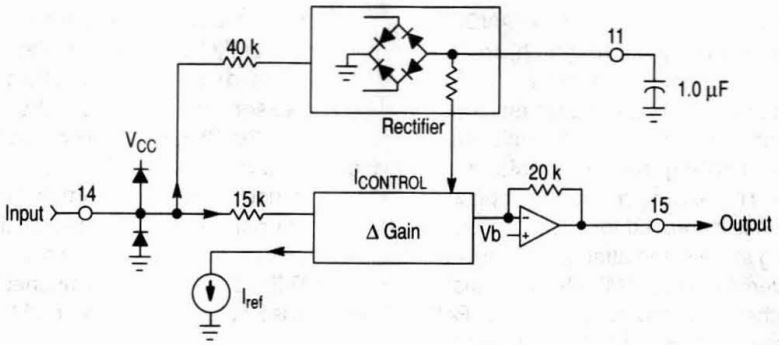
where 0 dB = 100 mVrms (See Figures 3 and 4).

The input and output are internally biased at Vb (≈ +1.5 V), and must therefore be capacitor coupled to external circuitry. Pin 3 input impedance is nominally 10 kΩ (± 20%), and the maximum functional input signal is listed in the Recommended Operating Conditions table. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow, and distortion will show up at the output and possibly in other parts of the circuit.

When AC signals are not present at the input, the variable gain cell will attempt to set a very high gain to comply with Equation 2. An internal clamp limits the maximum gain to ≈ 26 dB to prevent instabilities.

The output of the rectifier is filtered by the capacitor at Pin 5, which, in conjunction with an internal 20 k resistor, provides the time constant for the attack and decay times. The attack and decay times listed in the Electrical Characteristics were determined using the test procedure defined in EIA-553. Figure 9 indicates how the times vary with the capacitor value. If the attack and decay times are decreased using a smaller capacitor, performance at low frequencies will degrade.

Figure 16. Expander



Expander

The expander is an noninverting amplifier with a fixed feedback resistor and a variable gain cell in its input path as shown in Figure 16.

The input signal is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{CONTROL}$), representative of the AC input signal, to the variable gain cell. The reference current (I_{REF}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{CONTROL}$ increases, thereby providing expansion. The output is related to the input by the following equation (V_{in} and V_{out} are rms volts):

$$V_{out} = 10 \times (V_{in})^2 \quad (3)$$

In terms of dB levels, the relationship is:

$$Vo(dB) = 2.0 \times Vi(dB) \quad (4)$$

where 0 dB = 100 mVrms (See Figures 3 and 4).

The input and output are internally biased at Vb (≈ +1.5 V), and must therefore be capacitor coupled to external circuitry. The input impedance at Pin 14 is nominally 10.9 kΩ (± 20%), and the maximum functional input signal is listed in the Recommended Operating Conditions table. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow, and distortion will show up at the output, and possibly in other parts of the circuit.

The output of the rectifier is filtered by the capacitor at Pin 11, which, in conjunction with an internal 20 k resistor, provides the time constant for the attack and decay times. The attack and decay times listed in the Electrical Characteristics were determined using the test procedure defined in EIA-553. Figure 10 indicates how the times vary with the capacitor value. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Op Amps

The two op amps (at Pins 6, 7, 9, and 10) are identical and can be used for peripheral functions, such as a microphone amplifier, buffer, filter, etc. They have an open loop gain of ≈100 dB, and a bandwidth of ≈ 300 kHz. The noninverting inputs are internally biased at Vb (≈ +1.5 V). The inverting inputs (Pins 7, 9) require a bias current of ≈ 8.0 nA, which flows **into** the pin. The outputs can typically supply a maximum of 3.7 mA load current (see Electrical Characteristics).

NOTE: If an op amp is unused, its output MUST be tied to its input (Pin 6 to 7 and/or 9 to 10). Leaving an input open can affect other portions of the IC.

Logic Inputs

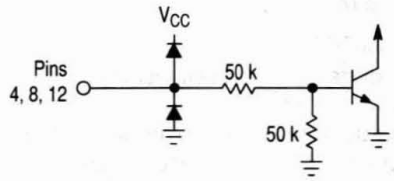
The three inputs (Pins 4, 8, 12) provide for muting and passthrough functions for the compressor and expander according to the following truth table:

CM (Pin 4)	EM (Pin 12)	PT (Pin 8)	Function
0	0	0	Normal Operation
1	X	X	Compressor Mute
X	1	X	Expander Mute
0	0	1	Passthrough

The logic section permits the compressor and expander to be muted independently. The Passthrough control affects both sections simultaneously, but only if the Mute inputs are at a logic level 0. If both the Passthrough and a Mute input are asserted, the Mute will override the Passthrough. The logic controls do not affect the two uncommitted op amps in any way.

Figure 17 depicts a typical logic input stage configuration, and Figure 14 indicates the typical input current. The inputs' threshold is ≈ +1.3 V, independent of V_{CC}. An open input is equivalent to a logic low, but good design practices dictate that inputs should never be left open. The inputs must be kept within the range of V_{CC} and GND. If an input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted.

Figure 17. Logic Input Stage



Power Supply

The MC33111 requires a supply voltage between 3.0 V and 7.0 V, and a nominal current of ≈ 1.6 mA. The supply voltage should be well filtered and free of ripple. A minimum of 4.7 μF in parallel with a 0.01 μF capacitor is recommended for filtering and RF bypass.

Vb is an internally generated reference set at ≈ +1.5 V, and is used internally as an AC ground. It is not available directly at any pins, but can be obtained as a buffered reference from either op amp by connecting the op amp as a follower.

APPLICATION INFORMATION

Typical Application Circuit

Figure 18 indicates a typical implementation of the MC33111 compander. The following points apply:

a) The values shown adjacent to some components are based on the expected use of the IC:
   — The input capacitors (Pins 3 and 14) provide a 3.0 dB rolloff of ≈ 30 Hz, a decade below the nominal voiceband.
   — The rectifier capacitors provide attack and decay times as indicated in the Electrical Tables.

b) The values for the unlabeled components are application dependent:
   — The components around the op amps depend on their use.
   — The value of the capacitors at the compressor and expander outputs depend on the circuit to which they are connected.

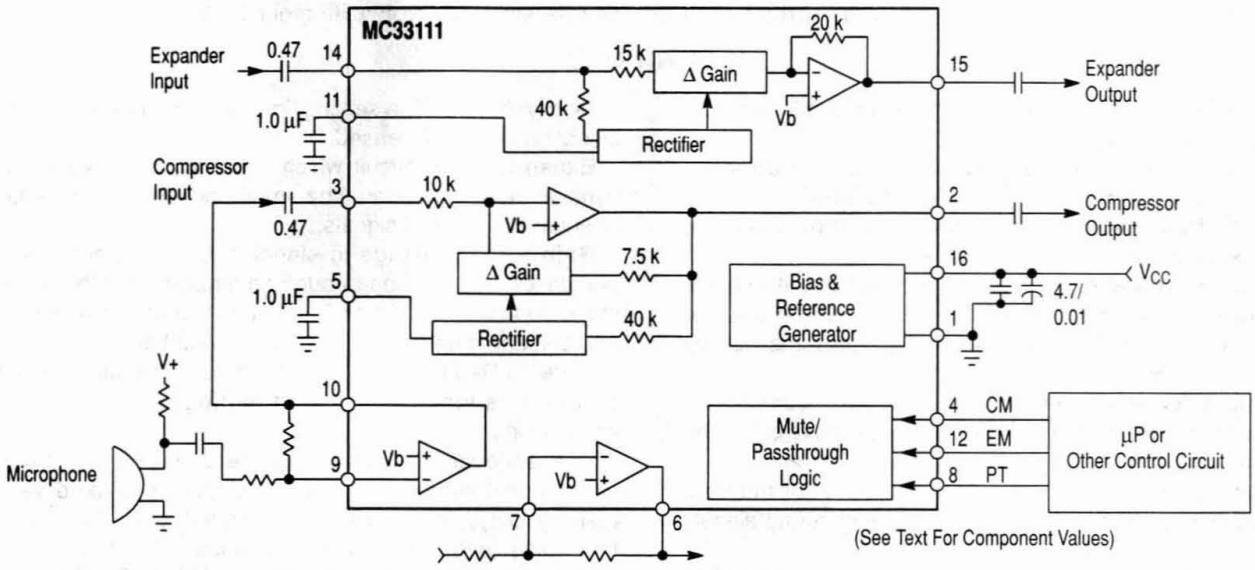
c) If either the compressor or expander is not used, its input **must** not be left open. It can be connected to ground either through a capacitor, or directly to ground.

d) The two op amps can be used for any purpose which suits the application. The indicated use of the one op amp as a microphone amplifier is only an example.

e) If an op amp is not used, its output and input **must** be connected together. Do not leave Pin 7 or Pin 9 open.

f) The logic inputs (Pins 4, 8, 12) are TTL/CMOS compatible. The logic high voltage must not exceed the V_{CC} voltage on the MC33111. Any unused input should be connected to ground and not left open.

Figure 18. Typical Application



Signal-To-Noise Improvement

Among the basic reasons for the original development of compander type circuits was to improve the signal-to-noise ratio of long distance communications circuits, and of voice circuits which are transmitted over RF links (CBs, walkie-talkies, cordless phones, etc.). Since much of the interfering noise heard at the receiving end of a transmission is due to noise picked up, for example, in the airway portion of the RF link, the compressor was developed to increase the low-level signals at the transmitting end. Then any noise picked up in the RF link would be a smaller percentage of the transmitted signal level. At the receiving end, the signal is then expanded back to is original level, retaining the same high signal-to-noise ratio. While the above explanation indicates it is not necessary to attenuate strong signals (at the transmitting end), a benefit of doing this is the reduced dynamic range which must be handled by the system transmitter and receiver. The MC33111 was designed for a two-to-one compression and expansion, i.e. a 60 dB dynamic signal is compressed to a 30 dB dynamic range, transmitted to the receiving end, and then expanded back to a 60 dB dynamic range.

The MC33111 compander is not limited to RF or long distance telephony applications. It can be used in any system requiring either an improved signal-to-noise ratio, or a reduced dynamic range. Such applications include telephones, speakerphones, tape recorders, wireless microphones, digital recording, and many others.

Power Supplies, Grounding

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC} or ground, can cause a distorted output, or incorrect gain levels.

V_{CC} must be decoupled to the appropriate ground **at the IC** (within 1″ max.) with a 4.7 μF capacitor and a 0.01 μF ceramic. A tantalum capacitor is recommended for the larger value if very high frequency noise is present, since electrolytic capacitors simply have too much inductance at those frequencies. The quality of the power supply voltage should be checked at the IC with a high frequency scope. Noise spikes (always present if digital circuits are near this IC) can easily exceed 400 mV, and if they get into the IC, the output can have noise or distortion. Noise can be reduced by inserting resistors and/or inductors between the supply and the IC.

If switching power supplies are used, there will be spikes of 0.5 V or greater at frequencies of 50 kHz – 1.0 MHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, a 3-terminal regulator (e.g., MC78L05ACP), with appropriate high frequency filtering, should be used and dedicated to the analog portion of the circuit.

The ripple content of the supply should not allow its magnitude to exceed the values in the Recommended Operating Conditions table.

The PC board tracks supplying V_{CC} and ground to the MC33111 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The analog circuitry containing the MC33111 should be close to the power supply, or the connector where the supply voltages enter the board. If V_{CC} is supplying considerable current to other parts of the board, then it is preferable to have dedicated lines directly to the MC33111 and associated circuitry.

PC Board Layout

Although this device is intended for use in the audio frequency range, the various amplifiers have a bandwidth of ≈ 300 kHz, and can therefore oscillate at frequencies outside the voiceband should there be excessive stray capacitance or other unintended feedback loops. A solid ground plane is strongly recommended to minimize coupling of any digital noise into the analog section. Use of wire wrapped boards should definitely be avoided.

Since many applications of the MC33111 compander involve voice transmission over RF links, care must be taken in the design of the product to keep RF signals out of the MC33111 and associated circuitry. This involves proper layout of the PC boards and the physical arrangement of the boards, shielding, proper RF ground, etc.

DEFINITIONS

Attack Time — The settling time for a circuit after its input signal has been increased.

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

Channel Separation — The ability of one circuit to reject outputting signals which are being processed by another circuit. Also referred to as crosstalk rejection, it is usually expressed in dB.

Compander — A contraction of the words compressor and expander. A compander is composed of two circuits, one of each kind.

Compressor — A circuit which compresses, or reduces, the dynamic range of a signal by attenuating strong signals and amplifying low level signals.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$10 \times \log (P_1/P_2)$ for power signals, and

$20 \times \log (V_1/V_2)$ for voltage signals.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is typically defined as 0 dBm for telecom applications. Any voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBm = – 90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

Decay Time — The settling time for a circuit after its input signal has been decreased.

Expander — A circuit which expands, or increases the dynamic range of a signal by amplifying strong signals and attenuating low level signals.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Mute — Reducing the level of an audio signal, generally so that it is inaudible. Partial muting is used in some applications.

Passthrough — Bypassing the compression and/or expansion function by setting the gain to a fixed value (usually unity). This is usually employed when data, rather than voice, is to be transmitted without attenuation.

Power Supply Rejection Ratio — The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

Signal to Noise Ratio — The ratio of the desired signal to unwanted signals (noise) within a defined frequency range. The larger the number, the better.

Voiceband — That portion of the audio frequency range used for transmission in the telephone system. Typically it is 300-3400 Hz.

Zero dB Point — The signal level which has its amplitude unchanged by a compressor or expander.

MOTOROLA

MC33128

Power Management Controller

The MC33128 is a power management controller specifically designed for use in battery powered cellular telephone and pager applications. This device contains all of the active functions required to interface the user to the system electronics via a microprocessor. This integrated circuit consists of a low dropout voltage regulator with power–up reset for MPU power, two low dropout voltage regulators for independant powering of analog and digital circuitry, and a negative charge pump voltage regulator for full depletion of gallium arsenide MESFETs.

Also included are protective system shutdown features consisting of a battery latch that is activated upon battery insertion, low battery voltage shutdown, and a thermal over temperature detector. This device is available in a 16–pin narrow body surface mount plastic package.

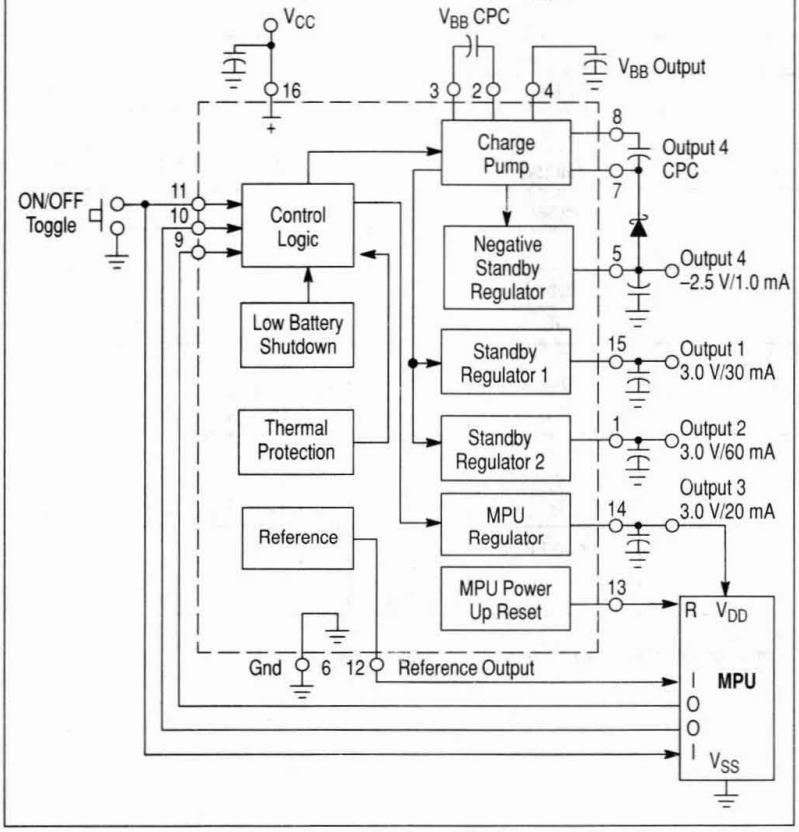
- Three Positive Regulated Outputs Featuring Low Dropout Voltage
- Negative Regulated Output for Full Depletion of GaAs MESFETs
- MPU Power Up Reset
- Battery Latch
- Low Battery Shutdown
- Pinned–Out Reference for MPU A/D Converter
- Low Start–Up and Operating Current
- Thermal Protection

POWER MANAGEMENT CONTROLLER

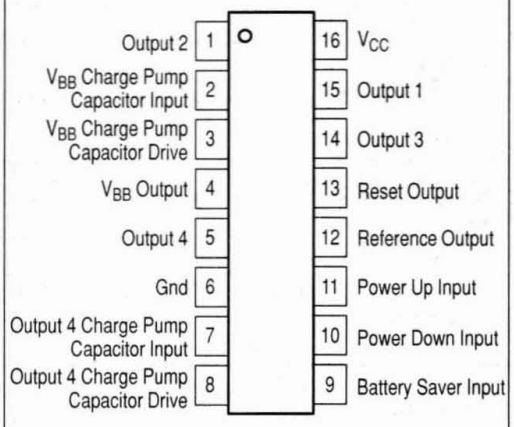
SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33128D	T_A = – 30° to +60°C	SO–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage (Pin 16)	V_{CC}	+7.0	V
Input Voltage Range Power Up, Power Down, and Battery Saver Inputs (Pins 11, 10, 9)	V_{in}	−1.0 to V_{CC} + 1.0	V
Charge Pump Capacitor Drive Outputs, Source or Sink Current (Pins 3, 8)	$I_{O(max)}$	30	mA
Schottky Diode Forward Current (Pins 16 to 2, 2 to 4, and 7 to 6)	$I_{F(max)}$	30	mA
Output Source Current (Note 1) Regulator Output 1 (Pin 15) Regulator Output 2 (Pin 1) Regulator Output 3 (Pin 14) Regulator Output 4 (Pin 5) Reference (Pin 12)	I_{Source}	 150 250 50 10 40	mA
Reset Sink Current (Pin 13)	I_{Sink}	5.0	mA
Power Dissipation and Thermal Characteristic D Suffix, Plastic Package Case 751B Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\varnothing JA}$	 560 180	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 1)	T_A	−30 to +60	°C
Storage Temperature	T_{stg}	−60 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER UP INPUT (Pin 11)					
Low State Input Threshold Voltage	$V_{th(toggle)}$	V_{CC} – 1.5	V_{CC} – 1.2	V_{CC} – 0.8	V
Input Current (V_{in} = V_{O3})	$I_{in(toggle)}$	–	–	120	µA
Internal Pull Up Resistance	$R_{PU(ON/OFF)}$	10	20	30	kΩ
POWER DOWN INPUT (Pin 10)					
High State Input Threshold Voltage (Places IC in Standby Mode)	$V_{th(PDI)}$	1.3	1.5	1.8	V
Input Current (V_{in} = V_{O3})	$I_{in(PDI)}$	–	–	120	µA
BATTERY SAVER INPUT (Pin 9)					
High State Input Threshold Voltage (V_{BB}, V_{O1}, V_{O2}, V_{O4} Activated)	$V_{th(BSI)}$	1.2	1.4	1.7	V
Input Current (V_{in} = V_{O3})	$I_{in(BSI)}$	–	–	120	µA
V_{BB} GENERATOR					
Oscillator Frequency	f_{OSC}	85	95	105	kHz
Oscillator Duty Cycle	DC	35	50	65	%
Charge Pump Capacitor Drive Output Voltage Swing (Pin 3) High State (I_{Source} = 3.0 mA) Low State (I_{Sink} = 3.0 mA)	 V_{OH} V_{OL}	 – –	 V_{CC} – 0.9 0.15	 – –	V
Schottky Diode (Pins 2, 4) Forward Voltage Drop (I_F = 3.0 mA) Reverse Leakage Current (V_{BB} = 7.0 V)	 V_F I_L	 – –	 0.5 0.01	 – –	 V µA
Output Voltage (Pin 4) V_{CC} = 4.5 V V_{CC} = 2.9 V	$V_{O(VBB)}$	 – –	 7.9 4.4	 – –	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT 1 (Pin 15)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O1} = 30 mA)	Reg_{line1}	2.9	3.0	3.1	V
Load Regulation (I_{O1} = 0 mA to 35 mA)	Reg_{load1}	–	5.0	30	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O1} = 30 mA)	$V_{in} - V_{O1}$	–	–	0.1	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 1	 – –	 70 40	 – –	dB
Turn ON Delay Time (Battery Saver Input to 90% V_{O1} Output)	t_{DLY1}	–	0.2	2.0	ms
REGULATOR OUTPUT 2 (Pin 1)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O2} = 60 mA)	Reg	2.9	3.0	3.1	V
Load Regulation (I_{O2} = 0 mA to 60 mA)	Reg_{load2}	–	5.0	40	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O2} = 60 mA)	$V_{in} - V_{O2}$	–	–	0.11	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 2	 – –	 70 40	 – –	dB
Turn ON Delay Time (Battery Saver Input to 90% V_{O2} Output)	t_{DLY2}	–	0.2	2.0	ms
REGULATOR OUTPUT 3 (Pin 14)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O3} = 20 mA)	Reg_{line3}	2.9	3.0	3.1	V
Load Regulation (I_{O3} = 0 mA to 20 mA)	Reg_{load3}	–	5.0	25	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O3} = 20 mA)	$V_{in} - V_{O3}$	–	–	0.1	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 3	 – –	 70 40	 – –	dB
Turn ON Delay Time (ON/OFF Toggle Input to 90% V_{O3} Output)	t_{DLY3}	–	0.5	3.0	ms
REGULATOR OUTPUT 4 (Pin 5)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O4} = 1.0 mA)	Reg_{line4}	−2.35	−2.5	−2.65	V
Load Regulation (I_{O4} = 0 mA to 1.0 mA)	Reg_{load4}	–	5.0	20	mV
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 4	 – –	 70 40	 – –	dB
Schottky Diode Forward Voltage Drop (Pins 7, 6, I_F = 1.0 mA)	V_F	–	0.5	–	V
Charge Pump Capacitor Drive Output Voltage Swing (Pin 8) High State (I_{Source} = 1.0 mA) Low State (I_{Sink} = 1.0 mA)	 V_{OH} V_{OL}	 – –	 V_{BB} – 0.25 0.15	 – –	V
Turn ON Delay Time (Battery Saver Input to 90% V_{O4} Output)	t_{DLY4}	–	4.0	10	ms
REFERENCE OUTPUT (Pin 12)					
Output Voltage (I_O = 0 mA to 10 mA)	Reg_{load}	1.46	1.5	1.54	V
MPU POWER UP RESET COMPARATOR (Pin 13)					
Threshold Voltage Low State Output (V_{O3} Decreasing) Hysteresis (V_{O3} Increasing)	 $V_{th(low)}$ V_H	 2.5 40	 2.6 60	 2.7 100	 V mV
Output Sink Saturation (I_{Sink} = 100 µA, V_{O3} = 2.5 V to 1.0 V)	$V_{CE(sat)}$	–	130	300	mV
Internal Pull–up Resistance	R_{PU}	10	26	40	kΩ
High State Output Voltage (V_{O3} = 2.8 V)	V_{OH}	0.95 V_{O3}	V_{O3}	–	V

NOTE: 2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOW BATTERY SHUTDOWN COMPARATOR (Pin 16)					
Shutdown Threshold Voltage (V_{CC} Decreasing, Pin 10 = Gnd)	$V_{th(LBSC)}$	2.25	2.4	2.55	V
TOTAL DEVICE (Pin 16)					
Power Supply Current (No Load On All Outputs)	I_{CC}				
Operating					
Battery Saver Input High (Pin 9 = 2.0 V)		–	2.6	4.0	mA
Battery Saver Input Low (Pin 9 ≤ 0.8 V)		–	270	330	µA
Standby (After Power Down Input Strobe)		–	8.0	12	µA

NOTE: 2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

Figure 1. Dropout Voltage versus Source Current

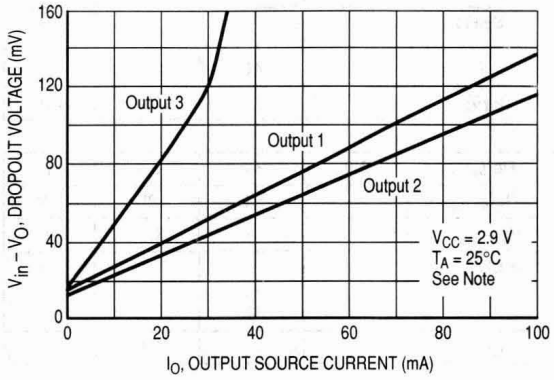


Figure 2. Output 4 Voltage versus Source Current

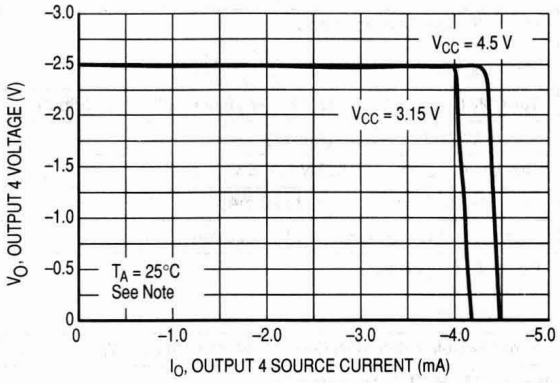


Figure 3. Reference Output Voltage Change versus Source Current

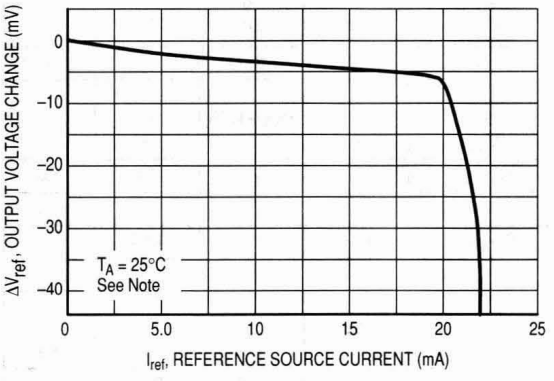
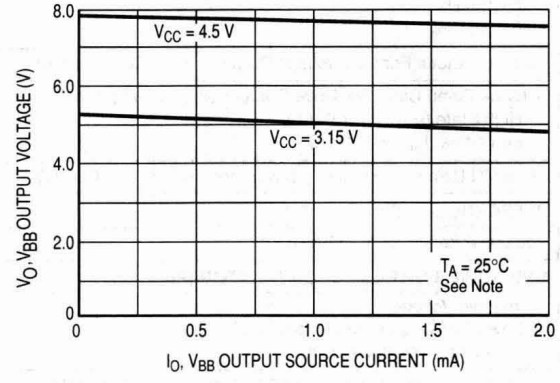


Figure 4. V_{BB} Output Voltage Change versus Source Current



NOTE: All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

OPERATING DESCRIPTION

The MC33128 is a complete power management controller that is designed to interface the user to the system electronics via a microprocessor.

Outputs

Three low dropout voltage regulators are provided at outputs 1, 2 and 3. Outputs 1 and 2 were contemplated for independent powering of the systems analog and digital circuitry. This significantly reduces the possibility of digitally generated noise and spurious signals from coupling into the RF and analog circuits. The low dropout characteristic of Outputs 1 and 2 is achieved by applying a boosted battery voltage, V_{BB}, to their respective driver transistors. This allows the output pass transistors to be driven into saturation when the battery voltage approaches 3.0 V. The V_{BB} Output appears at Pin 4 and can be used to provide gate bias for enhancing external N channel MOSFET switches. Excessive loading of the V_{BB} output will result in an increase in dropout voltage.

Output 4 is derived from a voltage inverting charge pump circuit and is intended to provide the negative gate bias required for full depletion of RF gallium arsenide MESFETs. In personal communication system applications such as cellular telephone, negative gate bias is usually required by the antenna switch and power amplifier circuit blocks with a typical combined current of less than 1.0 mA. Output 4 can supply in excess of 2.0 mA, but there will be an increase in dropout voltage of Outputs 1, 2 and 3.

Outputs 1, 2, 4, V_{BB} Generator and Thermal Protection are all enabled and disabled in unison by the Battery Saver Input, Pin 9. The microprocessor can be programmed to significantly extend the system battery operating time by periodically enabling the receiver circuitry.

Output 3 provides power to the microprocessor, flash EPROM and the system display. These blocks are enabled by the Power Up Input, Pin 11, and disabled by the Power Down Input, Pin 10. By having separate power up and power down inputs, the microprocessor can store any pending information before turning the system and then itself OFF. This allows a controlled or graceful shutdown. Note that the power down request is initiated by pressing the toggle switch while the system is "ON". This action generates a microprocessor non–maskable interrupt that initiates the graceful shutdown.

Battery Voltage Detection

Reverse biasing and eventual failure of the lowest capacity cell in the battery pack can occur if the system is accidentally left on for an extended time period. To prevent this condition the following circuit blocks were incorporated.

A means for low battery detection is accomplished by using the Reference Output, Pin 12, in conjunction with the microprocessor's analog to digital converter input. A microprocessor output (LBO) can be designated to flash a display enunciator when a low battery condition exists. The Reference Output is 1.5 V ±2.7% and is capable of sourcing in excess of 10 mA.

The Power Up Reset Output, Pin 13, is designed to hold the microprocessor reset input low until the voltage at Output 3 rises above 2.66 V. This feature prevents the microprocessor from hanging or writing invalid information into its memory during power up. Notice that the output of the MPU Power Up Reset comparator also drives the base of transistor Q_{PD}. If Output 3 should fall below 2.6 V, due to an overload or a low battery condition, the comparator will drive Q_{PD} "ON", causing its collector to pull high on the Power Down Input, immediately forcing the system into standby mode. Externally pulling down on Pin 13, base of Q_{PD}, will also force the system into standby mode.

A redundant Low Battery Shutdown circuit is included. This circuit directly monitors the battery voltage and also forces the system into standby mode when the battery voltage falls below 2.4 V. To test the functionality of this circuit, the high state signal generated by transistor Q_{PD} must be clamped low, to prevent resetting the ON/OFF Latch. An external short or a pull–down, capable of sinking 2.0 mA at less than 0.8 V, must be connected to Pin 10.

A Battery Latch circuit is designed into the IC to prevent the system from turning on when the batteries are inserted into the finished product. This feature is useful for the end customer as well as the equipment manufacturer. Upon initial application of battery voltage, the lower comparator (0.7 V threshold) forces the Battery Latch into a reset state with its "Q" output low. This in turn triggers a reset of the ON/OFF Latch via the OR gate and also locks out the set signal present at the upper input of the AND gate. As the voltage at Pin 11 rises above (V_{CC} – 1.5 V), the set signal disappears, leaving the state of the ON/OFF Latch unchanged (reset). When the voltage at Pin 11 rises above (V_{CC} –1.0 V), the upper comparator forces the Battery Latch into a set state causing its "Q" output to go high. This allows the AND gate and the ON/OFF Latch to receive a set signal from Pin 11. The initial Battery Latch lockout time is controlled by the internal 20 kΩ resistor and the external 0.1 μF capacitor.

Figure 5. MC33128 Block Diagram

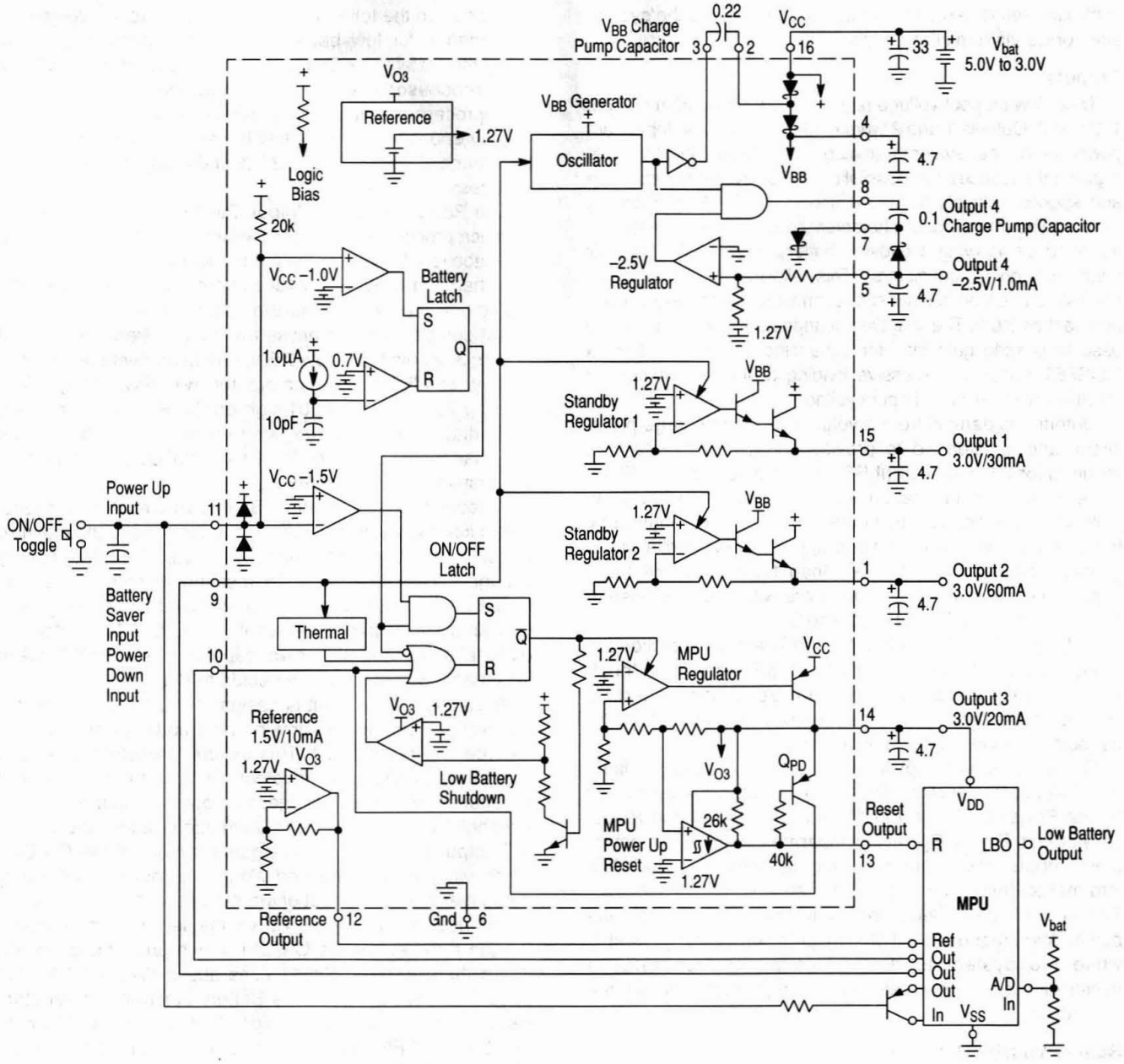
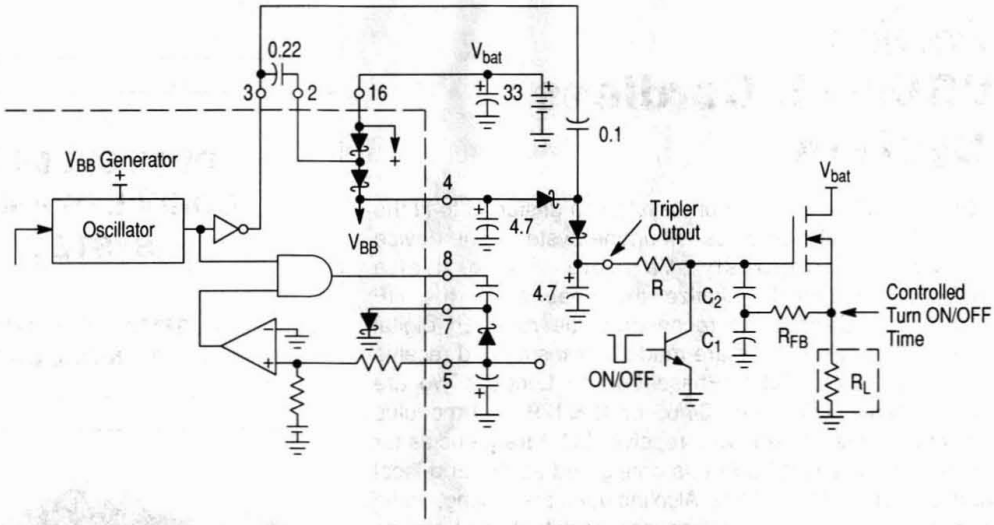


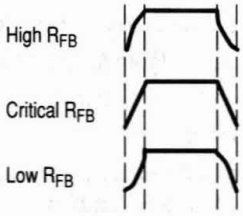
Figure 6. Voltage Tripler and Switch Driver



Tripler Output Voltage

Load Current (mA)	V_{CC} = 3.15 V	V_{CC} = 4.5 V
0	7.96	12.01
0.5	7.48	11.54
1.0	7.24	11.29
1.5	6.99	11.04
2.0	6.62	10.69

Load Turn ON/OFF Time



External Switch

A low threshold N–channel MOSFET can be used to switch the transmitting power amplifier (R_L) ON and OFF. To ensure that all of the available battery voltage appears across the load, the MOSFET must be fully enhanced over the system's required operating voltage range. With the addition of two Schottky diodes and two capacitors, the V_{BB} Generator can be made to function as a voltage tripler. The table in Figure 6 shows the output voltage characteristics of the tripler circuit.

In order to minimize adjacent channel splatter, the RF power amplifier must be turned ON and OFF in a controlled (soft) manner. The applied voltage rise and fall time, as well as the rate of change in rise and fall time, must be tailored to the amplifiers characteristics. The circuit consisting of resistors R, R_{FB}, and capacitors C_1 and C_2 is a simple solution allowing the system designer a means to control the ON and OFF time as well as the waveshape. Feedback resistor R_{FB} controls the waveshape. Capacitors C_1 and C_2 are usually of equal value.

MOTOROLA

MC33410

Product Preview

Dual CVSD/PLL Cordless Phone System

DUAL CVSD/PLL CORDLESS PHONE SYSTEM

SEMICONDUCTOR TECHNICAL DATA

The MC33410 Dual CVSD/Cordless Phone system is designed to fit the requirements of a 900 MHz digital cordless telephone system. The device contains a CVSD (Continuously Variable Slope Delta Modulator/Demodulator) Encoder to digitize the speech for the RF transmission, and a CVSD Decoder to reconstruct the received digital speech from the RF receiver. Provisions are made to transmit and receive data as well. Included are three PLLs (Phase–Locked Loops). Two are intended for use with external VCOs and 64/65 or 128/129 dual modulus prescalers, and can control the transmit and receive (LO1) frequencies for the 900 MHz communication. The third PLL is configured as the 2nd local oscillator (LO2), and is functional to 80 MHz. Also included are muting, audio gain adjust (internal and external), low battery/carrier detect, and a wide range for the PLL reference frequency. The power supply range is 2.7 to 5.5 V. A data only (non–voice) mode is also included.

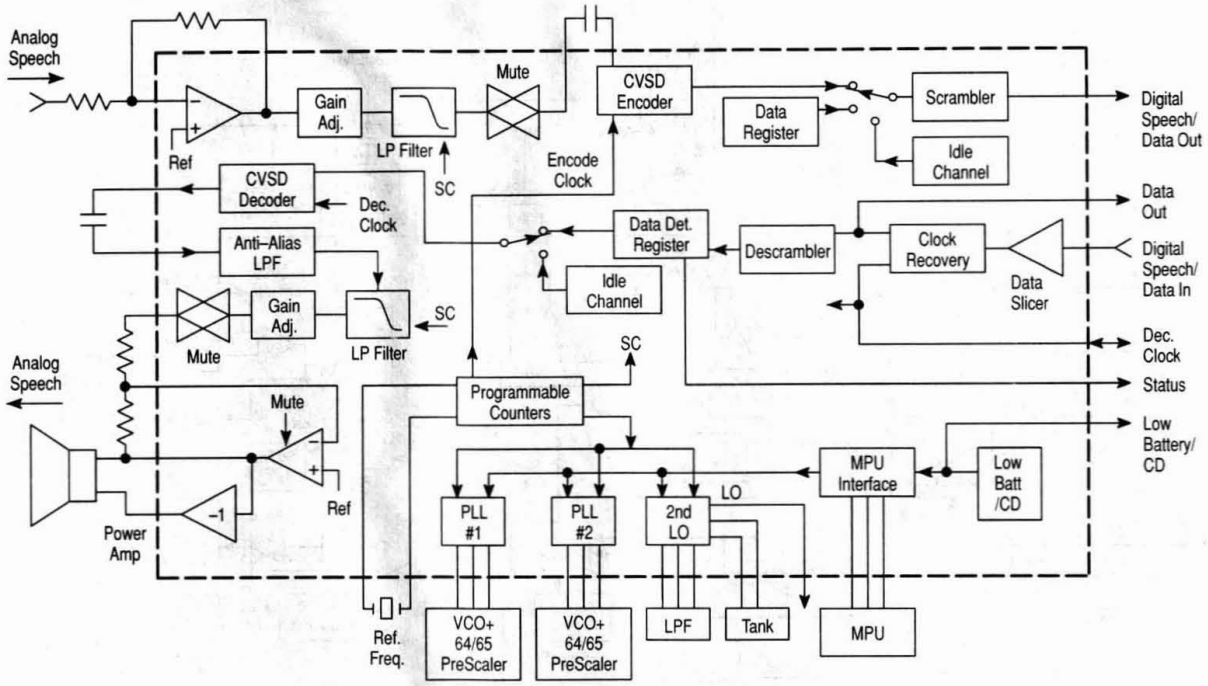
- Two Complete CVSD Sections for Full Duplex Operation
- Two PLLs and an LO Suitable for a 900 MHz System
- Adjustable Detection for Low Battery or Carrier Signal (RSSI)
- Minimal External Components
- Encode Path Includes Adjustable Gain Amplifiers, Filters, Mute, CVSD Encoder, Data Insert, and Scrambler
- Decoder Path Contains Data Slicer, Clock Recovery, Descrambler, Data Detect, CVSD Decoder, Filters, Mute and Power Amplifier
- Data can be Transmitted During Voice Conversation with Minimal or No Noticeable Audio Disruption
- Idle Channel Noise Control
- Independent Power Amplifier with Differential Outputs, Mute
- Selectable Frequency for Switched Capacitor Filters, CVSD Function, PLLs, and the LO
- Reference Frequency Source can be a Crystal or System Clock
- Serial µP Port to Control Gain, Mute, Frequency Selection, Phase Detector Gain, Power Down Modes, Idle Channel Control, Scrambler Operation, Low Battery Detect, and Others
- Mode Available for Data Only Transmission (non–voice)
- Ambient Temperature Range: –40 to 85°C
- Power Supply Range: 2.7 to 5.5 V
- Power Down Modes for Power Conservation
- 48 Pin LQFP with 0.5 mm Lead Pitch

FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Operating Temperature	Package
XC33410FTA	–40° to +85°C	LQFP–48

Simplified Block Diagram

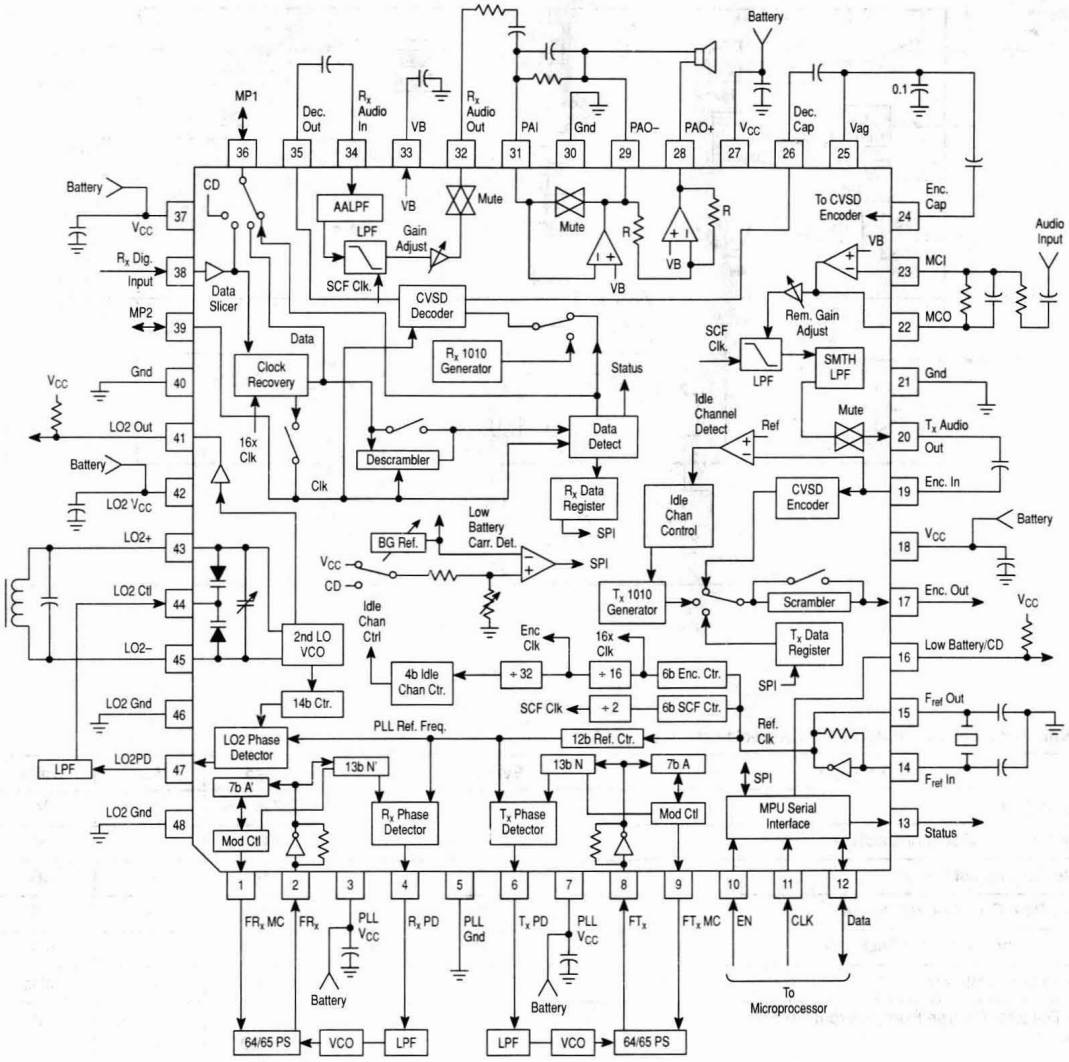


PRELIMINARY SPECIFICATIONS (Subject to change)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage		–	2.7 to 5.5	–	V
Supply Current (All sections active)		–	13	–	mA
Remote Gain Adjust Range		–	16	–	dB
Receive Path Gain Control Range		–	28.5	–	dB
Output Current Capability (PAO+, PAO–)		–	±5.0	–	mA
Max. 2nd LO frequency		–	80	–	MHz
Phase Detector Charge Pump Output Current High Low		 – –	 ±400 ±100	 – –	µA
Digital Input Signal Amplitude to Data Slicer		–	>200	–	mVpp
Operating Ambient Temperature		–	–40 to +85	–	°C

NOTE: 1. Above specs represent design objectives, and are subject to change.

Figure 1. Typical Applications Circuit



NOTE: Pin numbers are not firm and are not to be used for design–in purposes.

RECOMMENDED OPERATING CONDITIONS (Subject to change)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage		–	2.7 to 5.5	–	V
CVSD Clock Rate		–	32, 50, or 64	–	kHz
Encoder in Signal Level (max)		–	3.0	–	V_{pp}
Peak Output Current at PAO+, PAO–		–	±5.0	–	mA
Reference Frequency Amplitude (F_{ref} In)		–	>200	–	mVpp
R_x Digital Input Signal Amplitude Min Max		 – –	 0.20 0 to V_{CC}	 – –	V_{pp}
Crystal or Reference Frequency at Pin 14		–	4.0 to 18.25	–	MHz
Max. Input Frequency at FR_x, FT_x		–	TBD	–	MHz
LO2 VCO Control Voltage (Pin 44)		–	TBD	–	V
Max. 2nd LO Frequency		–	80	–	MHz
12 Bit Reference Counter Range (Note 1)		–	3 to 4095	–	–
13 Bit N Counter Range (Note 1)		–	3 to 8191	–	–
7 Bit A Counter Range (Note 1) with a 64/65 Modulus Prescaler with a 128/129 Modulus Prescaler		 – –	 0 to 63 0 to 127	 – –	–
14 Bit LO2 Counter Range (Note 1)		–	12 to 16383	–	–
6 Bit Counters (for SCF and Encode Clock) (Note 1)		–	3 to 63	–	–
Receive Path Gain Control Code Range (Note 1)		–	6 to 25	–	–
Operating Ambient Temperature		–	–40 to 85	–	°C

NOTES: 1. Values specified are pure numbers to the base 10.
2. Above specs represent design objectives, and are subject to change.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	FR_x MC	Modulus Control Output to the R_x 64/65 or 128/129 dual modulus prescaler.
2	FR_x	Input to the R_x PLL.
3	PLL V_{CC}	Supply pin for the R_x PLL section. Allowable range is 2.7 to 5.5 V.
4	R_x PD	Phase detector charge pump output of the R_x PLL.
5	PLL Gnd	Ground pin for the PLL sections.
6	T_x PD	Phase detector charge pump output of the T_x PLL.
7	PLL V_{CC}	Supply pin for the T_x PLL section and the MPU Serial Interface section. Allowable range is 2.7 to 5.5 V.
8	FT_x	Input to the T_x PLL.
9	FT_x MC	Modulus Control Output to the T_x 64/65 or 128/129 dual modulus prescaler.
10	EN	Enable input for the µP port. This signal latches in the register address and data.
11	CLK	Clock input for the µP port. Maximum frequency is 2.0 MHz.
12	Data	Bi–directional data line for the µP port. In Data Modem mode, this pin provides the recovered clock.
13	Status	Logic output which indicates that a predetermined 16 or 24–bit code word has been detected in the Data Detect register, and the following data word has been loaded into register 10. In Data Modem mode, this pin provides the Transmit Data clock.
14, 15	F_{ref} In, F_{ref} Out	A crystal, in the range of 4.0 to 18.25 MHz can be connected to these pins to provide the reference frequency. If an external reference source is used, it is to be capacitively coupled to F_{ref} In.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Description
16	Low Battery/CD	An open collector output. When low, indicates either the supply voltage (V_{CC}) is low, or the carrier level is above the threshold. This output is off when disabled.
17	Enc Out	The digital output of the scrambler, which passes data from the CVSD encoder, or the T_x Data register, or the T_x 1010 Generator. Source selection is done through the µP port.
18	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 27 and 37.
19	Enc In	The analog input to the CVSD encoder. Max. input level is 3.0 V_{pp}.
20	T_x Audio Out	Output of the transmit speech processing section.
21	Ground	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 30 and 40.
22	MCO	Output of the microphone amplifier, and input to the filters. This output has rail–to–rail capability.
23	MCI	Inverting input of the microphone amplifier. Gain and frequency response is set with external resistors and capacitors.
24	Enc Cap	This capacitor sets the time constant for the CVSD encoder. This pin is sensitive to leakage.
25	VAG	Analog ground for the audio section and the CVSD encoder and decoder.
26	Dec Cap	The capacitor sets the time constant for the CVSD decoder. This pin is sensitive to leakage.
27	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 18 and 37.
28, 29	PAO+, PAO–	Differential outputs of the power amplifier stage for driving an earpiece or hybrid network. The gain and frequency response are set with external resistors and capacitors.
30	Gnd	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 21 and 40.
31	PAI	Input to the power amplifier stage. This pin is a summing node.
32	R_x Audio Output	Output of the receive speech processing section.
33	VB	The capacitor filters the internal 1.5 V reference voltage. If VB is adjusted, it may be monitored at this pin. Max. load current is 10 µA.
34	R_x Audio In	Input to the receive speech processing section.
35	Dec Out	The analog output of the CVSD decoder.
36	MP1	As an output, provides the recovered R_x data, or the Data Detect output, or the data slicer output. Or it can be set to a high impedance input (600 kΩ) for the carrier detect input signal. Selection is done through the µP port. See Table 6.
37	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 18 and 27.
38	R_x Digital Input	The digital stream from the RF receiver is applied to the data slicer at this pin. Minimum amplitude is 200 mVpp. Hysteresis ≈50 mV.
39	MP2	As an output, this pin provides the recovered clock from the Clock Recovery block. As an input, the CVSD decoder clock can be applied to this pin. Or this pin may be set to a disabled state. Selection is done through the µP port. See Table 7. In Data Modem mode, the data to be transmitted is input to this pin.
40	Gnd	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 21 and 30.
41	LO2 Out	Buffered output of the 2nd LO frequency. A pullup resistor is required.
42	LO2 V_{CC}	Supply pin for the 2nd LO. Allowable range is 2.7 to 5.5 V.
43, 45	LO2+, LO2–	A tank circuit is connected to these pins for the 2nd LO.
44	LO2 Ctl	The varactor control pin for the 2nd LO.
46	LO2 Gnd	Ground for the 2nd LO section.
47	LO2 PD	Phase detector charge pump output of the 2nd LO PLL.
48	LO2 Gnd	Ground for the 2nd LO section.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

FUNCTIONAL DESCRIPTION

Note: In the following descriptions, control bits in the MPU Serial Interface for the various functions will be identified by register number and bit number. For example, bit 3/19 indicates bit 19 of register 3. Bits 5/14–11 indicates register 5, bits 14 through 11. Please refer to Figure 1.

Transmit Speech Processing Section

This section is made up of the externally adjustable microphone amplifier (Pins 22 to 23), internally adjustable gain stage, two low pass filters, and a mute switch.

The gain of the microphone amplifier is set with external resistors to receive the audio from the microphone (in the handset), or from the hybrid (in the base unit), or from any other audio source. The MCO output has rail–to–rail capability, and the dc bias level is at VB (≈1.5 V).

The adjustable gain stage, referred to as the Remote Gain Adjust, provides 5 levels of gain in 4.0 dB increments. It is controlled with bits 6/15–11 as shown in Table 1.

Table 1. Remote Gain Adjust

Register 6 Bits 15–11	Gain
00001	–8.0 dB
00010	–4.0 dB
00100	0 dB
01000	+4.0 dB
10000	+8.0 dB

Other combinations for the 5 bits are invalid.

The Low Pass Filter after the gain stage is a switched capacitor filter with a corner frequency at 5.0 kHz. The subsequent smoothing low pass filter has a corner frequency at 30 kHz, and is designed to filter out high frequency clock noise from the previously mentioned switched capacitor filter.

The mute switch at Pin 20 will mute a minimum of 60 dB. Bit 6/2 controls the mute.

CVSD Encoder/Idle Channel/T_x Data Register

The analog signals to be digitized are input at Pin 19 to the CVSD Encoder. The output of the encoder will be the digital equivalent of the audio, at the selected clock rate. Based on the reference frequency, bits 4/23–18 are used to set the 6 Bit Encoder Counter, in conjunction with the subsequent ÷16 divider, to set the CVSD Encoder frequency to 32, 50, or 64 kHz. Bits 3/16–15 will set the CVSD for proper operation at the selected frequency, according to Table 2.

Table 2. CVSD Clock/Data Rates

Register 3		
Bit 16	Bit 15	Clock/Data Rate
0	1	32 kHz
1	0	50 kHz
1	1	64 kHz

The Encoder's minimum step size can be selected using bits 2/22–21, according to Table 3.

Table 3. Minimum Step Size

Encoder Register 2 Bits 22, 21	Decoder Register 1 Bits 22, 21	Step Size
00	00	No minimum
01	01	1.4 mV
10	10	5.6 mV
11	11	22.4 mV

The T_x 1010 Generator, when selected, provides an alternating "1–0" pattern (a square wave at half the CVSD clock rate) to the scrambler. This represents the lowest amplitude analog signal, and can be used when it is desired to send a quiet signal. Selection of this block can occur either automatically, or intentionally, as follows:

a. The automatic selection occurs when the Idle Channel Detector senses the average audio signal at Pin 19 is below a threshold which is set with bits 5/17–15 (See Table 4). Bits 5/14–11 select a time delay for the automatic threshold detection to occur. The minimum delay is zero, with these bits set to 0000. Changing the bits provides delay in increments of 32 clock cycles (of the CVSD Encoder clock). The maximum delay is 480 clock cycles, (7.5 mS at 64 kHz). When the average audio signal at Pin 19 increases above the threshold, the T_x 1010 Generator will be deselected with no delay. This automatic switchover feature can be disabled with bit 7/2. Bit 5/21 indicates when an idle channel condition has been detected. This output bit will be functional even when the idle channel detector is disabled with bit 7/2. Bit 5/18 will power down the Idle Channel Detect Circuit as a power saving measure.

b. Bit 6/4 can be used to intentionally select the T_x 1010 Generator at any time.

Table 4. Idle Channel Detection Threshold

Register 5 Bits 17–15	Threshold		Register 5 Bits 17–15	Threshold
000	–50 dBV		100	–60 dBV
001	–52.5		101	–62.5
010	–55		110	–65
011	–57.5		111	–67.5

The T_x Data Register is used for the transmission of data between the handset and base units. The procedure is as follows:

a. At the receiving unit: The code word (16 or 24 bits, set with bit 7/11) identifying that a data transmission is occurring must be loaded into the T_x Data Register (by loading register 8). This is used to detect when a code word is sent from the transmitting unit.

b. At the transmitting unit: The same code word as above is loaded into register 8. It is automatically loaded into the T_x Data Register.

c. The data word (16 or 24 bits, set with bit 7/12) is then loaded into register 9.

d. Upon loading register 9, the MC33410 automatically sends out (at Pin 17) the code word, followed by the data word, at the CVSD clock rate.

When the data word is completely sent out, the MC33410 will then return Pin 17 to its previous source of digital information (CVSD Encoder or T_x 1010 Generator).

Scrambler/Digital Output

The scrambler receives digital data from the CVSD Encoder, or the T_x 1010 Generator, or the T_x Data Register, to be output at Pin 17. The output level is 0 to V_{CC}. The scrambler can be bypassed with Bit 7/1.

The scrambler, better known as a randomizer, provides not only a level of communication security, but also helps ensure the digital output will not contain an abnormally long string of 1s or 0s which can adversely affect the CVSD Decoder operation, as well as the RF section. The scrambler is a maximal–length shift register sequence generator. The length of the shift register is selectable to one of eight values with bits 7/10–8 (the descrambler in the receiving unit must be set the same). Table 5 lists the polynomial associated with each tap selection.

Table 5. Scrambler/Descrambler Tap Selection

Tap No.	Register 7			Shift Register Length	Polynomial
	Bit 10	Bit 9	Bit 8		
0	0	0	0	2	$1 + z^{-1} + z^{-2}$
1	0	0	1	3	$1 + z^{-2} + z^{-3}$
2	0	1	0	4	$1 + z^{-3} + z^{-4}$
3	0	1	1	5	$1 + z^{-3} + z^{-5}$
4	1	0	0	6	$1 + z^{-5} + z^{-6}$
5	1	0	1	7	$1 + z^{-6} + z^{-7}$
6	1	1	0	9	$1 + z^{-5} + z^{-9}$
7	1	1	1	10	$1 + z^{-7} + z^{-10}$

Data Slicer/Clock Recovery

The data slicer will receive the low level digital signal from the RF receiver section at Pin 38. The input signal to the data slicer must be >200 mVpp. Hysteresis of 50 mV is internally provided. The output of the data slicer will be same waveform, but with an amplitude of 0 to V_{CC}, and can be observed at Pin 36 (MP1) if bits 7/5–4 are set to 10. The output can be inverted by setting bit 5/19 = 1.

The clock recovery block will generate a phase locked clock, equal to the CVSD data rate, from the incoming data, as long as the Encoder Counter (bits 4/23–18) is set for that data rate. The recovered clock can be observed at Pin 39 (MP2) if bits 7/7–6 are set to 00. The data from the clock recovery block can be observed at Pin 36 if bits 7/5–4 are set to 00. The clock recovery block may be bypassed by setting bit 7/0 to 1. With this setting the data slicer output will go directly to the descrambler, and the encoder clock will replace the Clock Recovery Clock.

Tables 6 and 7 summarize the options available at MP1 and MP2 (Pins 36 and 39).

Table 6. MP1 Options (Pin 36)

Register 7		Function
Bit 5	Bit 4	
0	0	Data from clock recovery block
0	1	Data Detect Output
1	0	Data Slicer Output
1	1	Hi–Z/ CD Input

Table 7. MP2 Options (Pin 39)

Register 7		Function
Bit 7	Bit 6	
0	0	Output recovered clock
0	1	Input CVSD Decoder clock
1	X	Disabled (Hi–Z)

When MP1 is set to a Hi–Z condition, the pin is an input for the CD (Carrier Detect) function, with an input impedance of 600 KΩ. See the section entitled Low Battery/Carrier Detect for an explanation of this function.

Descrambler

The descrambler receives the scrambled data from the clock recovery block (or the data slicer if bit 7/0 = 1), and descrambles it to the original data as long as the selected taps are the same as those in the transmitting scrambler (see Table 5). The descrambler block is the same configuration as the scrambler, and is self–synchronizing. The descrambler can be bypassed with bit 7/1.

Data Detect Register/Status Output/R_x Data Register

The Data Detect register will continuously compare the descrambled data it receives with the 16 or 24–bit code word stored in the T_x Data Register (loaded through register 8). Upon detecting a match, and after the code word passes through the shift register, the following (16 or 24–bit) data word will be stored into the R_x Data Register, and then loaded into register 10 of the MPU Interface. At this time the Status

output at Pin 13, and bit 5/22, will go high. The external microprocessor can then retrieve the data word by reading register 10, at which time the Status pin and bit will go low.

Upon detection of a code word as described above, the CVSD Decoder will be provided with 32, 40, or 48–bits of a 1010 pattern (idle channel) to minimize disturbances to the audio. After the data word is loaded into register 10, the CVSD Decoder resumes receiving data from the descrambler. The audio is therefore interrupted with a low level signal for a maximum of 48 clock cycles (0.75 mSec at 64 kHz).

The Data Detect register can be bypassed by setting bit 7/3 = 1.

CVSD Decoder/Decoder Clock/Idle Channel

The CVSD Decoder will provide the analog equivalent, at Pin 35, of the digital data it receives from the descrambler, or from the 1010 generator (idle channel generator). There is a single pole filter at the Decoder output to reduce the clock noise normally present on a CVSD analog output. The CVSD Decoder is self synchronizing as long as the decoder clock matches the data rate, and the Decoder has been set with bits 3/16–15 according to Table 2.

The Decoder clock is provided from the Clock Recovery block by setting bits 7/7–6 to 00 or 1X. The clock is internally provided to the Decoder, and is available at Pin 39. Alternately, a Decoder clock can be provided from an external source to Pin 39 by setting bit 7/7–6 to 01 (see Table 7).

The R_x 1010 Generator provides an alternating 1–0 pattern (a square wave at half the CVSD clock rate) to the CVSD Decoder, resulting in the lowest amplitude analog signal at Pin 35. The 1010 Generator is automatically selected whenever data is detected and received by the Data Detection Circuit, as described above. Additionally, the 1010 Generator can be selected with bit 6/3 at any time.

The Decoder's minimum step size can be selected using bits 1/22–21, according to Table 3.

Receive Audio Path

The Receive Audio Path (Pins 34 to 32) consists of an anti–aliasing filter, a low pass filter, a gain adjust stage, and a mute switch.

Since the analog output of the CVSD Decoder (typically input at Pin 34) will contain noise at the CVSD clock rate, the anti–aliasing filter, with a corner frequency at 30 kHz, is provided to prevent aliasing of that clock noise with the subsequent switched capacitor filter.

The switched capacitor low pass filter is a 3 pole filter, with a corner frequency at 5.0 kHz. This is designed to remove the clock noise from the CVSD Decoder output signal, as well as provide bandwidth limiting in the audio range.

The gain stage provides 28.5 dB of gain adjustment in 19 steps (1.5 dB each), measured from Pin 34 to 32. Bits 6/10–6 are used to set the gain according to Table 8.

The mute switch at Pin 32, controlled by bit 6/1, will mute a minimum of 60 dB.

Table 8. Receive Gain Adjustment

Register 6 Bits 10...6	Gain	Register 6 Bits 10...6	Gain
00110	–13.5 dB	10000	+1.5 dB
00111	–12.0 dB	10001	+3.0 dB
01000	–10.5 dB	10010	+4.5 dB
01001	–9.0 dB	10011	+6.0 dB
01010	–7.5 dB	10100	+7.5 dB
01011	–6.0 dB	10101	+9.0 dB
01100	–4.5 dB	10110	+10.5 dB
01101	–3.0 dB	10111	+12.0 dB
01110	–1.5 dB	11000	+13.5 dB
01111	0.0 dB	11001	+15.0 dB

Power Amplifiers

The power amplifiers (Pins 28, 29, 31) are designed to drive the earpiece in a handset, or the telephone line via a hybrid circuit in the base unit. Each output (PAO+ and PAO–) can source and sink 5 mA, and can swing 2.0 V_{pp} each. The gain of the amplifiers is set with a feedback resistor from Pin 29 to 31, and an input resistor at Pin 31. The differential gain is 2x the resistor ratio. Capacitors can be used for frequency shaping. The pins' dc level is VB (≈1.5 V).

The Mute switch, controlled with bit 6/0, will provide 90 dB of muting with a 50 kΩ feedback resistor. The amount of muting will depend on the value of the feedback resistor.

Reference Clock

The reference clock provides the frequency basis for the three PLLs, the switched capacitor filters, and the CVSD Encoder section. The source for the reference clock can be a crystal in the range of 4.0 to 18.25 MHz connected to Pins 14 & 15, or it can be an external source connected to F_{ref} In (Pin 14). The reference frequency is directed to:

a. A programmable 12–bit counter to provide the reference frequency for the three PLLs. The 12–bit counter is to be set such that, in conjunction with the programmable counters within each PLL, the proper frequencies can be produced by each VCO.
b. A programmable 6–bit counter, followed by a ÷2 stage, to set the frequency for the switched capacitor filters to 256 kHz, or as close to that as possible.
c. A programmable 6–bit counter which provides the 16x clock for the Clock Recovery block. This is followed by a ÷16 stage which provides the CVSD Encoder clock. This is followed by a ÷32 stage, and a programmable 4–bit counter which sets the delay for the Idle Channel Detect circuit.

Transmit and Receive (LO1) PLL Sections

The transmit and receive PLLs (Pins 6 to 9 and 1 to 4, respectively) are designed to be part of a 900 MHz system. In

a typical application the Transmit PLL section will be set up to generate the transmit frequency, and the Receive PLL section will be set up to generate the LO1 frequency. The two sections are identical, and function independently. External requirements for each include a low pass filter, a 900 MHz VCO, and a 64/65 or 128/129 dual modulus prescaler.

The frequency output of the VCO is to be reduced by the dual modulus prescaler, and then input to the MC33410 (at Pin 2 or 8). That frequency is then further reduced by the programmable 13–bit counter (bits 1/19–7 or 2/19–7), and provided to one side of the Phase Detector, where it is compared with the PLL reference frequency. The output of the phase detector (at Pin 4 or 6) is a bi–directional charge pump which drives the VCO through the low pass filter. Bits 1/20 and 2/20 set the gain of each of the two charge pumps to either $100/2\pi$ µA/Radian or $400/2\pi$ µA/Radian. The polarity of the two phase detector outputs is set with bits 7/22 and 7/23. If the bit=0, the appropriate PLL is configured to operate with a non–inverting low pass filter/VCO combination. If the low pass filter/VCO combination is inverting, the polarity bit should be set to 1.

The 7–bit A and A' counters (bits 1/6–0 and 2/6–0) are to be set to drive the Modulus Control input of the 64/65 or 128/129 dual modulus prescalers. The Modulus Control outputs (Pins 1 and 9) can be set to either a voltage mode or a current mode with bit 7/13.

To calculate the settings of the N and A registers, the following procedure is used:

$$\frac{f_{VCO}}{f_{PLL}} = Nt \text{ (Nt must be an integer)} \qquad \text{Equation 1}$$

$$\frac{Nt}{P} = N \qquad \text{Equation 2}$$

A = Remainder of Equation 2 (decimal part of N x P) — Equation 3

where: f_{VCO} = the VCO frequency
f_{PLL} = the PLL Reference Frequency set within the MC33410
P = the smaller divisor of the dual modulus prescaler (64 for a 64/65 prescaler)
N = the whole number portion is the setting for the N (or N') counter within the MC33410
A = the setting for the A (or A') counter within the MC33410

For example, if the VCO is to provide 910 MHz, and the internal PLL reference frequency is 50 kHz, then the equations yield:

$$Nt = \frac{910 \times 10^6}{50 \times 10^3} = 18,200$$

$$N = \frac{18,200}{64} = 284.375$$

$$A = 0.375 \times 64 = 24$$

The N register setting is 284_d (0 0001 0001 1100), and the A register setting is 24_d (001 1000).

2nd LO (LO2)

This PLL is designed to be the 2nd Local Oscillator in a typical 900 MHz system, and is designed for frequencies up to 80 MHz. The VCO and varactor diodes are included, and are to be used with an external tank circuit (Pins 43 to 45).

Bits 7/20–18 are used to select an internal capacitor, with a value in the range of 0 to 7.6 pF, to parallel the varactor diodes and the tank's external capacitor. This permits a certain amount of fine tuning of the oscillator's performance. See Table 9.

A buffered output is provided to drive, e.g., a mixer. The frequency is set with the programmable 14–bit counter (bits 3/13–0) in conjunction with the PLL reference frequency. For example, if the reference frequency is 50 kHz, and the 2nd LO frequency is to be 63.3 MHz, the 14–bit counter needs to be set to 1266_d (00 0100 1111 0010). The output level is dependent on the value of the impedance at Pin 41, partly determined by the external pullup resistor.

The output of the phase detector is a bi–directional charge pump which drives the varactor diodes through an external low pass filter. Bit 3/14 sets the gain of the charge pump to either $100/2\pi$ µA/Radian or $400/2\pi$ µA/Radian. Bit 7/21 sets its polarity – if 0, the PLL is configured to operate with a non–inverting low pass filter/VCO combination. If the low pass filter/VCO combination is inverting, the polarity bit should be set to 1.

Table 9. LO2 Capacitor Selection

Register 7 Bits 20–18	Capacitor Value	Register 7 Bits 20–18	Capacitor Value
000	0 pF	100	4.3 pF
001	1.1 pF	101	5.4 pF
010	2.2 pF	110	6.5 pF
011	3.3 pF	111	7.6 pF

VB Reference Voltage

The VB voltage (≈1.5 V) is available at Pin 33. It will have a production tolerance of ±6%, and can be adjusted over a ±9% range using bits 3/20–17. The adjustment steps will be ≈1.2% each. VB can be used to bias external circuitry, as long as the load current on this pin does not exceed 10 µA.

Low Battery/Carrier Detect

This circuit will provide an indication of either Low Battery voltage, or a low carrier signal applied to Pin 36 (MP1) from an RSSI circuit. The desired mode is selected with bit 6/5.

A) Low Battery Mode (Bit 6/5 = 0)

The supply voltage at Pin 18 is applied to the comparator through an internal resistor divider, and is compared to the internal reference VB (≈1.5 V). The comparator has ≈15 mV of hysteresis, measured at V_{CC}. The resistor divider is adjustable using bits 3/23–21. The Low Battery threshold voltage will then be equal to the VB voltage multiplied by the factor listed in Table 10. For example, if VB = 1.5 V, and bits 3/23–21 = 011, the threshold will be 3.21 V.

B) Carrier Detect Mode (Bit 6/5 = 1)

Pin 36 (MP1) must be set to the Hi–Z/CD Input mode by setting bits 7/5–4 to 11. MP1 will then be an input with an input impedance of ≈600 kΩ, referenced to VB. An analog signal applied to MP1 will be applied to the comparator through an internal adjustable gain stage (adjustable using bits 3/23–21), and is compared to the internal reference VB. The comparator has ≈18.0 mV of hysteresis, measured at Pin 36. The threshold voltage will then be equal to the VB voltage multiplied by the factor listed in Table 10. For

example, if VB = 1.5 V, and bits 3/23–21 = 011, the threshold will be 0.576 V.

Table 10. LB/CD Threshold Adjustment Factor

Register 3 Bits 23–21	Low Battery Mode	Carrier Detect Mode
000	1.96	0.574
001	2.02	0.524
010	2.08	0.453
011	2.14	0.384
100	2.19	0.314
101	2.25	0.247
110	2.30	0.177
111	2.37	0.110

The comparator output is at bit 5/23, and at Pin 16 (open collector output). The outputs are high if the monitored V_{CC} voltage is above the threshold, or if the Carrier signal is below the threshold. Pin 16 requires an external pullup resistor. When this circuit is disabled (bit 5/10 = 1), bit 5/23 and Pin 16 will be high.

MPU Serial Interface

The MPU Serial Interface is a 3–wire interface, consisting of a Clock line, an Enable line, and a bi–directional Data line. The interface is always active, i.e. it cannot be powered down as all other sections of the MC33410 are disabled and enabled through this interface.

The clock must be supplied to the MC33410 at Pin 11 to write or read data, and can be any frequency up to 2.0 MHz. The clock need not be present when data is not being transferred. The Enable line must be low when data is not being transferred.

Internally there are 10 data registers, 24 bits each, addressed with four bits ranging from $1 to $A. Register 10, and bits 23–21 of register 5 contain data to be read out by the microprocessor, while all other register bits are to be written to by the microprocessor. The contents of the 10 registers can be read out at any time. All bits are written in, or read out, on the clock's positive transition. The write and read operations are as follows:

a) Write Operation:

To write data to the MC33410, the following sequence is required (see Figure 2):

7. The Enable line is taken high.
8. Five bits are entered:
   - The first bit must be a 0 to indicate a Write operation.
   - The next four bits identify the register address (0001–1010). The MSB is entered first.
9. After the 5th clock pulse is low, the Enable line is taken low. At this transition, the address is latched in and decoded.
10. The Enable line is maintained low while the data bits are clocked in. The MSB is entered first, and the LSB last. If 24 bits are written to a register which has less than 24 active bits (e.g., register 6), the unassigned bits are to be 0.
11. After the last bit is entered, the Enable line is to be taken high and then low. The falling edge of this pulse latches in the just entered data. The clock line can be at a logic high or low, but must not transition in either direction during this Enable pulse.
12. The Enable line must then be kept low until the next communication.

Note: If less than 24 bits are to be written to a data register, it is not necessary to enter the full 24 bits, as long as they are all lower order bits. For example, if bits 0–6 of a register are to be updated, they can be entered as 7 bits with 7 clock cycles in step 4 above. However, if this procedure is used, a minimum of 4 bits, with 4 clock pulses, must be entered.

Figure 2. Writing Data to the MC33410

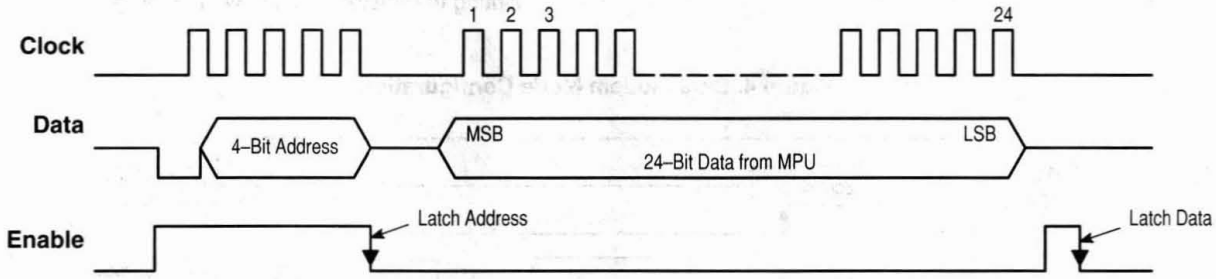
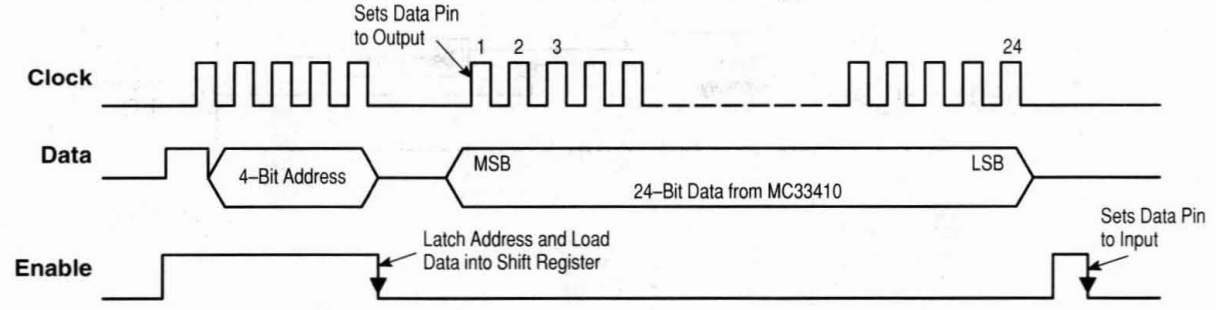


Figure 3. Reading Data from the MC33410



b) Read Operation:

To read the output bits (bits 5/23–21, or all of register 10), or the contents of any register, the following sequence is required (see Figure 3):

1. The Enable line is taken high.
2. Five bits are entered:
   - The first bit must be a 1 to indicate a Read operation.
   - The next four bits identify the register address (0001–1010). The MSB is entered first.
3. After the 5th clock is taken low, the Enable line is taken low. At this transition, the address is latched in and decoded, and the contents of the selected register is loaded into the 24–bit output shift register. At this point, the Data line (Pin 12) is still an input.
4. While maintaining the Enable line low, the data is read out. The first clock rising edge will change the Data line to an output, and the MSB will be present on this line.
5. The full contents of the register are then read out (MSB first, LSB last) with a total of 24 clock rising edges, including the one in step 4 above. It is recommended that the MPU read the bits at the clock's falling edge. If only bit 23, 22, or 21 of register 5 are to be read, this can be done with one, two, or three clock rising edges, respectively.
6. After the last clock pulse, the Enable line is to be taken high and then low. The falling edge of this pulse returns the Data pin to be an input. The clock line can be at a logic high or low, but must not transition in either direction during this Enable pulse.
7. The Enable line must then be kept low until the next communication.

Data Modem Mode

For applications where the MC33410 is to be used in a 900 MHz wireless system for transmitting data only (non–voice), a mode can be set which bypasses the speech digitizing sections. The resulting configuration makes use of those sections associated with data only, i.e., the scrambler, descrambler, and clock recovery section. Also functional are the three PLLs, the audio receive path (Pins 34 to 28), the transmit audio path (Pins 23 to 20), and the Low Battery circuit (but not the Carrier Detect mode).

In this mode, the MC33410 will provide the transmit data clock from the crystal, in conjunction with the internal 6–bit counter (bits 4/23–18) and the ÷16 block associated with that counter. The transmit data clock is available at Pin 13, and can be used to synchronize the external data source. The T_x data is input at Pin 39, passes through the scrambler, and outputs at Pin 17.

The demodulated data from the RF receiver is input at Pin 38, and is applied to the data slicer, and the clock recovery block. The recovered clock is output at Pin 12. The data passes through the descrambler, and is output at Pin 36.

Figure 4 is a diagram of the data paths through the MC33410.

The procedure for entering the Data Modem mode is in Table 11:

Table 11. Entering Data Modem Mode

Function	Bits	Bit Value
Set T_x Clock to desired frequency T_x Clk = $F_{crystal}$/(16 x Counter).	4/23 – 18	As Desired
Set Scrambler & Descrambler tap setting (Bit 7/1 = 0).	7/10 – 8	As Desired
Bypass Data Detect.	7/3	1
Set MP1 to Data Detect Output.	7/5 – 4	01
Set Test Mode bits to connect Encode Clock to Status (Pin 13).	7/17 – 15	110
Set Data Modem Mode (MP2 to scrambler Input).	5/20	1
Write to Register 11 as shown in Figure 5 to configure Pin 12.	N/A	N/A

The above sequence is not critical, except that the last two steps must be the setting of bit 5/20, and writing to register 11. Writing to register 11 is shown in Figure 5.

Figure 4. Data Modem Mode Configuration

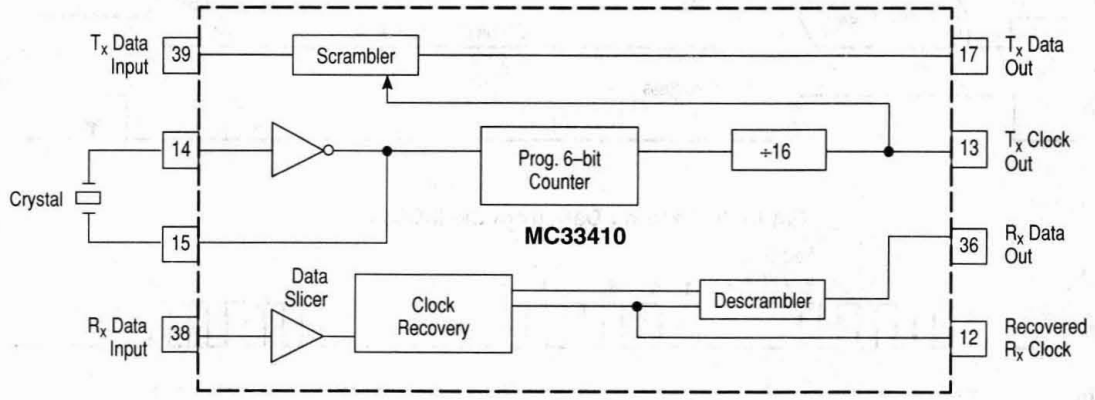
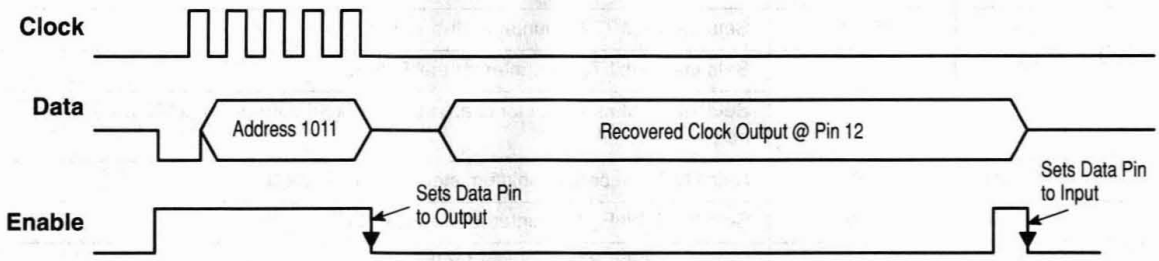


Figure 5. Entering/Exiting Data Modem Mode



After address 11 is clocked in, the Enable falling edge will cause Pin 12 (Data) to switch to an output, providing the recovered clock. The microprocessor's data pin must be changed to an input prior to this falling edge. This sequence is effective only if bit 5/20 is set to a 1.

During the time that recovered clock is available at Pin 12, the microprocessor port is unavailable for any control functions.

To exit the Data Modem mode, the Enable line is to be taken high and low (the clock is to be stable during this active high pulse). The falling edge will set Pin 12 to be an input, allowing normal use of the microprocessor port. The next step is to set bit 5/20 to a 0. Other register bits can then be set as needed.

To prevent inadvertent incorrect operation of the microprocessor port, bit 5/20 must always be set to 0 when the Data Modem mode is not in use.

Power Supply/Power Saving Modes

The power supply voltage, applied to all V_{CC} pins, can range from 2.7 to 5.5 V. All V_{CC} pins must be within ±0.5 V of each other, and each must be bypassed. It is recommended a ground plane be used, and all leads to the MC33410 be as short and direct as possible. The supply and ground pins are distributed as follows:

1. Pins 18, 27 and 37 are internally connected together, and provide power to the audio amplifiers, filters, CVSD encoder and decoder, and the low frequency (CVSD rate) logic circuits. Pins 21, 30 and 40 are the ground pins for these sections.
2. Pin 3 provides power to the R_x PLL section. Pin 5 is the ground pin.
3. Pin 7 provides power to the T_x PLL section, and the MPU interface. Pin 5 is the ground pin.
4. Pin 42 provides power to the 2nd LO section. Pins 46 and 48 are the ground pins.

To conserve power, various sections can be individually disabled, using bits 5/10–0 (setting a bit to 1 disables the section).

1. Reference Oscillator Disable (bit 5/0) – The reference oscillator at Pins 14 and 15 is disabled, thereby denying a clock to the three PLLs, the CVSD Encoder, and the switched capacitor filters.
2. T_x PLL Disable (bit 5/1) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 6 will be in a Hi–Z state.
3. R_x PLL Disable (bit 5/2) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 4 will be in a Hi–Z state.
4. LO2 PLL Disable (bit 5/3) – The VCO, 14–bit counter, output buffer, and phase detector are disabled. The charge pump output at Pin 47 will be in a Hi–Z state.
5. R_x Data Path Disable (bit 5/4) – The data slicer, clock recovery block, descrambler, data detect register, and the status output circuit are disabled. The state of the status line (Pin 13 and bit 5/22) will not change upon disabling this section.
6. CVSD Decoder Disable (bit 5/5) – The CVSD Decoder and the R_x 1010 Generator are disabled.
7. R_x Audio Path Disable (bit 5/6) – The anti–aliasing filter, low pass filter, and variable gain stage are disabled.
8. Power Amplifier Disable (bit 5/7) – The two power amplifiers are disabled. Their outputs will go to a Hi–Z state.
9. T_x Audio Path Disable (bit 5/8) – Disables the microphone amplifier, low pass filter, and smoothing filter.
10. CVSD Encoder Disable (bit 5/9) – The CVSD Encoder, Idle Channel detect circuit, the T_x 1010 Generator, the T_x Data register, and the scrambler are disabled.
11. Low Battery/Carrier Detect Disable (bit 5/10) – The LB/CD circuit is disabled. The output, at bit 5/23 and Pin 16 will be at a logic high.
12. Idle Channel Detect Disable (bit 5/18) – Powers down the Idle Channel Detect circuit.

Note: The 12–bit reference counter is disabled if the three PLLs are disabled (bits 5/1–3 = 1).

Table 12. Control Bit Listing (By Register Number)

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1 (23 bits total)	6 – 0	1000000	Sets the 7–bit T_x A counter for the T_x PLL.
	19 – 7	10....0	Sets the 13–bit T_x N counter for the T_x PLL.
	20	0	Sets the T_x phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	22, 21	00	Sets CVSD Decoder minimum step size per Table 3.
2 (23 bits total)	6 – 0	1000000	Sets the 7–bit R_x A' counter for the R_x PLL.
	19 – 7	10....0	Sets the 13–bit R_x N' counter for the R_x PLL.
	20	0	Sets the R_x phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	22, 21	00	Sets CVSD Encoder minimum step size per Table 3.
3 (24 bits total)	13 – 0	10....0	Sets the 14–bit counter for the 2nd LO.
	14	0	Sets the LO2 phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	16 – 15	11	Set the CVSD encoder/decoder for the selected clock rate. (Table 2)
	20 – 17	0111	Adjusts the VB reference voltage (≈1.5 V) to improve low battery detection accuracy. Total adjustment range is ≈±9%.
	23 – 21	011	Selects the threshold for Low Battery Detection or Carrier Signal Detection. See Table 10.
4 (24 bits total)	11 – 0	$800	Sets the 12–bit counter for the PLL Reference Clock.
	17 – 12	100000	Sets the 6–bit counter for the Switched Capacitor Filter clock.
	23 – 18	100000	Sets the 6–bit counter to set the CVSD Encoder clock rate.
5 (24 bits total)	0	0	Power down the Reference Oscillator
	1	0	Power down the T_x PLL.
	2	0	Power down the R_x PLL.
	3	0	Power down the LO2 PLL.
	4	0	Power down the R_x Data Path. Includes Data Slicer, Clock Recovery, Descrambler, Data Detect, and Status circuits.
	5	0	Power down the CVSD Decoder.
	6	0	Power down the R_x Audio path (Pin 32 to 30). Includes AALPF, LPF, and Gain Adjust circuits.
	7	0	Power down the Power Amplifiers (Pins 27, 28)
	8	0	Power down the T_x Audio Path (Pin 25 to 22). Includes micro–phone amplifier, LPF, and Smoothing LPF circuits.
	9	0	Power down the CVSD Encoder, Idle Channel Detector, 1010 Generator, T_x Data Register, and Scrambler circuits.
	10	0	Power down the Low Battery/Carrier Detect Circuit.
	14 – 11	0111	Sets the 4–bit counter to set the response delay for the idle channel detect circuit.
	17 – 15	100	Sets the idle channel detect threshold level. See Table 4.
	18	0	Power down the Idle Channel Detect Circuit.
	19	0	Inverts the Data Slicer output.
	20	0	Sets the Data Modem mode of operation.
	21	N/A	Indicates an idle channel condition has been detected (Output). This output is unaffected by bit 7/2.
	22	N/A	The Status Output (same as Pin 13) is read out from this bit.
	23	N/A	The output of the Low Battery/Carrier Detect Circuit is read from this bit.

Table 12. Control Bit Listing (By Register Number) (continued)

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
6 (16 bits total)	0	0	Mutes the power amplifiers (Pins 27 to 29).
	1	0	Mutes the receive speech processing path (Pin 30).
	2	0	Mutes the transmit speech processing path (Pin 22).
	3	0	Selects the R_x 1010 Generator to the CVSD decoder.
	4	0	Selects the T_x 1010 Generator to the scrambler.
	5	0	Sets Carrier Detect Mode vs. Low Battery mode.
	10 – 6	01111	Provides 19 steps, 1.5 dB each (28.5 dB range), of gain adjust in the receive speech audio path (Pins 32 to 30). See Table 8.
	15 – 11	00100	Provides 4 steps of 4.0 dB each, for the remote gain adjust in the transmit speech audio path (Pins 23 to 20).
7 (24 bits total)	0	0	Bypass the Clock Recovery Block (Data slicer output goes directly to the descrambler).
	1	0	Bypass the scrambler and descrambler.
	2	0	Disables the automatic idle channel detect at the CVSD encoder. Bit 5/21 is still active.
	3	0	Bypass the Data Detect block (Descrambler output goes directly to the CVSD Decoder).
	5 – 4	00	Determines the function for Pin 36 (MP1). See Table 6.
	7 – 6	00	Determines the function for Pin 39 (MP2). See Table 7.
	10 – 8	010	Selects one of 8 programmable taps in the scrambler and descrambler. See Table 5.
	11	1	Sets the code word size to be sent out via the T_x Data Register to 24 bits. If this bit is 0, the code word size is 16 bits.
	12	1	Sets the data word size to be sent out via the T_x Data Register to 24 bits. If this bit is 0, the data word size is 16 bits.
	13	0	Sets the FT_x MC and FR_x MC output level to be from ground to V_{CC}. If this bit is 0, the output level is ±100 μA.
	14	0	Disables the CVSD charge compensation circuit.
	17 – 15	000	Test modes for production testing only.
	20 – 18	000	Selects the value of the internal capacitor between Pins 43 to 45, to fine tune the LO2 tank circuit. See Table 9.
	21	0	Sets the polarity of the 2nd LO phase detector charge pump output for an inverting low pass filter/VCO combination.
	22	0	Sets the polarity of the R_x phase detector charge pump output for an inverting low pass filter/VCO combination.
	23	0	Sets the polarity of the T_x phase detector charge pump output for an inverting low pass filter/VCO combination.
8	23 – 0	$000000	Code word for the T_x Data Register is entered into this register.
9	23 – 0	$000000	Data word for the T_x Data Register is entered into this register.
10	23 – 0	$000000	The data word received into the R_x Data Register is read out via the μP port from this register.

Table 13. Control Bit Listing (By Function)

PLL Controls

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	6 – 0	1000000	Sets the 7–bit T_x A counter for the T_x PLL.
1	19 – 7	10....0	Sets the 13–bit T_x N counter for the T_x PLL.
2	6 – 0	1000000	Sets the 7–bit R_x A' counter for the R_x PLL.
2	19 – 7	10....0	Sets the 13–bit R_x N' counter for the R_x PLL.
3	13 – 0	10....0	Sets the 14–bit counter for the 2nd LO.
4	11 – 0	$800	Sets the 12–bit counter for the PLL Reference Clock.
7	13	0	Sets the FT_x MC and FR_x MC output level to be from ground to V_{CC}. If this bit is 0, the output level is ±100 µA.

PLL Phase Detectors

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	20	0	Sets the T_x phase detector charge pump output current. 0 = ±100 µA, and 1 = ±400 µA.
2	20	0	Sets the R_x phase detector charge pump output current. 0 = ±100 µA, and 1 = ±400 µA.
3	14	0	Sets the LO2 phase detector charge pump output current. 0 = ±100 µA, and 1 = ±400 µA.
7	20 – 18	000	Selects the value of the internal capacitor between Pins 43 to 45, to fine tune the LO2 tank circuit. See Table 9.
7	21	0	Sets the polarity of the 2nd LO phase detector charge pump output for an inverting low pass filter/VCO combination.
7	22	0	Sets the polarity of the R_x phase detector charge pump output for an inverting low pass filter/VCO combination.
7	23	0	Sets the polarity of the T_x phase detector charge pump output for an inverting low pass filter/VCO combination.

CVSD Controls

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	22, 21	00	Sets CVSD Decoder minimum step size per Table 3.
2	22, 21	00	Sets CVSD Encoder minimum step size per Table 3.
3	16 – 15	11	Set the CVSD encoder/decoder for the selected clock rate. (Table 2)
4	23 – 18	100000	Sets the 6–bit counter to set the CVSD Encoder clock rate.
6	3	0	Selects the R_x 1010 Generator to the CVSD decoder.
6	4	0	Selects the T_x 1010 Generator to the scrambler.
7	14	0	Disables the CVSD charge compensation circuit, which affects idle channel performance.

Idle Channel Detector

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	14 – 11	0111	Sets the 4–bit idle channel counter to set the response delay for the idle channel detect circuit.
5	17 – 15	100	Sets the idle channel detect threshold level. See Table 4.
5	21	N/A	Indicates an idle channel condition has been detected (Output). This output is unaffected by bit 7/2.
7	2	0	Disables the automatic idle channel detect at the CVSD encoder. Bit 5/21 is still active.

Table 13. Control Bit Listing (By Function) (continued)

Data Transmission/Reception

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	19	0	Inverts Data Slicer output.
5	20	0	Sets Data Modem mode.
5	22	N/A	The Status Output (same as Pin 13) is read out from this bit. A logic 1 indicates the Data Detect register has detected a code word.
7	0	0	Bypass the Clock Recovery Block (Data slicer output goes directly to the descrambler).
7	3	0	Bypass the Data Detect block (Descrambler output goes directly to the CVSD Decoder).
7	11	1	Sets the code word size to be sent out via the T_x Data Register to 24 bits. If this bit is 0, the code word size is 16 bits.
7	12	1	Sets the data word size to be sent out via the T_x Data Register to 24 bits. If this bit is 0, the data word size is 16 bits.
8	23 – 0	$000000	Code word for the T_x Data Register is entered into this register.
9	23 – 0	$000000	Data word for the T_x Data Register is entered into this register.
10	23 – 0	$000000	The data word received into the R_x Data Register is read out via the µP port from this register.

Scrambler/Descrambler

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
7	1	0	Bypass the scrambler and descrambler.
7	10 – 8	010	Selects one of 8 programmable taps in the scrambler and descrambler. See Table 5.

Multi Purpose Pin Control

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
7	5 – 4	00	Determines the function for Pin 36 (MP1). See Table 6.
7	7 – 6	00	Determines the function for Pin 39 (MP2). See Table 7.

Audio Paths

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
4	17 – 12	100000	Sets the 6–bit counter for the Switched Capacitor Filter clock.
6	0	0	Mutes the power amplifiers (Pins 27 to 29).
6	1	0	Mutes the receive speech processing path (Pin 30).
6	2	0	Mutes the transmit speech processing path (Pin 22).
6	10 – 6	01111	Provides 19 steps, 1.5 dB each (28.5 dB range), of gain adjust in the receive speech audio path (Pins 32 to 30). See Table 8.
6	15 – 11	00100	Provides 4 steps of 4.0 dB each, of gain adjust in the transmit speech audio path (Pins 23 to 20).

Low Battery/Carrier Detection

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
3	20 – 17	0111	Adjusts the VB reference voltage (≈1.5 V) to improve low battery detection accuracy. Total adjustment range is ≈±9%.
3	23 – 21	011	Selects the threshold for Low Battery Detection or Carrier Signal Detection. See Table 10.
5	23	N/A	The output of the Low Battery/Carrier Detect Circuit is read from this bit.
6	5	0	Sets Carrier Detect Mode vs. Low Battery Mode

Table 13. Control Bit Listing (By Function) (continued)

Power Down Control

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	0	0	Power down the Reference Oscillator
5	1	0	Power down the T_x PLL.
5	2	0	Power down the R_x PLL.
5	3	0	Power down the LO2 PLL.
5	4	0	Power down the R_x Data Path. Includes Data Slicer, Clock Recovery, Descrambler, Data Detect, and Status circuits.
5	5	0	Power down the CVSD Decoder.
5	6	0	Power down the R_x Audio path (Pin 32 to 30). Includes AALPF, LPF, and Gain Adjust circuits.
5	7	0	Power down the Power Amplifiers (Pins 27, 28)
5	8	0	Power down the T_x Audio Path (Pin 25 to 22). Includes micro–phone amplifier, LPF, and Smoothing LPF circuits.
5	9	0	Power down the CVSD Encoder, Idle Channel Detector, 1010 Generator, T_x Data Register, and Scrambler circuits.
5	10	0	Power down the Low Battery/Carrier Detect Circuit.
5	18	0	Power down the Idle Channel Detection Circuit.

Table 14. Register Map

Register Address	Register Number	MSB 23	22	21	20	19	18	17	16	15	14	13	12
0001	1		CVSD Decoder Minimum Step Size		Tx PhDet. Curr. Sel.	13 Bit Tx N Counter Divide Value (Bits 19 – 7)							
0010	2		CVSD Encoder Minimum Step Size		Rx PhDet. Curr. Sel.	13 Bit Rx N' Counter Divide Value (Bits 19 – 7)							
0011	3	Sets Low Battery/Carrier Detect Threshold			Adjust VB Reference Voltage				Set CVSD for the selected Clock Rate		LO2 PhD Curr. Sel.	14 bit LO2 Counter Divide Value (Bits 13 – 0)	
0100	4	6 Bit Encode Clock Counter Divide Value						6 Bit Switched Capacitor Filter Counter Divide Value					
0101	5	LB/CD Det. Out	Status Output	Idle Chan. Output	Data Modem Mode	Invert Data Slicer	Idle Channel Disable	Sets Idle Channel Threshold Level			4 Bit Idle Channel Counter Delay Value (Bits 14 – 11)		
0110	6									Remote Gain Adjust (Bits 15 – 11)			
0111	7	Tx Phase Detector Polarity	Rx Phase Detector Polarity	LO2 Ph. Detector Polarity	LO2 Capacitor Select			Production Test Modes & Data Modem Mode			Idle Charge Disable	FTxMC/ FRxMC Level	Data Word Size (16/24 bit)
1000	8	16 or 24 Bit Code Word for the Tx Data Register (Bits 23 – 0)											
1001	9	16 or 24 Bit Data Word for the Tx Data Register (Bits 23 – 0)											
1010	10	16 or 24 Bit Data Word Output from the Rx Data Register (Bits 23 – 0)											

Register Address	Register Number	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0001	1	13 Bit Tx N Counter Divide Value (Bits 19 – 7)					7 Bit Tx A Counter Divide Value						
0010	2	13 Bit Rx N' Counter Divide Value (Bits 19 – 7)					7 Bit Rx A' Counter Divide Value						
0011	3	14 bit LO2 Counter Divide Value (Bits 13 – 0)											
0100	4	12 Bit Reference Counter Divide Value											
0101	5	4 Bit Idle Channel Ctr. Value	LB/CD Detect Disable	CVSD Encoder Disable	Tx Audio Path Disable	Power Amplifier Disable	Rx Audio Path Disable	CVSD Decoder Disable	Rx Data Path Disable	LO2 PLL Disable	Rx PLL Disable	Tx PLL Disable	Ref. Osc. Disable
0110	6	Remote Gain Adj.	Rx Audio Path Gain Adjust (28.5 dB range)					Set CD Mode	Tx 1010 Generator	Rx 1010 Generator	Mute Tx Audio	Mute Rx Audio	Mute Pwr. Amps
0111	7	Code Word Size (16/24 bit)	Scrambler/Descrambler Tap Selection			MP2 Mode (See Table 7)		MP1 Mode (See Table 6)		Bypass Data Detect	Disable Idle Chnl. Detection	Bypass Scrambler/ Descrambler	Bypass Clock Recovery
1000	8	16 or 24 Bit Code Word for the Tx Data Register (Bits 23 – 0)											
1001	9	16 or 24 Bit Data Word for the Tx Data Register (Bits 23 – 0)											
1010	10	16 or 24 Bit Data Word Output from the Rx Data Register (Bits 23 – 0)											

Note: Shaded areas represent output bits to be read out.

MOTOROLA

MC34016

Cordless Universal Telephone Interface

The MC34016 is a telephone line interface meant for use in cordless telephone base stations for CT0, CT1, CT2 and DECT. The circuit forms the interface towards the telephone line and performs all speech and line interface functions like dc and ac line termination, 2–4 wire conversion, automatic gain control and hookswitch control. Adjustment of transmission parameters is accomplished by two 8–bit registers accessible via the integrated serial bus interface and by external components.

- DC Masks for Voltage and Current Regulation
- Supports Passive or Active AC Set Impedance Applications
- Double Wheatstone Bridge Sidetone Architecture
- Symmetrical Inputs and Outputs with Large Signal Swing Capability
- Gain Setting and Mute Function for T_x and R_x Amplifiers
- Very Low Noise Performance
- Serial Bus Interface SPI Compatible
- Operation from 3.0 to 5.5 V

FEATURES

Line Driver Architecture

- Two DC Masks for Voltage Regulation
- Two DC Masks for Current Regulation
- Passive or Active Set Impedance Adjustment
- Double Wheatstone Bridge Architecture
- Automatic Gain Control Function

Transmit Channel

- Symmetrical Inputs Capable of Handling Large Voltage Swing
- Gain Select Option via Serial Bus Interface
- Transmit Mute Function, Programmable via Bus
- Large Voltage Swing Capability at the Telephone Line

Receive Channel

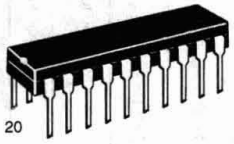
- Double Sidetone Architecture for Optimum Line Matching
- Symmetrical Outputs Capable of Producing High Voltage Swing
- Gain Select Option via Serial Bus Interface
- Receive Mute Function, Programmable via Serial Bus

Serial Bus Interface

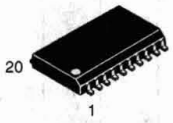
- 3–Wire Connection to Microcontroller
- One Programmable Output Meant for Driving a Hookswitch
- Two Programmable Outputs Capable of Driving Low Ohmic Loads
- Two 8–Bit Registers for Parameter Adjustment

CORDLESS UNIVERSAL TELEPHONE INTERFACE

SEMICONDUCTOR TECHNICAL DATA

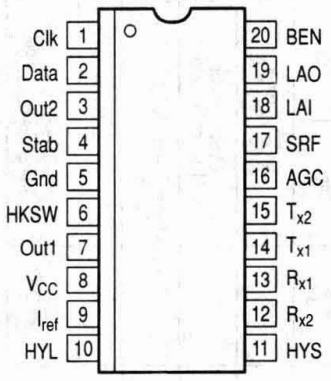


P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN CONNECTIONS

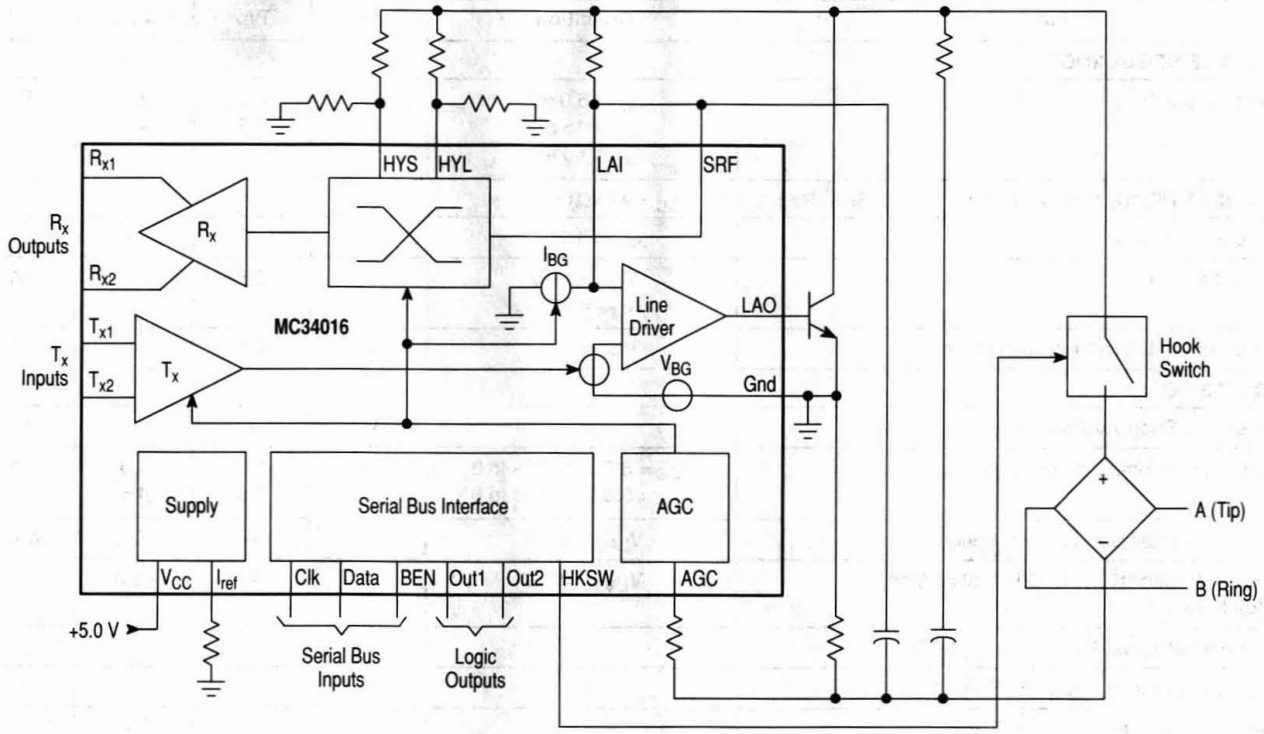


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34016P	T_A = –20° to +70°C	DIP
MC34016DW		SO–20

Representative Block Diagram



This device contains 610 active transistors + 242 gates.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operation Supply Voltage	V_{CC}	–0.5, 6.5	V
All Other Inputs	V_{in}	–0.5, V_{CC} +0.5	V
Operating Ambient Temperature	T_A	–20 to +70	°C
Junction Temperature	T_J	+150	°C

NOTE: ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
VOLTAGE REGULATION					
Line Voltage V_{line}	I_{line} = 5.0 mA I_{line} = 15 mA I_{line} = 60 mA	3.7 4.2 6.6	4.0 4.5 6.85	4.3 4.8 7.1	V
CURRENT REGULATION (Bit 4, Reg.1 = 1; Bit 1, Reg. 2 = 1; R_{AGC} = 47 kΩ)					
Line Voltage V_{line}	I_{line} = 15 mA	4.2	4.5	4.8	V
Line Current I_{line}	V_{line} = 10 V V_{line} = 35 V	– –	35 56	– –	mA
Line Current I_{line} in Protection Mode	V_{line} = 70 V	–	28	–	mA
DC BIASING					
Operating Supply Voltage V_{CC}	–	3.0	–	5.5	V
Current Consumption from V_{CC}	V_{CC} = 3.0 V, all Bits to 0 V_{CC} = 5.0 V, all Bits to 0	– –	3.0 3.5	4.0 4.5	mA
Source Capabiltiy Pin LAO in Speech Mode	V_{LAO} = 0.7 V	–	–	–2.0	mA
Source Capability Pin LAO in Dialing Mode (Bit 5, Reg. 1 = 1)	V_{LAO} = 0.7 V	–	–	–5.0	mA
Internal Pull Down Resistor at Pin LAO	–	–	11	–	kΩ
Bias Voltage at Pins HYL, HYS and LAI	–	–	1.3	–	V
Bias Voltage at Pins T_{x1} and T_{x2}	–	–	1.5	–	V
Bias Voltage at Pins R_{x1} and R_{x2}	–	–	1.3	–	V
LOGIC INPUTS					
Logic Low Level Pins Clk, Data, BEN	–	–	–	0.6	V
Logic High Level Pins Clk, Data, BEN	–	2.2	–	–	V
LOGIC OUTPUTS					
Source Capability from Pins HKSW, Out1, Out2	Output Voltage at V_{CC} – 1.3 V	–	–	–1.0	mA
Sink Capability into Pins HKSW, Out1, Out2	Output Voltage at 0.5 V	5.0	–	–	mA

AC ELECTRICAL CHARACTERISTICS (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
TRANSMIT CHANNEL					
Transmit Gain from VT_x to V_{line}	MC34016P MC34016DW VT_x = 0.1 Vrms	–1.0 –1.25	0.25 –0.20	1.5 0.85	dB
Gain Variation with Line Current Referred to I_{line} = 15 mA with the AGC Function Switched "Off"	I_{line} = 70 mA, Bit 0, Reg. 2 = 1	–0.7	–	0.7	dB
Gain Increase in 6.0 dB Mode	Bit 4, Reg. 2 = 1	5.3	6.0	6.7	dB
Gain Reduction in Mute Condition	Bit 2, Reg. 2 = 1	65	–	–	dB
Input Impedance at T_{x1} or T_{x2}	–	–	30	–	kΩ
Maximum Input Swing for VT_x	THD ≤ 2%	–	4.0	–	Vpp
THD at the Line (V_{line})	VT_x = 3.0 dBm	–	1.0	2.0	%
Psophometrically Weighted Noise Level at the Line (V_{line})	200 Ω Between T_{x1} and T_{x2}	–	–79	–	dBmp
RECEIVE CHANNEL					
Receive Gain from V_{line} to VR_x	V_{line} = 0.1 Vrms	–1.0	0	1.0	dB

AC ELECTRICAL CHARACTERISTICS (continued) (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
RECEIVE CHANNEL					
Gain Variation with Line Current Referred to I_{line} = 15 mA with the AGC Function Switched "Off"	I_{line} = 70 mA, Bit 0, Reg. 2 = 1	–0.7	–	0.7	dB
Gain Increase in 6.0 dB Mode	Bit 5, Reg. 2 = 1	5.3	6.0	6.7	dB
Gain Reduction in Mute Condition	Bit 3, Reg. 2 = 1	70	–	–	dB
Input Impedance at HYL or HYS	–	–	30	–	kΩ
Output Impedance at R_{x1} or R_{x2}	–	–	150	–	Ω
Maximum Input Swing at HYL or HYS	for THD ≤ 2%	–	800	–	mVpp
Maximum Output Swing VR_x	for THD ≤ 10%	–	3.5	–	Vpp
Total Harmonic Distortion at VR_x	V_{line} = 3.0 dBm	–	1.0	2.0	%
Psophometrically Weighted Noise Level at VR_x	200 Ω Between T_{x1} and T_{x2}	–	80	–	µVrms
AUTOMATIC GAIN CONTROL					
Gain Reduction in Transmit and Receive Channel with Respect to I_{line} = 15 mA	I_{line} = 70 mA	5.0	6.0	7.0	dB
Highest Line Current for Maximum Gain	–	–	20	–	mA
Lowest Line Current for Minimum Gain	–	–	60	–	mA
Gain Reduction in Transmit and Receive Channel with Respect to I_{line} = 35 mA	I_{line} = 85 mA, Bit 1, Reg. 2 = 1	5.0	6.0	7.0	dB
Highest Line Current for Maximum Gain	Bit 1, Reg. 2 = 1	–	40	–	mA
Lowest Line Current for Minimum Gain	Bit 1, Reg. 2 = 1	–	80	–	mA
BALANCE RETURN LOSS					
Balance Return Loss with Respect to 600Ω	f = 1.0 kHz	20	–	–	dB
SIDETONE					
Voltage Gain from VT_x to VR_x	I_{line} = 15 mA, Bit 0, Reg. 2 = 1	–	–	–20	dB
SERIAL BUS					
Clock Frequency	–	–	–	550	kHz
BEN Rising Edge Setup Time Before First Clk Rising Edge	See t1 in Timing Diagram	500	–	–	ns
Data Setup Time Before Clk Rising Edge	See t2 in Timing Diagram	500	–	–	ns
Data Hold Time After Clk Rising Edge	See t3 in Timing Diagram	500	–	–	ns
BEN Falling Edge Delay Time After Last Clk Rising Edge	See t4 in Timing Diagram	1.5	–	–	µs
BEN Rising Edge Delay Time After Last BEN Falling Edge	See t5 in Timing Diagram	6.0	–	–	µs
Power Supply Reset Voltage V_{CC}	–	–	2.5	–	V

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Clk	Serial bus clock input
2	Data	Serial bus data input
3	Out2	Logic output 2
4	Stab	Line driver compensation
5	Gnd	Ground
6	HKSW	Logic output for the hook switch
7	Out1	Logic output 1
8	V_{CC}	Supply input (+5.0 V)
9	I_{ref}	Reference current adjustment
10	HYL	Hybrid input for long lines
11	HYS	Hybrid input for short lines
12	R_{x2}	Receive output 2
13	R_{x1}	Receive output 1
14	T_{x1}	Transmit input 1
15	T_{x2}	Transmit input 2
16	AGC	Automatic gain control input
17	SRF	Sidetone reference input
18	LAI	Line amplifier input
19	LAO	Line amplifier output
20	BEN	Serial bus enable input

DESCRIPTION OF THE CIRCUIT

Throughout this part, please refer to the typical application of Figure 10. The data given in this chapter refers to typical data of the characteristics.

DC OPERATION

For dc, the MC34016 incorporates four different masks which can be selected via the serial bus interface:

Bit 4, Reg. 1 'DC Mask'	Bit 5, Reg. 1 'DC Mode'	Bit 1, Reg. 2 'AGC Ratio'	DC Mask Selected
0	0	X	Voltage Regulation Mask
X	1	X	Pulse Dial Mask
1	0	0	Current Regulation Mask with AGC Ratio 1:2
1	0	1	Current Regulation Mask with AGC Ratio 3:5

X = don't care

Voltage Regulation Mask

The voltage regulation mask is the default setting of the MC34016 after power–up. In this mode, the circuit behaves as a zener with a series resistor. The line voltage can be expressed as:

$$V_{line} = V_{BG} + (I_{BG} \times R_{DC1}) + (I_{line} \times R_S)$$

with: V_{BG} =1.3 V

I_{BG} = 5.2 µA

R_{DC1} = DC setting resistor of 470 kΩ in the typical application

I_{line} = Line current

R_S = Slope resistor of 50 Ω in the typical application

thus: $V_{line} = 3.75 + (50 \times I_{line})$

By choosing different values of R_{DC1}, the zener voltage can be adjusted to fit country specific requirements. In Figure 1, a curve shows V_{line} versus I_{line} for different R_{DC1} values.

Pulse Dial Mask

In this mask, the circuit is forced into a very low voltage drop mode meant for pulse dialing (e.g. make period during pulse dialing). Pin LAO of the MC34016 sources a current of 5.0 mA in this mode, saturating output transistor Q1. The line voltage V_{line} is now determined by the saturation voltage of Q1 and the dc slope resistor R_S:

$$V_{line} = V_{CE(sat)Q1} + (R_S \times I_{line}) \cong 0.1 + (50 \times I_{line})$$

Figure 2 shows V_{line} versus I_{line}.

Current Regulation Masks

These masks are equal to the voltage regulation mask up to a knee current. Above this current, the dc slope changes to a higher value fulfilling requirements such as those in France.

$$V_{line} = 3.75 + (R_S \times I_{line}) \quad \text{for } I_{AGC} < I_{knee}$$

$$V_{line} = [I_{BG} + (2.5 \times (I_{AGC} - I_{knee}))] \times R_{DC1} + [V_{BG} + (R_S \times I_{line})] \quad \text{for } I_{AGC} > I_{knee}$$

with: $I_{AGC} = I_{line} \times \frac{R_S}{R_{AGC}}$

I_{knee} = 21 µA for AGC ratio 1:2
I_{knee} = 31 µA for AGC ratio 3:5

With R_S = 50 Ω and R_{AGC} = 47 kΩ, and the AGC ratio set to 3:5, I_{AGC} will equal I_{knee} at a line current of 29 mA. With the AGC ratio set to 1:2, the knee occurs at 20 mA. Above these line currents, it can be derived that the dc slope of the circuit changes to:

$$R_{Slope} = 2.5 \times \frac{R_S \times R_{DC1}}{R_{AGC}} + R_S$$

With the component values mentioned, a slope of 1300 Ω will occur. Figures 3 and 4 shows V_{line} versus I_{line} in the two current regulation masks for different values of R_{DC1}.

When I_{AGC} reaches 62 µA for AGC ratio 3:5 or 52 µA in case of AGC ratio 1:2, the MC34016 will enter protection mode after about 800 ms. In practice this mode occurs only under overload conditions. In protection mode, the MC34016 decreases the power dissipation in Q1 by drastically increasing the dc slope starting from I_{knee}. This results in a reduced line current which remains practically constant over line voltage. With the equation for Iagc it can be derived that:

AGC ratio	Line Current to Enter Protection Mode	Line Current in Protection Mode
3:5	58 mA	29 mA
1:2	49 mA	20 mA

Once the MC34016 enters protection mode, it remains there until the output HKSW is toggled via Bit 0 of Register 1 (on–hook, off–hook).

Supply Voltage V_{CC}

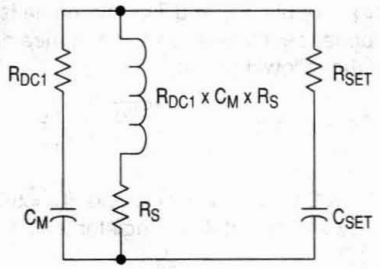
The MC34016 operates from an external supply within a voltage range of 3.0 to 5.5 V. The current consumption with all bits set to 0, equals 3.0 mA at 3.0 V and 3.5 mA at 5.5 V.

AC SET IMPEDANCE

The MC34016 offers two possibilities for the adjustment of the ac set impedance. Either a passive or an active set impedance can be obtained.

Passive Set Impedance

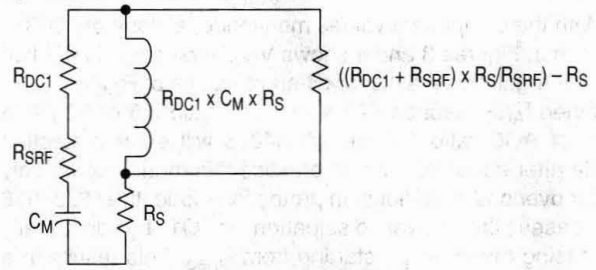
In this application, the set impedance is formed by the ac impedance of the circuit itself in parallel with resistor R_{SET} and capacitor C_{SET}. An equivalent network equals:



With the component values of the typical application, the inductor has a value of about 2.4 H and R_{DC1} equals 470 kΩ. In the audio range of 300–3400 Hz, these components form a fairly large parallel impedance to R_{SET} and C_{SET}. Therefore, the set impedance is mainly determined by the passive network R_{SET} and C_{SET}. In the typical application, R_{SET} is 600 Ω, but it can easily be replaced by a complex network to obtain a complex set impedance.

Active Set Impedance

An active set impedance can be obtained by placing a resistor between pin LAI and SRF (R_{SRF}) as shown in Figure 11. By doing so, the MC34016 itself generates the ac set impedance and R_{SET} and C_{SET} can be omitted. An equivalent network now equals:



Ignoring the effect of the inductor and the parallel path R_{DC1} + R_{SRF} again for audio frequencies, the set impedance is now determined by:

$$Z_{SET} = \frac{R_S}{R_{SRF}} \times (R_{DC1} + R_{SRF})$$

With R_S = 50 Ω and R_{DC1} = 470 kΩ, R_{SRF} should be 43 kΩ to obtain a 600 Ω set impedance. To obtain a complex set impedance, R_{DC1} can be made complex. In such case, the dc mask can be adjusted with the dc value of R_{DC1} and the set impedance can be adjusted with the ac value of R_{DC1}. An application with an active set impedance is interesting, particularly in countries like France, where with the dc current regulation mask, rather high line voltages can be reached. With a passive set impedance, this would result in a high cost for capacitor C_{SET}.

TRANSMIT CHANNEL

Inputs

The inputs T_{x1} and T_{x2} are designed to handle large signal levels of up to +3.0 dBm. The input impedance for both T_{x1} and T_{x2} equals 30 kΩ. The inputs are designed for symmetrical as well as asymmetrical use. In asymmetrical drive, one input can be tied to Gnd via an external capacitor.

Gain

The gain from inputs T_{x1} and T_{x2} to the line is dependent on the set impedance, the line load impedance and dc slope resistor R_S in the following way:

$$A_{TX} = \frac{1}{6 \times R_S} \times \frac{Z_{SET} \times Z_{line}}{Z_{SET} + Z_{line}}$$

With Z_{SET} = 600 Ω, Z_{line} = 600 Ω and R_S = 50 Ω the gain equals 0 dB. By setting Bit 4 of Register 2 to 1, the gain is raised by 6.0 dB.

Outputs

In order to transmit signals to the line, the output stage of the MC34016 (line driver) modulates the zener previously described. To guarantee stability of the output stage capacitor C_{STB} of 100 pF is required

SIDETONE

The MC34016 is equipped with a double Wheatstone bridge architecture to optimize sidetone. One sidetone network is used for short lines and one for long lines. Switchover between both networks is dependent on line current and is described in the automatic gain control section. Different sidetone equations apply depending on whether a passive or an active set impedance is set.

Sidetone Cancellation with Passive Set Impedance

In a passive set impedance application, the set impedance is a part of the equations for optimum sidetone. For short lines optimum cancellation occurs if:

$$Z_{HS1} = \frac{R_{HS2}}{R_S} \times \frac{Z_{SET} \times Z_{lineshort}}{Z_{SET} + Z_{lineshort}}$$

with: $Z_{lineshort}$ = impedance of a short telephone line

and for long lines:

$$Z_{HL1} = \frac{R_{HL2}}{R_S} \times \frac{Z_{SET} \times Z_{linelong}}{Z_{SET} + Z_{linelong}}$$

with: $Z_{linelong}$= impedance of a long telephone line

Sidetone Cancellation with Active Set Impedance

In the active set impedance application, the set impedance does not appear in the equations for optimum sidetone cancellation as it does in the passive application. For short lines, optimum cancellation occurs if:

$$Z_{HS1} = \frac{R_{HS2}}{R_S} \times Z_{lineshort}$$

and for long lines:

$$Z_{HL1} = \frac{R_{HL2}}{R_S} \times Z_{linelong}$$

RECEIVE CHANNEL

Inputs

The inputs HYS and HYL have an input resistance of 30 kΩ and can handle signals up to 800 mVpp. This corresponds to a signal at the telephone line of about 8.0 dBm in the typical application. The switchover from HYS to HYL is dependent on line current and described in the automatic gain control section.

Gain

The overall gain from the line to the outputs R_{x1} and R_{x2} for short lines and passive impedance equals:

$$A_{RX} = 7.6 \times \frac{R14'}{R14' + Z_{HYS}}$$

For active impedance it follows:

$$A_{RX} = 7.6 \times \frac{R14'}{R14' + Z_{HYS}} \times \left(1 + \frac{R1 \times Z_{HYS}}{R14 \times Z_{SET}}\right)$$

In these relations, R14′ is the resistor R14 in parallel with the input impedance at HYS of 30 kΩ. The gain for long

lines can be derived by replacing Z_{HYS} and R14 by Z_{HYL} and R17. With R14 = 3.0 kΩ and Z_{HYS} = 18 kΩ the receive gain equals 0 dB for the passive impedance application.

Outputs

The outputs R_{x1} and R_{x2} of the receive channel have an output impedance of 150 Ω and are designed to drive a 10 kΩ resistive load or a 47 nF capacitive load with a 3.5 Vpp swing.

AUTOMATIC GAIN CONTROL

The automatic gain control function (AGC) controls the transmit and receive gains and the switchover for the sidetone networks for short and long lines according to the line current (which represents line length). The effect of AGC on the transmit and receive amplifiers is 6.0 dB at default and it can be disabled via the serial bus. The switchover for the sidetone networks tracks the AGC curves for the transmit and receive amplifier gain. This feature can also be disabled via the serial bus:

Bit 6, Reg. 2 'PABX Mode'	Bit 0, Reg. 2 'AGC Range'	Description
0	0	AGC Gain Range of 6.0 dB, Sidetone Switchover Enabled
0	1	No AGC Gain Range, Sidetone Switchover Enabled
1	0	AGC Range of 6.0 dB, only HYS Input Active, HYL Muted
1	1	No AGC Gain Range, only HYS Input Active, HYL Muted

The ratio between start and stop current for the AGC curves is programmable for both voltage and current regulation mode:

Bit 4, Reg. 1 'DC Mask'	Bit 1, Reg. 2 'AGC Ratio'	AGC Ratio Selected	$I_{AGCstart}$ (μA)	$I_{AGCstop}$ (μA)
0	0	Voltage Regulation, AGC Ratio 1:3	10	31
0	1	Voltage Regulation, AGC Ratio 1:2	21	42
1	0	Current Regulation, AGC Ratio 1:2	21	42
1	1	Current Regulation, AGC Ratio 3:5	31	52

The relation between line current and I_{start} and I_{stop} is given by:

$$I_{linestart} = \frac{R_{AGC}}{R_S} \times I_{AGCstart}$$

$$I_{linestop} = \frac{R_{AGC}}{R_S} \times I_{AGCstop}$$

Figures 5, 6, 7 and 8 show the AGC curves for both voltage regulation and current regulation. In current regulation, the start point for the AGC curves is coupled to the knee point of the dc characteristic, or: $I_{knee} = I_{AGCstart}$.

LOGIC OUTPUT DRIVERS

The MC34016 is equipped with three logic outputs meant to interface to the front end of a telephone. The outputs can be controlled via the serial bus interface. As shown in the characteristics, the logic outputs are capable of sourcing at least 1.0 mA and sinking at least 5.0 mA.

Output HKSW

Output HKSW is dedicated to drive the hookswitch. With HKSW low, the line is opened via Q2 and Q3 and automatically switches off the line driver transistor Q1. This feature guarantees fast dc settling after line breaks occurring during pulse dialing.

Outputs Out1 and Out2

Outputs Out1 and Out2 may be used for any logic function, such as control of an earth switch and/or a shunt wire.

SERIAL BUS INTERFACE

The serial interface of the MC34016 enables a simple three wire connection to a micro controller.

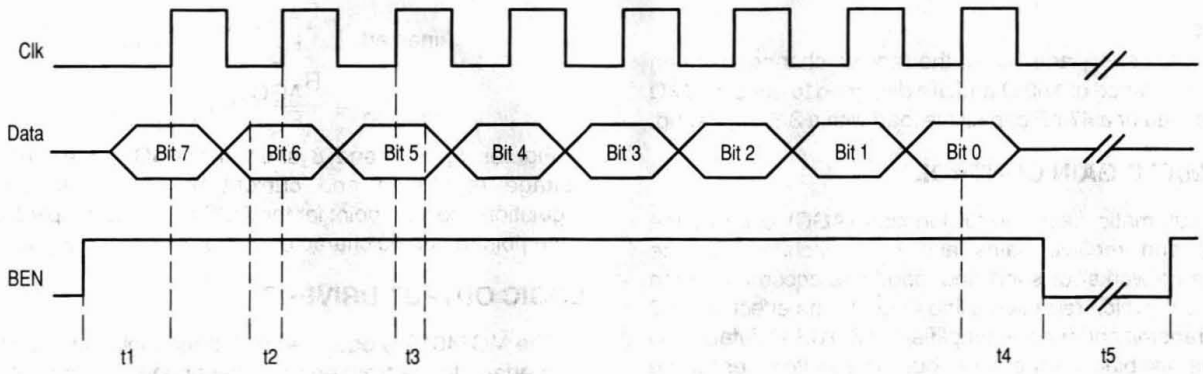
Timing

Times t1, t2, t3, t4 and t5 are specified in the electrical characteristics.

With BEN high, data can be clocked into the serial port by using Data and Clk lines. On the rising edge of the Clk, the data enters the MC34016. The last 8–bits of data entered are shifted into the registers when BEN is forced low. With BEN low, the serial port of the MC34016 is disabled. BEN must be kept low until the next register update is needed. Data should be written by entering the most significant bit first (Bit 7) and the least significant bit (Bit 0) last.

With BEN low, the Data and Clk lines may be used to control other devices in the application.

Timing Diagram



Registers

The MC34016 is equipped with two 8–bit registers which are selected by the value of the most significant bit (Bit 7). If the supply voltage of the MC34016 drops below 2.5 V, all registers are set to 0. This RESET function enables a smooth power–up of the device. The registers are as follows:

Register 1 (Bit 7 = 0)

Bit	Function	Operation	Default
0	Output HKSW	0: HKSW is Low 1: HKSW is High	0
1	Output Out1	0: Out1 is Low 1: Out1 is High	0
2	Output Out2	0: Out2 is Low 1: Out2 is High	0
3	Not Used	–	–
4	DC Mask	0: Voltage Regulation Mask 1: Current Regulation Mask for France	0
5	DC Mode	0: Speech Mode/Normal Operation 1: Dialing Mode for Low Voltage Drop	0
6	Test Mode	Only Used During Manufacturing	0

Register 2 (Bit 7 = 1)

Bit	Function	Operation		Default
0	AGC Range	0: AGC Range 6.0 dB 1: AGC Range 0 dB (Switched "Off")		0
1	AGC Ratio	Voltage Regulation: (Bit 4, Reg. 1 = 0) 0: Ratio 1:3 1: Ratio 1:2	Current Regulation: (Bit 4, Reg. 1 = 1) 0: Ratio 1:2 1: Ratio 3:5	0
2	Transmit Mute	0: Transmit Channel Active 1: Transmit Channel Muted		0
3	Receive Mute	0: Receive Channel Active 1: Receive Channel Muted		0
4	Transmit Gain	0: Transmit Channel Gain = 0 dB 1: Transmit Channel Gain = 6.0 dB		0
5	Receive Gain	0: Receive Channel Gain = 0 dB 1: Receive Channel Gain = 6.0 dB		0
6	PABX Mode	0: Normal Mode 1: PABX Mode (only Input HYS Selected)		0

Figure 1. Line Voltage versus Line Current
(Voltage Regulation Mask)

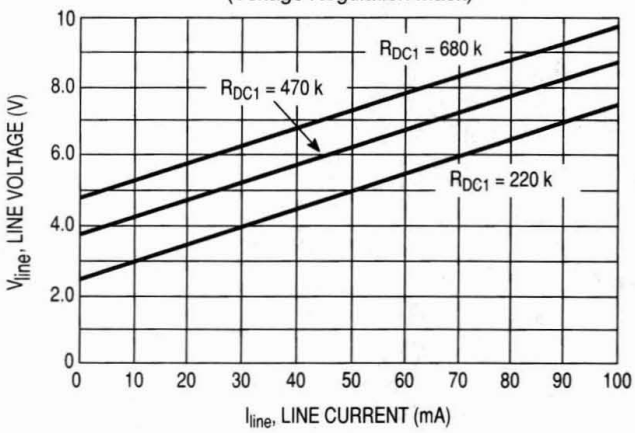


Figure 2. Line Voltage versus Line Current
(Pulse Dial Mask)

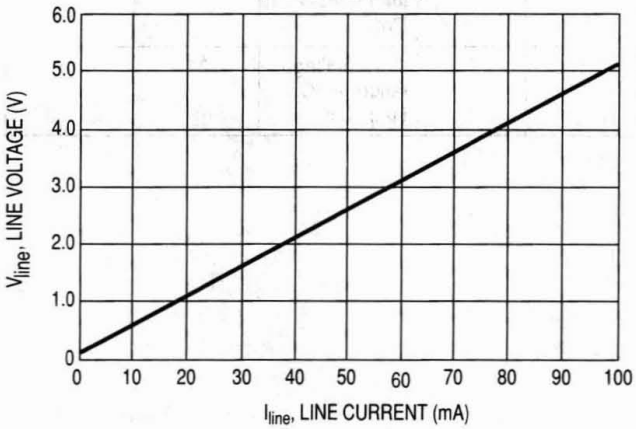


Figure 3. Line Voltage versus Line Current
(Current Regulation Mask)

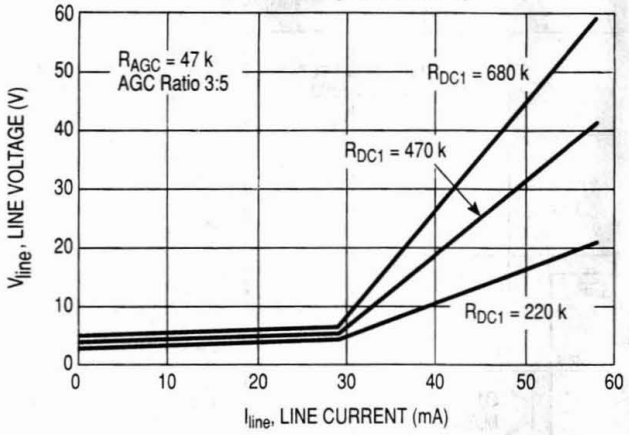


Figure 4. Line Voltage versus Line Current
(Current Regulation Mask)

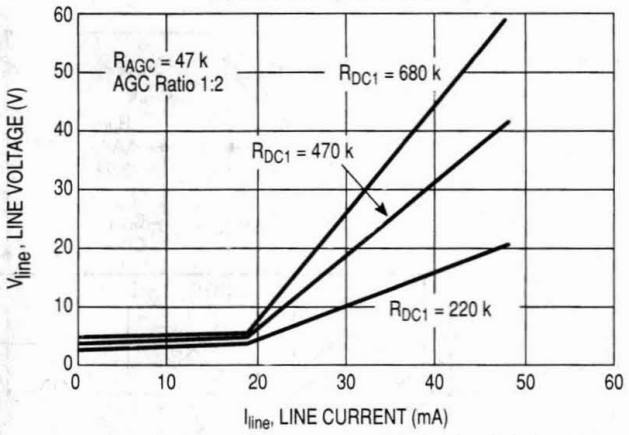


Figure 5. AGC Weighting Factor versus I_{line}
(Voltage Regulation Mask)

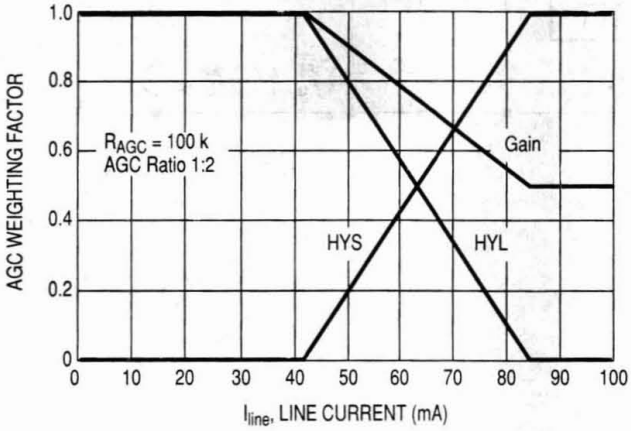


Figure 6. AGC Weighting Factor versus I_{line}
(Voltage Retulation Mask)

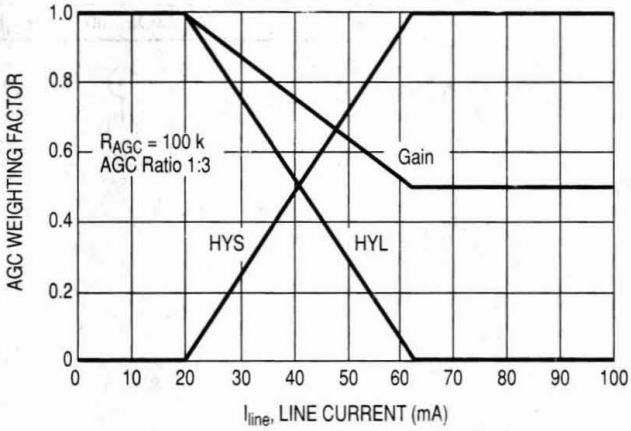


Figure 7. AGC Weighting Factor versus I_{line}
(Current Regulation Mask)

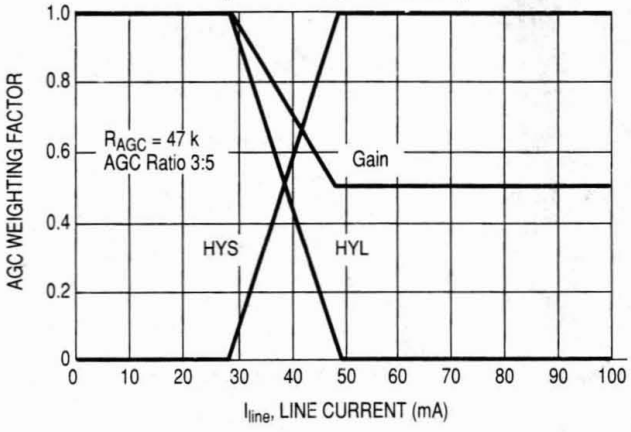


Figure 8. AGC Weighting Factor versus I_{line}
(Currrent Regulation Mask)

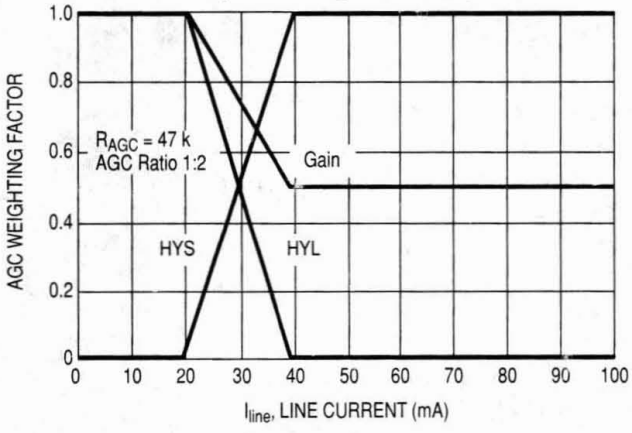


Figure 9. Test Diagram

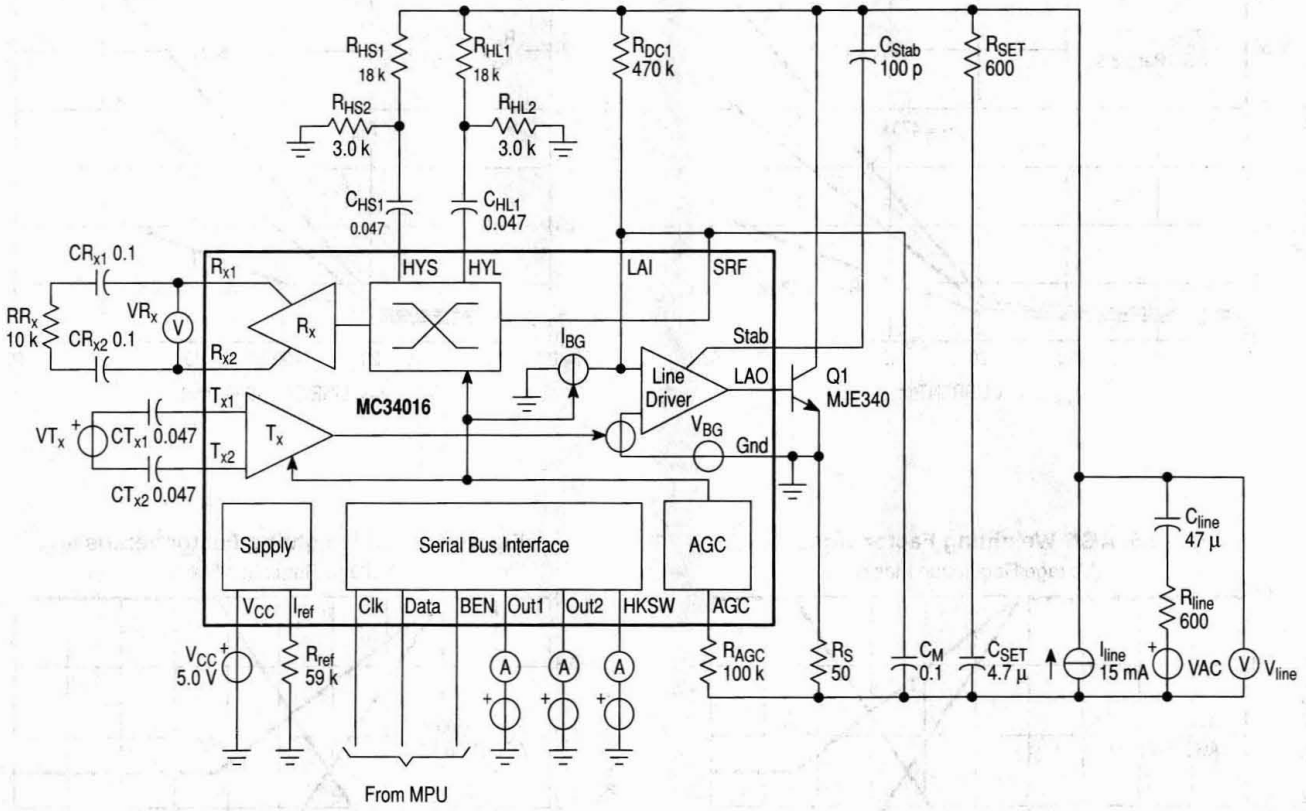
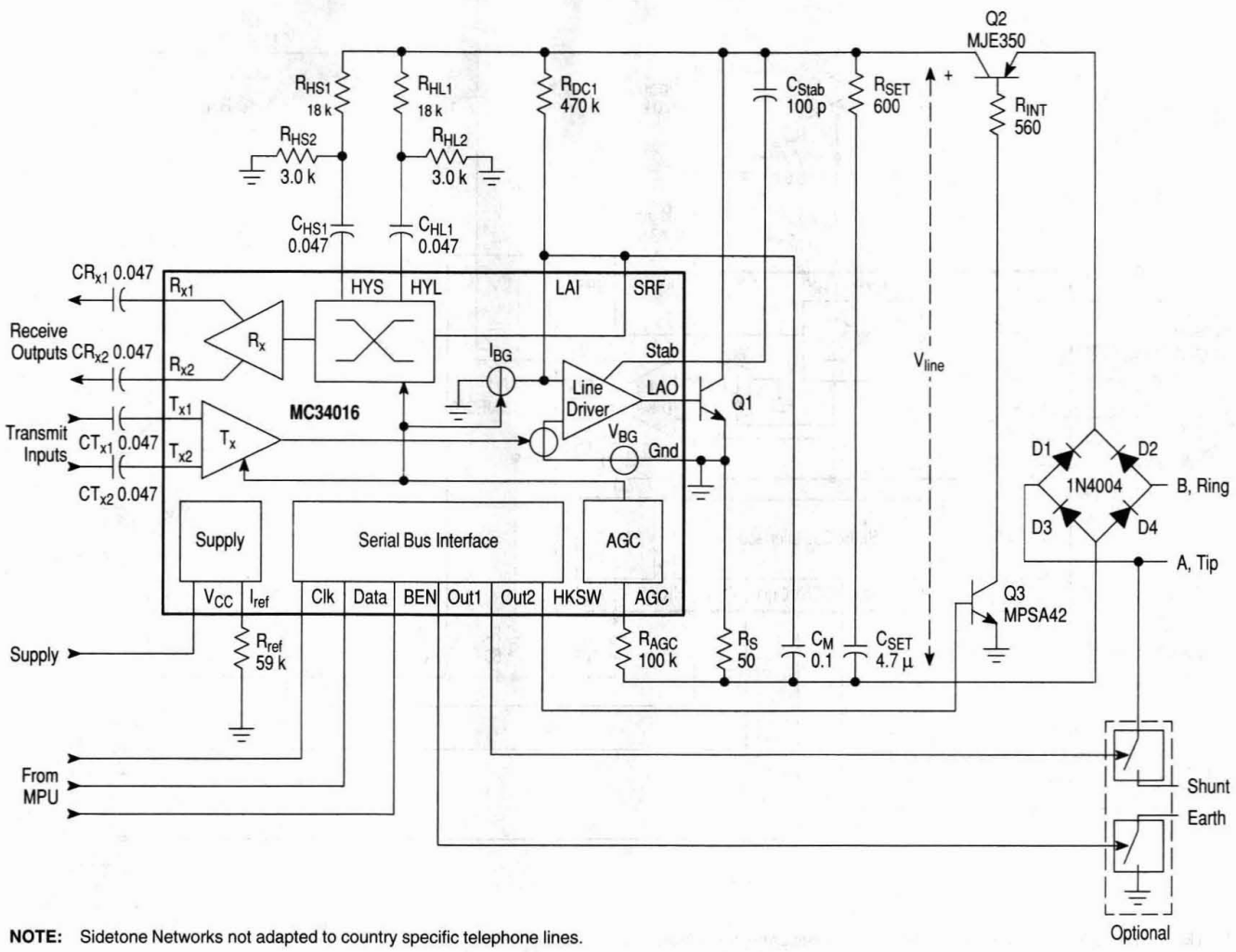
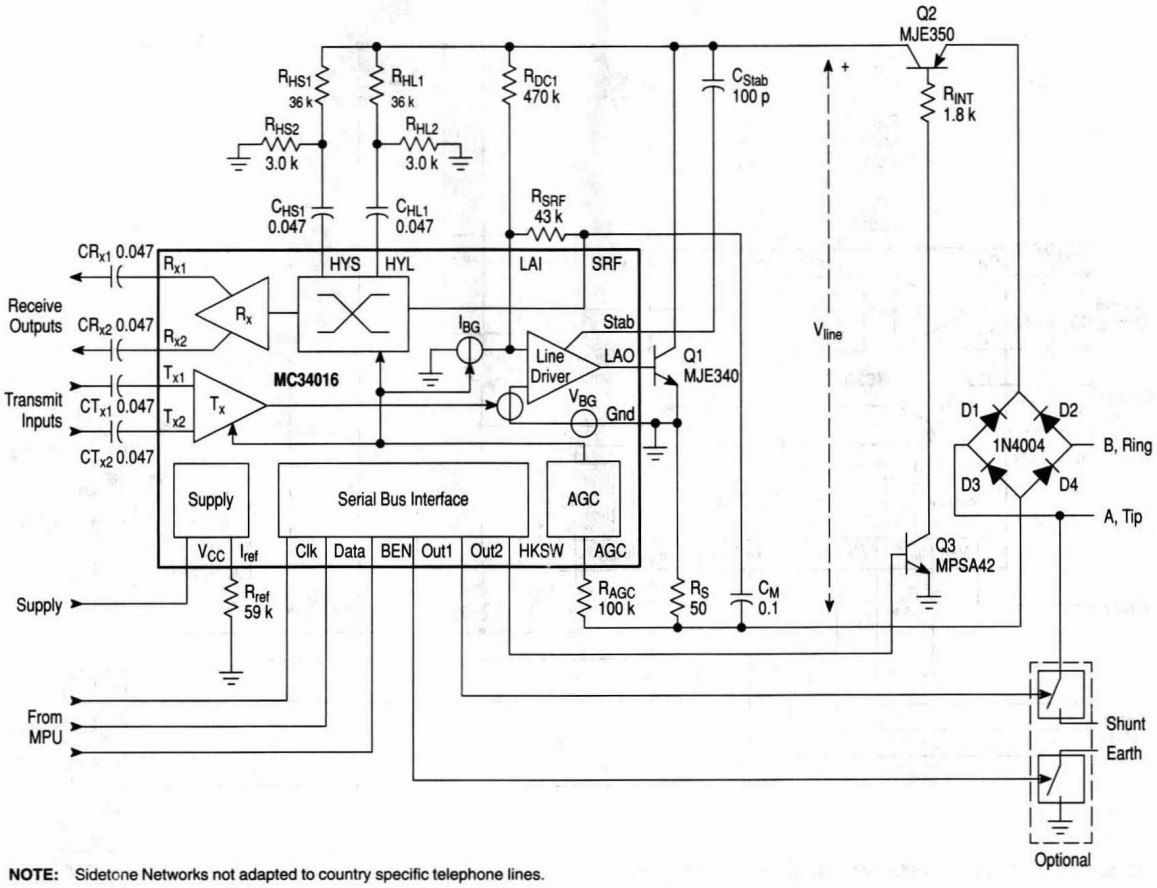


Figure 10. Typical Application with Passive Impedance and Voltage Regulation



NOTE: Sidetone Networks not adapted to country specific telephone lines.

Figure 11. Typical Application with Active Impedance and Current Regulation



NOTE: Sidetone Networks not adapted to country specific telephone lines.

Encoder and Decoder Pairs
CMOS

MC145026
MC145027
MC145028
SC41343
SC41344

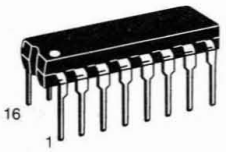
These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable ($\overline{TE}$) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

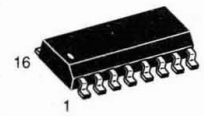
The MC145027 decoder receives the serial stream and interprets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpreted as four bits of binary data. The valid transmission (VT) output goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4 bits of data must match the last valid data received. The active VT indicates that the information at the Data output pins has been updated.

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The VT output goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

- Operating Temperature Range: – 40 to + 85°C
- Very–Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- RC Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ± 5% Components
- Internal Power–On Reset Forces All Decoder Outputs Low
- Operating Voltage Range: MC145026 = 2.5 to 18 V*
  MC145027, MC145028 = 4.5 to 18 V
- Low–Voltage Versions Available:
  SC41343 = 2.8 to 10 V Version of the MC145027
  SC41344 = 2.8 to 10 V Version of the MC145028
- For Infrared Applications, See Application Note AN1016/D



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

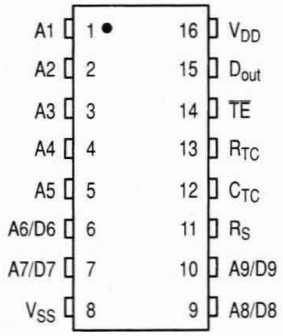
DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

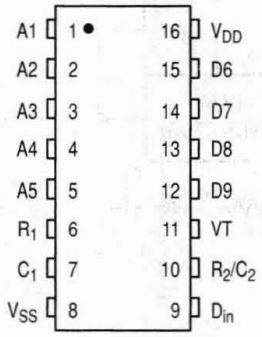
MC145026P	Plastic DIP
MC145026D	SOG Package
MC145027P, SC41343P	Plastic DIP
MC145027DW, SC41343DW	SOG Package
MC145028P, SC41344P	Plastic DIP
MC145028DW, SC41344DW	SOG Package

PIN ASSIGNMENTS

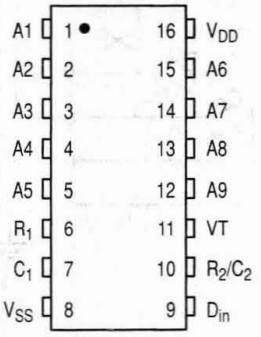
MC145026 ENCODER



MC145027/SC41343 DECODERS



MC145028/SC41344 DECODERS



* All MC145026 devices manufactured after date code 9314 or 314 are guaranteed over this wider voltage range. All previous designs using the low–voltage SC41342 should convert to the MC145026, which is a drop–in replacement. The SC41342 part number has been discontinued.

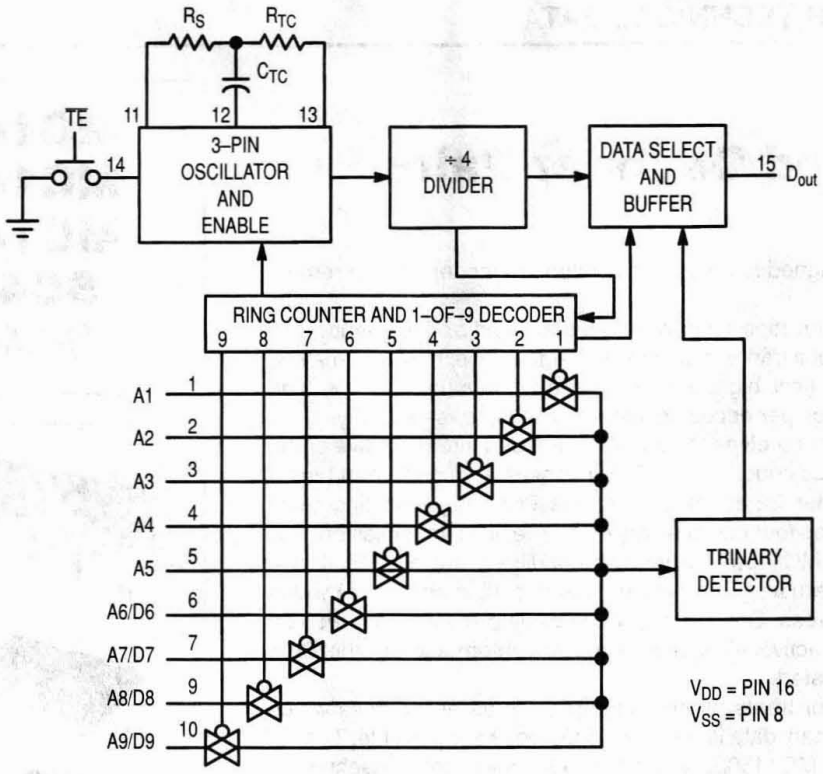


Figure 1. MC145026 Encoder Block Diagram

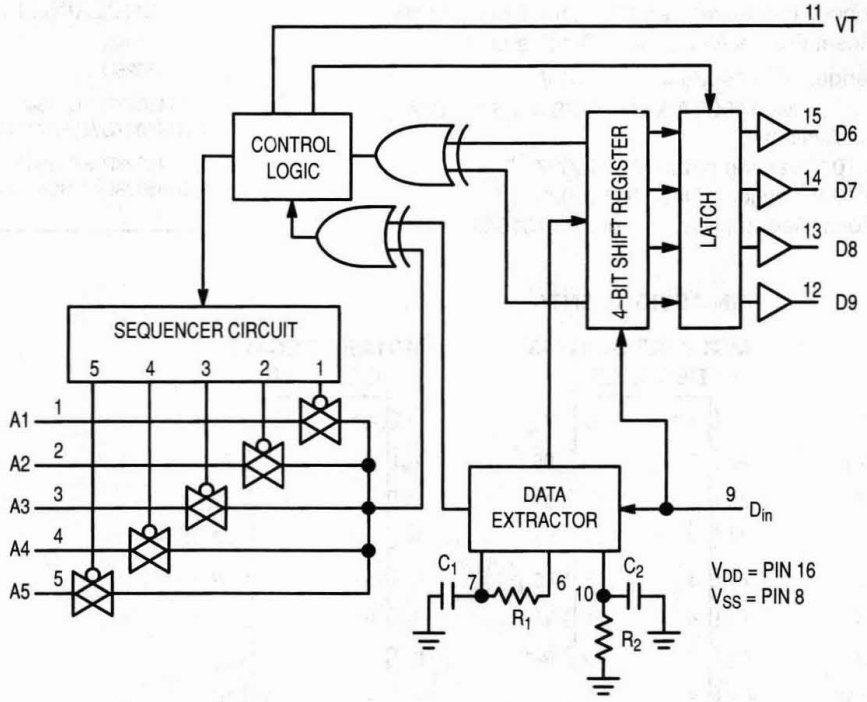


Figure 2. MC145027 Decoder Block Diagram

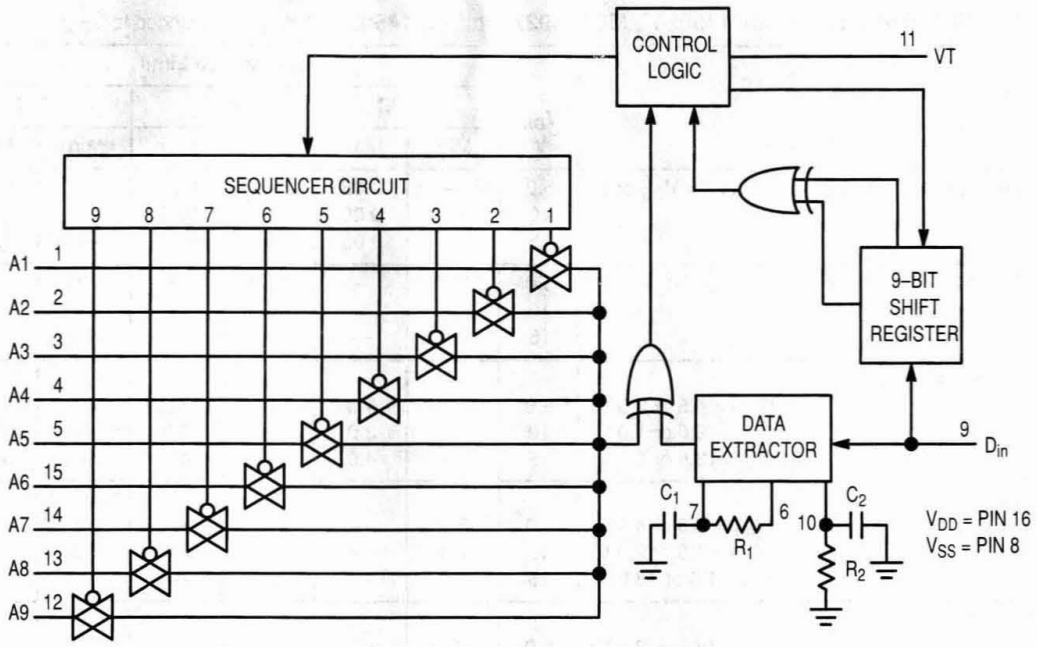


Figure 3. MC145028 Decoder Block Diagram

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
V_{DD}	DC Supply Voltage (except SC41343, SC41344)	– 0.5 to + 18	V
V_{DD}	DC Supply Voltage (SC41343, SC41344 only)	– 0.5 to + 10	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS — MC145026*, MC145027, and MC145028 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = V_{DD} or 0)	5.0	—	0.05	—	0.05	—	0.05	V
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{OH}	High–Level Output Voltage (V_{in} = 0 or V_{DD})	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
V_{IL}	Low–Level Input Voltage								V
	(V_{out} = 4.5 or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
	(V_{out} = 13.5 or 1.5 V)	15	—	4.0	—	4.0	—	4.0	
V_{IH}	High–Level Input Voltage								V
	(V_{out} = 0.5 or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
	(V_{out} = 1.5 or 13.5 V)	15	11	—	11	—	11	—	
I_{OH}	High–Level Output Current								mA
	(V_{out} = 2.5 V)	5.0	– 2.5	—	– 2.1	—	– 1.7	—	
	(V_{out} = 4.6 V)	5.0	– 0.52	—	– 0.44	—	– 0.36	—	
	(V_{out} = 9.5 V)	10	– 1.3	—	– 1.1	—	– 0.9	—	
	(V_{out} = 13.5 V)	15	– 3.6	—	– 3.0	—	– 2.4	—	
I_{OL}	Low–Level Output Current								mA
	(V_{out} = 0.4 V)	5.0	0.52	—	0.44	—	0.36	—	
	(V_{out} = 0.5 V)	10	1.3	—	1.1	—	0.9	—	
	(V_{out} = 1.5 V)	15	3.6	—	3.0	—	2.4	—	
I_{in}	Input Current — $\overline{TE}$	5.0	—	—	3.0	11	—	—	µA
	(MC145026, Pull–Up Device)	10	—	—	16	60	—	—	
		15	—	—	35	120	—	—	
I_{in}	Input Current	15	—	± 0.3	—	± 0.3	—	± 1.0	µA
	R_S (MC145026), D_{in} (MC145027, MC145028)								
I_{in}	Input Current								µA
	A1 – A5, A6/D6 – A9/D9 (MC145026),	5.0	—	—	—	± 110	—	—	
	A1 – A5 (MC145027),	10	—	—	—	± 500	—	—	
	A1 – A9 (MC145028)	15	—	—	—	± 1000	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current — MC145026	5.0	—	—	—	0.1	—	—	µA
		10	—	—	—	0.2	—	—	
		15	—	—	—	0.3	—	—	
I_{DD}	Quiescent Current — MC145027, MC145028	5.0	—	—	—	50	—	—	µA
		10	—	—	—	100	—	—	
		15	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current — MC145026	5.0	—	—	—	200	—	—	µA
	(f_c = 20 kHz)	10	—	—	—	400	—	—	
		15	—	—	—	600	—	—	
I_{dd}	Dynamic Supply Current — MC145027, MC145028	5.0	—	—	—	400	—	—	µA
	(f_c = 20 kHz)	10	—	—	—	800	—	—	
		15	—	—	—	1200	—	—	

* Also see next Electrical Characteristics table for 2.5 V specifications.

ELECTRICAL CHARACTERISTICS — MC145026 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	—	0.05	—	0.05	—	0.05	V
V_{OH}	High–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	2.45	—	2.45	—	2.45	—	V
V_{IL}	Low–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	—	0.3	—	0.3	—	0.3	V
V_{IH}	High–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	2.2	—	2.2	—	2.2	—	V
I_{OH}	High–Level Output Current (V_{out} = 1.25 V)	2.5	0.28	—	0.25	—	0.2	—	mA
I_{OL}	Low–Level Output Current (V_{out} = 0.4 V)	2.5	0.22	—	0.2	—	0.16	—	mA
I_{in}	Input Current ($\overline{TE}$ — Pull–Up Device)	2.5	—	—	0.09	1.8	—	—	µA
I_{in}	Input Current (A1–A5, A6/D6–A9/D9)	2.5	—	—	—	± 25	—	—	µA
I_{DD}	Quiescent Current	2.5	—	—	—	0.05	—	—	µA
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.5	—	—	—	40	—	—	µA

ELECTRICAL CHARACTERISTICS — SC41343 and SC41344 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	—	0.05	—	0.05	—	0.05	V
		5.0	—	0.05	—	0.05	—	0.05	
		10	—	0.05	—	0.05	—	0.05	
V_{OH}	High–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	2.75	—	2.75	—	2.75	—	V
		5.0	4.95	—	4.95	—	4.95	—	
		10	9.95	—	9.95	—	9.95	—	
V_{IL}	Low–Level Input Voltage								V
	(V_{out} = 2.3 V or 0.5 V)	2.8	—	0.84	—	0.84	—	0.84	
	(V_{out} = 4.5 V or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 V or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
V_{IH}	High–Level Input Voltage								V
	(V_{out} = 0.5 V or 2.3 V)	2.8	1.96	—	1.96	—	1.96	—	
	(V_{out} = 0.5 V or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 V or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
I_{OH}	High–Level Output Current								mA
	(V_{out} = 1.4 V)	2.8	– 0.73	—	– 0.7	—	– 0.55	—	
	(V_{out} = 4.5 V)	5.0	– 0.59	—	– 0.5	—	– 0.41	—	
	(V_{out} = 9.0 V)	10	– 1.3	—	– 1.1	—	– 0.9	—	
I_{OL}	Low–Level Output Current								mA
	(V_{out} = 0.4 V)	2.8	0.35	—	0.3	—	0.24	—	
	(V_{out} = 0.5 V)	5.0	0.8	—	0.6	—	0.4	—	
	(V_{out} = 1.0 V)	10	3.5	—	2.9	—	2.3	—	
I_{in}	Input Current — D_{in}	10	—	± 0.3	—	± 0.3	—	± 1.0	µA
I_{in}	Input Current	2.8	—	—	—	± 30	—	—	µA
	A1 – A5 (SC41343)	5.0	—	—	—	± 140	—	—	
	A1 – A9 (SC41344)	10	—	—	—	± 600	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current	2.8	—	—	—	60	—	—	µA
		5.0	—	—	—	75	—	—	
		10	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.8	—	—	—	300	—	—	µA
		5.0	—	—	—	500	—	—	
		10	—	—	—	1000	—	—	

SWITCHING CHARACTERISTICS — MC145026*, MC145027, and MC145028 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4,8	5.0 10 15	— — —	200 100 80	ns
t_r	D_{in} Rise Time — Decoders	5	5.0 10 15	— — —	15 15 15	µs
t_f	D_{in} Fall Time — Decoders	5	5.0 10 15	— — —	15 5.0 4.0	µs
f_{osc}	Encoder Clock Frequency	6	5.0 10 15	0.001 0.001 0.001	2.0 5.0 10	MHz
f	Decoder Frequency — Referenced to Encoder Clock	12	5.0 10 15	1.0 1.0 1.0	240 410 450	kHz
t_w	$\overline{TE}$ Pulse Width — Encoders	7	5.0 10 15	65 30 20	— — —	ns

* Also see next Switching Characteristics table for 2.5 V specifications.

SWITCHING CHARACTERISTICS — MC145026 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.5	—	450	ns
f_{osc}	Encoder Clock Frequency	6	2.5	1.0	250	kHz
t_w	$\overline{TE}$ Pulse Width	7	2.5	1.5	—	µs

SWITCHING CHARACTERISTICS — SC41343 and SC41344 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.8 5.0 10	— — —	320 200 100	ns
t_r	D_{in} Rise Time	5	2.8 5.0 10	— — —	15 15 15	µs
t_f	D_{in} Fall Time	5	2.8 5.0 10	— — —	15 15 5.0	µs
f	Decoder Frequency — Referenced to Encoder Clock	12	2.8 5.0 10	1.0 1.0 1.0	100 240 410	kHz

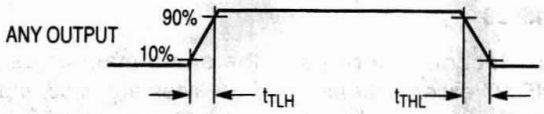


Figure 4.

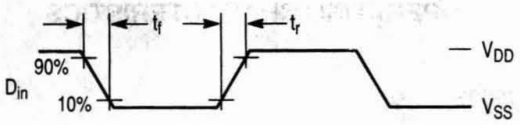


Figure 5.

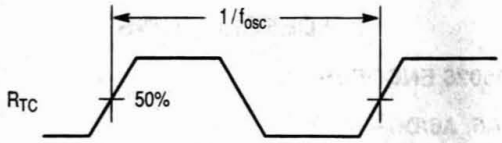


Figure 6.

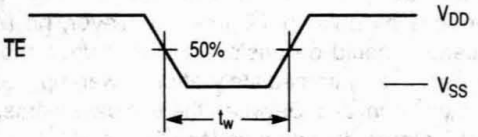
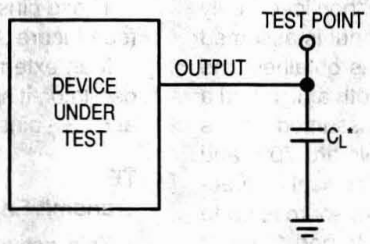


Figure 7.



* Includes all probe and fixture capacitance.

Figure 8. Test Circuit

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits trinary data as defined by the state of the A1 – A5 and A6/D6 – A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Upon power–up, the MC145026 can continuously transmit as long as $\overline{TE}$ remains low (also, the device can transmit two–word sequences by pulsing $\overline{TE}$ low). However, no MC145026 application should be designed to rely upon the first data word transmitted immediately after power–up because this word may be invalid. Between the two data words, no signal is sent for three data periods (see Figure 10).

Each transmitted trinary digit is encoded into pulses (see Figure 11). A logic 0 (low) is encoded as two consecutive short pulses, a logic 1 (high) as two consecutive long pulses, and an open (high impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak "output" device to try to force each input high then low. If only a high state results from the two tests, the input is assumed to be hardwired to V_{DD}. If only a low state is obtained, the input is assumed to be hardwired to V_{SS}. If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The "high" and "low" levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics table. The weak "output" device sinks/sources up to 110 μA at a 5 V supply level, 500 μA at 10 V, and 1 mA at 15 V.

The $\overline{TE}$ input has an internal pull–up device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high and the second–word transmission has timed out, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the D_{out} pin.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, the next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods (see Figure 10).

Although the address information may be encoded in trinary, the data information must be either a 1 or 0. A trinary (open) data line is decoded as a logic 1.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a VT output signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

PIN DESCRIPTIONS

MC145026 ENCODER

A1 – A5, A6/D6 – A9/D9
Address, Address/Data Inputs (Pins 1 – 7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the D_{out} pin.

R_S, C_{TC}, R_{TC}
(Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder (see Figure 9).

If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$
Transmit Enable (Pin 14)

This active–low transmit enable input initiates transmission when forced low. An internal pull–up device keeps this input normally high. The pull–up current is specified in the Electrical Characteristics table.

D_{out}
Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.

MC145027 AND MC145028 DECODERS

A1 – A5, A1 – A9
Address Inputs (Pins 1 – 5) — MC145027,
Address Inputs (Pins 1 – 5, 15, 14, 13, 12) — MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

D6 – D9
Data Outputs (Pins 15, 14, 13, 12) — MC145027 Only

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is

acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

D_{in}
Data In (Pin 9)

This pin is the serial data input to the decoder. The input voltage must be at CMOS logic levels. The signal source driving this pin must be dc coupled.

R_1, C_1
Resistor 1, Capacitor 1 (Pins 6, 7)

As shown in Figures 2 and 3, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant $R_1 \times C_1$ should be set to 1.72 encoder clock periods:

$$R_1 C_1 = 3.95 R_{TC} C_{TC}$$

R_2/C_2
Resistor 2/Capacitor 2 (Pin 10)

As shown in Figures 2 and 3, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder clock periods (four data periods per Figure 11): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time constant is used to determine whether the D_{in} pin has remained low for four data periods (end of transmission). A separate on–chip comparator looks at the voltage–equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

VT
Valid Transmission Output (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

1. the received addresses of both words match the local decoder address, and
2. the received data bits of both words match.

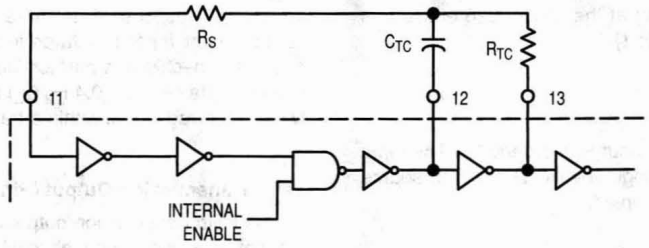
VT remains high until either a mismatch is received or no input signal is received for four data periods.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.



This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3\ R_{TC}\ C_{TC}'} \text{ (Hz)}$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC}' = C_{TC} + C_{layout} + 12$ pF

$R_S \approx 2\ R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF < C_{TC} < 15 µF

The value for R_S should be chosen to be ≥ 2 times R_{TC}. This range ensures that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that R_S x 5 pF (input capacitance) is small compared to R_{TC} x C_{TC}.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

Figure 9. Encoder Oscillator Information

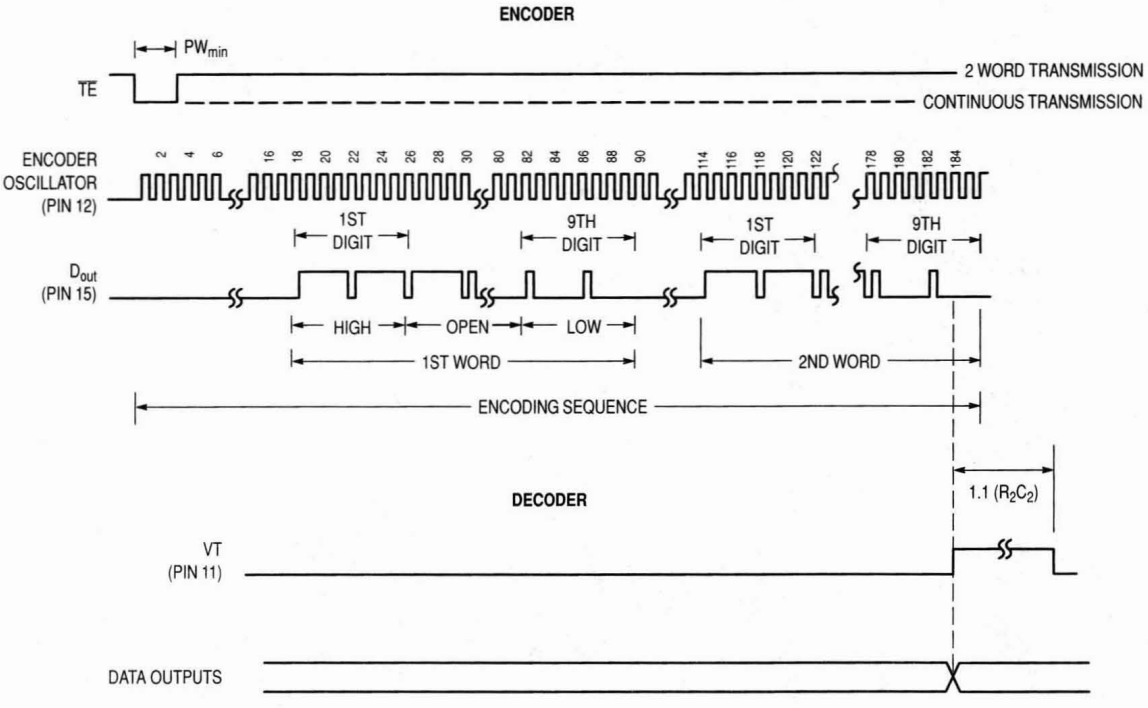


Figure 10. Timing Diagram

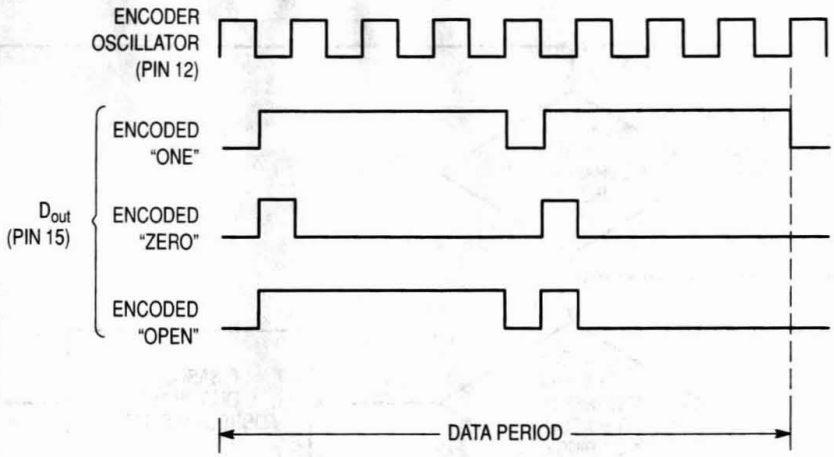


Figure 11. Encoder Data Waveforms

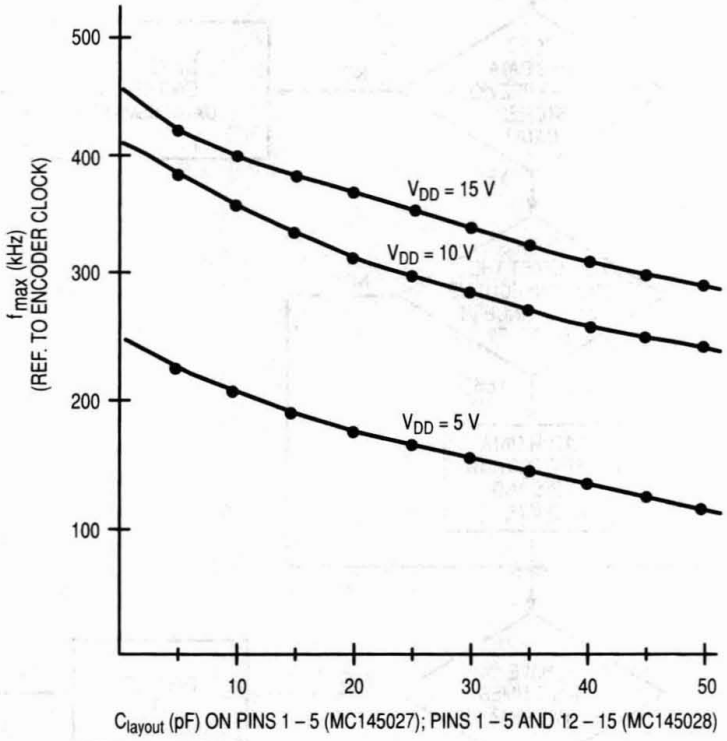


Figure 12. f_{max} vs C_{layout} — Decoders Only

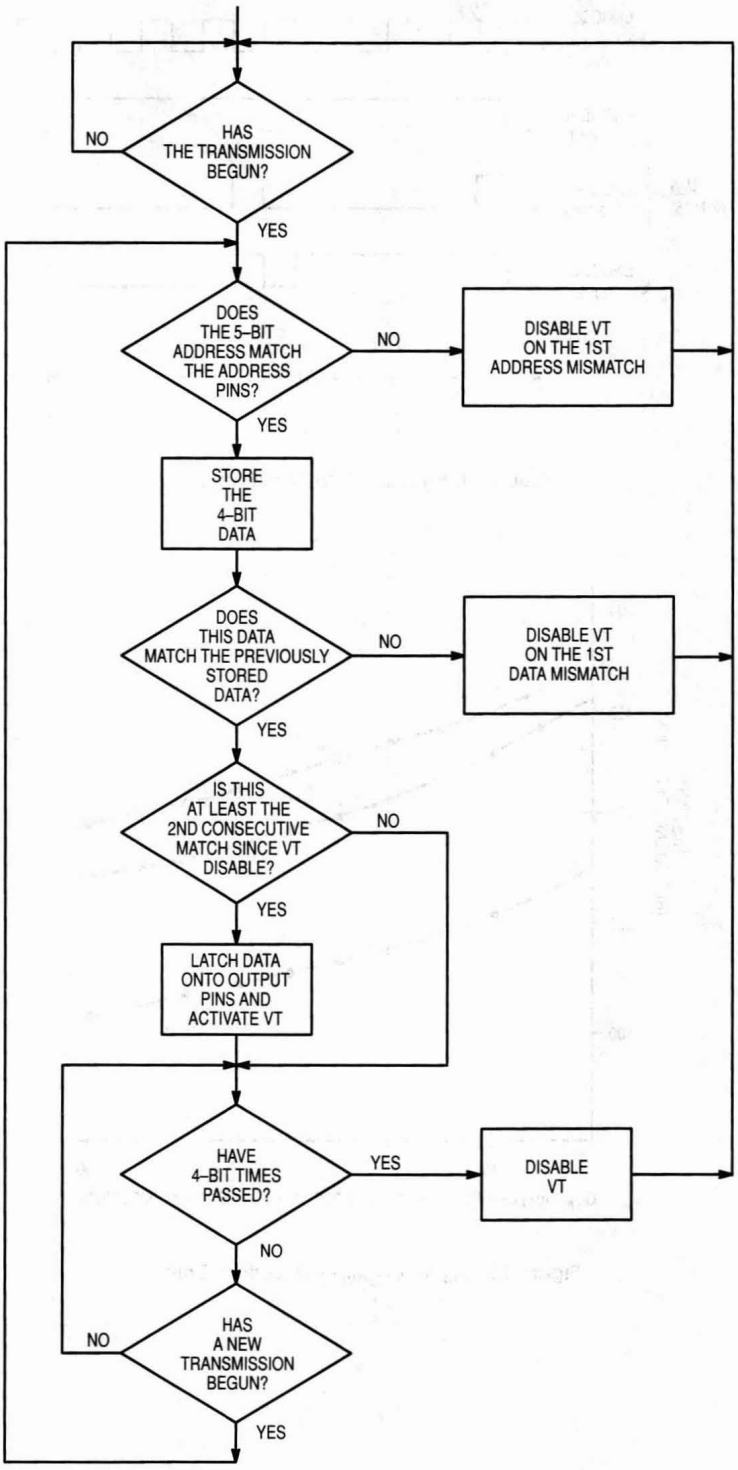


Figure 13. MC145027 Flowchart

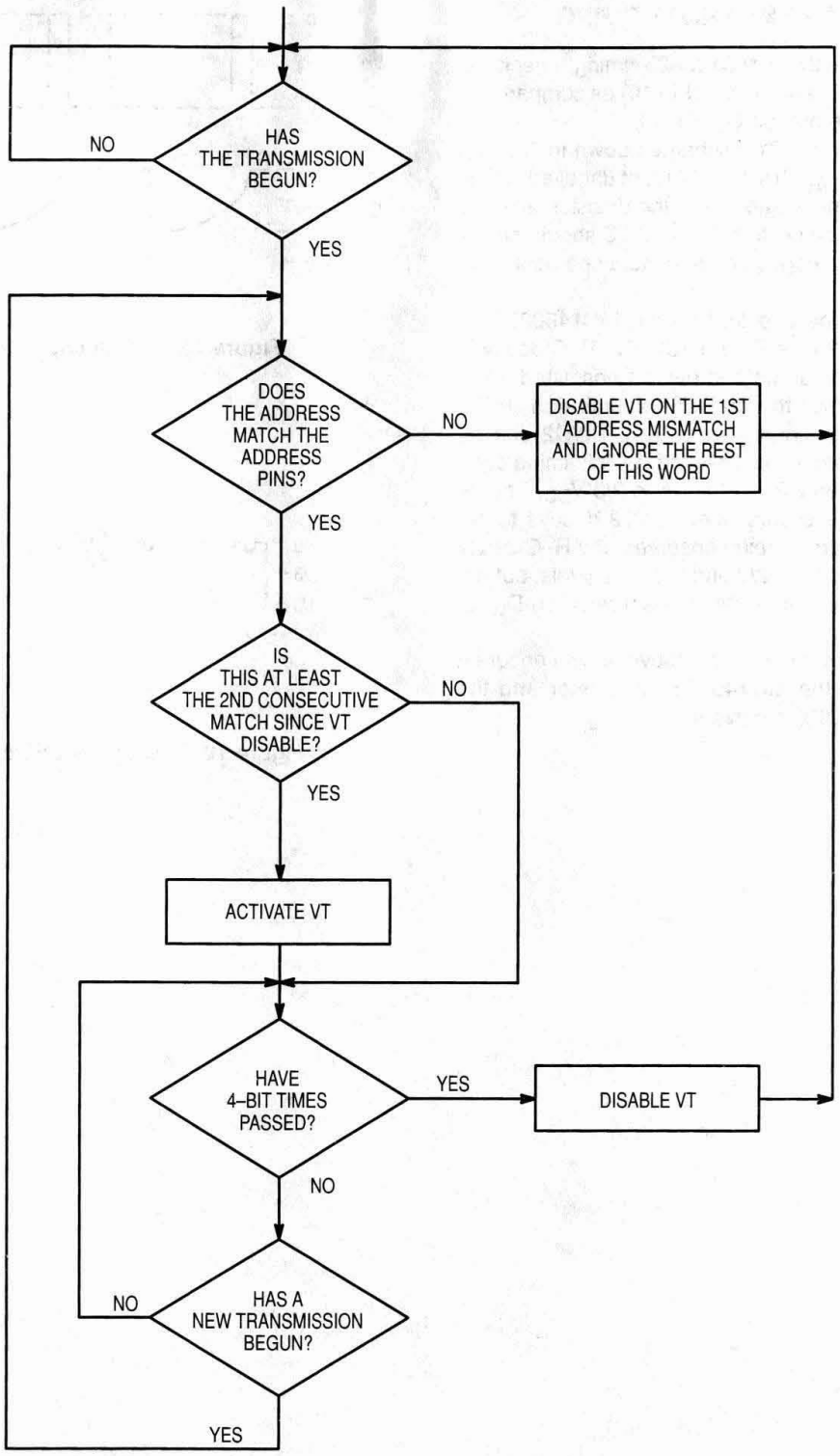


Figure 14. MC145028 Flowchart

MC145027 AND MC145028 TIMING

To verify the MC145027 or MC145028 timing, check the waveforms on C1 (Pin 7) and R2/C2 (Pin 10) as compared to the incoming data waveform on D_{in} (Pin 9).

The R–C decay seen on C1 discharges down to 1/3 V_{DD} before being reset to V_{DD}. This point of reset (labelled "DOS" in Figure 15) is the point in time where the decision is made whether the data seen on D_{in} is a 1 or 0. DOS should not be too close to the D_{in} data edges or intermittent operation may occur.

The other timing to be checked on the MC145027 and MC145028 is on R2/C2 (see Figure 16). The R–C decay is continually reset to V_{DD} as data is being transmitted. Only between words and after the end–of–transmission (EOT) does R2/C2 decay significantly from V_{DD}. R2/C2 can be used to identify the internal end–of–word (EOW) timing edge which is generated when R2/C2 decays to 2/3 V_{DD}. The internal EOT timing edge occurs when R2/C2 decays to 1/3 V_{DD}. When the waveform is being observed, the R–C decay should go down between the 2/3 and 1/3 V_{DD} levels, but not too close to either level before data transmission on D_{in} resumes.

Verification of the timing described above should ensure a good match between the MC145026 transmitter and the MC145027 and MC145028 receivers.

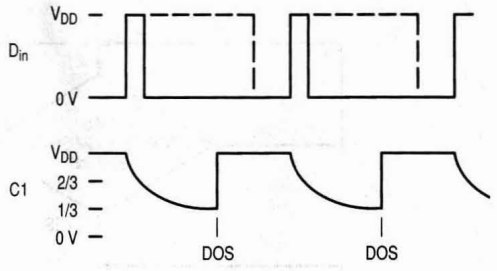


Figure 15. R–C Decay on Pin 7 (C1)

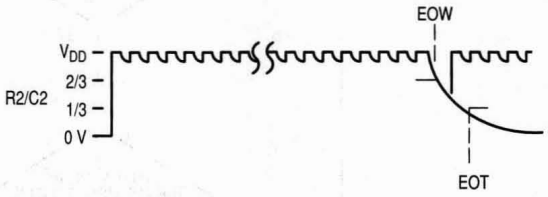
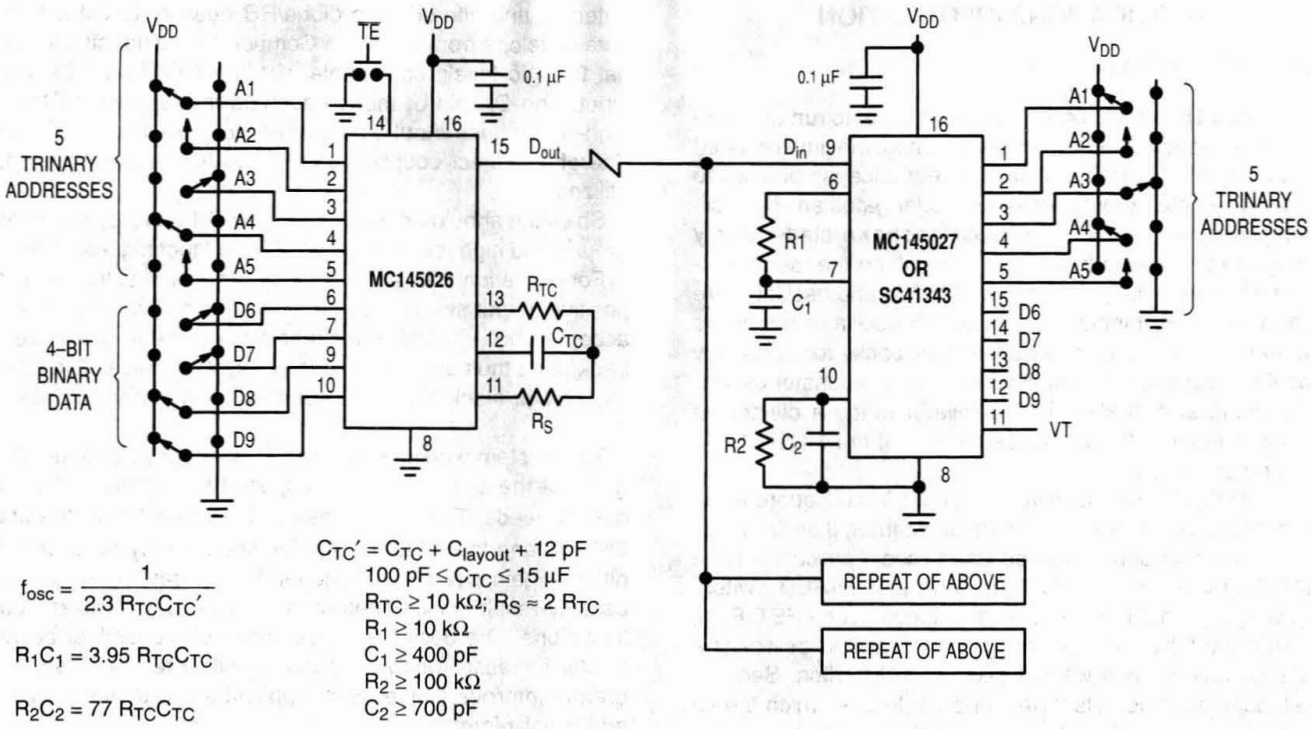


Figure 16. R–C Decay on Pin 10 (R2/C2)



$$f_{osc} = \frac{1}{2.3\ R_{TC}C_{TC'}}$$

$R_1C_1 = 3.95\ R_{TC}C_{TC}$

$R_2C_2 = 77\ R_{TC}C_{TC}$

$C_{TC'} = C_{TC} + C_{layout} + 12\ pF$

$100\ pF \le C_{TC} \le 15\ \mu F$

$R_{TC} \ge 10\ k\Omega$; $R_S \approx 2\ R_{TC}$

$R_1 \ge 10\ k\Omega$

$C_1 \ge 400\ pF$

$R_2 \ge 100\ k\Omega$

$C_2 \ge 700\ pF$

Example R/C Values (All Resistors and Capacitors are ± 5%)

($C_{TC'} = C_{TC} + 20\ pF$)

f_{osc} (kHz)	R_{TC}	$C_{TC'}$	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

Figure 17. Typical Application

APPLICATIONS INFORMATION

INFRARED TRANSMITTER

In Figure 18, the MC145026 encoder is set to run at an oscillator frequency of about 4 to 9 kHz. Thus, the time required for a complete two–word encoding sequence is about 20 to 40 ms. The data output from the encoder gates an RC oscillator running at 50 kHz; the oscillator shown starts rapidly enough to be used in this application. When the "send" button is not depressed, both the MC145026 and oscillator are in a low–power standby state. The RC oscillator has to be trimmed for 50 kHz and has some drawbacks for frequency stability. A superior system uses a ceramic resonator oscillator running at 400 kHz. This oscillator feeds a divider as shown in Figure 19. The unused inputs of the MC14011UB must be grounded.

The MLED81 IRED is driven with the 50 kHz square wave at about 200 to 300 mA to generate the carrier. If desired, two IREDs wired in series can be used (see Application Note AN1016 for more information). The bipolar IRED switch, shown in Figure 18, offers two advantages over a FET. First, a logic FET has too much gate capacitance for the MC14011UB to drive without waveform distortion. Second, the bipolar drive permits lower supply voltages, which are an advantage in portable battery–powered applications.

The configuration shown in Figure 18 operates over a supply range of 4.5 to 18 V. A low–voltage system which operates down to 2.5 V could be realized if the oscillator section of a MC74HC4060 is used in place of the MC14011UB. The data output of the MC145026 is inverted and fed to the RESET pin of the MC74HC4060. Alternately, the MC74HCU04 could be used for the oscillator.

Information on the MC14011UB is in book number DL131/D. The MC74HCU04 and MC74HC4060 are found in book number DL129/D.

INFRARED RECEIVER

The receiver in Figure 20 couples an IR–sensitive diode to input preamp A1, followed by band–pass amplifier A2 with a gain of about 10. Limiting stage A3 follows, with an output of about 800 mV p–p. The limited 50 kHz burst is detected by comparator A4 that passes only positive pulses, and peak–detected and filtered by a diode/RC network to extract the data envelope from the burst. Comparator A5 boosts the signal to logic levels compatible with the MC145027/28 data input. The D_{in} pin of these decoders is a standard CMOS high–impedance input which must ***not*** be allowed to float. Therefore, direct coupling from A5 to the decoder input is utilized.

Shielding should be used on at least A1 and A2, with good ground and high–sensitivity circuit layout techniques applied.

For operation with supplies higher than + 5 V, limiter A4's positive output swing needs to be limited to 3 to 5 V. This is accomplished via adding a zener diode in the negative feedback path, thus avoiding excessive system noise. The biasing resistor stack should be adjusted such that V3 is 1.25 to 1.5 V.

This system works up to a range of about 10 meters. The gains of the system may be adjusted to suit the individual design needs. The 100 Ω resistor in the emitter of the first 2N5088 and the 1 kΩ resistor feeding A2 may be altered if different gain is required. In general, more gain does not necessarily result in increased range. This is due to noise floor limitations. The designer should increase transmitter power and/or increase receiver aperature with Fresnal lensing to greatly improve range. See Application Note AN1016 for additional information.

Information on the MC34074 is in data book DL128/D.

TRINARY SWITCH MANUFACTURERS

Midland Ross–Electronic Connector Div.
Greyhill
Augat/Alcoswitch
Aries Electronics

The above companies may not have the switches in a DIP. For more information, call them or consult *eem Electronic Engineers Master Catalog* or the *Gold Book*. ***Ask for SPDT with center OFF.***

Alternative: An SPST can be placed in series between a SPDT and the Encoder or Decoder to achieve trinary action.

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of trinary switch manufacturers.

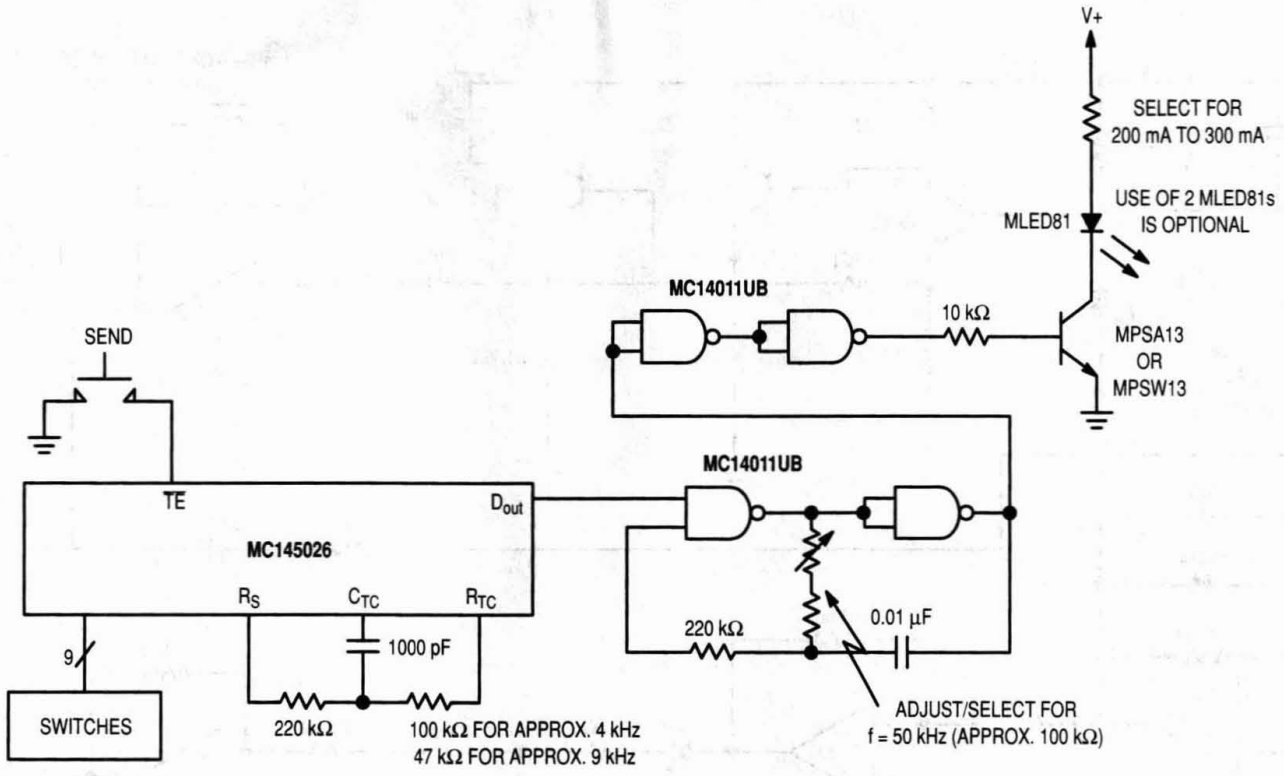


Figure 18. IRED Transmitter Using RC Oscillator to Generate Carrier Frequency

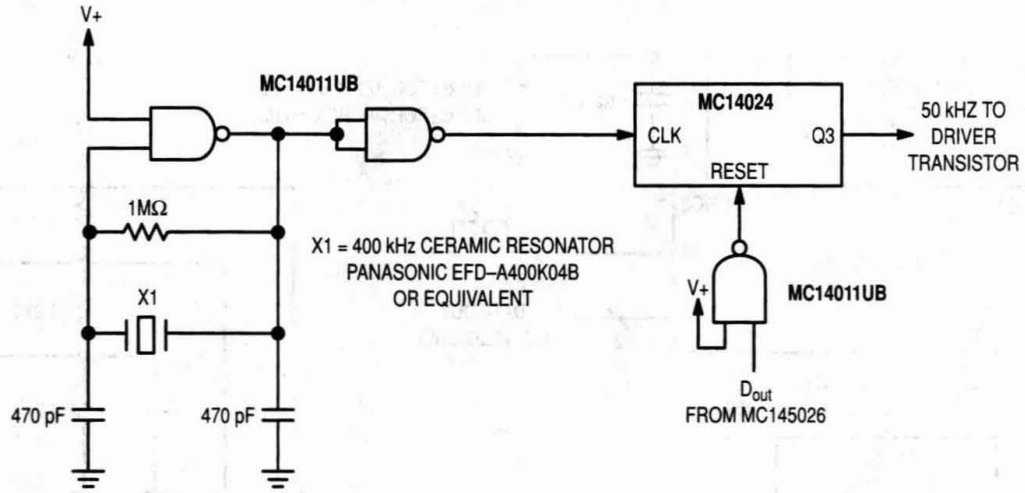


Figure 19. Using a Ceramic Resonator to Generate Carrier Frequency

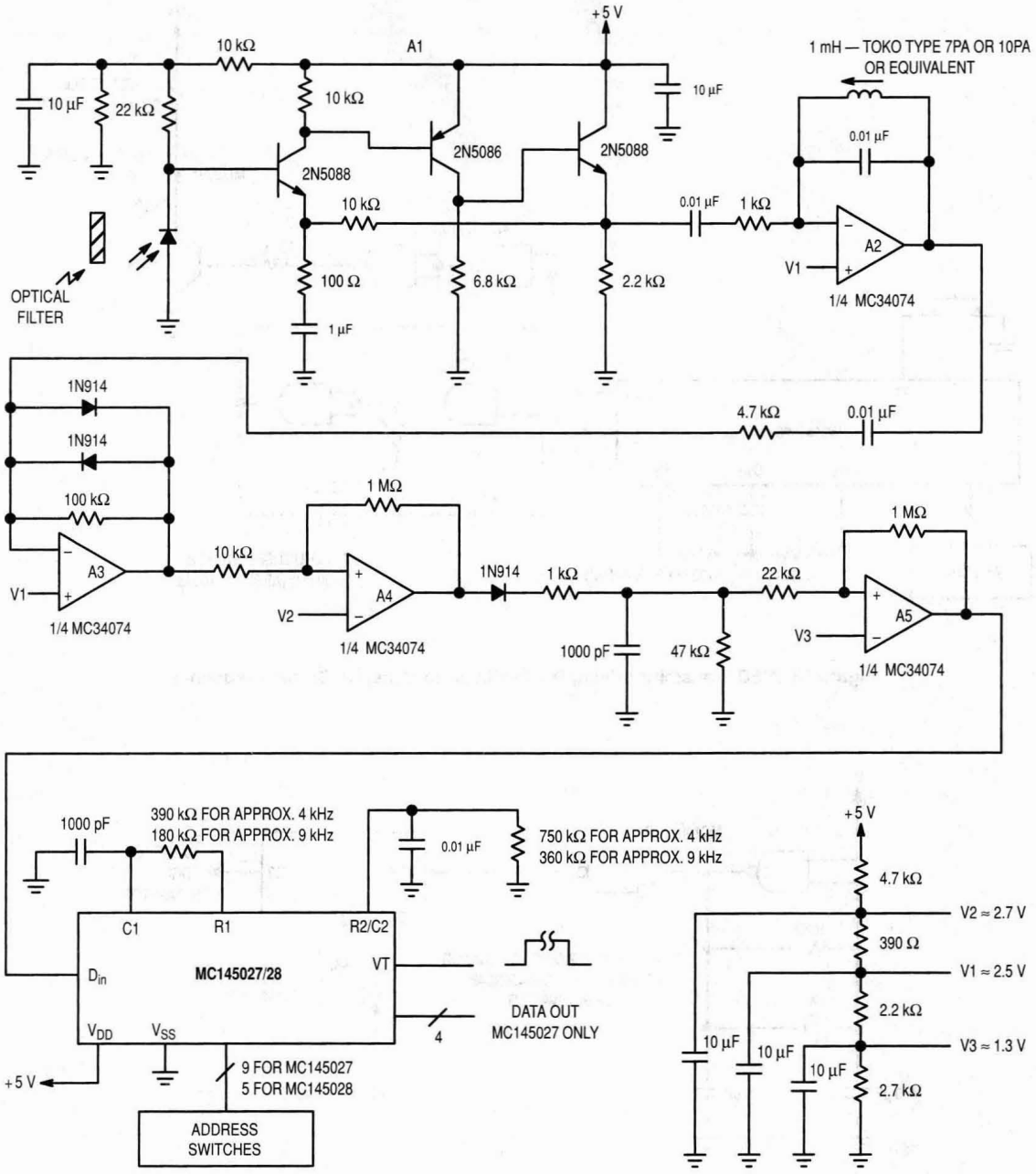
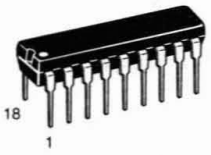


Figure 20. Infrared Receiver

MC145106

PLL Frequency Synthesizer
CMOS



P SUFFIX
PLASTIC DIP
CASE 707

DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

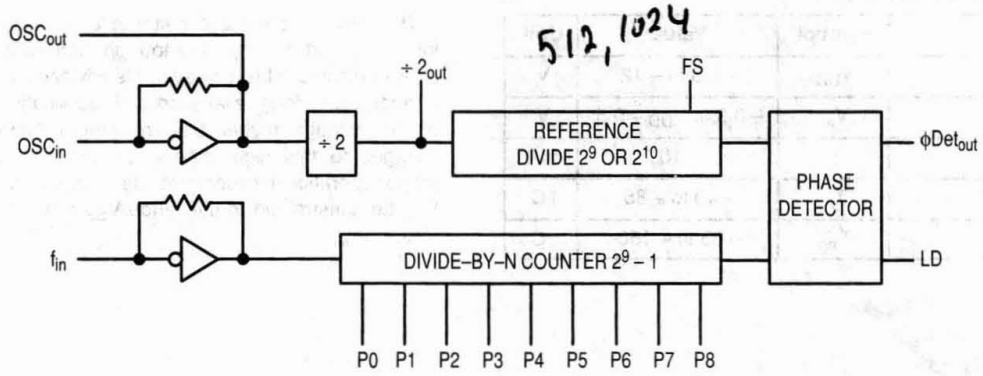
MC145106P	Plastic DIP
MC145106DW	SOG Package

The MC145106 is a phase–locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal, and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground–to–supply binary signals. Pull–down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out–of–lock signal is provided from the on–chip lock detector with a "0" level for the out–of–lock condition.

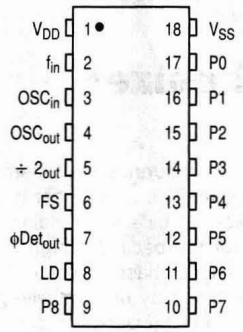
- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On–Chip Pull–Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (Including ÷ 2)
- Three–State Phase Detector
- See Application Note AN535 and Article Reprint AR254
- Chip Complexity: 880 FETs or 220 Equivalent Gates
- See the MC145151–2 and MC145152–2 for Higher Performance and Added Flexibility

BLOCK DIAGRAM

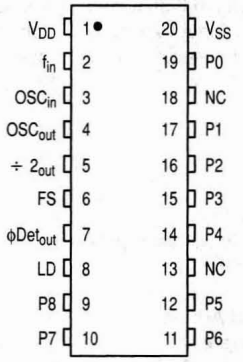


PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 12	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ*	Max	
Power Supply Voltage Range	V_{DD}	—	4.5	—	12	V
Supply Current	I_{DD}	5.0	—	6	10	mA
		10	—	20	35	
		12	—	28	50	
Input Voltage "0" Level	V_{IL}	5.0	—	—	1.5	V
		10	—	—	3.0	
		12	—	—	3.6	
"1" Level	V_{IH}	5.0	3.5	—	—	
		10	7.0	—	—	
		12	8.4	—	—	
Input Current "0" Level FS, Pull–Up Resistor Source Current)	I_{in}	5.0	– 5.0	– 20	– 50	µA
		10	– 15	– 60	– 150	
		12	– 20	– 80	– 200	
(P0 – P8)		5.0	—	—	– 0.3	
		10	—	—	– 0.3	
		12	—	—	– 0.3	
(FS) "1" Level		5.0	—	—	0.3	
		10	—	—	0.3	
		12	—	—	0.3	
(P0 – P8, Pull–Down Resistor Sink Current)		5.0	7.5	30	75	
		10	22.5	90	225	
		12	30	120	300	
(OSC_{in}, f_{in}) "0" Level		5.0	– 2.0	– 6.0	– 15	
		10	– 6.0	– 25	– 62	
		12	– 9.0	– 37	– 92	
(OSC_{in}, f_{in}) "1" Level		5.0	2.0	6.0	15	
		10	6.0	25	62	
		12	9.0	37	92	
Output Drive Current	I_{OH}					mA
(V_O = 4.5 V) Source		5.0	– 0.7	– 1.4	—	
(V_O = 9.5 V)		10	– 1.1	– 2.2	—	
(V_O = 11.5 V)		12	– 1.5	– 3.0	—	
(V_O = 0.5 V) Sink	I_{OL}	5.0	0.9	1.8	—	
(V_O = 0.5 V)		10	1.4	2.8	—	
(V_O = 0.5 V)		12	2.0	4.0	—	
Input Amplitude	—					V p–p
(f_{in} @ 4.0 MHz)		—	1.0	0.2	—	Sine
(OSC_{in} @ 10.24 MHz)		—	1.5	0.3	—	
Input Resistance	R_{in}					MΩ
(OSC_{in}, f_{in})		5.0	—	1.0	—	
		10	—	0.5	—	
		12	—	—	—	
Input Capacitance (OSC_{in}, f_{in})	C_{in}	—	—	6.0	—	pF
Three–State Leakage Current (ϕDet_{out})	I_{OZ}	5.0	—	—	1.0	µA
		10	—	—	1.0	
		12	—	—	1.0	
Input Frequency (– 40 to + 85°C)	f_{in}	4.5	0	—	4.0	MHz
		12	0	—	4.0	
Oscillator Frequency (– 40 to + 85°C)	OSC_{in}	4.5	0.1	—	10.24	MHz
		12	0.1	—	10.24	

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TYPICAL CHARACTERISTICS*

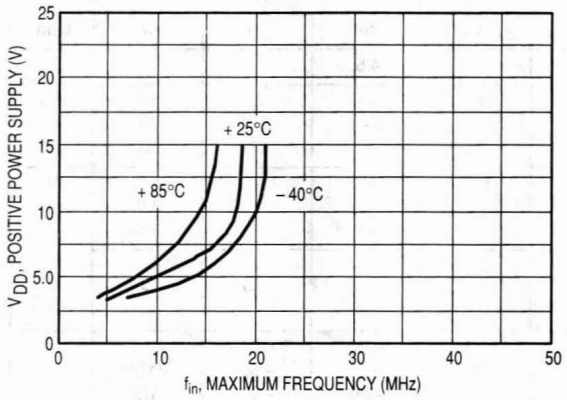


Figure 1. Maximum Divider Input Frequency versus Supply Voltage

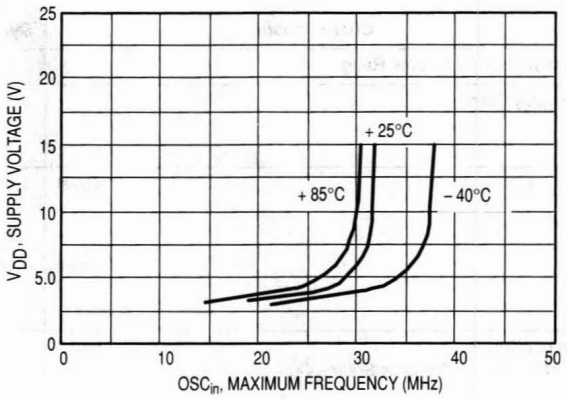


Figure 2. Maximum Oscillator Input Frequency versus Supply Voltage

* Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide by N
0	0	0	0	0	0	0	0	0	2*
0	0	0	0	0	0	0	0	1	3*
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	1	255
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}.
0: Voltage level = 0 or open circuit input.
* The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the $2^N - 1$ sequence. When pin is not connected the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0 – P8
Programmable Inputs (PDIP — Pins 17 – 9; SOG — Pins 19, 17 – 14, 12 – 9)

Programmable divider inputs (binary).

f_{in}
Frequency Input (PDIP, SOG — Pin 2)

Frequency input to programmable divider (derived from VCO).

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (PDIP, SOG — Pins 3, 4)

Oscillator/amplifier input and output terminals.

LD
Lock Detector (PDIP, SOG — Pin 8)

LD is high when loop is locked, pulses low when out–of–lock.

ϕDet_{out} (PDIP, SOG — Pin 7)

Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator — input frequency typically 5.0 or 10 kHz.

NOTE

Phase Detector Gain = $V_{DD}/4\pi$.

FS
Reference Oscillator Frequency Division Select (PDIP, SOG — Pin 6)

When using 10.24 MHz OSC frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.

$\div 2_{out}$ (PDIP, SOG — Pin 5)

Reference OSC frequency divided by 2 output; when using 10.24 MHz OSC frequency, this output is 5.12 MHz for frequency tripling applications.

V_{DD}
Positive Power Supply (PDIP, SOG — Pin 1)

V_{SS}
Ground (PDIP — Pin 18, SOG — Pin 20)

PLL SYNTHESIZER APPLICATIONS

The MC145106 is well suited for applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer, using a single crystal reference, is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145106 can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling, and loop programming techniques. In general, 300 – 400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft synthesizer of Figure 5, the VHF loop (top) will provide a 50 kHz, 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720–channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transceivers. The VCO operates on frequency during transmit and is offset downward during receive. The offset corresponds to the receive IF (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

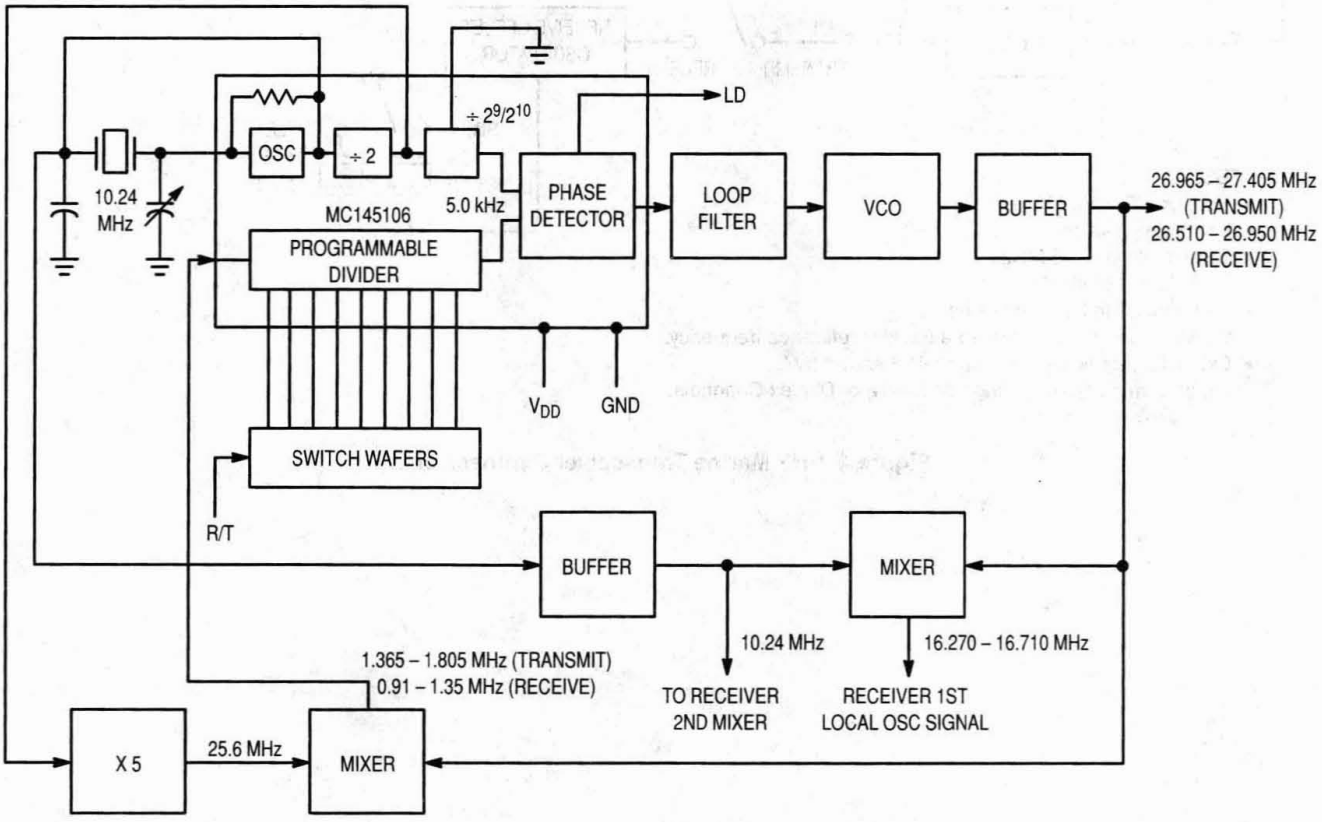
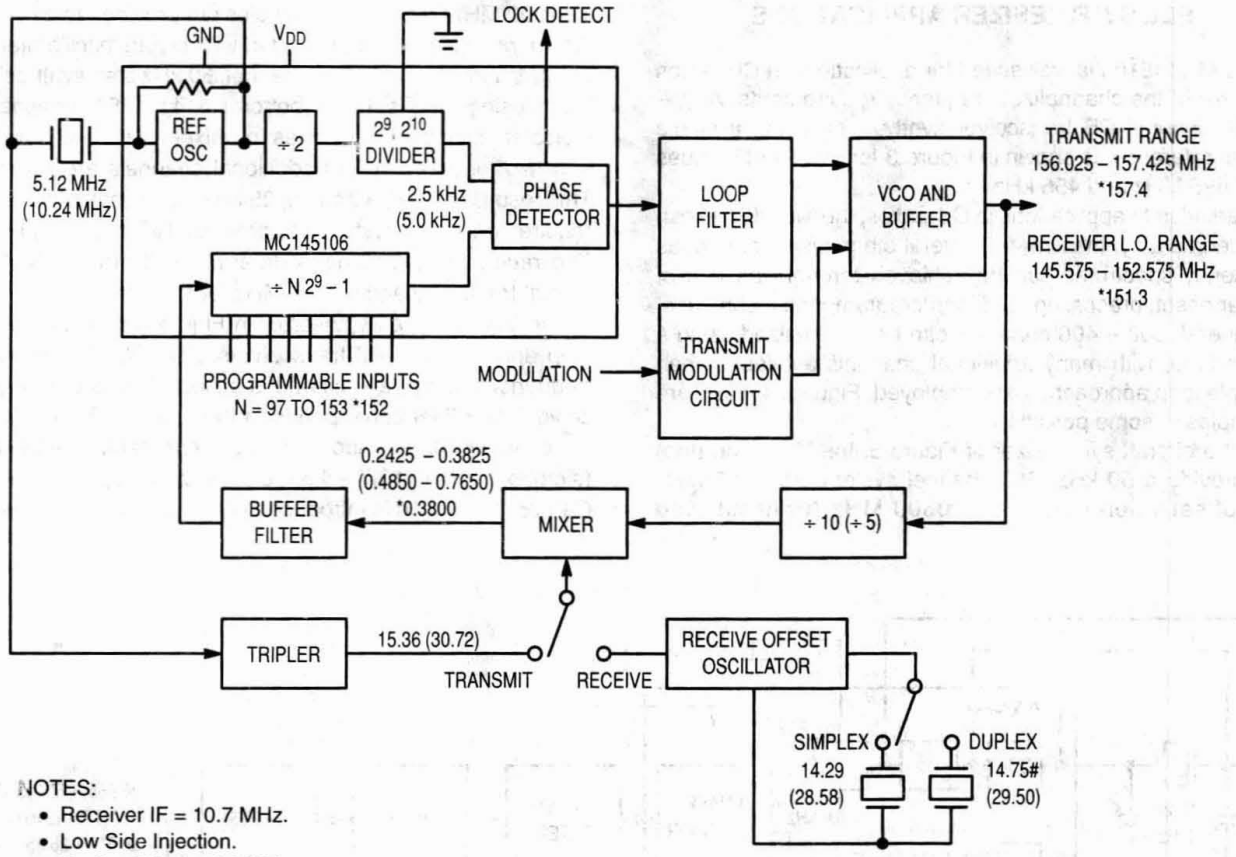


Figure 3. Single Crystal CB Synthesizer Featuring On–Frequency VCO During Transmit



NOTES:

- Receiver IF = 10.7 MHz.
- Low Side Injection.
- Duplex Offset = 4.6 MHz.
- Step Size = 25 kHz.
- Frequencies in MHz unless noted.
- Values in parentheses are for a 5.0 kHz reference frequency.
- Example frequencies for Channel 28 shown by *.

#Can be eliminated by adding 184 to ÷ N for Duplex Channels.

Figure 4. VHF Marine Transceiver Synthesizer

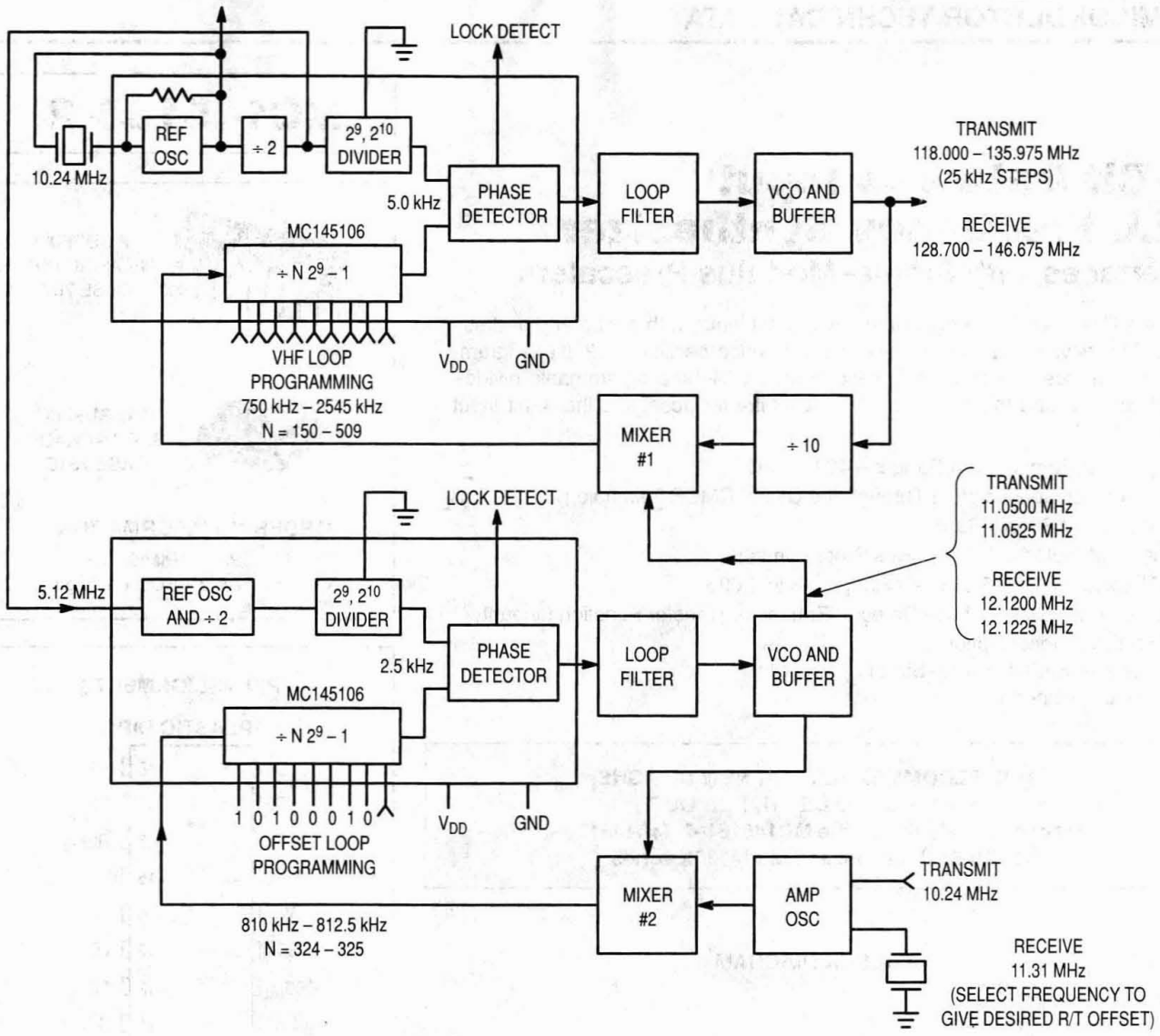


Figure 5. VHF Aircraft 720 Channel Two Crystal Frequency Synthesizer

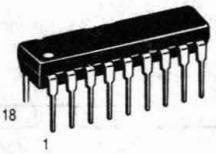
MC145145-2

4-Bit Data Bus Input PLL Frequency Synthesizer

Interfaces with Single–Modulus Prescalers

The MC145145–2 is programmed by a 4–bit input, with strobe and address lines. The device features consist of a reference oscillator, 12–bit programmable reference divider, digital phase detector, 14–bit programmable divide–by–N counter, and the necessary latch circuitry for accepting the 4–bit input data.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Single Modulus 4–Bit Data Bus Programming
- ÷N Range = 3 to 16,383, ÷R Range = 3 to 4,095
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single–Ended (Three–State)
  - Double–Ended



P SUFFIX
PLASTIC DIP
CASE 707

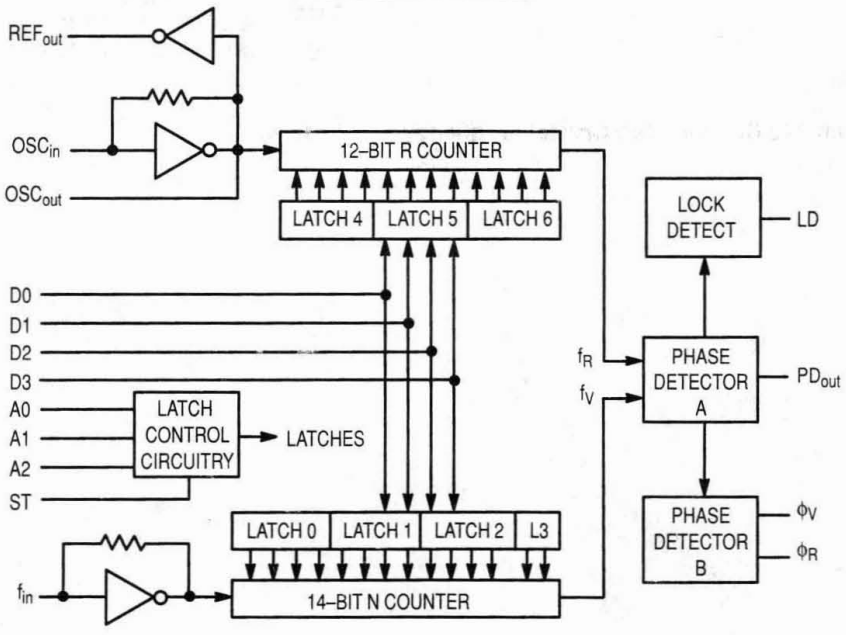
DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

MC145145P2	Plastic DIP
MC145145DW2	SOG Package

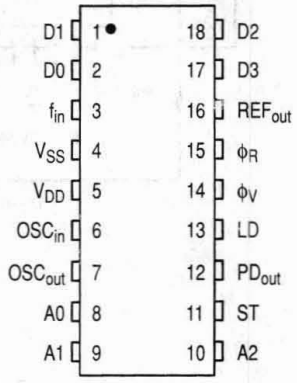
NOT RECOMMENDED FOR NEW DESIGNS;
PRODUCT TO BE PHASED OUT.
Closest equivalents are the MC145151–2, MC145170–1, MC14519X series, and MC14520X series.

BLOCK DIAGRAM

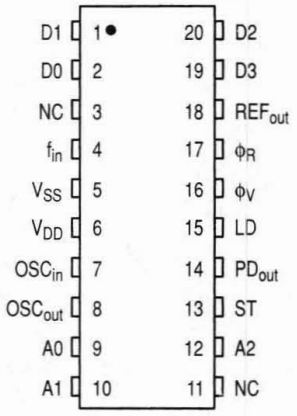


PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

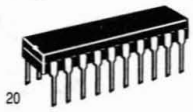
MC145146-2

4-Bit Data Bus Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

The MC145146–2 is programmed by a 4–bit input, with strobe and address lines. The device features consist of a reference oscillator, 12–bit programmable reference divider, digital phase detector, 10–bit programmable divide–by–N counter, 7–bit divide–by–A counter, and the necessary latch circuitry for accepting the 4–bit input data.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Programmable Reference Divider for Values Between 3 and 4095
- Dual–Modulus 4–Bit Data Bus Programming
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single–Ended (Three–State)
  - Double–Ended



P SUFFIX
PLASTIC DIP
CASE 738

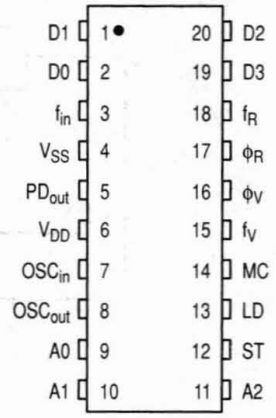
DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

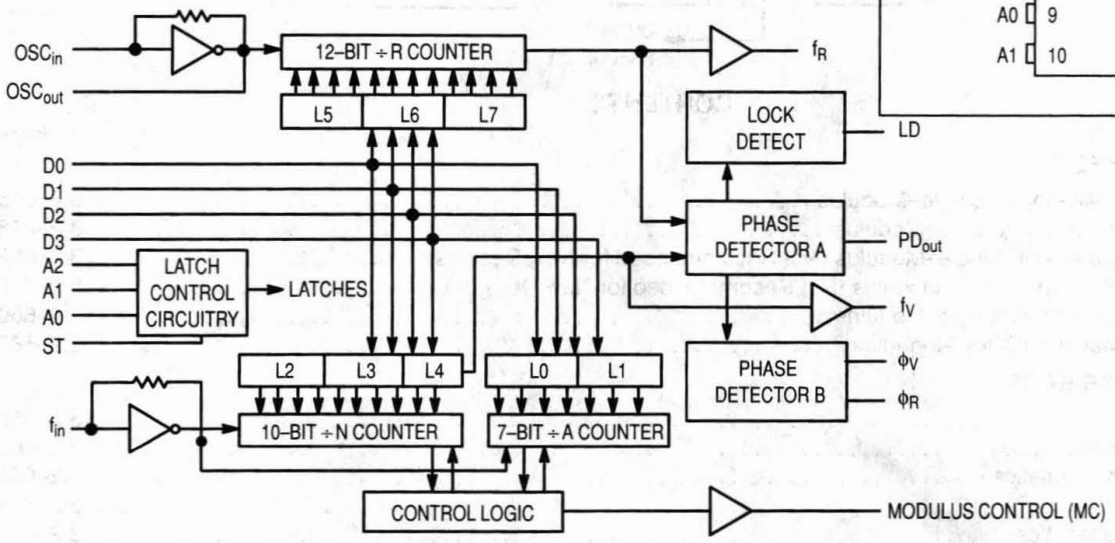
MC145146P2	Plastic DIP
MC145146DW2	SOG Package

NOT RECOMMENDED FOR NEW DESIGNS;
PRODUCT TO BE PHASED OUT.
Closest equivalents are the MC145152–2, MC145170–1, MC14519X series, and MC14520X series.

PIN ASSIGNMENT



BLOCK DIAGRAM



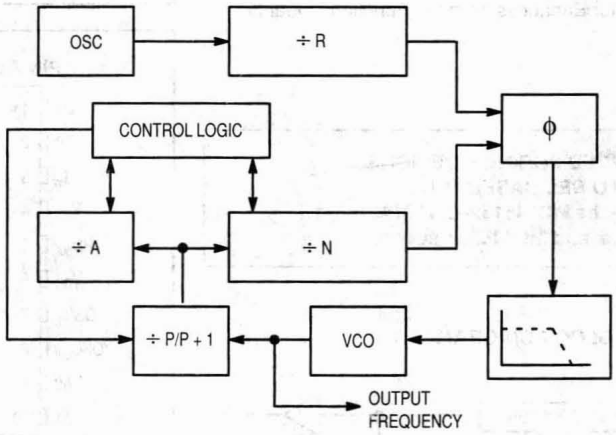
MC145151-2
MC145152-2
MC145155-2
MC145156-2
MC145157-2
MC145158-2

PLL Frequency Synthesizer Family
CMOS

The devices described in this document are typically used as low–power, phase–locked loop frequency synthesizers. When combined with an external low–pass filter and voltage–controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two–Way Radios	Amateur Radio



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MC145151-2

Parallel-Input PLL Frequency Synthesizer

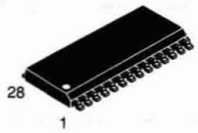
Interfaces with Single–Modulus Prescalers

The MC145151–2 is programmed by 14 parallel–input data lines for the N counter and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, and 14–bit programmable divide–by–N counter.

The MC145151–2 is an improved–performance drop–in replacement for the MC145151–1. The power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates

P SUFFIX
PLASTIC DIP
CASE 710

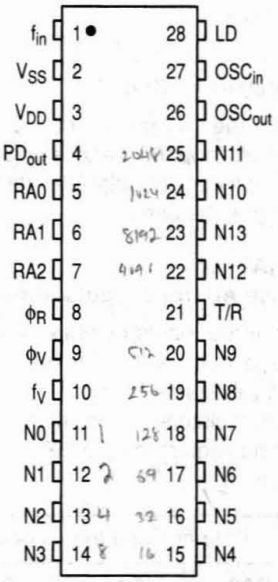


DW SUFFIX
SOG PACKAGE
CASE 751F

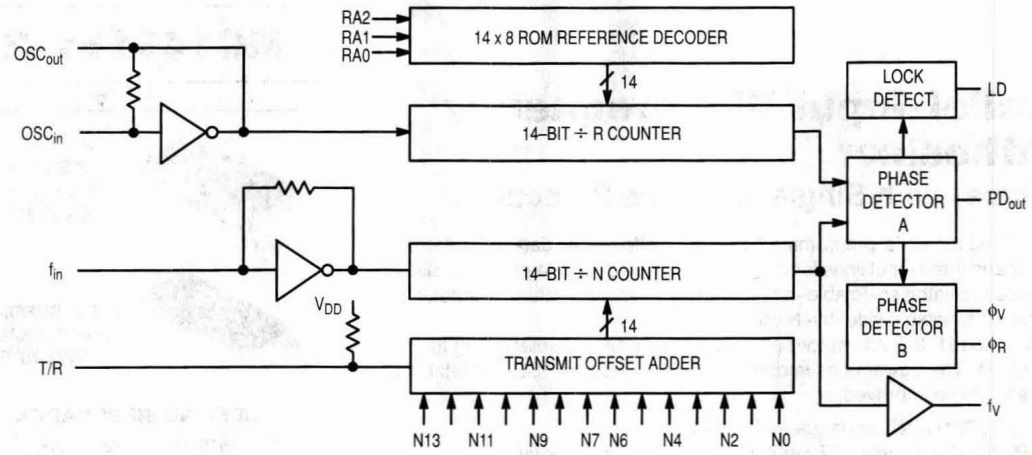
ORDERING INFORMATION

MC145151P2	Plastic DIP
MC145151DW2	SOG Package

PIN ASSIGNMENT



MC145151–2 BLOCK DIAGRAM



NOTE: N0 – N13 inputs and inputs RA0, RA1, and RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0 – RA2
Reference Address Inputs (Pins 5, 6, 7)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N0 – N11
N Counter Programming Inputs (Pins 11 – 20, 22 – 25)

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant and N13 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only an SPST switch to alter data to the zero state.

T/R
Transmit/Receive Offset Adder Input (Pin 21)

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull–up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 4)

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 8, 9)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V
N Counter Output (Pin 10)

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS

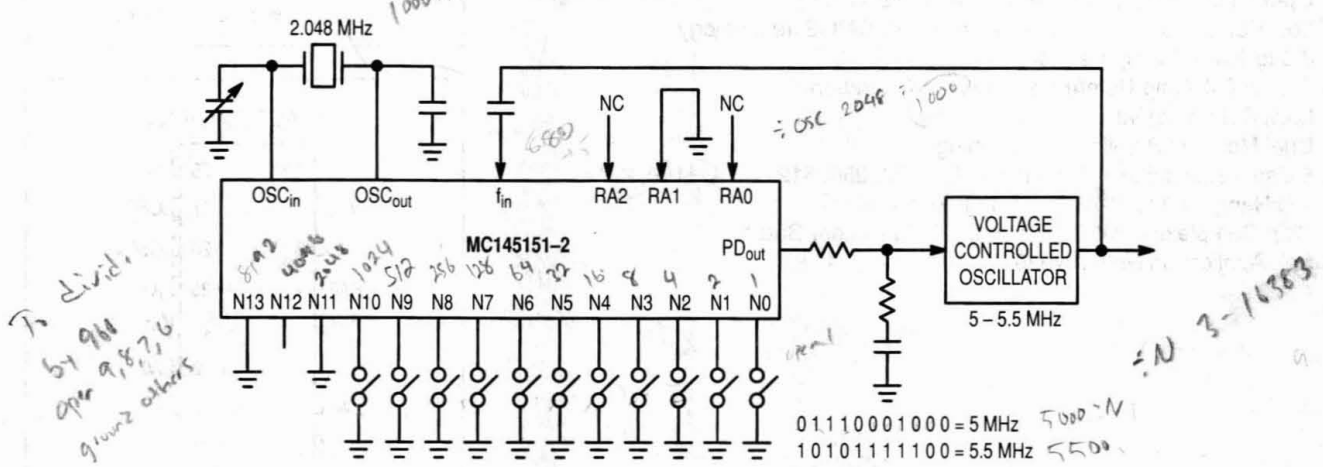
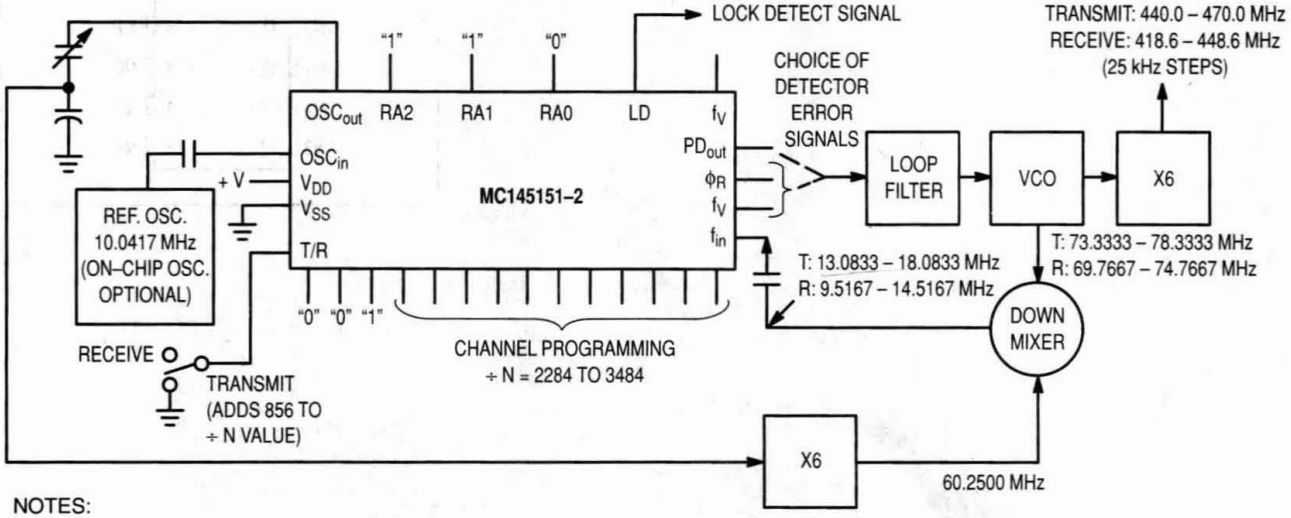


Figure 1. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440 – 470 MHz band. Similar implementation applies to the 406 – 440 MHz band. For 470 – 512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Figure 2. Synthesizer for Land Mobile Radio UHF Bands

MC145151–2 Data Sheet Continued on Page 3.2–666

MC145152-2

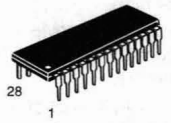
Parallel-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

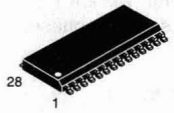
The MC145152–2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, two–output phase detector, 10–bit programmable divide–by–N counter, and 6–bit programmable ÷ A counter.

The MC145152–2 is an improved–performance drop–in replacement for the MC145152–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
- See Application Note AN980



P SUFFIX
PLASTIC DIP
CASE 710

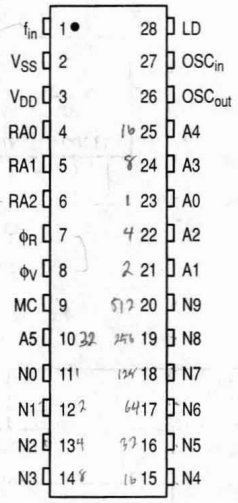


DW SUFFIX
SOG PACKAGE
CASE 751F

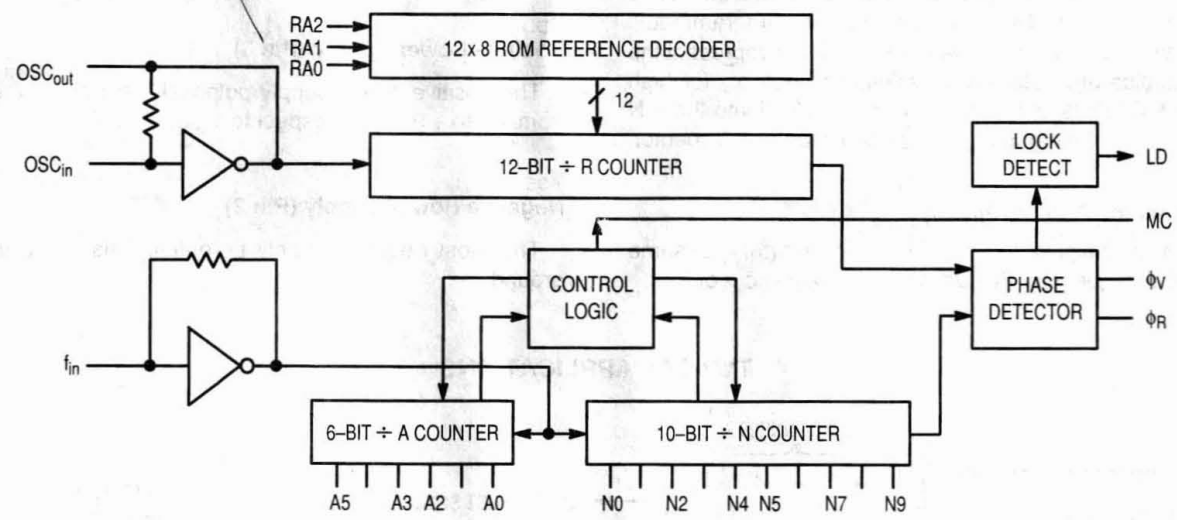
ORDERING INFORMATION

MC145152P2	Plastic DIP
MC145152DW2	SOG Package

PIN ASSIGNMENT



MC145152–2 BLOCK DIAGRAM



NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2
Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N0 – N9
N Counter Programming Inputs (Pins 11 – 20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

A0 – A5
A Counter Programming Inputs
(Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of f_{in} that require a logic 0 on the MC output (see **Dual–Modulus Prescaling** section). The A inputs all have internal pull–up resistors that ensure that inputs left open will remain at a logic 1.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop–error signal.

If the frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 9)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the counts down from its programmed value (N – A additional counts first since both ÷ N and ÷ A are counting down during

portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

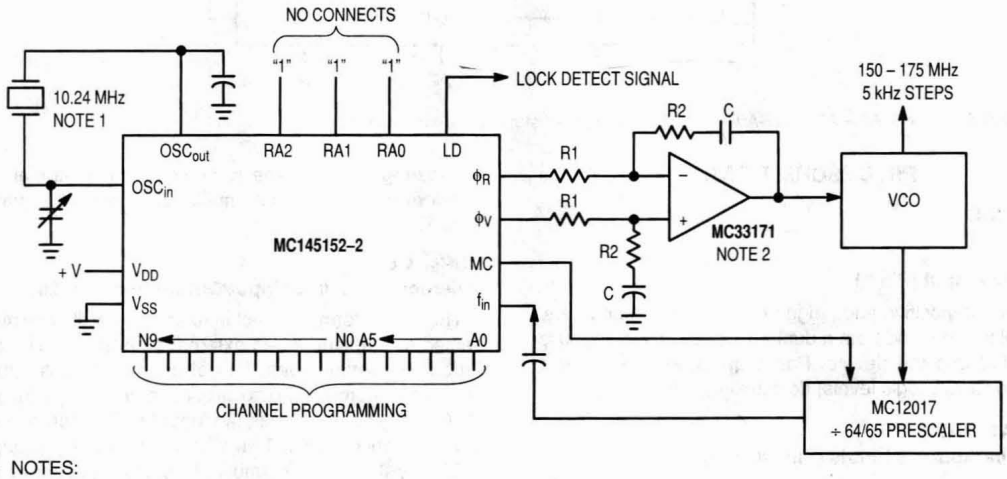
V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

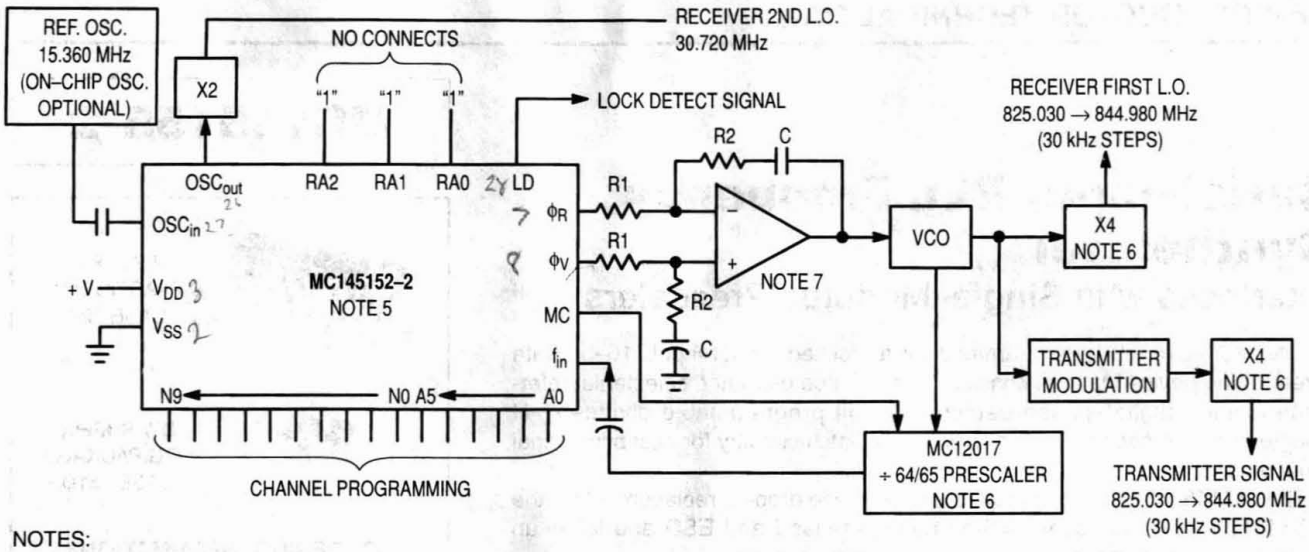
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



NOTES:
1. Off–chip oscillator optional.
2. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

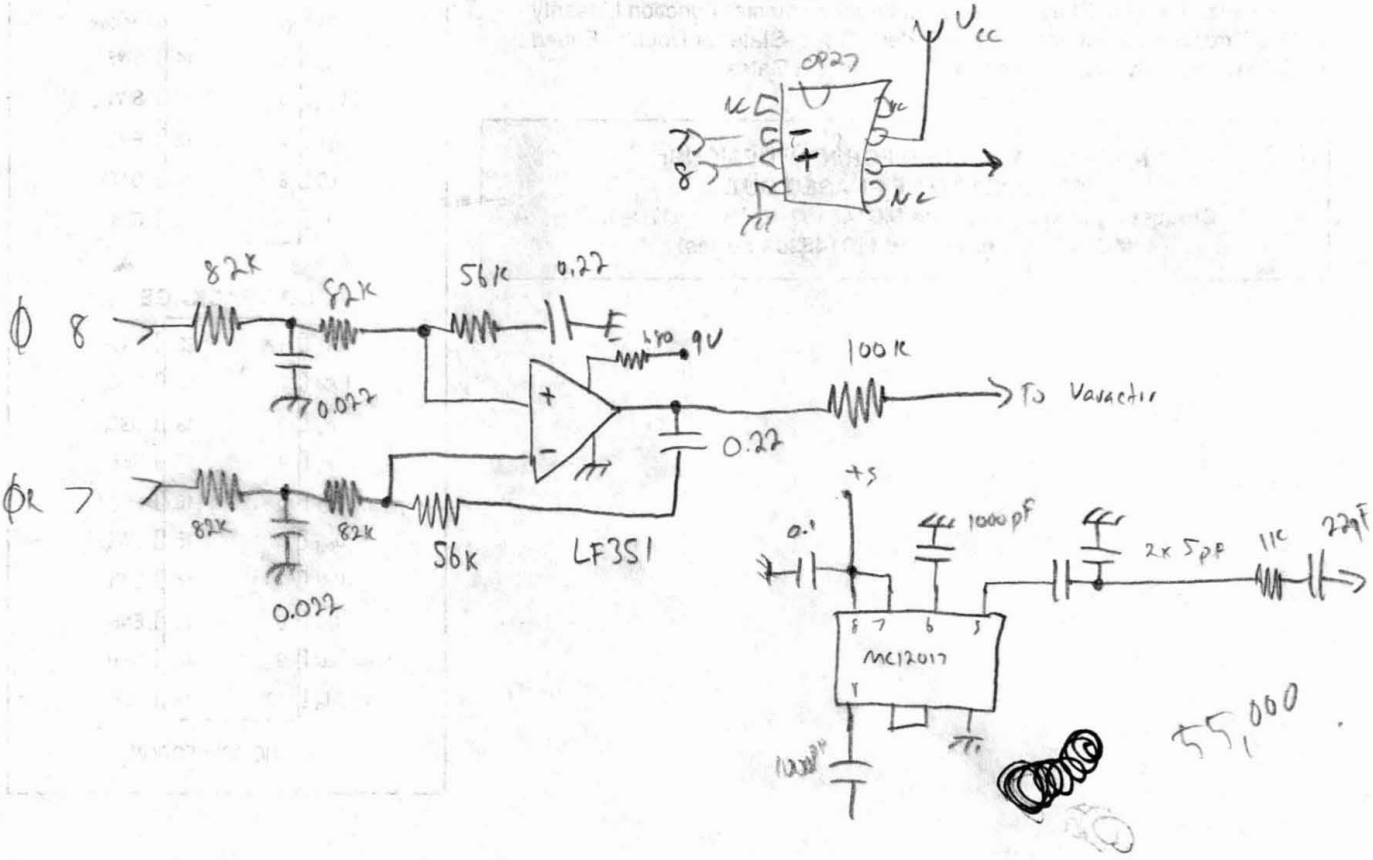
Figure 1. Synthesizer for Land Mobile Radio VHF Bands



NOTES:

1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3. f_R = 7.5 kHz; ÷ R = 2048.
4. N_{total} = N • 64 + A = 27501 to 28166; N = 429 to 440; A = 0 to 63.
5. MC145158–2 may be used where serial data entry is desired.
6. High frequency prescalers (e.g., MC12018 [520 MHz] and MC12022 [1 GHz]) may be used for higher frequency VCO and f_{ref} implementations.
7. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. 666–Channel, Computer–Controlled, Mobile Radiotelephone Synthesizer for 800 MHz Cellular Radio Systems



MC145152–2 Data Sheet Continued on Page 3.2–666

MC145155-2

Serial-Input PLL Frequency Synthesizer

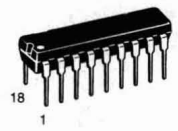
Interfaces with Single–Modulus Prescalers

The MC145155–2 is programmed by a clocked, serial input, 16–bit data stream. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, 14–bit programmable divide–by–N counter, and the necessary shift register and latch circuitry for accepting serial input data.

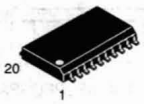
The MC145155–2 is an improved–performance drop–in replacement for the MC145155–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open–Drain Switch Outputs
- 8 User–Selectable ÷ R Values: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates

**NOT RECOMMENDED FOR NEW DESIGNS;
PRODUCT TO BE PHASED OUT.
Closest equivalents are the MC145157–2, MC145170–1, MC14519X series, and MC14520X series.**



P SUFFIX
PLASTIC DIP
CASE 707



DW SUFFIX
SOG PACKAGE
CASE 751D

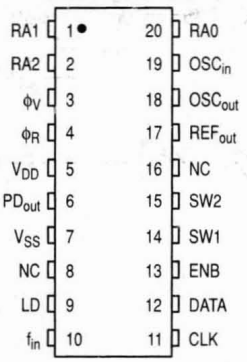
ORDERING INFORMATION

MC145155P2	Plastic DIP
MC145155DW2	SOG Package

PIN ASSIGNMENTS

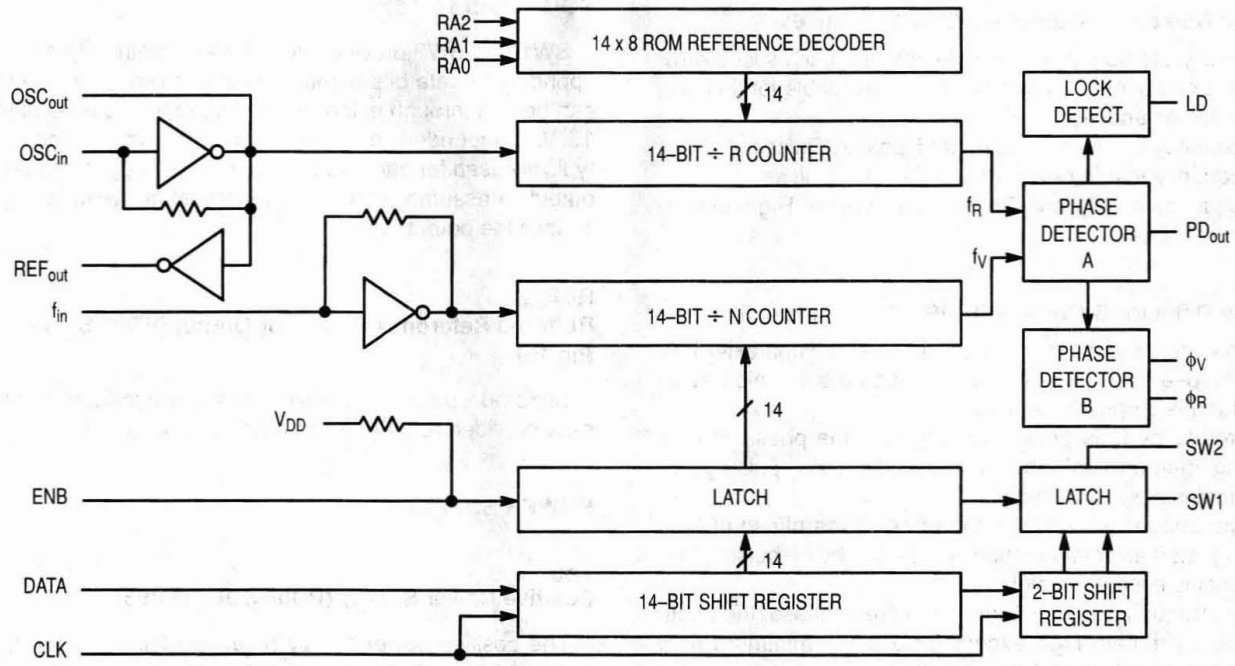
PLASTIC DIP

SOG PACKAGE



NC = NO CONNECTION

MC145155–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (PDIP – Pin 9, SOG – Pin 10)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

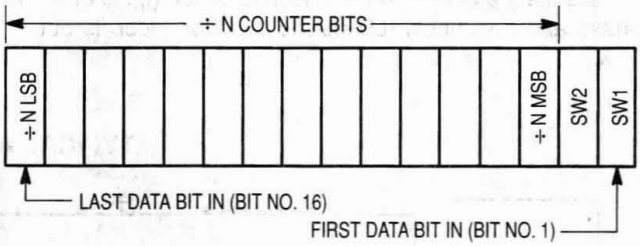
RA0, RA1, RA2
Reference Address Inputs (PDIP – Pins 18, 1, 2; SOG – Pins 20, 1, 2)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

CLK, DATA
Shift Register Clock, Serial Data Inputs (PDIP – Pins 10, 11; SOG – Pins 11, 12)

Each low–to–high transition clocks one bit into the on–chip 16–bit shift register. The Data input provides programming information for the 14–bit ÷ N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENB
Latch Enable Input (PDIP – Pin 12, SOG – Pin 13)

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on–chip pull–up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (PDIP – Pins 17, 16; SOG – Pins 19, 18)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (PDIP, SOG – Pin 6)

Three–state output of phase detector for use as loop error signal. Double–ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (PDIP, SOG – Pins 4, 3)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

LD
Lock Detector Output (PDIP – Pin 8, SOG – Pin 9)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). LD pulses low when loop is out of lock.

SW1, SW2
Band Switch Outputs (PDIP – Pins 13, 14; SOG – Pins 14, 15)

SW1 and SW2 provide latched open–drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high–impedance state, while a logic 0 causes the output to be low.

REF_{out}
Buffered Reference Oscillator Output (PDIP, SOG – Pin 15)

Buffered output of on–chip reference oscillator or externally provided reference–input signal.

POWER SUPPLY

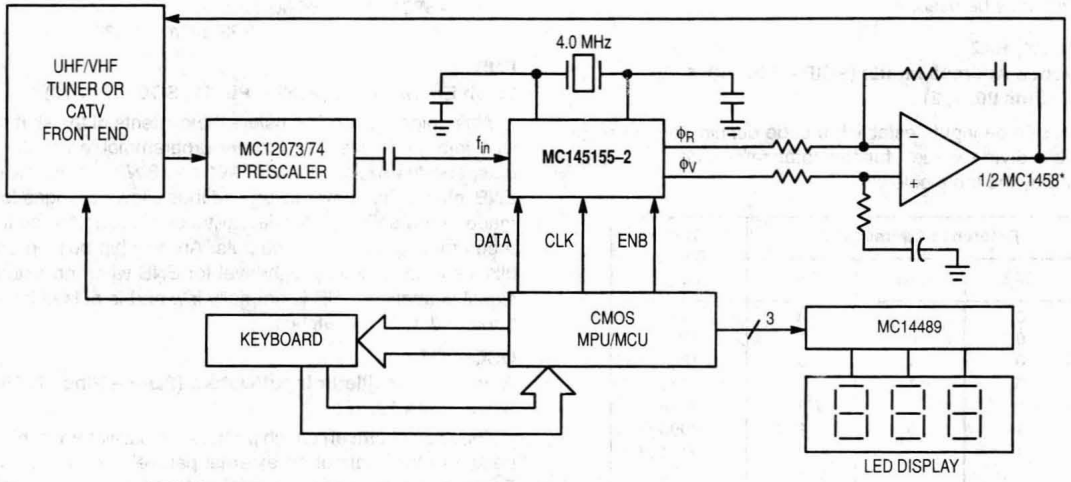
V_{DD}
Positive Power Supply (PDIP, SOG – Pin 5)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (PDIP, SOG – Pin 7)

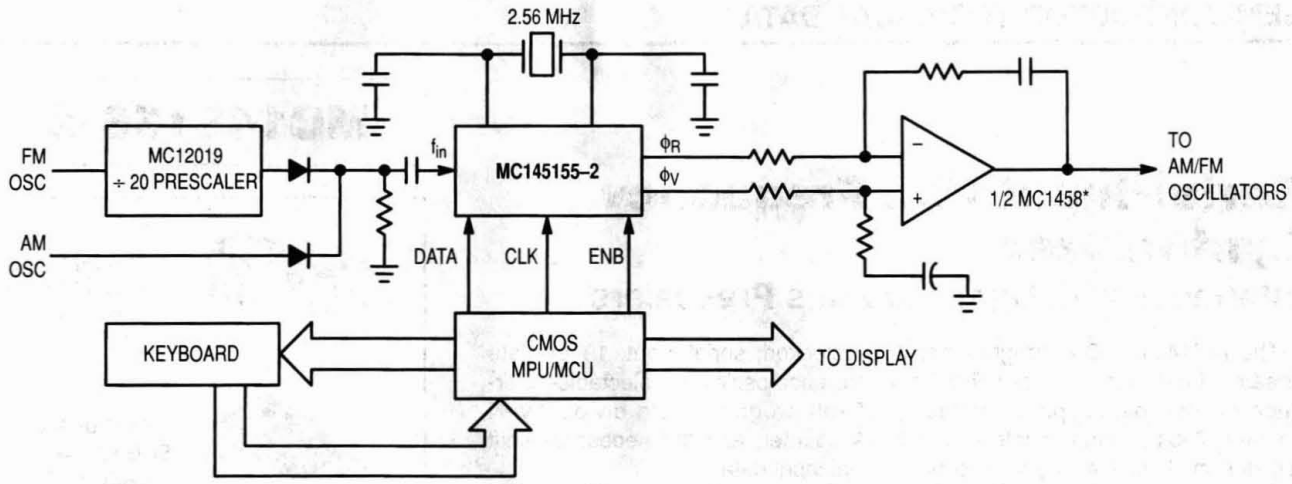
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. Microprocessor–Controlled TV/CATV Tuning System with Serial Interface



* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. AM/FM Radio Synthesizer

MC145155–2 Data Sheet Continued on Page 3.2–666

MC145156-2

Serial-Input PLL Frequency Synthesizer

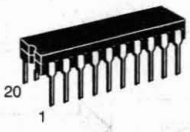
Interfaces with Dual–Modulus Prescalers

The MC145156–2 is programmed by a clocked, serial input, 19–bit data stream. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, 10–bit programmable divide–by–N counter, 7–bit programmable divide–by–A counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145156–2 is an improved–performance drop–in replacement for the MC145156–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open–Drain Switch Outputs
- Dual Modulus/Serial Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 640, 1000, 1024, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates

NOT RECOMMENDED FOR NEW DESIGNS;
PRODUCT TO BE PHASED OUT.
Closest equivalents are the MC145158–2, MC145170–1, MC14519X series, and MC14520X series.



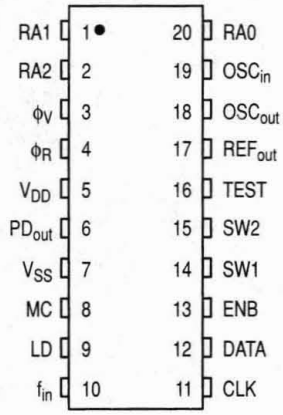
P SUFFIX
PLASTIC DIP
CASE 738

DW SUFFIX
SOG PACKAGE
CASE 751D

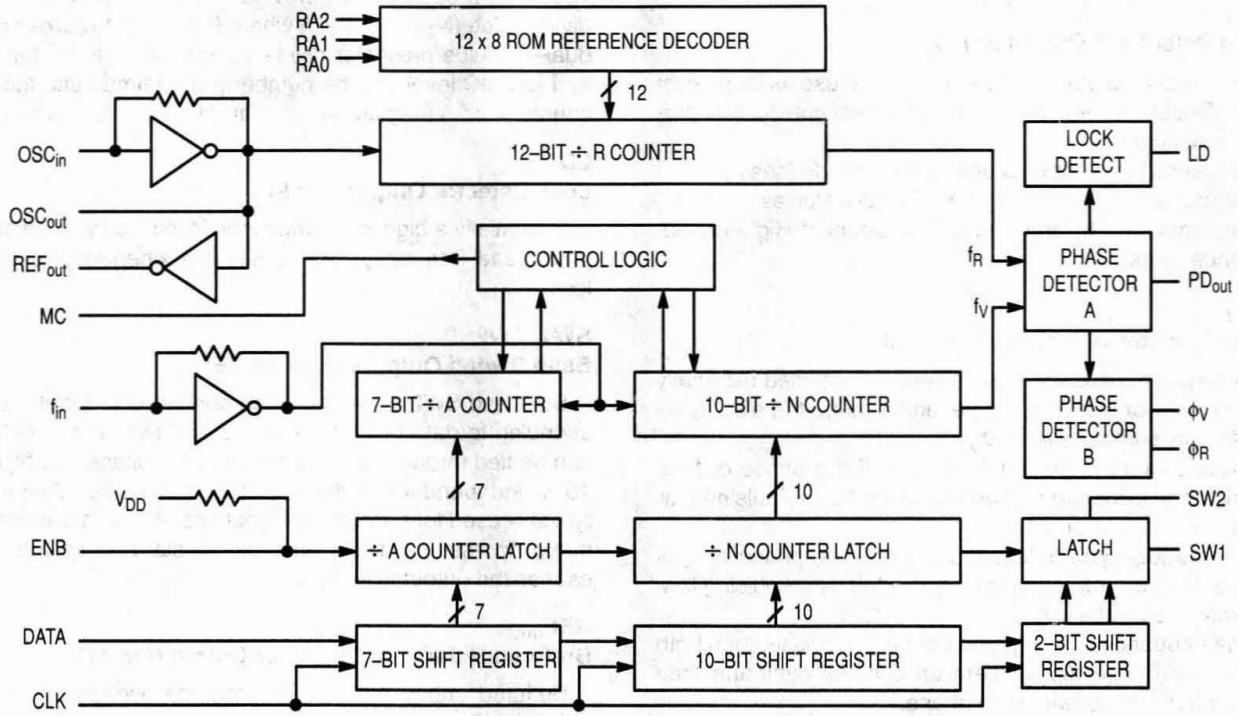
ORDERING INFORMATION

MC145156P2	Plastic DIP
MC145156DW2	SOG Package

PIN ASSIGNMENT



MC145156–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 10)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

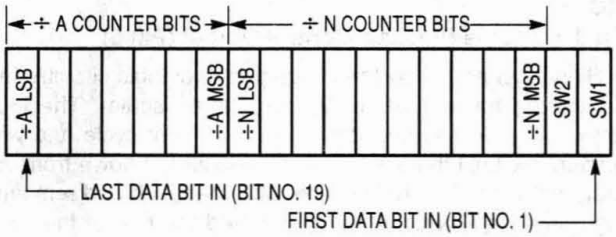
RA0, RA1, RA2
Reference Address Inputs (Pins 20, 1, 2)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	1	2048

CLK, DATA
Shift Register Clock, Serial Data Inputs (Pins 11, 12)

Each low–to–high transition clocks one bit into the on–chip 19–bit shift register. The data input provides programming information for the 10–bit ÷ N counter, the 7–bit ÷ A counter, and the two switch signals SW1 and SW2. The entry format is as follows:



ENB
Latch Enable Input (Pin 13)

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on–chip pull–up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 19, 18)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

TEST
Factory Test Input (Pin 16)

Used in manufacturing. Must be left open or tied to V_{SS}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 6)

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 4, 3)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 8)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 9)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). LD pulses low when loop is out of lock.

SW1, SW2
Band Switch Outputs (Pins 14, 15)

SW1 and SW2 provide latched open–drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high–impedance state, while a logic 0 causes the output to be low.

REF_{out}
Buffered Reference Oscillator Output (Pin 17)

Buffered output of on–chip reference oscillator or externally provided reference–input signal.

POWER SUPPLY

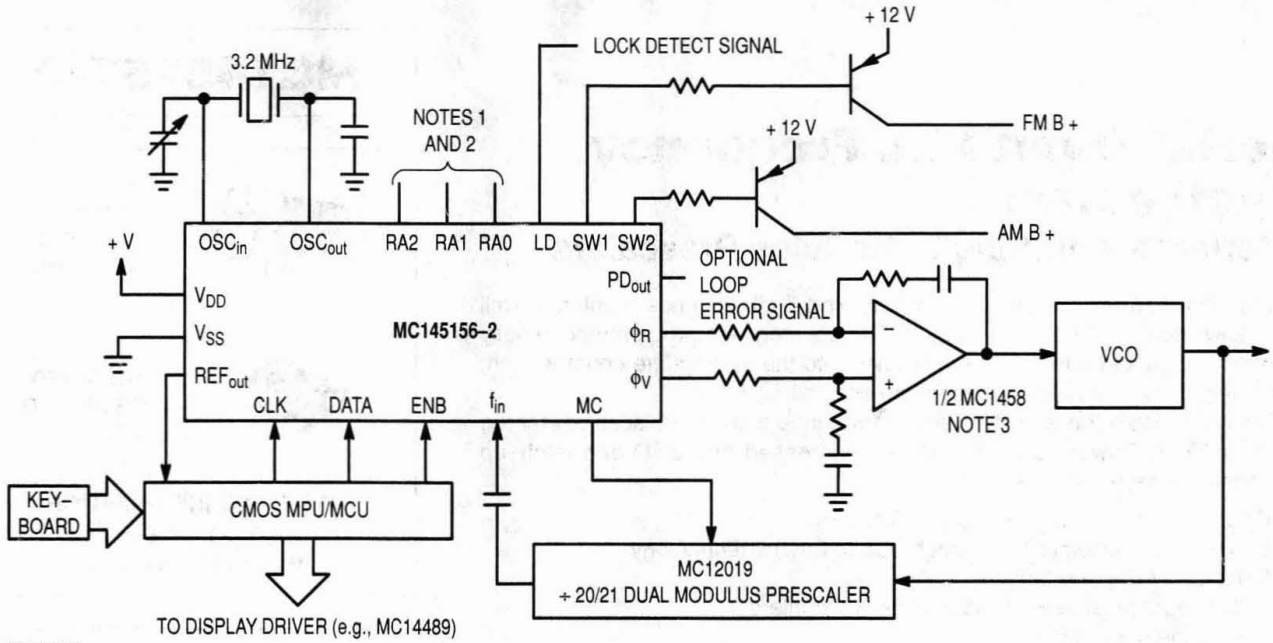
V_{DD}
Positive Power Supply (Pin 5)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 7)

The most negative supply potential. This pin is usually ground.

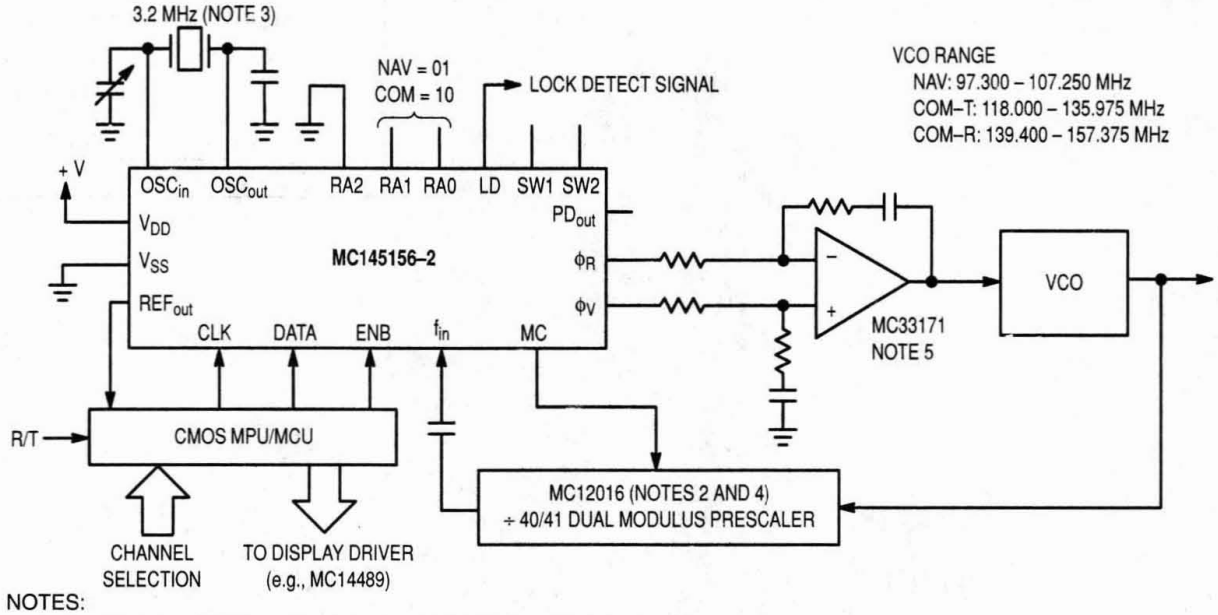
TYPICAL APPLICATIONS



NOTES:

1. For AM: channel spacing = 5 kHz, ÷ R = ÷ 640 (code 100).
2. For FM: channel spacing = 25 kHz, ÷ R = ÷ 128 (code 010).
3. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. AM/FM Radio Broadcast Synthesizer



NOTES:

1. For NAV: f_R = 50 kHz, ÷ R = 64 using 10.7 MHz lowside injection, N_{total} = 1946 – 2145.
   For COM–T: f_R = 25 kHz, ÷ R = 128, N_{total} = 4720 – 5439.
   For COM–R: f_R = 25 kHz, ÷ R = 128, using 21.4 MHz highside injection, N_{total} = 5576 – 6295.
2. A ÷ 32/33 dual modulus approach is provided by substituting an MC12015 for the MC12016. The devices are pin equivalent.
3. A 6.4 MHz oscillator crystal can be used by selecting ÷ R = 128 (code 010) for NAV and ÷ R = 256 (code 011) for COM.
4. MC12013 + MC10131 combination may also be used to form the ÷ 40/41 prescaler.
5. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. Avionics Navigation or Communication Synthesizer

MC145156–2 Data Sheet Continued on Page 3.2–666

MC145157-2

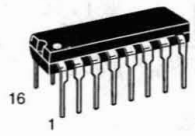
Serial-Input PLL Frequency Synthesizer

Interfaces with Single–Modulus Prescalers

The MC145157–2 has a fully programmable 14–bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145157–2 is an improved–performance drop–in replacement for the MC145157–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



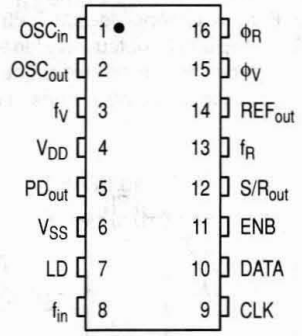
P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG PACKAGE
CASE 751G

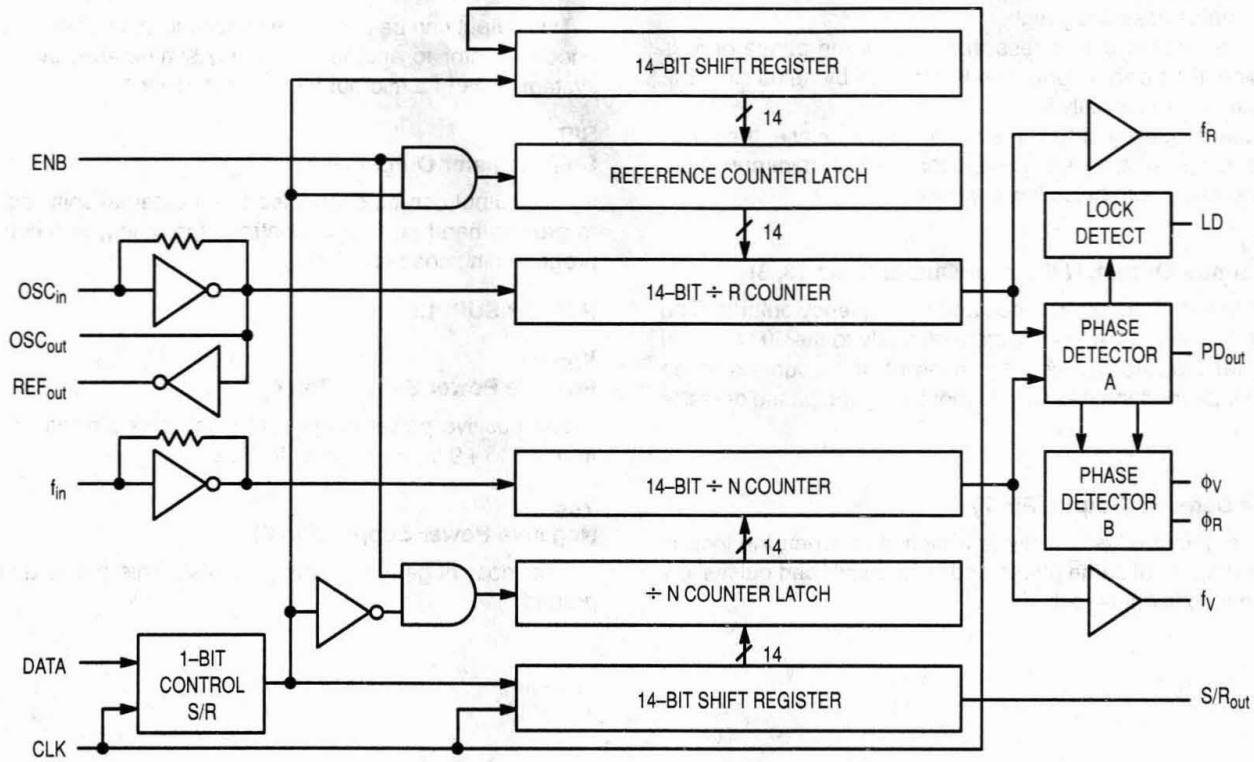
ORDERING INFORMATION

MC145157P2	Plastic DIP
MC145157DW2	SOG Package

PIN ASSIGNMENT



MC145157–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the clock shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ N counter latch. The entry format is as follows:

ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Single–Ended Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Double–Ended Phase Detector B Outputs (Pins 16, 15)

These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

S/R_{out}
Shift Register Output (Pin 12)

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

913-

30,000 Hz

30,500

R = 512
N = 476
A = 36

~~500~~ · 64 + 36 = 30,500

476

MC145157–2 Data Sheet Continued on Page 3.2–666

MC145158-2

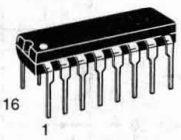
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

The MC145158–2 has a fully programmable 14–bit reference counter, as well as fully programmable ÷ N and ÷ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145158–2 is an improved–performance drop–in replacement for the MC145158–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 1023
- Dual Modulus Capability; ÷ A Range = 0 to 127
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



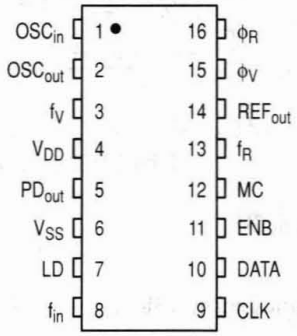
P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG PACKAGE
CASE 751G

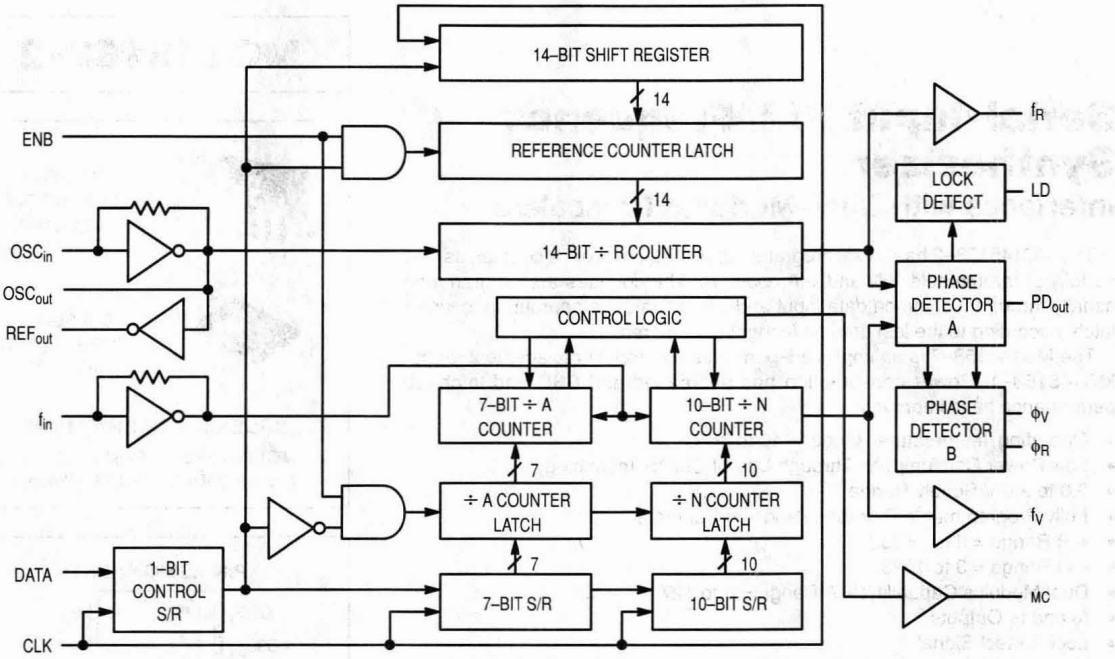
ORDERING INFORMATION

MC145158P2	Plastic DIP
MC145158DW2	SOG Package

PIN ASSIGNMENT



MC145158–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

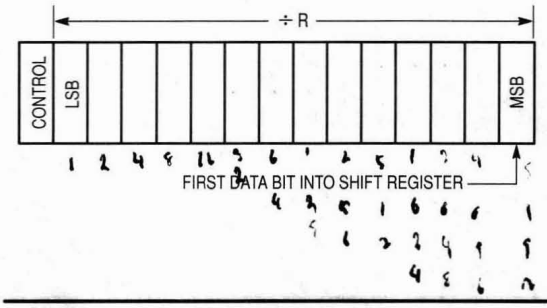
INPUT PINS

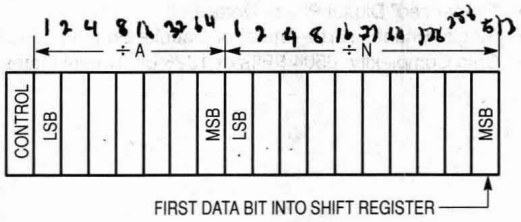
f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the CLK shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ A, ÷ N counter latch. The data entry format is as follows:





ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses

Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses

Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 16, 15)

Double–ended phase detector outputs. These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 12)

This output generates a signal by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual–modulus version offers a distinct advantage. The dual–modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

MC14515X–2 FAMILY CHARACTERISTICS AND DESCRIPTIONS

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage (DC or Transient), SW1, SW2 ($R_{pull-up}$ = 4.7 kΩ)	– 0.5 to + 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: – 12 mW/°C from 65 to 85°C
SOG Package: – 7 mW/°C from 65 to 85°C

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3	9	3	9	3	9	V
I_{ss}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3 5 9	— — —	3.5 10 30	— — —	3 7.5 24	— — —	3 7.5 24	mA
I_{SS}	Quiescent Supply Current (not including pull–up current component)	$V_{in} = V_{DD}$ or V_{SS} I_{out} = 0 µA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge$ 2.1 V Input dc $V_{out} \ge$ 3.5 V coupled $V_{out} \ge$ 6.3 V square wave	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le$ 0.9 V Input dc $V_{out} \le$ 1.5 V coupled $V_{out} \le$ 2.7 V square wave	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9	± 2	± 50	± 2	± 25	± 2	± 22	µA
I_{IL}	Input Leakage Current (Data, CLK, ENB — without pull–ups)	$V_{in} = V_{SS}$	9	—	– 0.3	—	– 0.1	—	– 1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9	—	0.3	—	0.1	—	1.0	µA

(continued)

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{IL}	Pull–up Current (all inputs with pull–ups)	$V_{in} = V_{SS}$	9	– 20	– 400	– 20	– 200	– 20	– 170	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
$V_{(BR)DSS}$	Drain–to–Source Breakdown Voltage — SW1, SW2	$R_{pull–up} = 4.7$ kΩ	—	15	—	15	—	15	—	V
I_{OL}	Low–Level Sinking Current — MC	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	mA
I_{OH}	High–Level Sourcing Current — MC	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.60 – 0.90 – 1.50	— — —	– 0.50 – 0.75 – 1.25	— — —	– 0.30 – 0.50 – 0.80	— — —	mA
I_{OL}	Low–Level Sinking Current — LD	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.25 0.64 1.30	— — —	0.20 0.51 1.00	— — —	0.15 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — LD	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.25 – 0.64 – 1.30	— — —	– 0.20 – 0.51 – 1.00	— — —	– 0.15 – 0.36 – 0.70	— — —	mA
I_{OL}	Low–Level Sinking Current — SW1, SW2	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.05	— — —	mA
I_{OL}	Low–Level Sinking Current — Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.44 – 0.64 – 1.30	— — —	– 0.35 – 0.51 – 1.00	— — —	– 0.22 – 0.36 – 0.70	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 1.0	µA
I_{OZ}	Output Leakage Current — SW1, SW2	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 3.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, ENB to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

SWITCHING WAVEFORMS

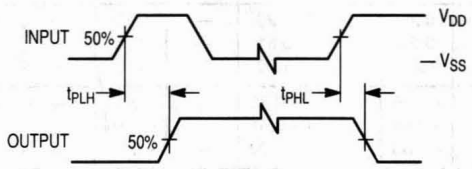
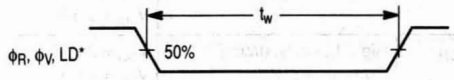


Figure 1.



* f_R in phase with f_V.

Figure 2.

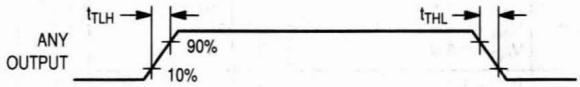
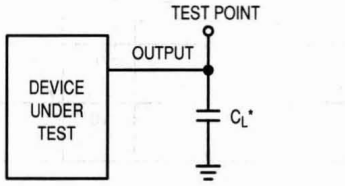
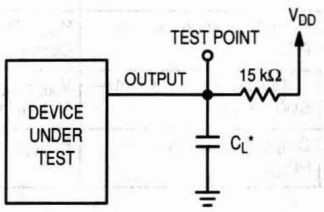


Figure 3.



* Includes all probe and fixture capacitance.

Figure 4. Test Circuit



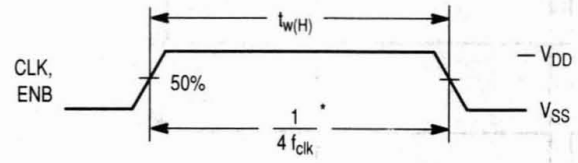
* Includes all probe and fixture capacitance.

Figure 5. Test Circuit

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 6)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to CLK (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, CLK to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, CLK to ENB (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, ENB to CLK (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, CLK and ENB (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times — Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	µs

SWITCHING WAVEFORMS



*Assumes 25% Duty Cycle.

Figure 6.

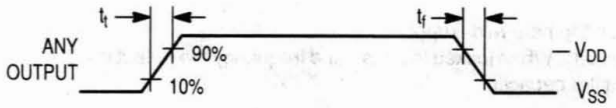


Figure 8.

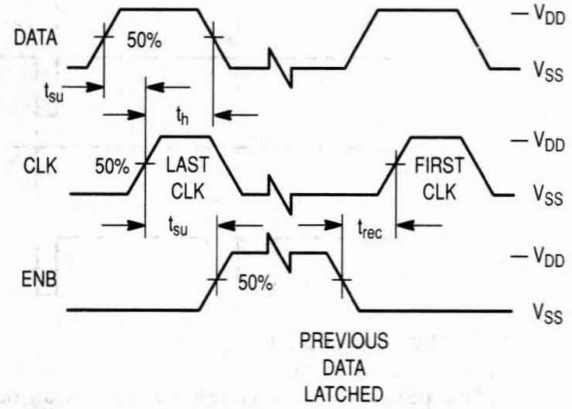
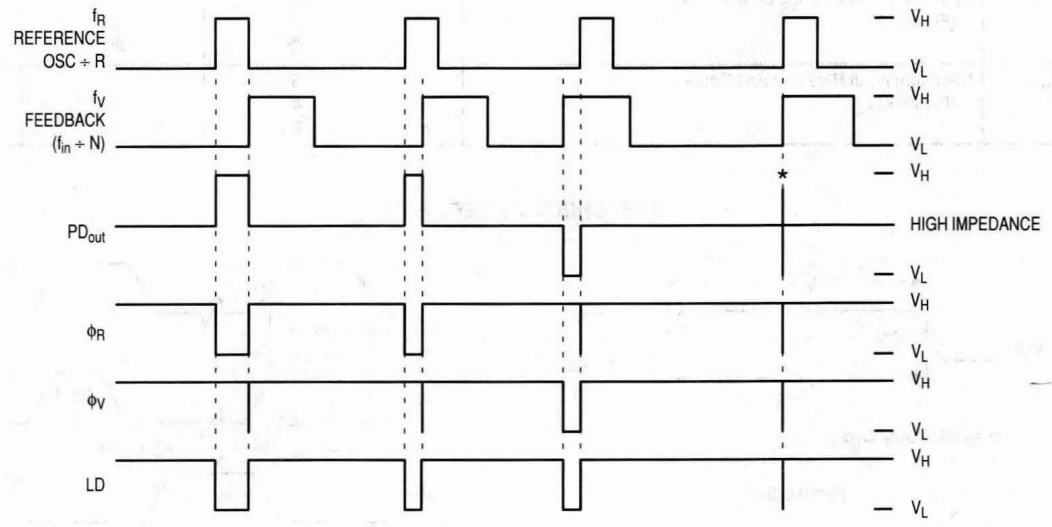


Figure 7.

FREQUENCY CHARACTERISTICS (Voltages References to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ =10 ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1 V p–p ac coupled sine wave	3 5 9	— — —	12 22 25	— — —	12 20 22	— — —	7 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 $V_{in} = V_{DD}$ to V_{SS} dc coupled square wave	3 5 9	— — —	13 25 25	— — —	12 22 25	— — —	8 22 25	MHz

NOTE: Usually, the PLL's propagation delay from f_{in} to MC plus the setup time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P/(t_P + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual modulus prescaler ratios, t_P is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler setup time in seconds.
For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the setup time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P/(t_P + t_{set}) = 64/(70 + 16) = 744$ MHz.



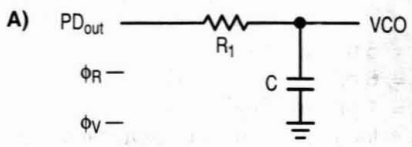
V_H = High Voltage Level.
V_L = Low Voltage Level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid–supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low–pass filter capacitor.

Figure 9. Phase Detector/Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

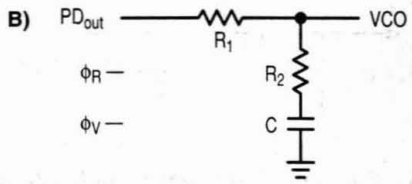


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

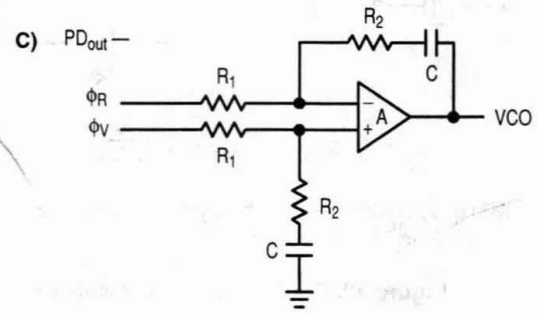


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

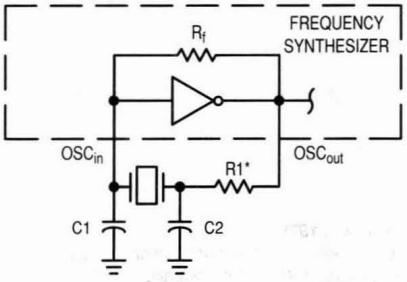
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

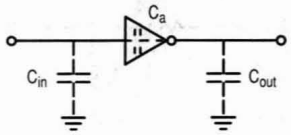
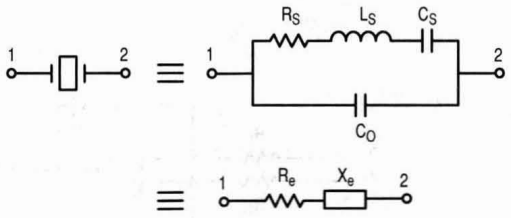


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

Table 1. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145152–2, MC145156–2, or MC145158–2 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12028A	÷ 32/33 or ÷ 64/65	1.1 GHz
MC12052A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12054A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application:

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\,P + A$ or $(P - 1)\,P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

For the maximum frequency into the prescaler (f_{VCOmax}), the value used for P must be large enough such that:

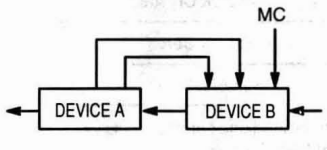
1. f_{VCOmax} divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its MC signal.
   c. Propagation time from f_{in} to the MC output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.

3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable (shown in Figure 13).



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 13. Dual–Modulus Values

MC145159-1

Serial-Input PLL Frequency Synthesizer with Analog Phase Detector

Interfaces with Dual–Modulus Prescalers

The MC145159–1 has a programmable 14–bit reference counter, as well as fully programmable divide–by–N/divide–by–A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

When combined with a loop filter and VCO, this device can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operations, a down mixer or a dual–modulus prescaler can be used between the VCO and the PLL.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- ÷ R Range = 3 to 16383
- ÷ N Range = 16 to 1023, ÷ A Range = 0 to 127
- High–Gain Analog Phase Detector
- See Application Note AN969

P SUFFIX
PLASTIC DIP
CASE 738

DW SUFFIX
SOG PACKAGE
CASE 751D

VF SUFFIX
SSOP
CASE TBD

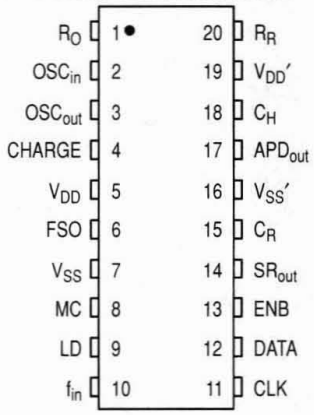
ORDERING INFORMATION

MC145159P1	Plastic DIP
MC145159DW1	SOG Package
MC145159VF1	SSOP

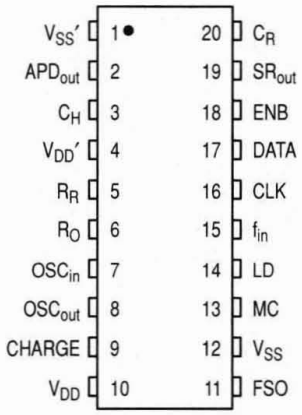
NOT RECOMMENDED FOR NEW DESIGNS;
PRODUCT TO BE PHASED OUT.
Please see the MC14519X and MC14520X series.

PIN ASSIGNMENTS

PLASTIC DIP AND SOG PACKAGE



SSOP



MC145162
MC145162-1

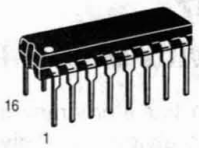
60 MHz and 85 MHz Universal Programmable Dual PLL Frequency Synthesizers
CMOS

The MC145162 is a dual phase–locked loop (PLL) frequency synthesizer especially designed for CT–1 cordless phone applications worldwide. This frequency synthesizer is also for any product with a frequency operation at 60 MHz or below.

The MC145162–1 is a high frequency derivative of the MC145162, for products with operating frequencies of 85 MHz or below.

The device features fully programmable receive, transmit, reference, and auxiliary reference counters accessed through an MCU serial interface. This feature allows this device to operate in any CT–1 cordless phone application. The device consists of two independent phase detectors for transmit and receive loops. A common reference oscillator, driving two independent reference frequency counters, provides independent reference frequencies for transmit and receive loops. The auxiliary reference counter allows the user to select an additional reference frequency for receive and transmit loops if required.

- Operating Voltage Range: 2.5 to 5.5 V
- Operating Temperature Range: – 40 to + 75°C
- Operating Power Consumption: 3.0 mA @ 2.5 V
- Maximum Operating Frequency:
  - MC145162 — 60 MHz @ 200 mV p–p, V_{DD} = 2.5 V
  - MC145162–1 — 85 MHz @ 250 mV p–p, V_{DD} = 2.5 V
- Three or Four Pins Used for Serial MCU Interface
- Built–In MCU Clock Output with Frequency of Reference Oscillator ÷3/÷4
- Power Saving Mode Controlled by MCU
- Lock Detect Signal
- On–Chip Reference Oscillator Supports External Crystals to 16.0 MHz
- Reference Frequency Counter Division Range: 16 to 4095
- Auxiliary Reference Frequency Counter Division Range: 16 to 16,383
- Transmit Counter Division Range: 16 to 65,535
- Receive Counter Division Range: 16 to 65,535



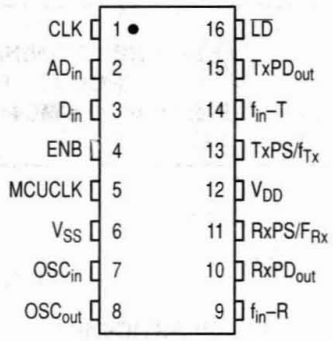
P SUFFIX
PLASTIC DIP
CASE 648

D SUFFIX
SOG PACKAGE
CASE 751B

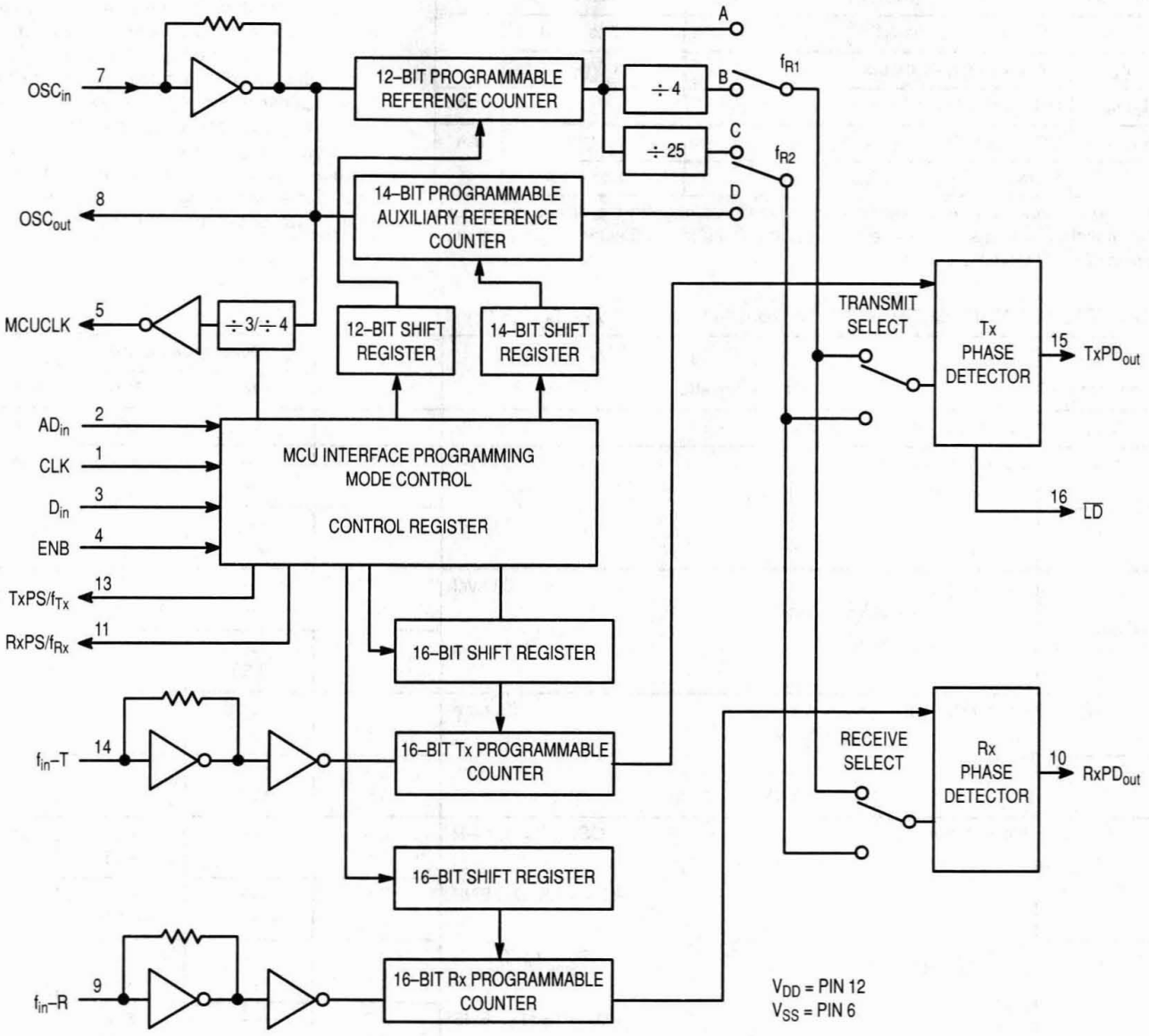
ORDERING INFORMATION

MC145162P	Plastic DIP
MC145162D	SOG Package
MC145162P1	Plastic DIP
MC145162D1	SOG Package

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused pins must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
V_{DD}	Power Supply Voltage Range	—	2.5	5.5	V
V_{OL}	Output Voltage 0 Level (I_{out} = 0)	2.5 5.5	— —	0.1 0.1	V
V_{OH}	(V_{in} = V_{DD} or 0) 1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage 0 Level (V_{out} = 0.5 V or V_{DD} – 0.5 V)	2.5 5.5	— —	0.75 1.65	V
V_{IH}	1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) (V_{out} = 5.0 V) Source	2.5 5.5	– 0.18 – 0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) (V_{out} = 0.5 V) Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0) OSC_{in}, f_{in}–T, f_{in}–R	2.5 5.5	— —	– 30 – 66	µA
	AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	– 1.0 – 1.0	
I_{IH}	(V_{in} = V_{DD} – 0.5) OSC_{in}, f_{in}–T, f_{in}–R	2.5 5.5	— —	30 66	
	AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	5.0 5.0	
I_{OZ}	Three–State Leakage Current (V_{out} = 0 V or 5.5 V)	5.5	—	± 100	nA
C_{in}	Input Capacitance	—	—	8.0	pF
C_{out}	Output Capacitance	—	—	8.0	pF
$I_{DD(stdby)}$	Standby Current (All Counters are in Power–Down Mode with Oscillator On)	2.5 5.5	— —	0.3 1.5	mA
I_{DD}	Operating Current MC145162: 200 mV p–p input at f_{in}–T and f_{in}–R = 60 MHz MC145162–1: 250 mV p–p input at f_{in}–T and f_{in}–R = 85 MHz with OSC = 10.24 MHz	2.5 5.5	— —	3.0 10	mA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic		Figure No.	V_{DD}	Guaranteed Limit		Unit
					Min	Max	
t_{TLH}	Output Rise Time		1	2.5 5.5	— —	200 100	ns
t_{THL}	Output Fall Time		1	2.5 5.5	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time	OSC_{in}	2	2.5 5.5	— —	5.0 4.0	µs
t_w	Input Pulse Width	CLK and ENB	3	2.5 5.5	80 60	— —	ns
f_{max}	Input Frequency Input = Sine Wave @ ≥ 200 mV p–p for MC145162 Input = Sine Wave @ ≥ 250 mV p–p for MC145162–1	OSC_{in} f_{in}–R, f_{in}–T f_{in}–R, f_{in}–T		2.5 – 5.5 2.5 – 5.5 2.5 – 5.5	— — —	16 60 85	MHz
t_{st}	Minimum Start–Up Time					10	ms
t_{su}	Setup Time	DATA to CLK ENB to CLK	5	2.5 5.5	100 200	— —	ns
t_h	Hold Time	CLK to DATA	5	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time	ENB to CLK	5	3.0 5.0	80 40	— —	ns
t_{su1}	Setup Time	ENB to CLK	4	2.5 – 5.5	80	—	ns
t_{h1}	Hold Time	CLK to ENB	4	2.5 – 5.5	600	—	ns
f	Phase Detector Frequency				dc	12.5	kHz
f_{MCUCLK}	Output Clock Frequency (OSC_{in} ÷ 3)	MCUCLK			dc	5.33	MHz

SWITCHING WAVEFORMS

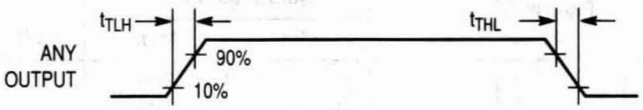


Figure 1.

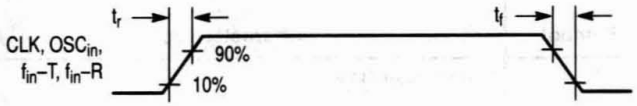


Figure 2.

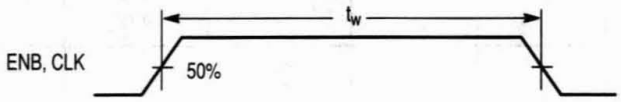


Figure 3.

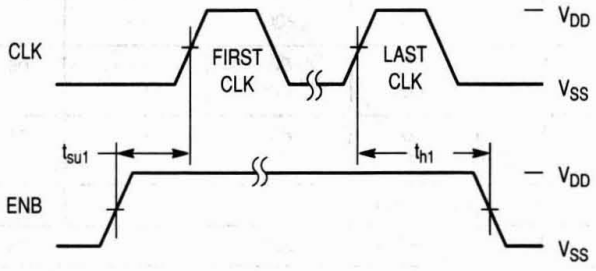


Figure 4. ENB High During Serial Transfer

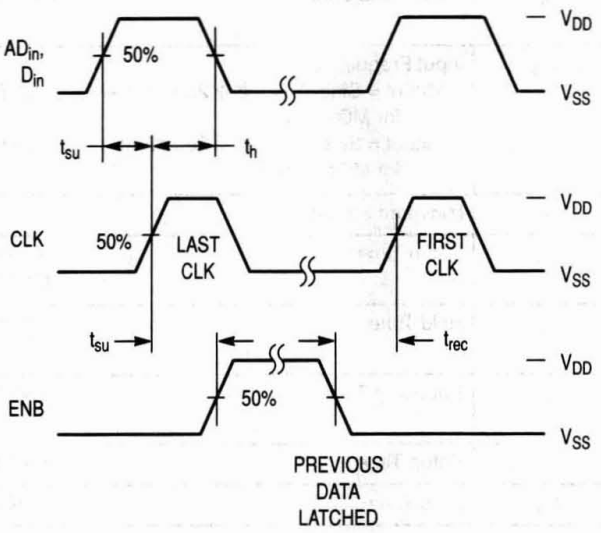


Figure 5. ENB Low During Serial Transfer

PIN DESCRIPTIONS

INPUT PINS

OSC_{in} /OSC_{out}
Reference Oscillator Input/Output (Pins 7, 8)

These pins form a reference oscillator when connected to an external parallel–resonant crystal. Figure 6 shows the relationship of different crystal frequencies and reference frequencies for cordless phone applications in various countries. OSC_{in} may also serve as input for an externally generated reference signal which is typically ac coupled.

MCUCLK
System Clock (Pin 5)

This output pin provides a signal of the crystal frequency (OSC_{out}) divided by 3 or 4 that is controlled by a bit in the control register.

This signal can be a clock source for the MCU or other system clocks.

AD_{in}, D_{in}, CLK, ENB
Auxiliary Data In, Data In, Clock, Enable (Pins 2, 3, 1, 4)

These four pins provide an MCU serial interface for programming the reference counter, the transmit–channel counter, and the receive–channel counter. They also provide various controls of the PLL including the power saving mode and the programming format.

$TxPS/f_{Tx}$, $RxPS/f_{Rx}$
Transmit Power Save, Receive Power Save (Pins 13, 11)

For a normal application, these output pins provide the status of the internal power saving mode operation. If the transmit–channels counter circuitry is in power down mode, $TxPS/f_{Tx}$ outputs a high state. If the receive–channels counter circuitry is in power down mode, $RxPS/f_{Rx}$ is set high. These outputs can be applied for controlling the external power switch for the transmitter and the receiver to save MCU control pins.

In the Tx/Rx channel counter test mode, the $TxPS/f_{Tx}$ and $RxPS/f_{Rx}$ pins output the divided value of the transmit channel counter (f_{Tx}) and the receive channel counter (f_{Rx}), respectively. This test mode operation is controlled by the control register. Details of the counter test mode are in the **Tx/Rx Channel Counter Test** section of this data sheet.

f_{in}–T/f_{in}–R
Transmit/Receive Counter Inputs (Pins 14, 9)

f_{in}–T and f_{in}–R are inputs to the transmit and the receive counters, respectively. These signals are typically driven from the loop VCO and ac coupled. The minimum input signal level is 200 mV p–p @ 60.0 MHz.

OUTPUT PINS

$TxPD_{out}$/$RxPD_{out}$
Transmit/Receive Phase Detector Outputs (Pins 15, 10)

These are three–state outputs of the transmit and receive phase detectors for use as loop error signals (see Figure 7 for phase detector output waveforms). Phase detector gain is $V_{DD}/4\ \pi$ volts per radian.

Frequency $f_V > f_R$ or f_V leading: output = negative pulse.
Frequency $f_V < f_R$ or f_V lagging: output = positive pulse.
Frequency $f_V = f_R$ and phase coincidence: output = high–impedance state.
NOTE: f_R is the divided–down reference frequency at the phase detector input and f_V is the divided–down VCO frequency at the phase detector input.

$\overline{LD}$
Lock Detect (Pin 16)

The lock detect signal is associated with the transmit loop. The output at a high level indicates an out–of–lock condition (see Figure 7 for the $\overline{LD}$ output waveform).

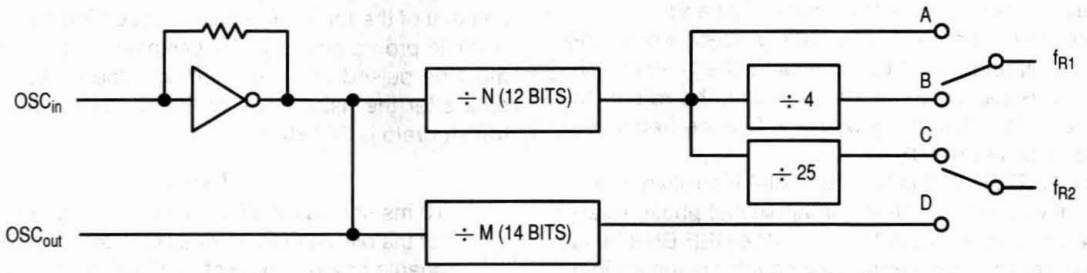
POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 12)

V_{DD} is the most positive power supply potential ranging from 2.5 to 5.5 V with respect to V_{SS}.

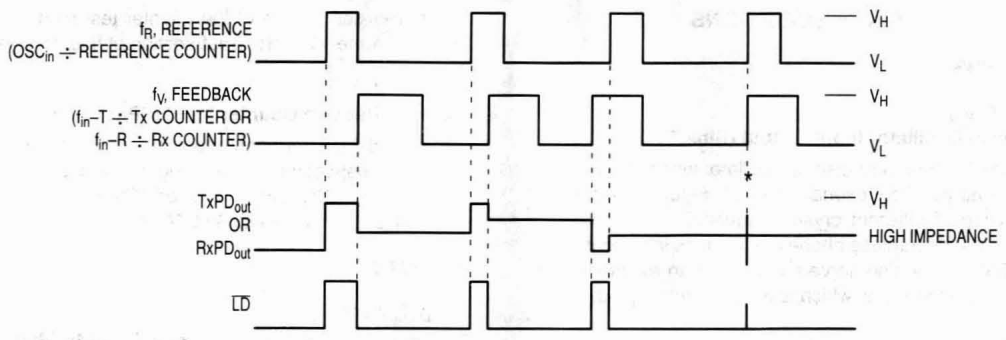
V_{SS}
Negative Power Supply (Pin 6)

V_{SS} is the most negative supply potential and is usually connected to ground.



Crystal	÷ N Value	$f_{R1 \rightarrow B}$	$f_{R2 \rightarrow C}$
11.150 MHz	446	6.25 kHz	1.0 kHz
11.150 MHz	223	12.5 kHz	
10.240 MHz	512	5.0 kHz	
12.000 MHz	600	5.0 kHz	

Figure 6. Reference Frequencies for Cordless Phone Applications of Various Countries



V_H = High voltage level.
V_L = Low voltage level.
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.

NOTE: The $TxPD_{out}$ and $RxPD_{out}$ generate error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 7. Phase Detector/Lock Detector Output Waveforms

MCU PROGRAMMING SCHEME

The MCU programming scheme is defined in two formats controlled by the ENB input. If the enable signal is high during the serial data transfer, control register/reference frequency programming is selected. If the ENB is low, programming of the transmit and receive counters is selected. During programming of the transmit and receive counters, both AD_{in} and D_{in} pins can input the data to the transmit and receive counters. Both counters' data is clocked into the PLL internal shift register at the leading edge of the CLK signal. It is not necessary to reprogram the reference frequency counter/control register when using the enable signal to program the transmit/receive channels.

In programming the control register/reference frequency scheme, the most significant bit (MSB) of the programming word identifies whether the input data is the control word or the reference frequency data word. If the MSB is 1, the input data is the control word (Figure 8). Also see Figure 8 and Table 1 for control register and bit function. If the MSB is 0, the input data is the reference frequency (Figure 9).

The reference frequency data word is a 32–bit word containing the 12–bit reference frequency data, the 14–bit auxiliary reference frequency counter information, the reference frequency selection plus, the auxiliary reference frequency counter enable bit (Figure 9).

If the AUX REF ENB bit is high, the 14–bit auxiliary reference frequency counter provides an additional phase reference frequency output for the loops. If AUX REF ENB bit is low, the auxiliary reference frequency counter is forced into power–down mode for current saving. (Other power down modes are also provided through the control register per Table 2 and Figure 8.) At the falling edge of the ENB signal, the data is stored in the registers.

There are two interfacing schemes for the universal channel mode: the three–pin and the four–pin interfacing schemes. The three–pin interfacing scheme is suited for use with the MCU SPI (serial peripheral interface) (Figure 10), while the four–pin interfacing scheme is commonly used for general I/O port connection (Figure 11).

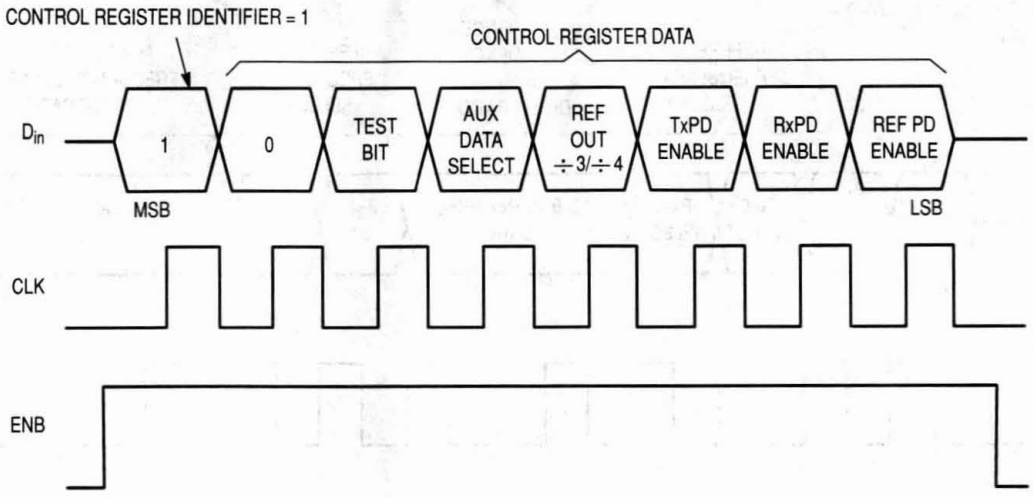
For the three–pin interfacing scheme, the auxiliary data select bit is set to 0. All 32 bits of data, which define both the 16–bit transmit counter and the 16–bit receive counter, latch into the PLL internal register through the data in pins at the leading edge of CLK. See Figures 12 and 13.

For the four–pin interfacing scheme, the auxiliary data select bit is set to 1. In this scheme, the 16–bit transmit counter's data enters into the AD_{in} pin at the same time as the 16–bit receive counter's data enters into the D_{in} pin. This simultaneous entry of the transmit and receive counters causes the programming period of the four–pin scheme to be half that of the three–pin scheme (see Figures 14 and 15).

While programming Tx/Rx Channel Counter, the ENB pin must be pulsed to provide falling edge to latch the shifted data after the rising edge of the last clock. Maximum data transfer rate is 500 kbps.

NOTE

10 ms should be allowed for initial start–up time for the oscillator to allow all registers to clear and enable programming of new register values.



NOTE: ENB must be high during the serial transfer.

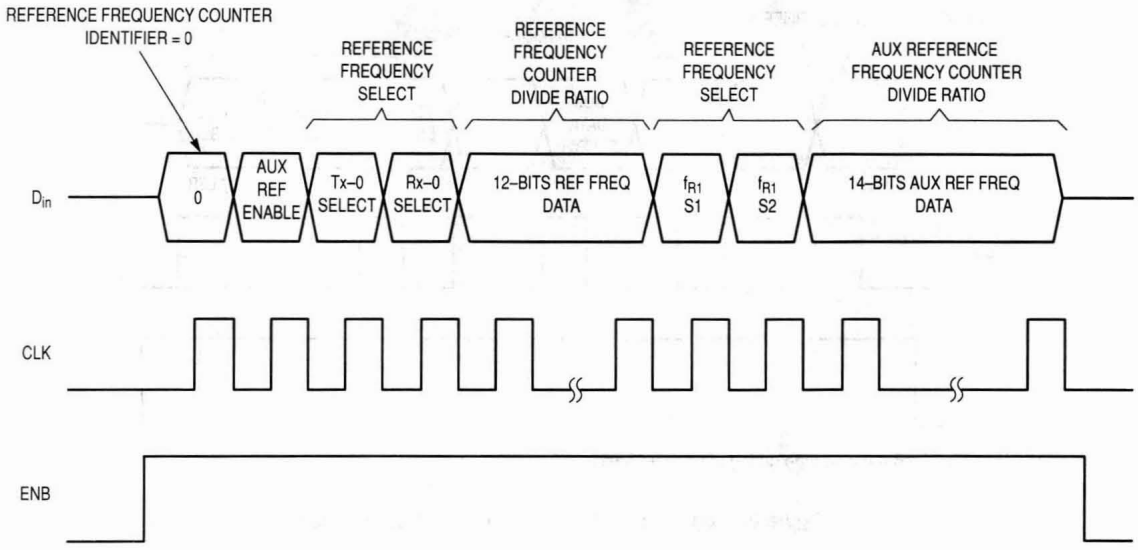
Figure 8. Programming Format of the Control Register

Table 1. Control Register Function Bits Description

Test Bit	Set to 1 for Tx/Rx channel counter test mode Set to 0 for normal application
Aux Data Select	Set to 1 for both AD_{in} and D_{in} pins inputting the transmit 16–bits data and receive 16–bits data respectively. Set to 0 for normal application interfacing with MCU serial peripheral interface. Does not use AD_{in} pin; tie AD_{in} to V_{SS}.
$REF_{out} \div 3/\div 4$	If set to 1, REF_{out} output frequency is equal to $OSC_{out} \div 3$. If set to 0, REF_{out} output is $OSC_{out} \div 4$.
TxPD Enable	If set to 1, the transmit counter, transmit phase detector, and the associated circuitry is in power–down mode. Tx PS/f_{Tx} is set "High".
RxPD Enable	If set to 1, the receive counter, receive phase detector, and the associated circuitry is in power–down mode. Rx PS/f_{Rx} is set "High".
Ref PD Enable	If set to 1, both 12–bit and 14–bit reference frequency counters are in power–down mode.

Table 2. Control Register Power Down Bits Function

TxPD Enable	RxPD Enable	REF PD Enable	Tx–Channel Counter	Rx–Channel Counter	Reference Frequency Counter
0	0	0	—	—	—
0	0	1	—	—	Power Down
0	1	0	—	Power Down	—
0	1	1	—	Power Down	Power Down
1	0	0	Power Down	—	—
1	0	1	Power Down	—	Power Down
1	1	0	Power Down	Power Down	—
1	1	1	Power Down	Power Down	Power Down



NOTE: ENB must be high during the serial transfer.

Figure 9. Programming Format of the Auxiliary/Reference Frequency Counters

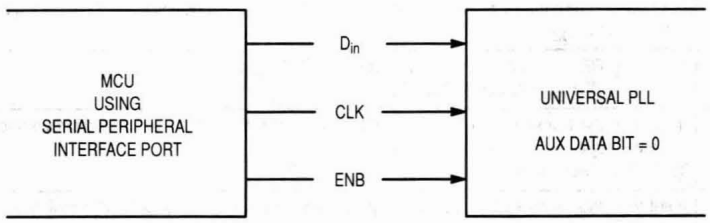


Figure 10. MCU Interface Using SPI

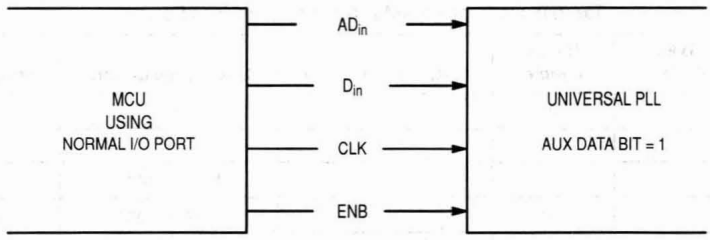
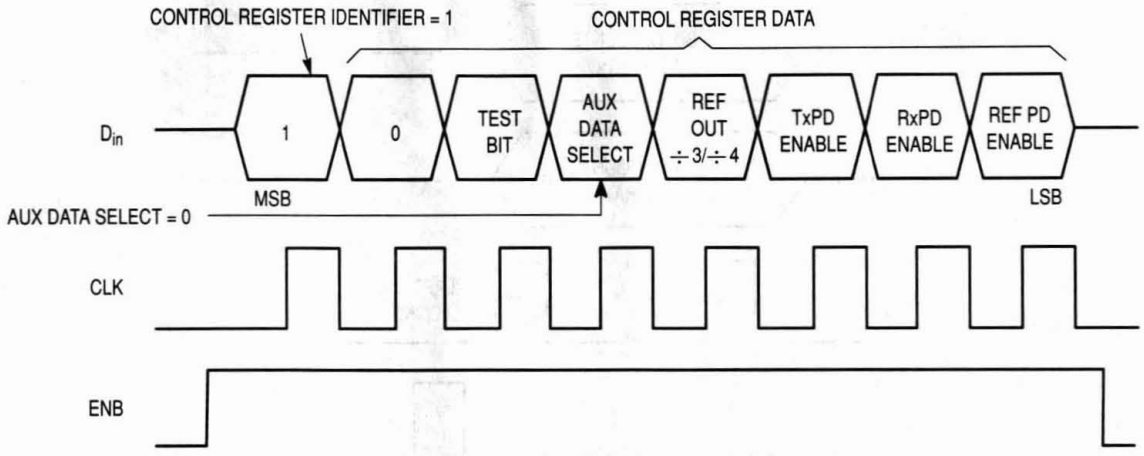
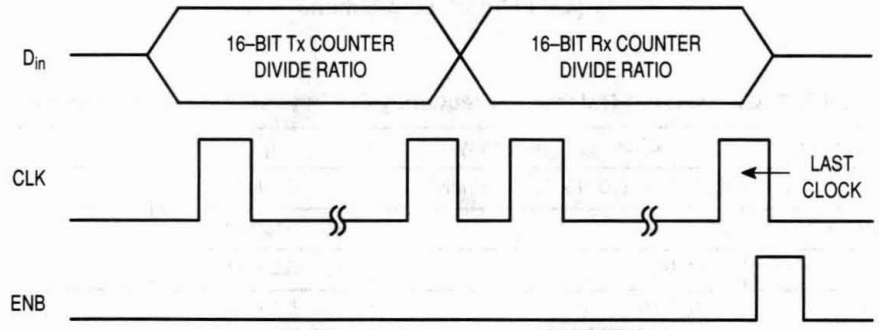


Figure 11. MCU Interface Using Normal I/O Ports with Both D_{in} and AD_{in} for Faster Programming Time



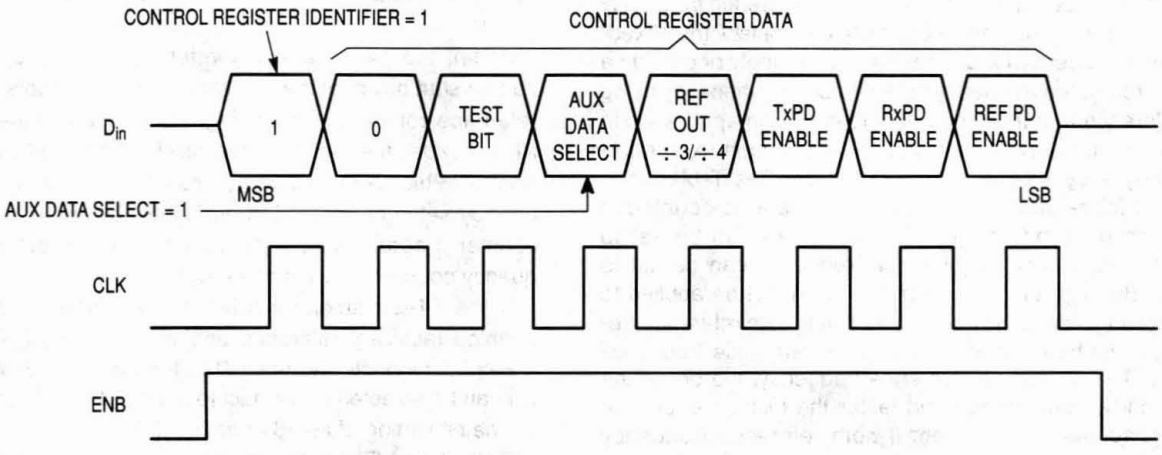
NOTE: ENB must be high during the serial transfer.

Figure 12. Programming Format for Control Register (3–Pin Interfacing Scheme)



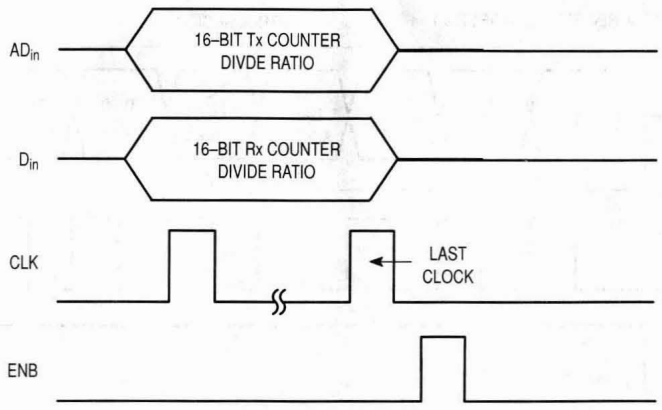
NOTE: ENB must be low during the serial transfer.

Figure 13. Programming Format for Transmit and Receive Counters (3–Pin Interfacing Scheme)



NOTE: ENB must be high during the serial transfer.

Figure 14. Programming Format for Control Register (4–Pin Interfacing Scheme)



NOTE: ENB must be low during the serial transfer.

Figure 15. Programming Format for Transmit and Receive Counters (4–Pin Interfacing Scheme)

Table 3. Global CT–1 Reference Frequency Setting vs Channel Frequencies

Country	Channels Frequency	f_{R1}	f_{R2}
U.S.A.	46/49 MHz (10, 15, 25 Channels)	5.0 kHz	—
France	26/41 MHz	6.25 kHz/12.5 kHz	—
Spain	31/41 MHz	5.0 kHz	—
Australia	30/39 MHz	5.0 kHz	—
U.K.	1.7/47 MHz	6.25 kHz	1.0 kHz
New Zealand	1.7/34/40 MHz	6.25 kHz	1.0 kHz

REFERENCE FREQUENCY SELECTION AND PROGRAMMING

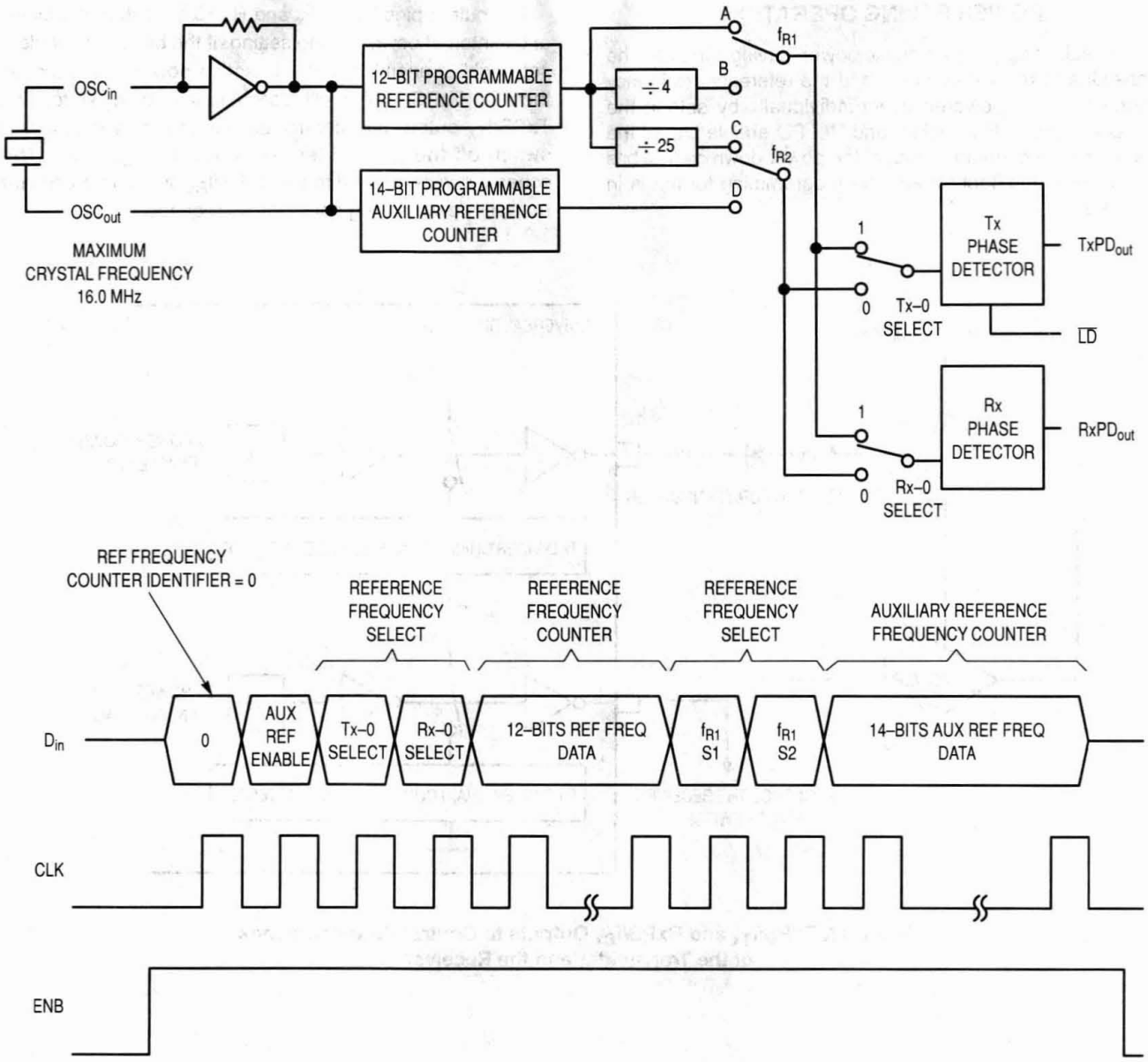
Figure 16 shows the bit function of the reference frequency programming word. The user can either select the "fixed" reference frequency for all channels accordingly or provide a specific reference frequency for a particular channel by using two reference frequency counters (e.g., for an application in France, the base set transmit channel common fixed reference frequency is 6.25 kHz or 12.5 kHz). (See Table 3 and Figure 6 for reference frequencies for various countries.) However, transmit channels 6, 8, and 14 can be set to 25 kHz, and channel 8 reference frequency can be set to 50 kHz. But this reference frequency may not be applied to the receiving side; therefore, the receiving side reference frequency must be generated by another reference frequency counter. The higher the reference frequency, the better the phase noise performance and faster the lock time, but the PLL consumes more current if both reference frequency counters are in operation.

In general, the 12–bit reference frequency counter plus the ÷ 4 and ÷ 25 module can offer all the reference frequencies for global CT–1 transmit and receive channel requirements. Users can select their own reference frequency by introducing the additional 14–bit auxiliary reference frequency counter.

Again, the 14–bit auxiliary reference frequency counter can be shut down by the auxiliary reference enable bit in the reference counter programming word by setting the bit to 0. At this state, the f_{R2} is automatically connected to point C (the ÷ 25 block output), and f_{R1} can be connected to point A or B by setting the f_{R1}–S1 and f_{R1}–S2 bits in the reference counter program word. The 14–bit auxiliary reference frequency counter data will be in "Don't Care" state.

If the 14–bit auxiliary reference frequency counter is enabled (auxiliary reference enable = 1), then f_{R2} is automatically connected to point D (14–bit counter output), and f_{R1} can be selected to connect to point A, B, or C, depending on the bit setting of f_{R1}–S1 and f_{R1}–S2.

Table 4 and Figure 16 describe the functions of the auxiliary reference enable bit and the f_{R1}–S1 and f_{R1}–S2 bits selection.



NOTE: ENB must be high during the serial transfer.

Figure 16. Reference Frequency Counter/Selection Programming Mode

Table 4. Bit Function and the Reference Frequency Selection Bit Setting of the Reference Frequency Counter Programming Word

AUX REF Enable	Auxiliary Reference Frequency Counter Mode	Module Select	f_{R1} S1	f_{R1} S2	f_{R1} Routing
0	14–Bit Auxiliary Reference Frequency Counter Disable	$f_{R2} \rightarrow C$	0	0	N/A
			0	1	$f_{R1} \rightarrow A$
			1	0	$f_{R1} \rightarrow B$
			1	1	N/A
1	14–Bit Auxiliary Reference Frequency Counter Enable	$f_{R2} \rightarrow D$	0	0	N/A
			0	1	$f_{R1} \rightarrow A$
			1	0	$f_{R1} \rightarrow B$
			1	1	$f_{R1} \rightarrow C$

N/A = Not Applicable

POWER SAVING OPERATION

This PLL has a programmable power–saving scheme. The transmit and receive counters and the reference frequency counter can be powered down individually by setting the TxPD enable, RxPD enable, and Ref PD enable bits of the control register. The functions of the power down control bits are explained in Table 2 and the programming format is in Figure 8.

The output pins TxPS/f_{Tx} and RxPS/f_{Rx} output the status of the internal power saving setting. If the bit TxPD enable is set "high" (transmit counter is set to power–down mode), then the TxPS/f_{Tx} pin will also output a "high" state. This TxPS/f_{Tx} output can control an external power switch to switch off the transmitter, as shown in Figure 17. This scheme can be applied to the RxPS/f_{Rx} output to control the receiver power saving operation as required.

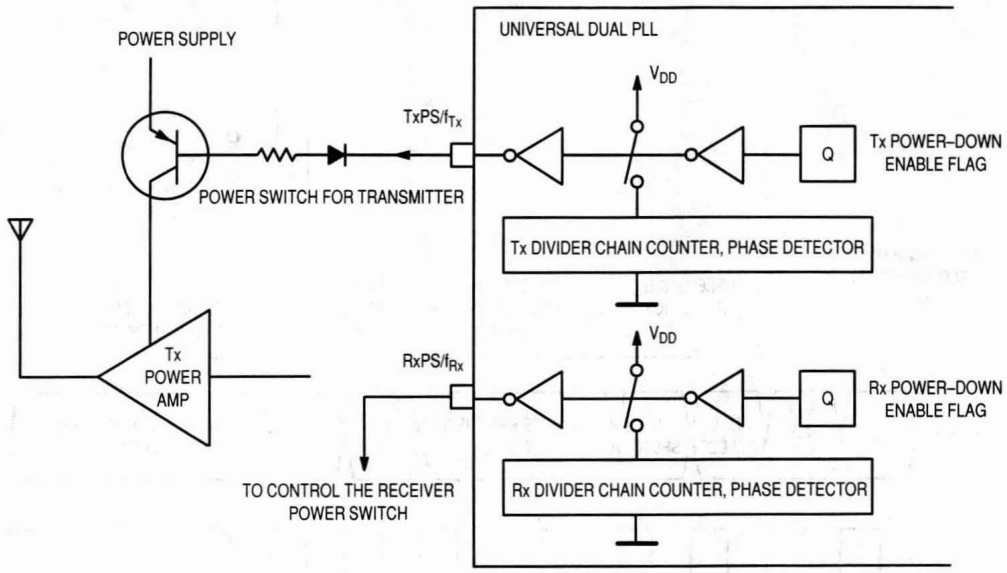


Figure 17. TxPS/f_{Tx} and RxPS/f_{Rx} Outputs to Control Power Switches of the Transmitter and the Receiver

Tx/Rx CHANNEL COUNTER TEST

In normal applications, the TxPS/f_{Tx} and the RxPS/f_{Rx} output pins indicate the power saving mode status. However, the user can examine the Tx and Rx channel counter outputs by setting the Test bit in the control register to 1. The final value of the transmit–channel counter and the receive–channel counter multiplex out to TxPS/f_{Tx} and RxPS/f_{Rx} respectively. The user can verify the divided–down output waveform associated with the RF input level in the PLL circuitry implementation (Figure 18).

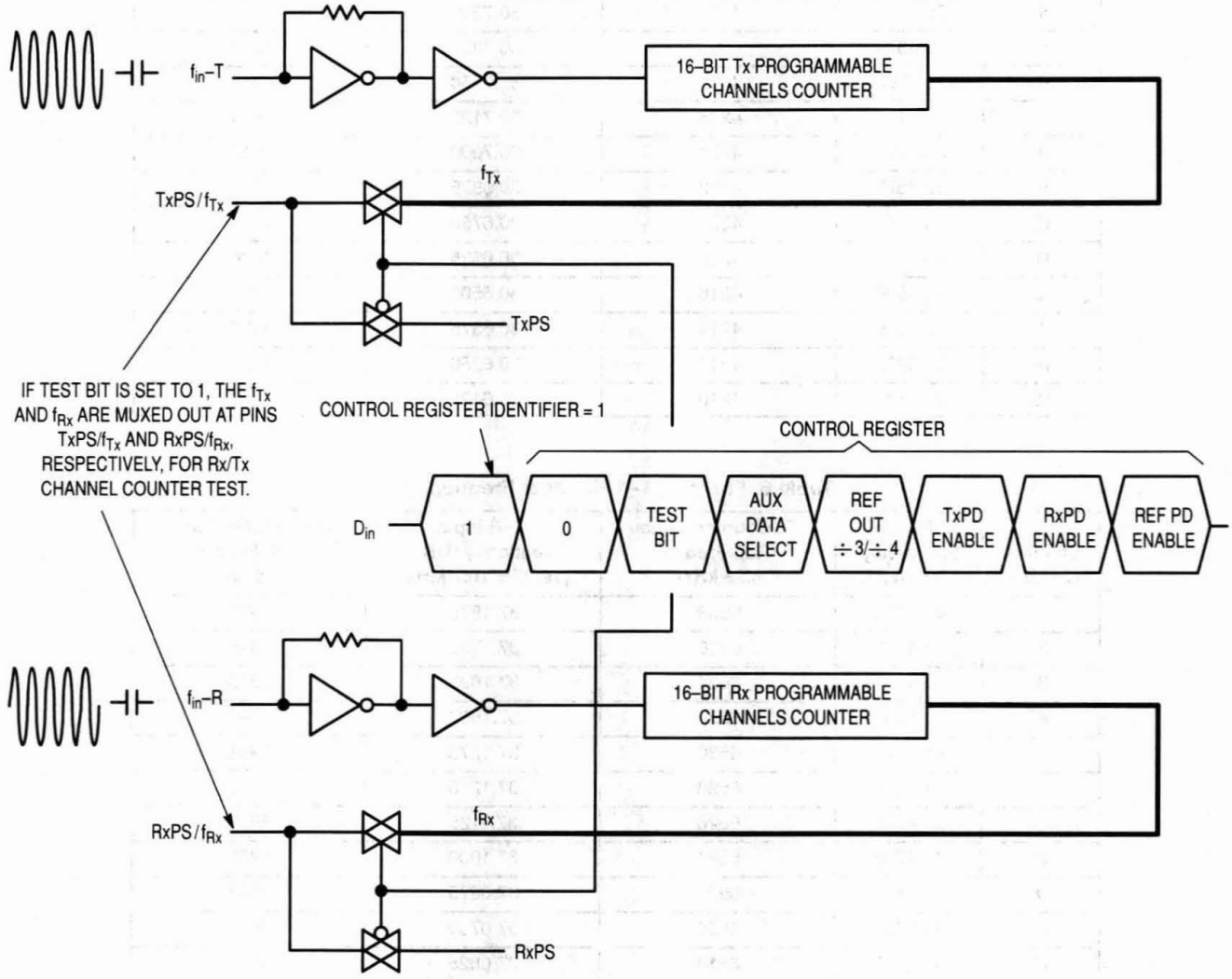


Figure 18. RF Buffer Sensitivity

Table 5. France CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	26.4875	4238	30.7875	4926
2	26.4750	4236	30.7750	4924
3	26.4625	4234	30.7625	4922
4	26.4500	4232	30.7500	4920
5	26.4375	4230	30.7375	4918
6	26.4250	4228	30.7250	4916
7	26.4125	4226	30.7125	4914
8	26.4000	4224	30.7000	4912
9	26.3875	4222	30.6875	4910
10	26.3750	4220	30.6750	4908
11	26.3625	4218	30.6625	4906
12	26.3500	4216	30.6500	4904
13	26.3375	4214	30.6375	4902
14	26.3250	4212	30.6250	4900
15	26.3125	4210	30.6125	4898

Table 6. France CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	41.4875	6638	37.1875	5950
2	41.4750	6636	37.1750	5948
3	41.4625	6634	37.1625	5946
4	41.4500	6632	37.1500	5944
5	41.4375	6630	37.1375	5942
6	41.4250	6628	37.1250	5940
7	41.4125	6626	37.1125	5938
8	41.4000	6624	37.1000	5936
9	41.3875	6622	37.0875	5934
10	41.3750	6620	37.0750	5932
11	41.3625	6618	37.0625	5930
12	41.3500	6616	37.0500	5928
13	41.3375	6614	37.0375	5926
14	41.3250	6612	37.0250	5924
15	41.3125	6610	37.0125	5922

Table 7. Spain CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	31.0250	6205	29.2300	5846
2	31.0500	6210	29.2550	5851
3	31.0750	6215	29.2800	5856
4	31.1000	6220	29.3050	5861
5	31.1250	6225	29.3300	5866
6	31.1500	6230	29.3550	5871
7	31.1750	6235	29.3800	5876
8	31.2000	6240	29.4050	5881
9	31.2500	6250	29.4550	5891
10	31.2750	6255	29.4800	5896
11	31.3000	6260	29.5050	5901
12	31.3250	6265	29.5300	5906

Table 8. Spain CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.9250	7985	20.3300	4066
2	39.9500	7990	20.3550	4071
3	39.9750	7995	20.3800	4076
4	40.0000	8000	20.4050	4081
5	40.0250	8005	20.4300	4086
6	40.0500	8010	20.4550	4091
7	40.0750	8015	20.4800	4096
8	40.1000	8020	20.5050	4101
9	40.1500	8030	20.5550	4111
10	40.1750	8035	20.5800	4116
11	40.2000	8040	20.6050	4121
12	40.2250	8045	20.6300	4126

Table 9. New Zealand CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.7820	1782	29.7625	4762
2	1.7620	1762	29.7500	4760
3	1.7420	1742	29.7375	4758
4	1.7220	1722	29.7250	4756
5	1.7020	1702	29.7125	4754
6	34.3500	5496	29.7000	4752
7	34.3625	5498	29.6875	4750
8	34.3750	5500	29.6750	4748
9	34.3875	5502	29.6625	4746
10	34.4000	5504	29.6500	4744

Ref Freq = 1.0 kHz

Ref Freq = 6.25 kHz

Table 10. New Zealand CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz)	Rx Counter Value
1	40.4625	6474	2.2370	2237
2	40.4500	6472	2.2170	2217
3	40.4375	6470	2.1970	2197
4	40.4250	6468	2.1770	2177
5	40.4125	6466	2.1570	2157
6	40.4000	6464	23.6500	3784
7	40.3875	6462	23.6625	3786
8	40.3750	6460	23.6750	3788
9	40.3625	6458	23.6875	3790
10	40.3500	6456	23.7000	3792

Ref Freq = 455 kHz

Ref Freq = 1.0 kHz

Ref Freq = 10.7 kHz

Ref Freq = 6.25 kHz

Table 11. Australia CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	30.0750	6015	29.0800	5816
2	30.1250	6025	29.1300	5826
3	30.1750	6035	29.1800	5836
4	30.2250	6045	29.2300	5846
5	30.2750	6055	29.2800	5856
6	30.1000	6020	29.1050	5821
7	30.1500	6030	29.1550	5831
8	30.2000	6040	29.2050	5841
9	30.2500	6050	29.2550	5851
10	30.3000	6060	29.3050	5861

Table 12. Australia CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.7750	7955	19.3800	3876
2	39.8250	7965	19.4300	3886
3	39.8750	7975	19.4800	3896
4	39.9250	7985	19.5300	3906
5	39.9750	7995	19.5800	3916
6	39.8000	7960	19.4050	3881
7	39.8500	7970	19.4550	3891
8	39.9000	7980	19.5050	3901
9	39.9500	7990	19.5550	3911
10	40.0000	8000	19.6050	3921

Table 13. U.K. CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 1.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.6420	1642	36.75625	5881
2	1.6620	1662	36.76875	5883
3	1.6820	1682	36.78125	5885
4	1.7020	1702	36.79375	5887
5	1.7220	1722	36.80625	5889
6	1.7420	1742	36.81875	5891
7	1.7620	1762	36.83125	5893
8	1.7820	1782	36.84375	5895

Table 14. U.K. CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 455 kHz]	Rx Counter Value (Ref. Freq. = 1.00 kHz)
1	47.45625	7593	2.097	2097
2	47.46875	7595	2.117	2117
3	47.48125	7597	2.137	2137
4	47.49375	7599	2.157	2157
5	47.50625	7601	2.177	2177
6	47.51875	7603	2.197	2197
7	47.53125	7605	2.217	2217
8	47.54375	7607	2.237	2237

Table 15. U.S.A. (10 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855

Table 16. U.S.A. (10 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255

Table 17. U.S.A. (25 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	43.72	8744	38.06	7612
2	43.74	8748	38.14	7628
3	43.82	8764	38.16	7632
4	43.84	8768	38.22	7644
5	43.92	8784	38.32	7664
6	43.96	8788	38.38	7676
7	44.12	8824	38.40	7680
8	44.16	8832	38.46	7692
9	44.18	8836	38.50	7700
10	44.20	8840	38.54	7708
11	44.32	8864	38.58	7716
12	44.36	8872	38.66	7732
13	44.40	8880	38.70	7740
14	44.46	8892	38.76	7752
15	44.48	8896	38.80	7760
16	46.61	9322	38.97	7794
17	46.63	9326	39.145	7829
18	46.67	9334	39.16	7832
19	46.71	9342	39.07	7814
20	46.73	9346	39.175	7835
21	46.77	9354	39.13	7826
22	46.83	9366	39.19	7838
23	46.87	9374	39.23	7846
24	46.93	9386	39.29	7858
25	46.97	9394	39.27	7854

Table 18. U.S.A. (25 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.76	9752	33.02	6604
2	48.84	9768	33.04	6608
3	48.86	9772	33.12	6624
4	48.92	9748	33.14	6628
5	49.02	9804	33.22	6644
6	49.08	9816	33.26	6652
7	49.10	9820	33.42	6684
8	49.16	9832	33.46	6692
9	49.20	9840	33.48	6696
10	49.24	9848	33.50	6700
11	49.28	9856	33.62	6724
12	49.36	9872	33.66	6732
13	49.40	9880	33.70	6740
14	49.46	9892	33.76	6752
15	49.50	9900	33.78	6756
16	49.67	9934	33.91	7182
17	49.845	9969	33.93	7186
18	49.86	9972	33.97	7194
19	49.77	9954	36.01	7202
20	49.875	9975	36.03	7206
21	49.83	9966	36.07	7214
22	49.89	9978	36.13	7226
23	49.93	9986	36.17	7234
24	49.99	9998	36.23	7246
25	49.97	9994	36.27	7254

Table 19. Korea CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

Table 20. Korea CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	49.725	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

Table 21. China CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	45.250	9050	37.550	7510
2	45.275	9055	37.575	7515
3	45.300	9060	37.600	7520
4	45.325	9065	37.625	7525
5	45.350	9070	37.650	7530
6	45.375	9075	37.675	7535
7	45.400	9080	37.700	7540
8	45.425	9085	37.725	7545
9	45.450	9090	37.750	7550
10	45.475	9095	37.775	7555

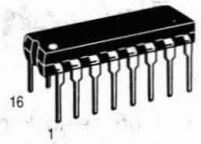
Table 22. China CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.250	9650	34.550	6910
2	48.275	9655	34.575	6915
3	48.300	9660	34.600	6920
4	48.325	9665	34.625	6925
5	48.350	9670	34.650	6930
6	48.375	9675	34.675	6935
7	48.400	9680	34.700	6940
8	48.425	9685	34.725	6945
9	48.450	9690	34.750	6950
10	48.475	9695	34.775	6955

MC145165

Low-Voltage 60 MHz Universal Programmable Dual PLL Frequency Synthesizer

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC145165P	Plastic DIP
MC145165D	SOG Package

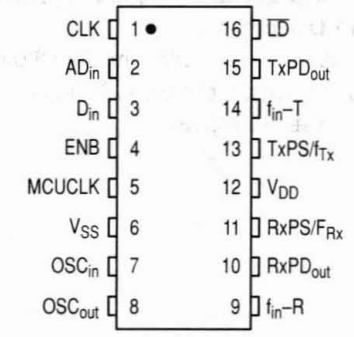
The MC145165 is a low–voltage dual phase–locked loop (PLL) frequency synthesizer especially designed for CT–1 cordless phone applications worldwide. This frequency synthesizer is also for any product with a frequency operation at 60 MHz or below.

This chip is suitable for any portable RF products which use two 1.2 V chargeable Ni–Cd batteries. The feature of low operating voltage can reduce the current consumption and the cost of the portable RF products by reducing the number of batteries used.

The device features fully programmable receive, transmit, reference, and auxiliary reference counters accessed through an MCU serial interface. This feature allows this device to operate in any CT–1 cordless phone application. The device consists of two independent phase detectors for transmit and receive loops. A common reference oscillator, driving two independent reference frequency counters, provides independent reference frequencies for transmit and receive loops. The auxiliary reference counter allows the user to select an additional reference frequency for receive and transmit loops if required. All of the functions and features of the MC145165 are fully compatible with the MC145162.

- Operating Voltage Range: 1.8 to 3.6 V
- Operating Temperature Range: – 40 to + 75°C
- Operating Power Consumption: 1.5 mA @ 1.8 V
- Maximum Operating Frequency: 60 MHz
- Minimum Input Sensitivity: 60 MHz @ 200 mV p–p, V_{DD} = 1.8 V
- Three or Four Pins Used for Serial MCU Interface
- Built–In MCU Clock Output with Frequency of Reference Oscillator ÷3/÷4
- Power Saving Mode Controlled by MCU
- Lock Detect Signal
- On–Chip Reference Oscillator Supports External Crystals to 16.0 MHz
- Reference Frequency Counter Division Range: 16 to 4095
- Auxiliary Reference Frequency Counter Division Range: 16 to 16,383
- Transmit Counter Division Range: 16 to 65,535
- Receive Counter Division Range: 16 to 65,535

PIN ASSIGNMENT



NOT RECOMMENDED FOR NEW DESIGNS;
PRODUCT TO BE PHASED OUT.
The MC145162 is a drop–in replacement for supply voltages ≥ 2.5 V.

MC145166
MC145167

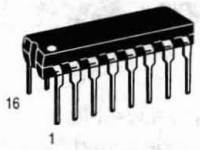
Dual PLLs for 46/49 MHz Cordless Telephones
CMOS

These devices are dual phase–locked loop (PLL) frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 10 channels. These parts contain two mask–programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

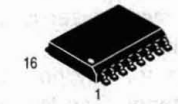
Frequency selection is accomplished via a 4–bit parallel input for the MC145166. The MC145167 utilizes a serial interface.

Other features include a lock detect circuit for the transmit loop, illegal code default, and a 5 kHz tone output.

- Synthesizes Up to Ten Channel Pairs
- Maximum Operating Frequency: 60 MHz @ V_{in} = 200 mV p–p
- Operating Temperature Range: – 40 to + 75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On–Chip Oscillator Circuit Supports External Crystal
- Lock Detect Signal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V
- Also See MC145162



P SUFFIX
PLASTIC DIP
CASE 648



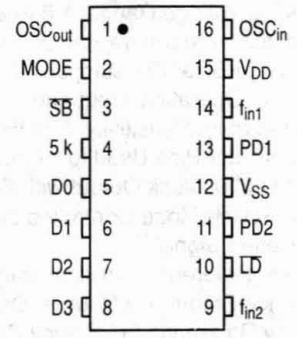
DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

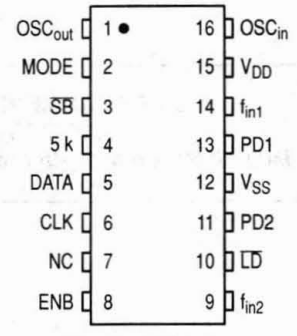
MC145166P	Plastic DIP
MC145166DW	SOG Package
MC145167P	Plastic DIP
MC145167DW	SOG Package

PIN ASSIGNMENTS

MC145166P
MC145166DW

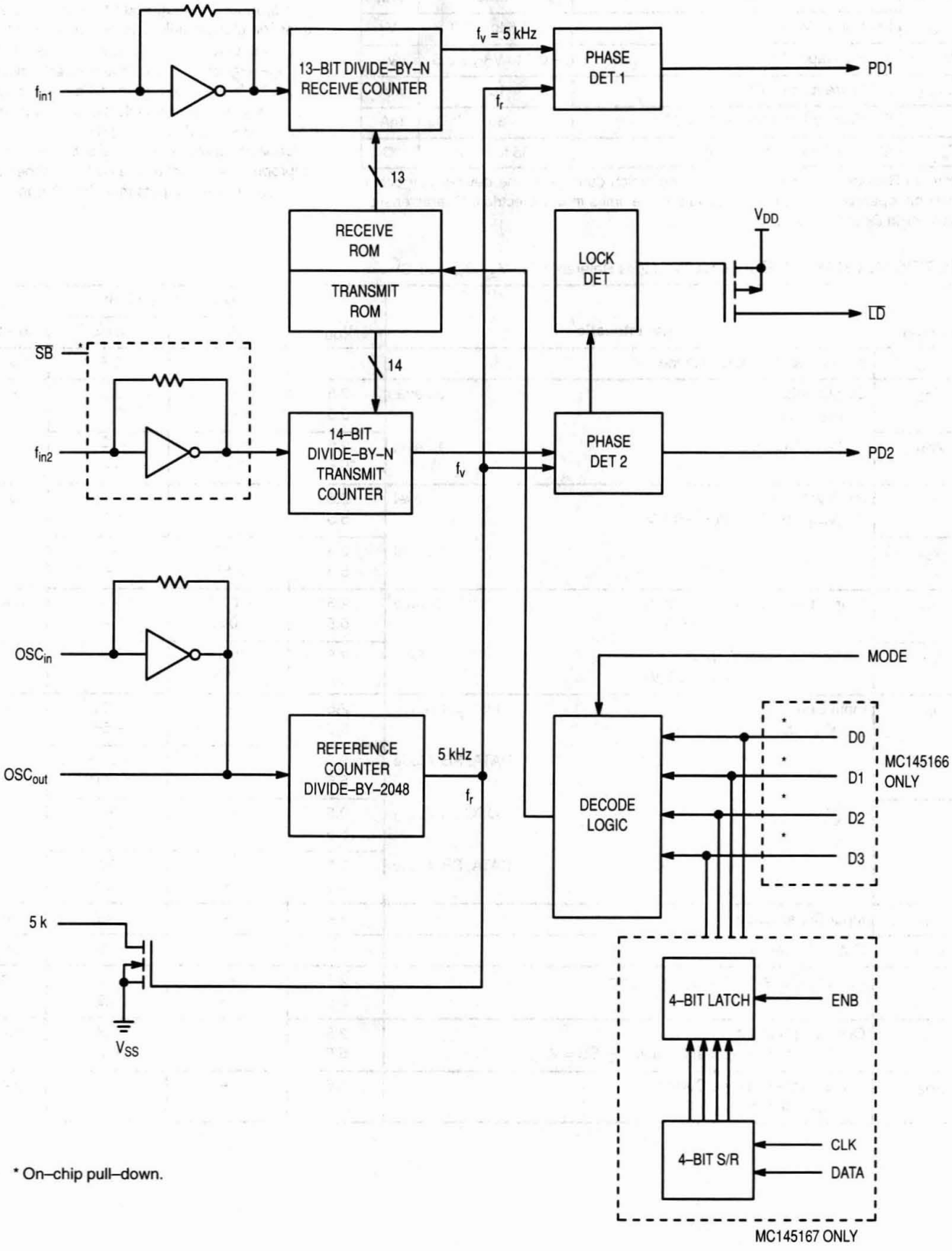


MC145167P
MC145167DW



NC = NO CONNECTION

BLOCK DIAGRAM



* On–chip pull–down.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
V_{DD}	Power Supply Voltage Range	—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out} = 0) 0 Level	2.5 5.5	— —	0.05 0.05	V
V_{OH}	(V_{in} = V_{DD} or 0) 1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out} = 0.5 V or V_{DD} – 0.5 V) 0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}	1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) Source (V_{out} = 5.0 V)	2.5 5.5	– 0.18 – 0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) Sink (V_{out} = 0.5 V)	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0) OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	– 30 – 66	µA
	DATA, $\overline{SB}$, Mode	2.5 5.5	— —	– 0.05 – 0.11	
I_{IH}	(V_{in} = V_{DD} – 0.5) OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
	DATA, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance	—	—	14.0	pF
C_{out}	Output Capacitance	—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$ = V_{SS} or Open	2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mV p–p input at f_{in1} and f_{in2}, $\overline{SB}$ = V_{DD})	2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three–State Leakage Current (V_{out} = 0 or 5.5 V)	5.5	—	± 1.0	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time	1, 5	3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time	1, 5	3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in}	2	3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency OSC_{in} Input = Sine Wave 200 mV p–p f_{in1} f_{in2}		3.0 – 5.0 3.0 – 5.0 3.0 – 5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145167) DATA to CLK	3	3.0 5.0	100 50	— —	ns
	ENB to CLK		3.0 5.0	200 100	— —	
t_h	Hold Time (MC145167), CLK to DATA	3	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145167), ENB to CLK	3	3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145167), CLK and ENB	4	3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

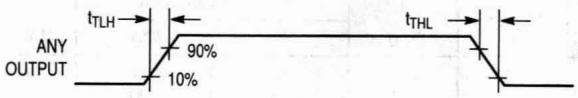


Figure 1.

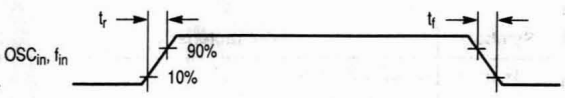


Figure 2.

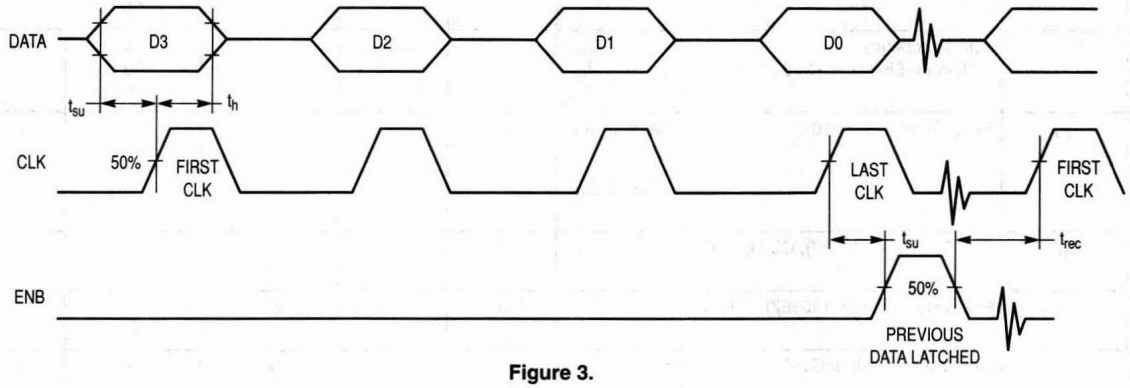


Figure 3.

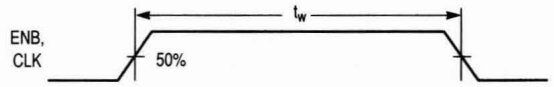


Figure 4.

PIN DESCRIPTIONS

INPUT PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1,16)

These pins form a reference oscillator when connected to an external parallel–resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

MODE
Mode Select (Pin 2)

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull–down device.

$\overline{SB}$
Standby Input (Pin 3)

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull–down device.

D0 – D3
Data Inputs (MC145166 — Pins 5 – 8)

These inputs provide the BCD code for selecting the one of ten channels to be locked in both the transmit and receive loop. When address data other than 1 – 10 are input, the decoding logic defaults to channel 10. The frequency assignments with reference to Mode and D0 – D3 are shown in Table 1. These inputs have internal pull–down devices.

f_{in1}, f_{in2}
Frequency Inputs (Pins 14, 9)

f_{in1} and f_{in2} are inputs to the divide–by–N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used. The minimum input level is 200 mV p–p.

CLK, DATA
Clock, Data (MC145167 — Pins 5, 6)

These pins provide the BCD input by using serial channel programming instead of parallel. Logical high represents a 1. Each low–to–high transition of the clock shifts one bit of data into the on–chip shift register.

ENB
Enable (MC145167 — Pin 8)

The enable pin controls the data transfer from the shift register to the 4–bit latch. A positive pulse latches the data.

OUTPUT PINS

5 k
5 kHz Tone Signals (Pin 4)

The 5 kHz tone signals are N–channel, open–drain outputs derived from the reference oscillator.

$\overline{LD}$
Lock Detect Signal (Pin 10)

The lock detect signal is associated with the transmit loop. The lock output goes high to indicate an out–of–lock condition. This is a P–channel open–drain output.

PD1, PD2
Phase Detector Outputs (Pins 13, 11)

These are three–state outputs of the transmit and receive phase detectors for use as loop error signals. Phase detector gain is $V_{DD}/4\ \pi$ volts per radian.

Frequency $f_v > f_r$ or f_v leading: Output = Negative pulses
Frequency $f_v < f_r$ or f_v lagging: Output = Positive pulses
Frequency $f_v = f_r$ and phase coincidence: Output = High–impedance state

POWER SUPPLY

V_{SS}
Negative Power Supply (Pin 12)

This pin is the negative supply potential and is usually ground.

V_{DD}
Positive Power Supply (Pin 15)

This pin is the positive supply potential and may range from + 2.5 to + 5.5 V with respect to V_{SS}.

Table 1. MC145166/67 Divide Ratios and VCO Frequencies

Channels					Handset (Mode = 0)				Base (Mode = 1)			
					Transmit		Receive		Transmit		Receive	
D3	D2	D1	D0	CH#	f_{in2} (MHz)	÷ N	f_{in1} (MHz)	÷ N	f_{in2} (MHz)	÷ N	f_{in1} (MHz)	÷ N
0	0	0	1	1	49.670	9934	35.915	7183	46.610	9322	38.975	7795
0	0	1	0	2	49.845	9969	35.935	7187	46.630	9326	39.150	7830
0	0	1	1	3	49.860	9972	35.975	7195	46.670	9334	39.165	7833
0	1	0	0	4	49.770	9954	36.015	7203	46.710	9342	39.075	7815
0	1	0	1	5	49.875	9975	36.035	7207	46.730	9346	39.180	7836
0	1	1	0	6	49.830	9966	36.075	7215	46.770	9354	39.135	7827
0	1	1	1	7	49.890	9978	36.135	7227	46.830	9366	39.195	7839
1	0	0	0	8	49.930	9986	36.175	7235	46.870	9374	39.235	7847
1	0	0	1	9	49.990	9998	36.235	7247	46.930	9386	39.295	7859
1	0	1	0	10	49.970	9994	36.275	7255	46.970	9394	39.275	7855

NOTES:
1. Other input combinations will be defaulted to channel 10.
2. 0 = logic low, 1 = logic high.

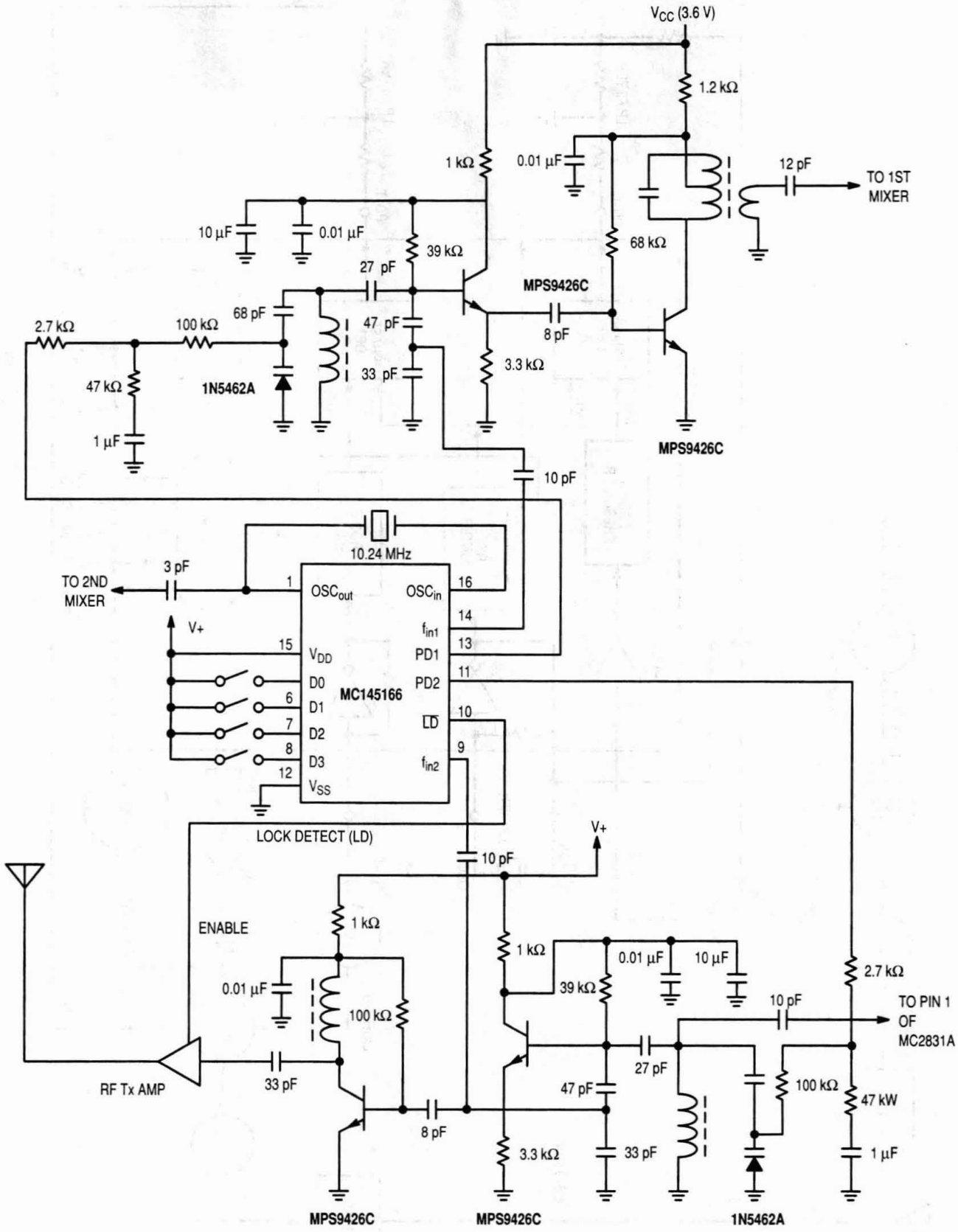


Figure 5. MC145166 Circuit Example

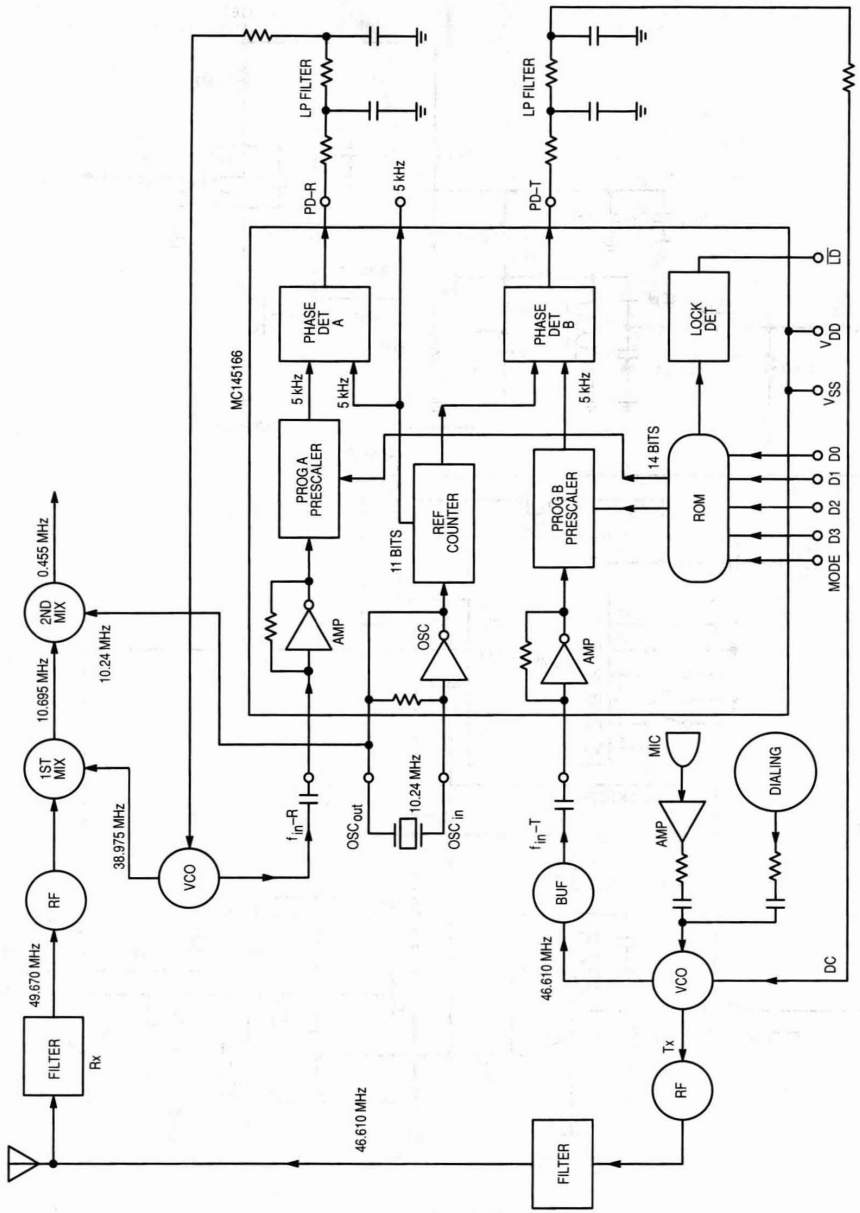


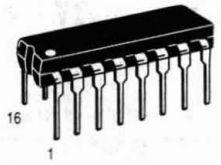
Figure 6. DPLL Application in 46/49 MHz Cordless Phone

MC145168
MC145169

Advance Information

Dual PLLs for 46/49 MHz Cordless Telephones

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC145168P	Plastic DIP
MC145168DW	SOG Package
MC145169P	Plastic DIP
MC145169DW	SOG Package

These devices are dual phase–locked loop frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 15 channels. These parts contain two mask–programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

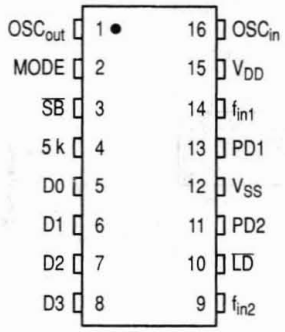
Other features include a lock detect circuit for the transmit loop, illegal code default, a buffered oscillator output for mixing purposes in the system, and a 5.0 kHz tone output.

- Maximum Operating Frequency: 60 MHz @ V_{in} = 200 mV p–p
- Operating Temperature Range: – 40 to + 75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On–Chip Oscillator Circuit Supports External Crystal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Lock Detect Signal
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V
- Two Versions:
  - MC145168 — Up to 15–Channel ROM with 4–Bit Binary Code Input for Channel Pair Selection
  - MC145169 — Up to 15–Channel ROM with Serial Interface for Channel Pair Selection
- Custom 20–Channel ROM Versions of the MC145169 are Possible; Consult Factory

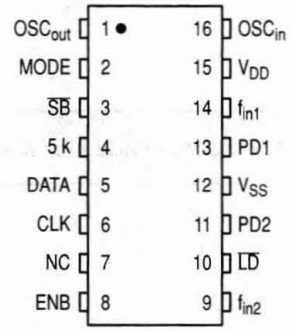
**NOT RECOMMENDED FOR NEW DESIGNS;
PRODUCT TO BE PHASED OUT.
Closest equivalent is MC145162.**

PIN ASSIGNMENTS

MC145168



MC145169



NC = NO CONNECTION

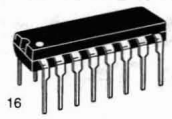
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC145170-1

Advance Information

PLL Frequency Synthesizer with Serial Interface

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

D SUFFIX
SOG PACKAGE
CASE 751B

DT SUFFIX
TSSOP
CASE 948C

ORDERING INFORMATION

MC145170P1	Plastic DIP
MC145170D1	SOG Package
MC145170DT1	TSSOP

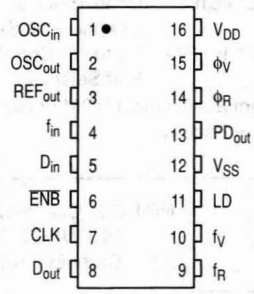
The MC145170–1 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

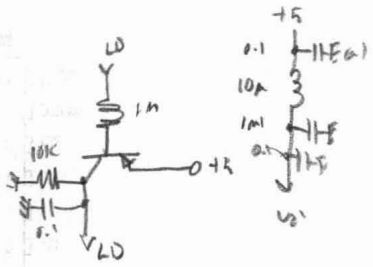
In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam–loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.5 to 5.5 V
- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mV p–p, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mV p–p, 3.0 V Minimum Supply
- Operating Supply Current: 0.6 mA @ 3 V, 30 MHz
  1.5 mA @ 3 V, 100 MHz
  3.0 mA @ 5 V, 50 MHz
  5.8 mA @ 5 V, 185 MHz
- Operating Temperature Range: – 40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates
- See Application Note AN1207/D

PIN ASSIGNMENT

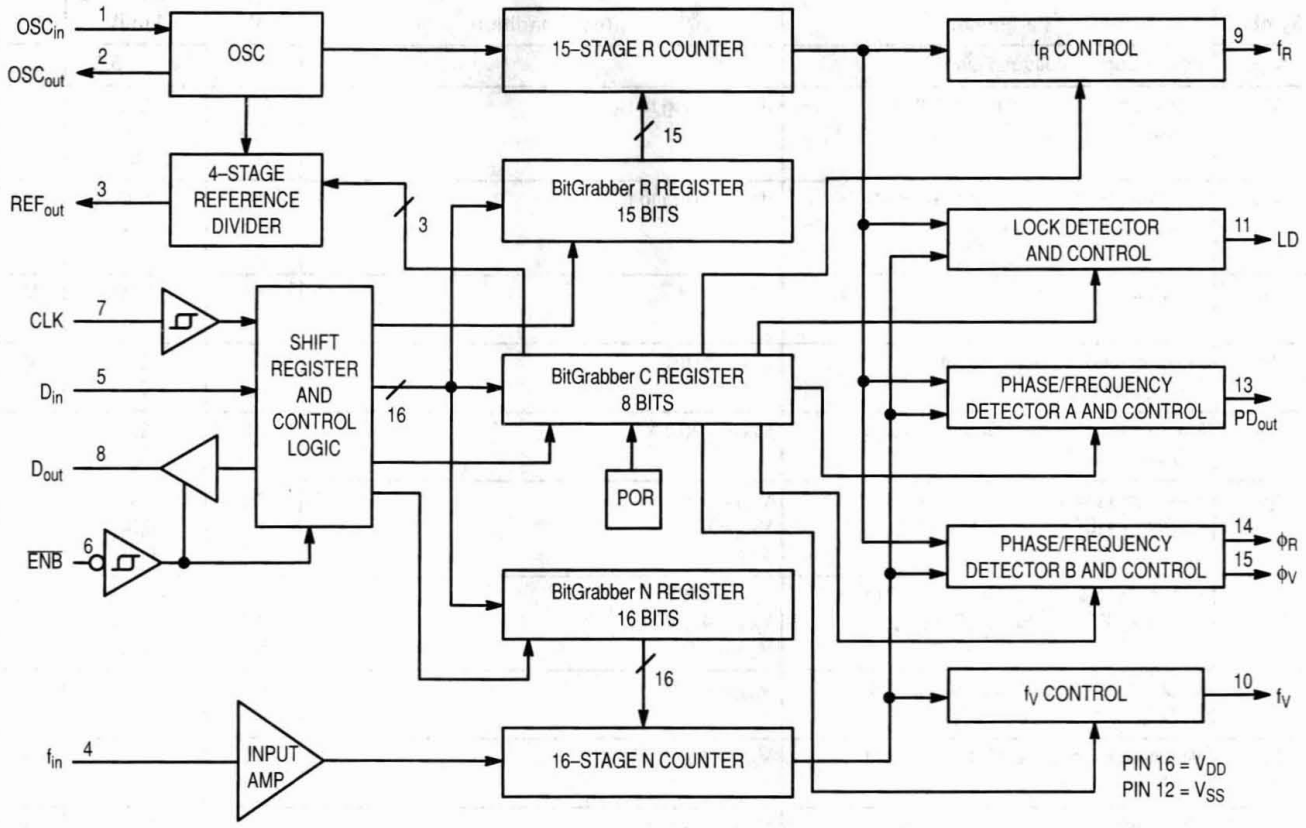


The MC145170–2 is recommended for new designs.



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 5.5	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.5 to 5.5	V
V_{IL}	Maximum Low–Level Input Voltage* (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	2.5 4.5 5.5	0.50 1.35 1.65	V
V_{IH}	Minimum High–Level Input Voltage* (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	2.5 4.5 5.5	2.00 3.15 3.85	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		2.5 5.5	0.15 0.20	V
V_{OL}	Maximum Low–Level Output Voltage (Any Output)	I_{out} = 20 µA	2.5 5.5	0.1 0.1	V
V_{OH}	Minimum High–Level Output Voltage (Any Output)	I_{out} = – 20 µA	2.5 5.5	2.4 5.4	V
I_{OL}	Minimum Low–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	2.5 4.5 5.5	0.12 0.36 0.36	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.2 V V_{out} = 4.1 V V_{out} = 5.0 V	2.5 4.5 5.5	– 0.12 – 0.36 – 0.36	mA
I_{OL}	Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	4.5	1.6	mA
I_{OH}	Minimum High–Level Output Current (D_{out})	V_{out} = 4.1 V	4.5	– 1.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	5.5	± 1.0	µA
I_{in}	Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	5.5	± 120	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{in} = V_{DD} or V_{SS}, Output in High–Impedance State	5.5	± 100	nA
	(D_{out})		5.5	± 5	µA
I_{DD}	Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	5.5	100	µA
I_{dd}	Maximum Operating Supply Current	f_{in} = 500 mV p–p; OSC_{in} = 1 MHz @ 1 V p–p; LD, f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out} = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	—	**	mA

* When dc coupling to the OSC_{in} pin is used, the pin must be driven rail–to–rail. In this case, OSC_{out} should be floated.

** The nominal values at 3 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

AC INTERFACE CHARACTERISTICS (T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	1	2.5 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to D_{out}	1, 5	2.5 4.5 5.5	150 85 85	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, D_{out} Active to High Impedance	2, 6	2.5 4.5 5.5	300 200 200	ns
t_{PZL}, t_{PZH}	Access Time, D_{out} High Impedance to Active	2, 6	2.5 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, D_{out} CL = 50 pF	1, 5	2.5 4.5 5.5	150 50 50	ns
	CL = 200 pF	1, 5	2.5 4.5 5.5	900 150 150	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		—	10	pF
C_{out}	Maximum Output Capacitance – D_{out}		—	10	pF

TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	2.5 4.5 5.5	55 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	4	2.5 4.5 5.5	135 100 100	ns
$t_{w(H)}$	Minimum Inactive–High Pulse Width, $\overline{ENB}$	4	2.5 4.5 5.5	400 300 300	ns
t_w	Minimum Pulse Width, CLK	1	2.5 4.5 5.5	166 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	2.5 4.5 5.5	100 100 100	µs

SWITCHING WAVEFORMS

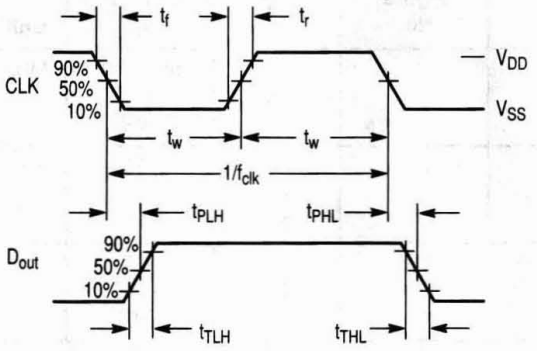


Figure 1.

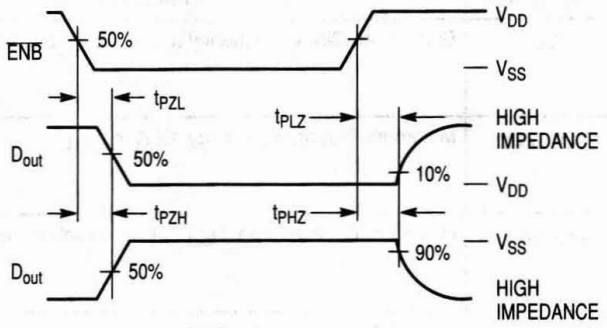


Figure 2.

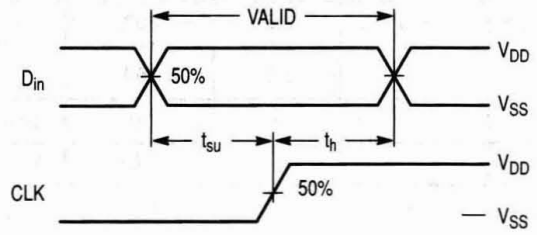


Figure 3.

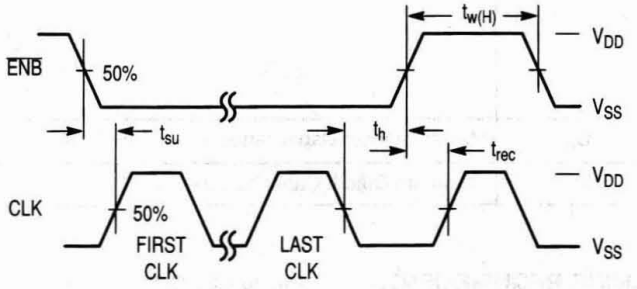
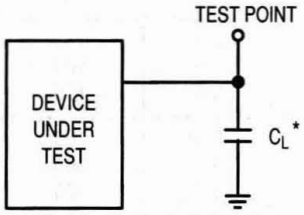
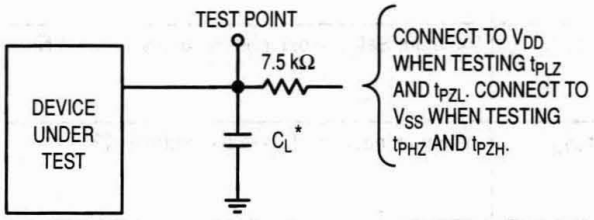


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS ($T_A = -40$ to $+85°C$)

Symbol	Parameter	Test Condition	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
f	Input Frequency, f_{in}	$V_{in} \geq 500$ mV p–p Sine Wave, N Counter Set to Divide Ratio Such that $f_V \leq 2$ MHz	7	2.5 3.0 4.5 5.5	5* 5* 25* 45*	TBD 100 185 185	MHz
f	Input Frequency, OSC_{in} Externally Driven with ac–Coupled Signal	$V_{in} \geq 1$ V p–p Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that $f_R \leq 2$ MHz	8	2.5 3.0 4.5 5.5	1* 1* 1* 1*	12 14 25 25	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	9	2.5 3.0 4.5 5.5	2 2 2 2	12 12 15 15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	2.5 4.5 5.5	dc dc dc	TBD 10 10	MHz
f	Operating Frequency of the Phase Detectors			2.5 4.5 5.5	dc dc dc	TBD 2 2	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	11, 12	2.5 4.5 5.5	TBD 20 16	TBD 100 90	ns
t_{TLH}, t_{THL}	Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	11, 12	2.5 4.5 5.5	— — —	TBD 65 60	ns
C_{in}	Input Capacitance f_{in} OSC_{in}		— —	— —	— —	7 7	pF

* If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac–coupled case. Also, see Figure 22 for dc decoupling.

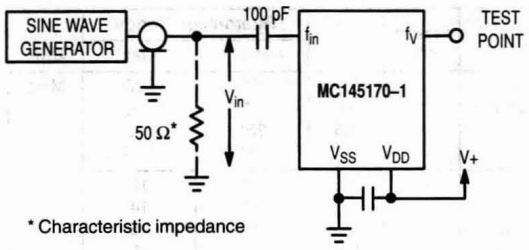


Figure 7. Test Circuit

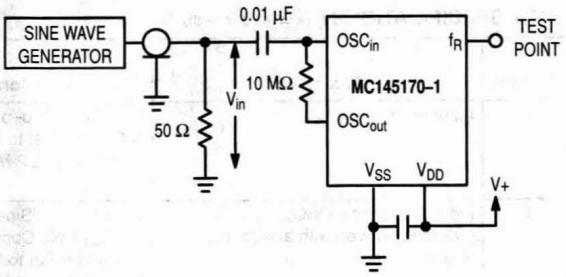


Figure 8. Test Circuit

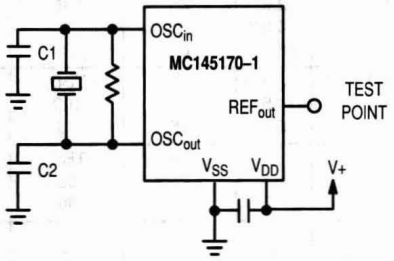


Figure 9. Test Circuit

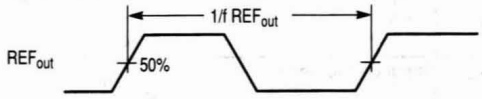


Figure 10. Switching Waveform

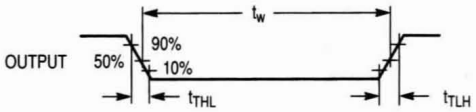


Figure 11. Switching Waveform

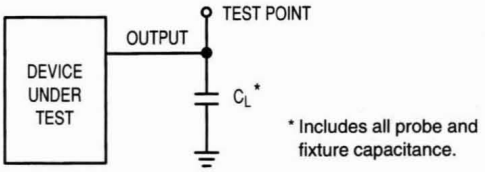


Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15–bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.5 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
4 + 5	(Reset)	
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	See Figures 24 — 31	

CLK
Serial Data Clock Input (Pin 7)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 — 31.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.5 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

$\overline{ENB}$
Active–Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}
Three–State Serial Data Output (Pin 8)

Data is transferred out of the 16–1/2–stage shift register through D_{out} on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in–line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

REFERENCE PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 μF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case (see Figure 8). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings rail–to–rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 22.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on–chip power–on–initialize circuit forces REF_{out} to the OSC_{in} divided–by–8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15–stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16–stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on–chip amplifier which drives the N counter. This signal is normally sourced from an external voltage–controlled oscillator (VCO), and is ac–coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 22.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 13)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

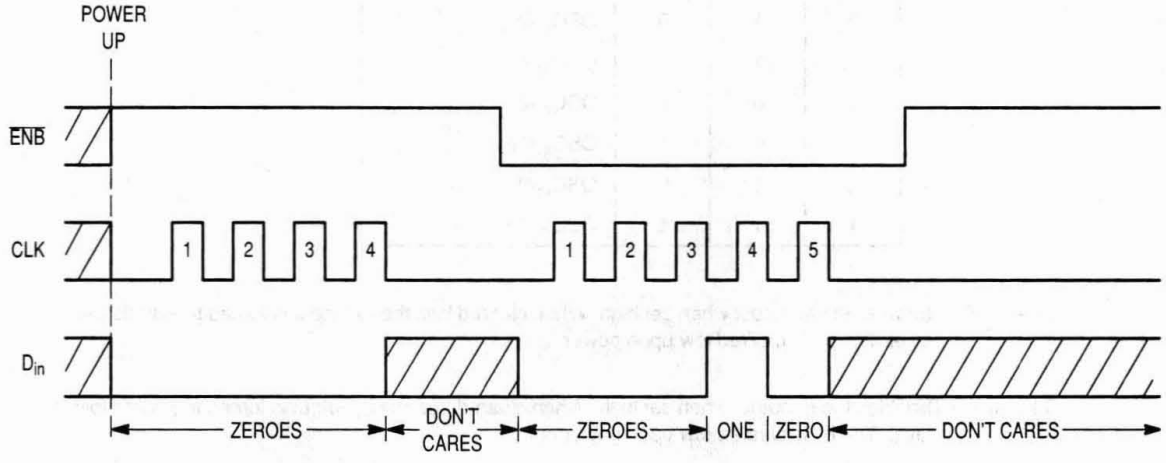
V_{DD}
Most Positive Supply Potential (Pin 16)

This pin may range from + 2.5 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

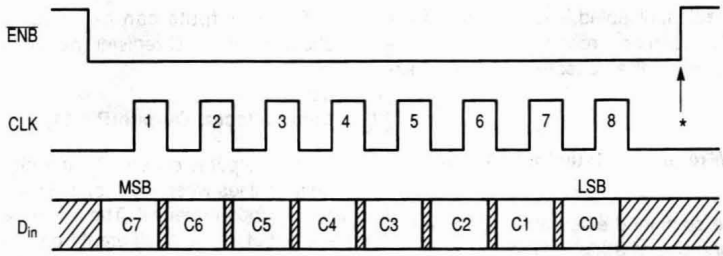
V_{SS}
Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.



NOTE: This initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (pin 7) toggles or floats upon power up, use the above sequence to reset the device.
Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.5 V, but not down to 0 V (for example, the supply drops down to 1 V). This is necessary because the on–chip power–on reset is only activated when the supply ramps up from 0 V.

Figure 13. Reset Sequence



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 — f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0 — f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)

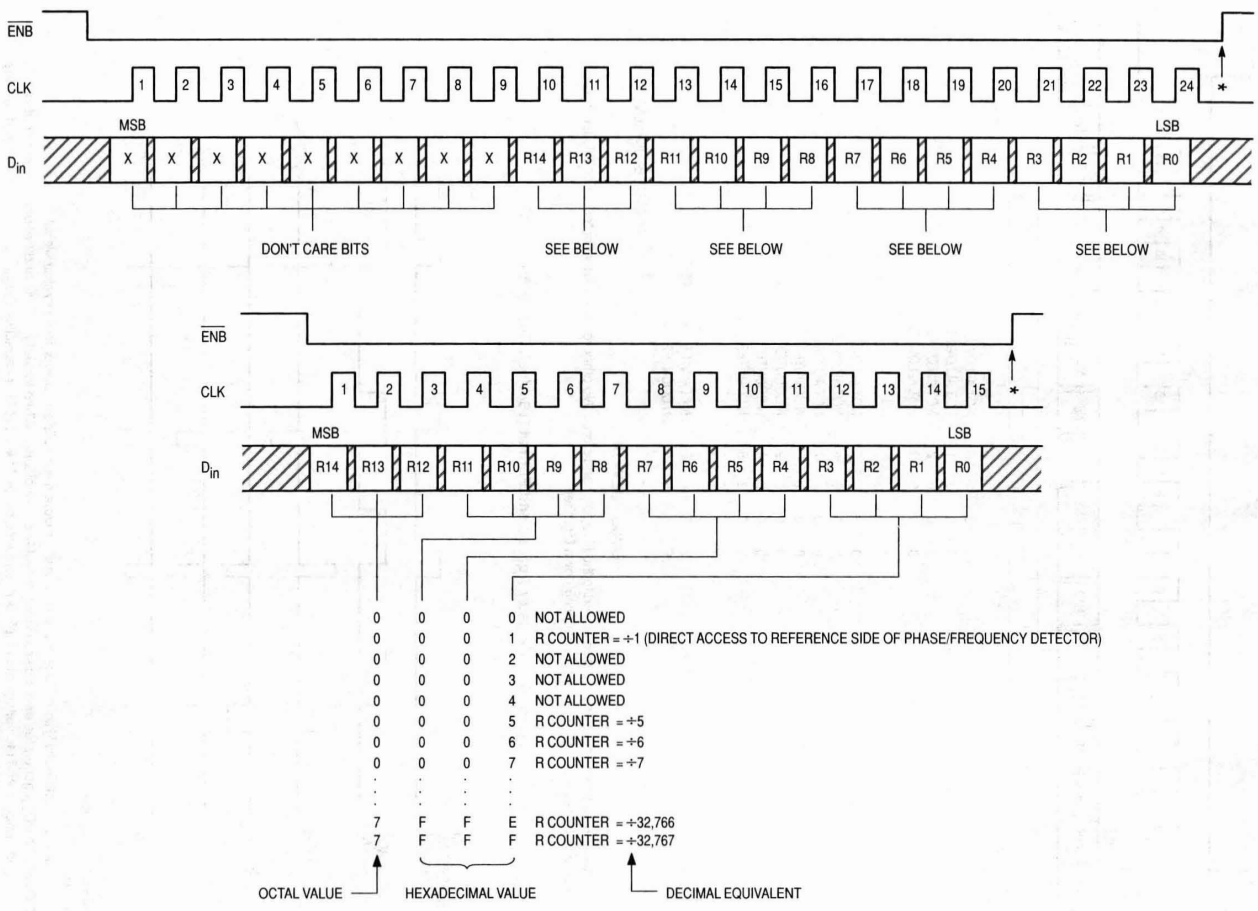
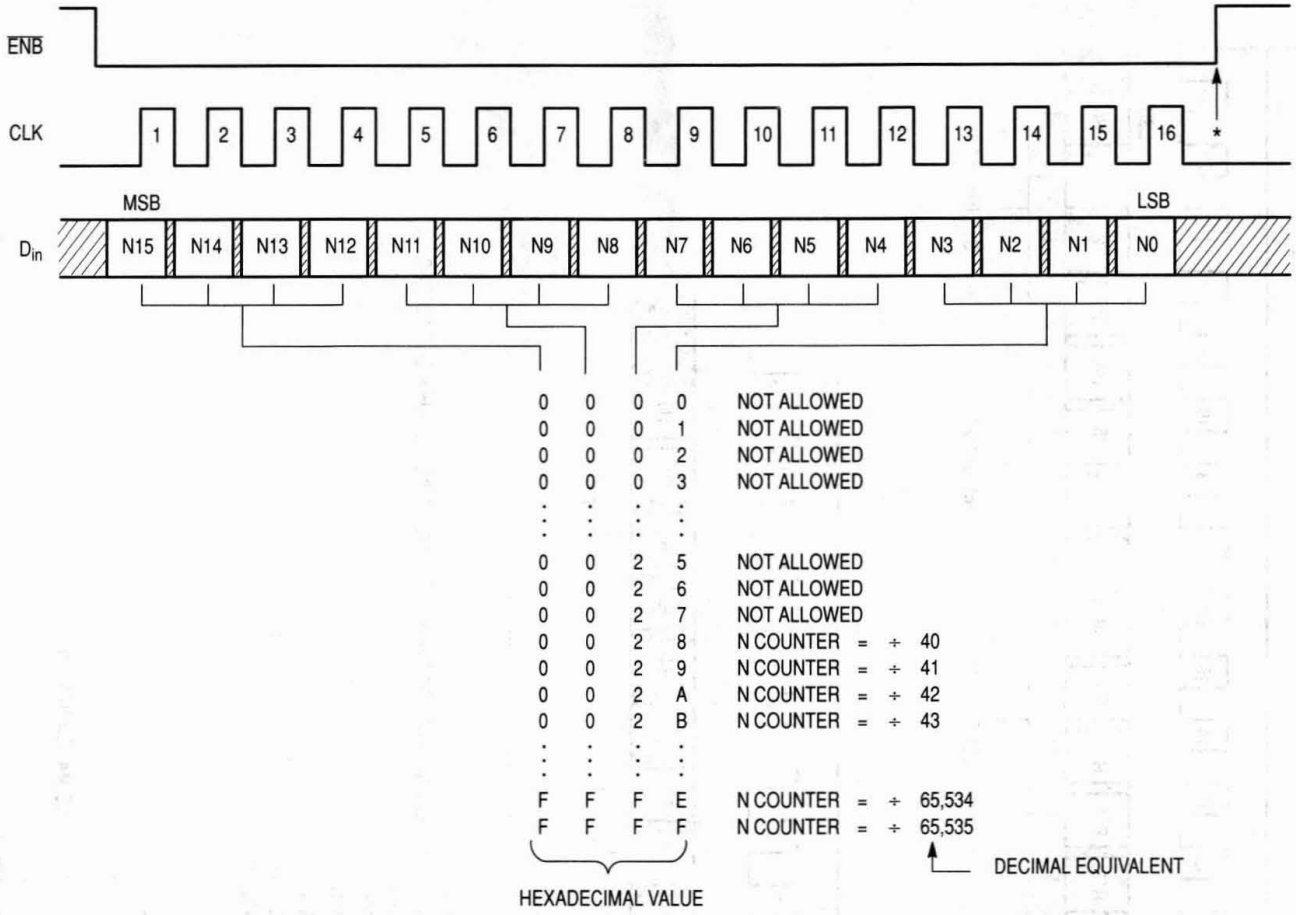

ENB
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 *
MSB
LSB
Din
X X X X X X X X X R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
DON'T CARE BITS
SEE BELOW
SEE BELOW
SEE BELOW
SEE BELOW
ENB
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 *
MSB
LSB
Din
R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
0 0 0 0 NOT ALLOWED
0 0 0 1 R COUNTER = ÷1 (DIRECT ACCESS TO REFERENCE SIDE OF PHASE/FREQUENCY DETECTOR)
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 0 4 NOT ALLOWED
0 0 0 5 R COUNTER = ÷5
0 0 0 6 R COUNTER = ÷6
0 0 0 7 R COUNTER = ÷7
7 F F E R COUNTER = ÷32,766
7 F F F R COUNTER = ÷32,767
OCTAL VALUE
HEXADECIMAL VALUE
DECIMAL EQUIVALENT

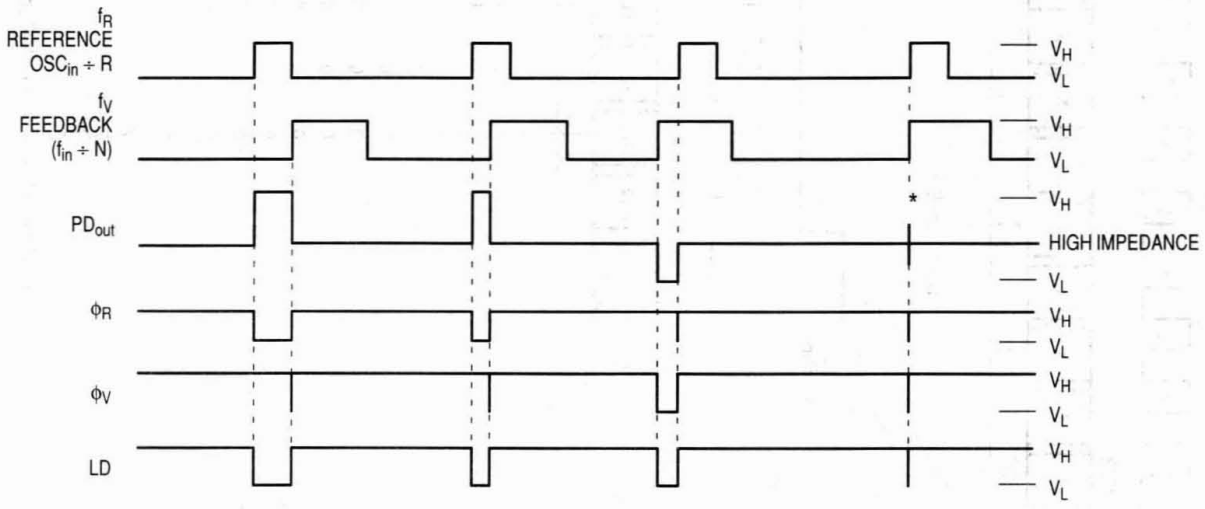
Figure 15. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)

* At this point, the new data is transferred to the R register and stored. No other registers are affected.


ENB
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 *
MSB
LSB
Din
N15 N14 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3 N2 N1 N0
0 0 0 0 NOT ALLOWED
0 0 0 1 NOT ALLOWED
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 2 5 NOT ALLOWED
0 0 2 6 NOT ALLOWED
0 0 2 7 NOT ALLOWED
0 0 2 8 N COUNTER = ÷ 40
0 0 2 9 N COUNTER = ÷ 41
0 0 2 A N COUNTER = ÷ 42
0 0 2 B N COUNTER = ÷ 43
F F F E N COUNTER = ÷ 65,534
F F F F N COUNTER = ÷ 65,535
DECIMAL EQUIVALENT
HEXADECIMAL VALUE

* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam–loaded and begin counting down together.

Figure 16. N Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level

V_L = Low voltage level

*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in} (see Figure 18). For large amplitude signals (standard CMOS logic levels), dc coupling is used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

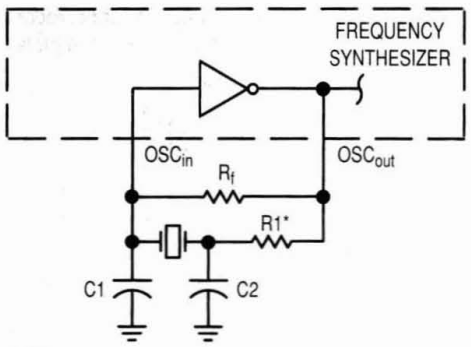
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

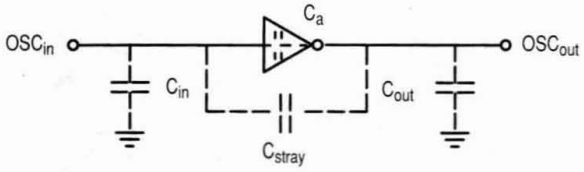
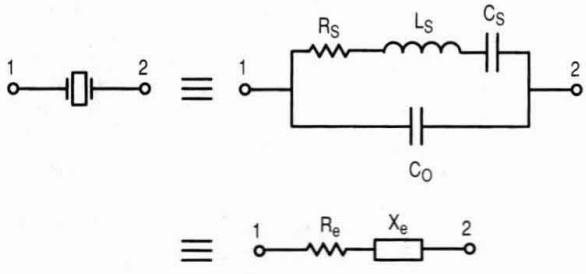


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design,* March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design,* April 25, 1985.

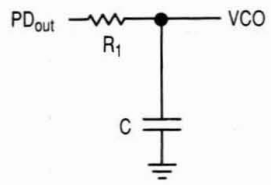
Table 2. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN

(A)

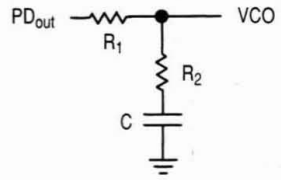


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

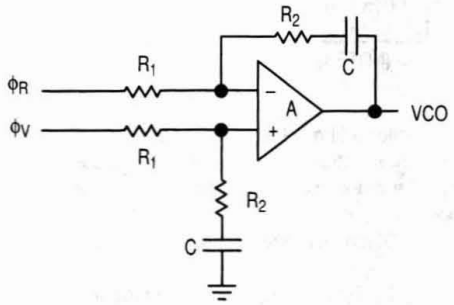


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE:

For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/ 4\pi$ V/radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ V/radian for ϕ_V and ϕ_R

$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

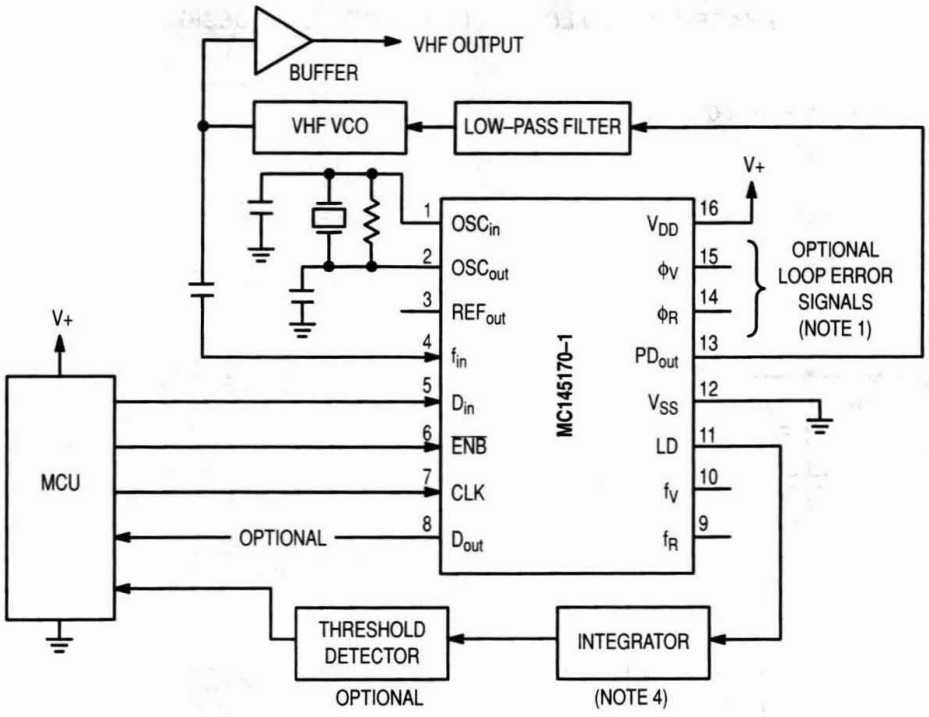
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

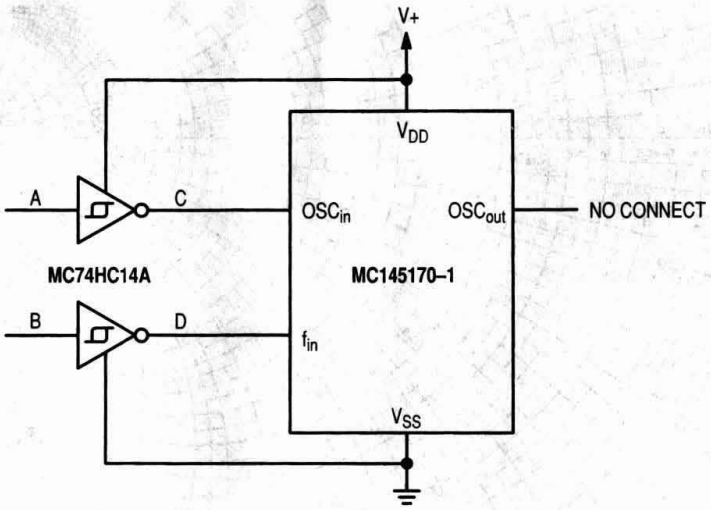
AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.



NOTES:

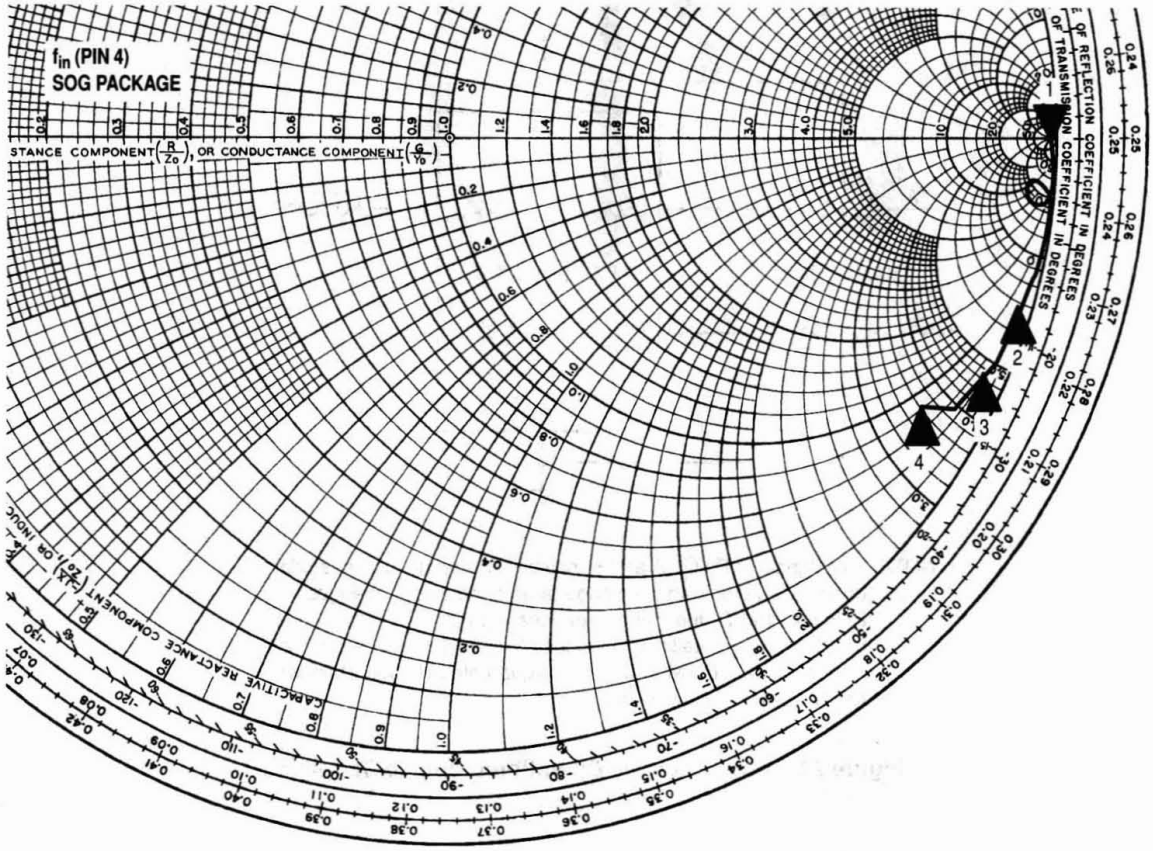
1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low–inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.
4. May be an R–C low–pass filter.

Figure 21. Example Application



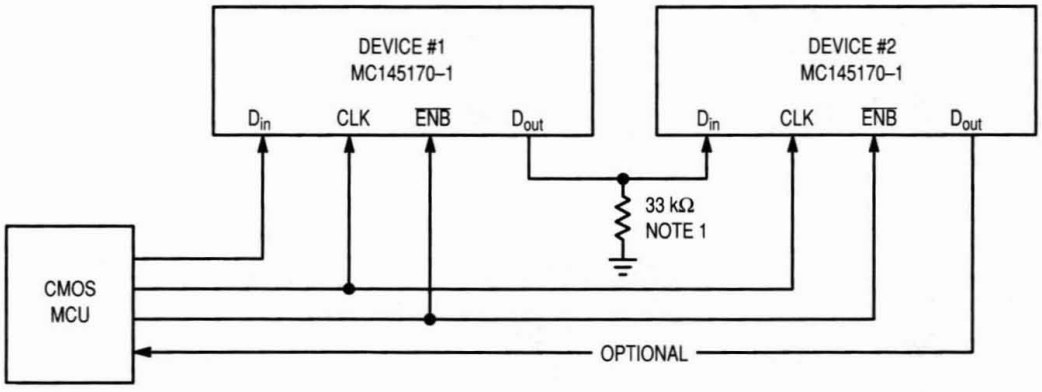
NOTE: The signals at Points A and B may be low–frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail–to–rail signal swings. With signals as described at Points C and D, the MC145170–1 is guaranteed to operate down to a frequency as low as dc.

Figure 22. Low Frequency Operation Using dc Coupling



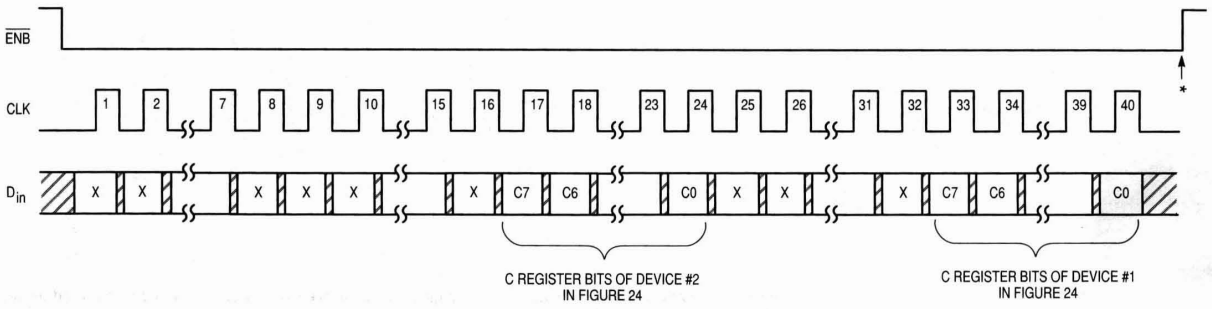
Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	– 5900	5.39
2	100	39.2	– 347	4.58
3	150	25.8	– 237	4.48
4	185	42.6	– 180	4.79

Figure 23. Input Impedance at f_{in} — Series Format (R + jX) (5 MHz to 185 MHz)



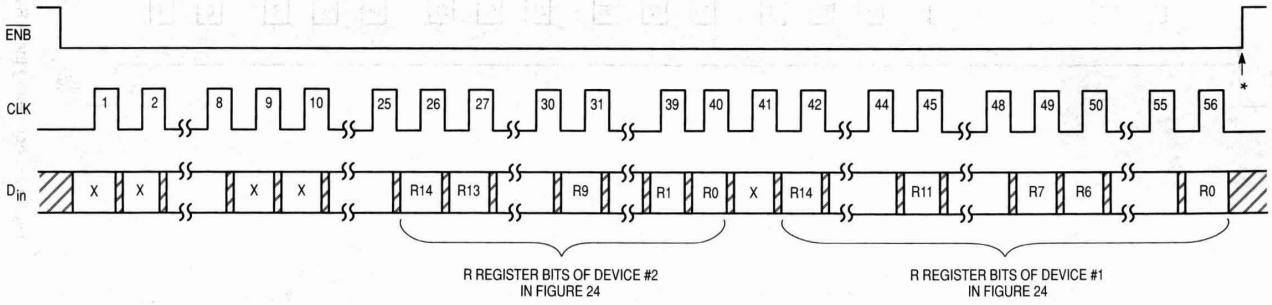
NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. See related Figures 25, 26, and 27.

Figure 24. Cascading Two MC145170–1 Devices



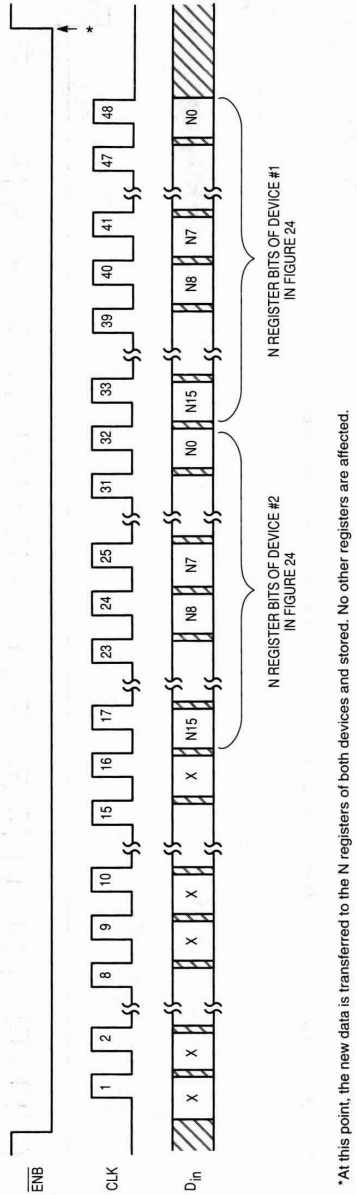
*At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 25. Accessing the C Registers of Two Cascaded MC145170–1 Devices



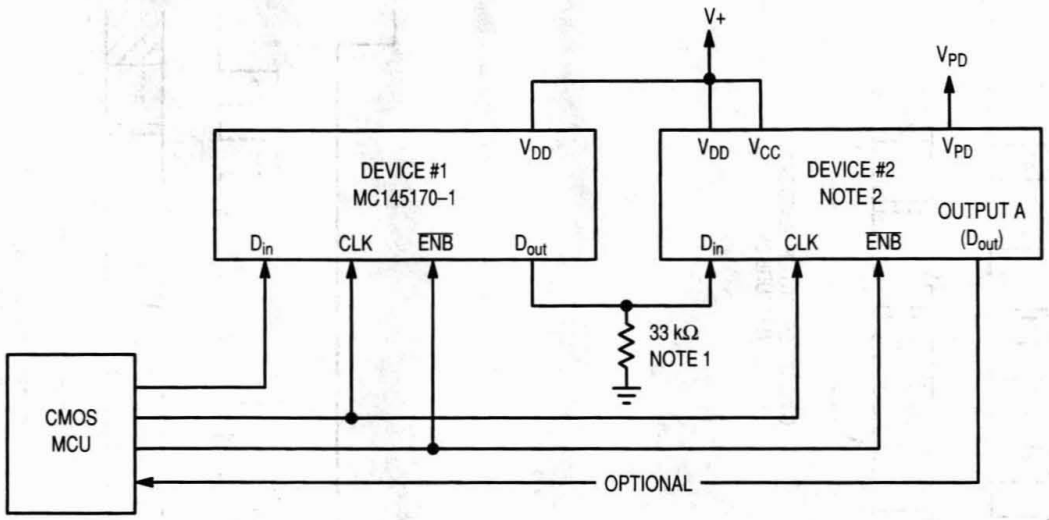
*At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

Figure 26. Accessing the R Registers of Two Cascaded MC145170–1 Devices



*At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

Figure 27. Accessing the N Registers of Two Cascaded MC145170–1 Devices



NOTES:

1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3. See related Figures 29, 30, and 31.

Figure 28. Cascading Two Different Device Types

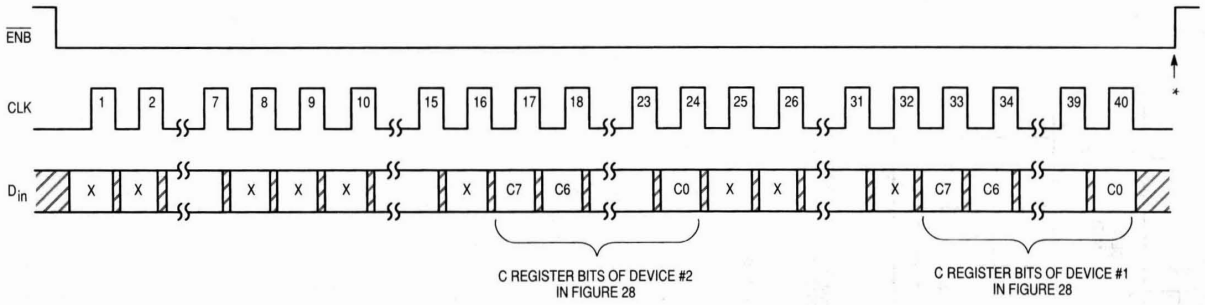


Figure 29. Accessing the C Registers of Two Different Device Types

*At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

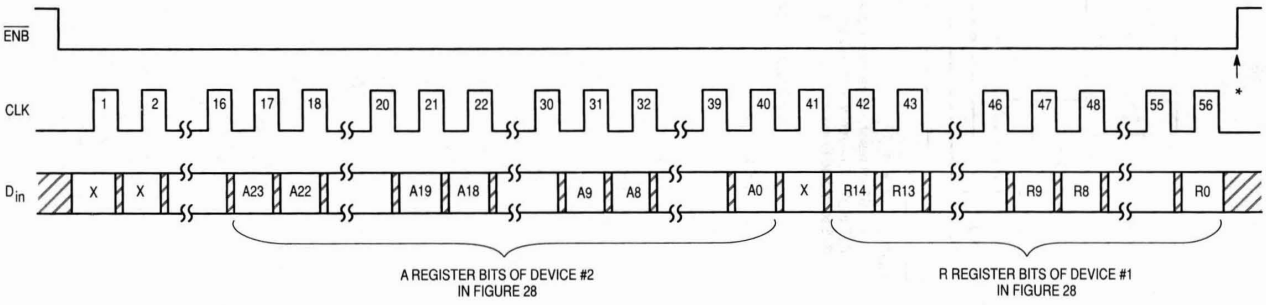
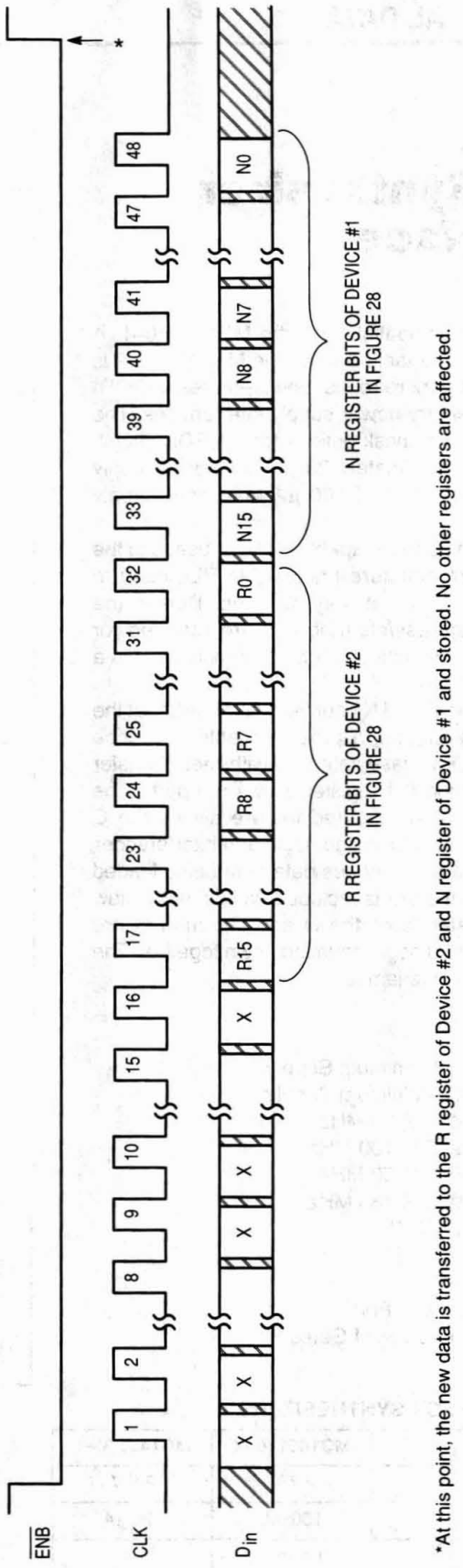


Figure 30. Accessing the A and R Registers of Two Different Device Types

*At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.



*At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

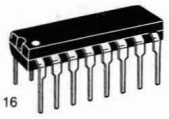
Figure 31. Accessing the R and N Registers of Two Different Device Types

MC145170-2

Advance Information

PLL Frequency Synthesizer with Serial Interface

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

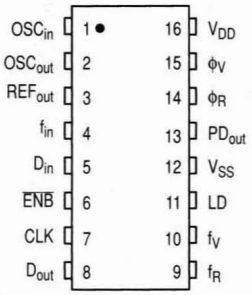
D SUFFIX
SOG PACKAGE
CASE 751B

DT SUFFIX
TSSOP
CASE 948C

ORDERING INFORMATION

MC145170P2	Plastic DIP
MC145170D2	SOG Package
MC145170DT2	TSSOP

PIN ASSIGNMENT



See web site *motorola.com/pll* for MC145170–2 control software. Look under Overview/Support Products/PLL Demonstration Software. Choose PLLGEN.EXE.

The new MC145170–2 is pin–for–pin compatible with the MC145170–1. A comparison of the two parts is shown in the table below. The MC145170–2 is recommended for new designs and has a more robust power–on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20 μA additional supply current. Note that the maximum specification of 100 μA quiescent supply current has not changed.

The MC145170–2 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam–loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

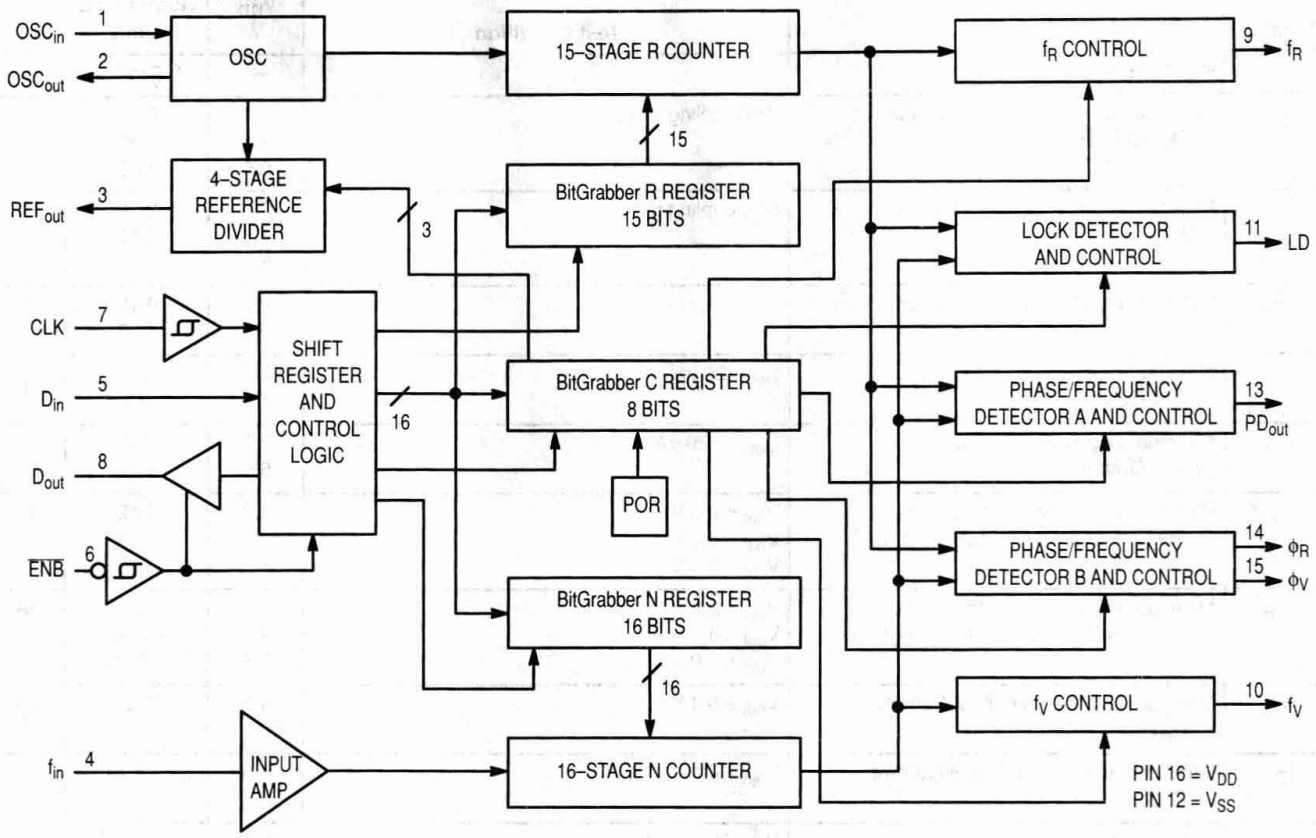
- Operating Voltage Range: 2.7 to 5.5 V
- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mV p–p, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mV p–p, 3.0 V Minimum Supply
- Operating Supply Current: 0.6 mA @ 3 V, 30 MHz
  1.5 mA @ 3 V, 100 MHz
  3.0 mA @ 5 V, 50 MHz
  5.8 mA @ 5 V, 185 MHz
- Operating Temperature Range: – 40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI Serial Data Port
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates
- See Application Note AN1207/D

COMPARISION OF THE PLL FREQUENCY SYNTHESIZERS

Parameter	MC145170–2	MC145170–1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, f_{in}	150 μA	120 μA
Dynamic Characteristics, f_{in} (Figure 23)	Unchanged	—
Power–On Reset Circuit	Improved	—

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 5.5	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.7 to 5.5	V
V_{IL}	Maximum Low–Level Input Voltage* (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	2.7 4.5 5.5	0.54 1.35 1.65	V
V_{IH}	Minimum High–Level Input Voltage* (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	2.7 4.5 5.5	2.16 3.15 3.85	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		2.7 5.5	0.15 0.20	V
V_{OL}	Maximum Low–Level Output Voltage (Any Output)	I_{out} = 20 µA	2.7 5.5	0.1 0.1	V
V_{OH}	Minimum High–Level Output Voltage (Any Output)	I_{out} = – 20 µA	2.7 5.5	2.6 5.4	V
I_{OL}	Minimum Low–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	2.7 4.5 5.5	0.12 0.36 0.36	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.4 V V_{out} = 4.1 V V_{out} = 5.0 V	2.7 4.5 5.5	– 0.12 – 0.36 – 0.36	mA
I_{OL}	Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	4.5	1.6	mA
I_{OH}	Minimum High–Level Output Current (D_{out})	V_{out} = 4.1 V	4.5	– 1.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	5.5	± 1.0	µA
I_{in}	Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	5.5	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{in} = V_{DD} or V_{SS}, Output in High–Impedance State	5.5	± 100	nA
	(D_{out})		5.5	± 5	µA
I_{DD}	Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	5.5	100	µA
I_{dd}	Maximum Operating Supply Current	f_{in} = 500 mV p–p; OSC_{in} = 1 MHz @ 1 V p–p; LD, f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out} = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	—	**	mA

*When dc coupling to the OSC_{in} pin is used, the pin must be driven rail–to–rail. In this case, OSC_{out} should be floated.

**The nominal values at 3 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

AC INTERFACE CHARACTERISTICS (T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	1	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to D_{out}	1, 5	2.7 4.5 5.5	150 85 85	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, D_{out} Active to High Impedance	2, 6	2.7 4.5 5.5	300 200 200	ns
t_{PZL}, t_{PZH}	Access Time, D_{out} High Impedance to Active	2, 6	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, D_{out} CL = 50 pF	1, 5	2.7 4.5 5.5	150 50 50	ns
	CL = 200 pF	1, 5	2.7 4.5 5.5	900 150 150	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		—	10	pF
C_{out}	Maximum Output Capacitance – D_{out}		—	10	pF

TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	2.7 4.5 5.5	55 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	4	2.7 4.5 5.5	135 100 100	ns
$t_{w(H)}$	Minimum Inactive–High Pulse Width, $\overline{ENB}$	4	2.7 4.5 5.5	400 300 300	ns
t_w	Minimum Pulse Width, CLK	1	2.7 4.5 5.5	166 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	2.7 4.5 5.5	100 100 100	µs

SWITCHING WAVEFORMS

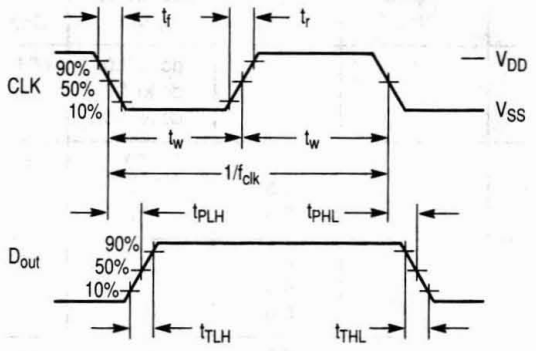


Figure 1.

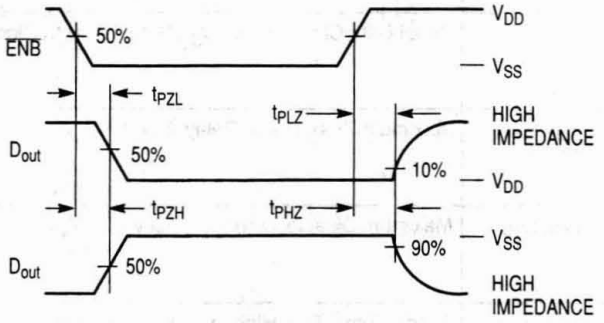


Figure 2.

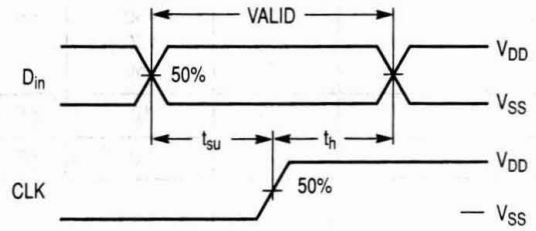


Figure 3.

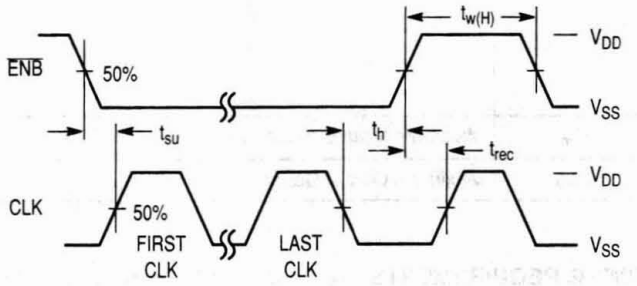
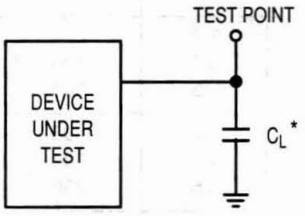
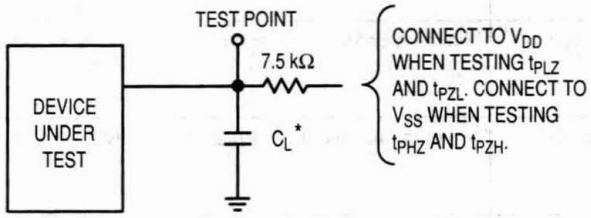


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS ($T_A = -40$ to $+85°C$)

Symbol	Parameter	Test Condition	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
f	Input Frequency, f_{in}	$V_{in} \geq 500$ mV p–p Sine Wave, N Counter Set to Divide Ratio Such that $f_V \leq 2$ MHz	7	2.7 3.0 4.5 5.5	5* 5* 25* 45*	TBD 100 185 185	MHz
f	Input Frequency, OSC_{in} Externally Driven with ac–Coupled Signal	$V_{in} \geq 1$ V p–p Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that $f_R \leq 2$ MHz	8a	2.7 3.0 4.5 5.5	1* 1* 1* 1*	12 14 25 25	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	9	2.7 3.0 4.5 5.5	2 2 2 2	12 12 15 15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	2.7 4.5 5.5	dc dc dc	TBD 10 10	MHz
f	Operating Frequency of the Phase Detectors			2.7 4.5 5.5	dc dc dc	TBD 2 2	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	11, 12	2.7 4.5 5.5	TBD 20 16	TBD 100 90	ns
t_{TLH}, t_{THL}	Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	11, 12	2.7 4.5 5.5	— — —	TBD 65 60	ns
C_{in}	Input Capacitance f_{in} OSC_{in}		— —	— —	— —	7 7	pF

* If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac–coupled case. Also, see Figure 22 for dc coupling.

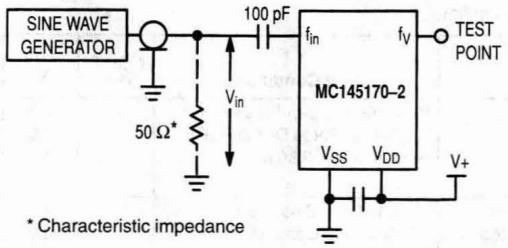


Figure 7. Test Circuit, f_{in}

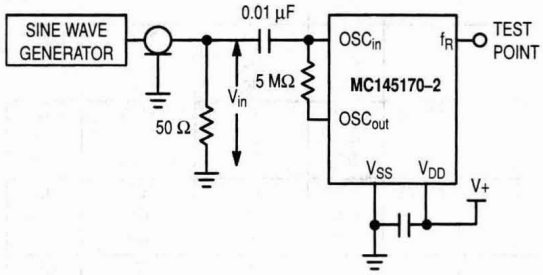


Figure 8a. Test Circuit, OSC Circuit Externally Driven*

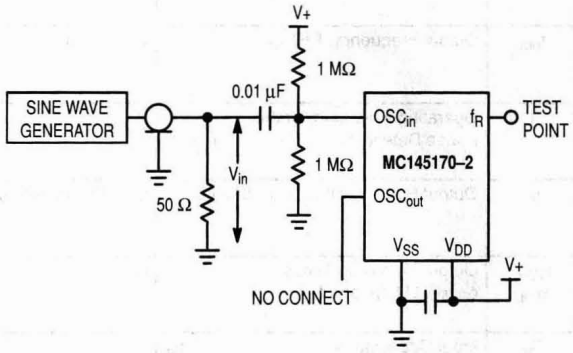


Figure 8b. Circuit to Eliminate Self–Oscillation, OSC Circuit Externally Driven*

Figure 8.

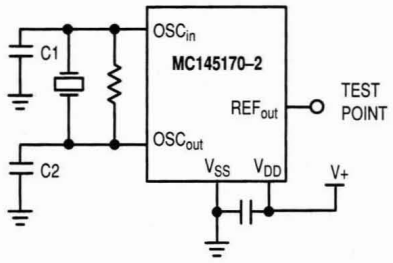


Figure 9. Test Circuit, OSC Circuit with Crystal

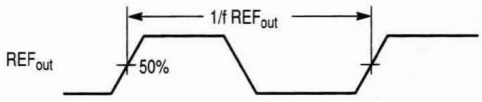


Figure 10. Switching Waveform

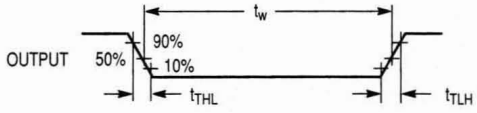


Figure 11. Switching Waveform

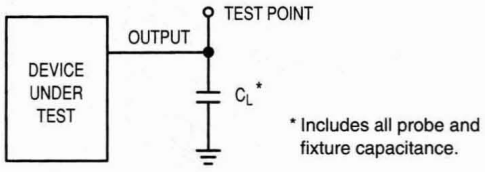


Figure 12. Test Load Circuit

* Use the circuit of Figure 8b to eliminate self–oscillation of the OSC_{in} pin when the MC145170–2 has power applied with no external signal applied at V_{in}. (Self–oscillation is not harmful to the MC145170–2 and does not damage the IC.)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15–bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 13	(Reset)
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	See Figures 24 — 31	

CLK
Serial Data Clock Input (Pin 7)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 — 31.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

$\overline{ENB}$
Active–Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}
Three–State Serial Data Output (Pin 8)

Data is transferred out of the 16–1/2–stage shift register through D_{out} on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in–line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

REFERENCE PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 5 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 μF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 5 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case (see Figure 8a or alternate circuit 8b). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings virtually rail–to–rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 22.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on–chip power–on–initialize circuit forces REF_{out} to the OSC_{in} divided–by–8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15–stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the OSC_{in} pin signal, except when a divide ratio of 1 is selected. When 1 is selected, the OSC_{in} signal is buffered and appears at the f_R pin.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16–stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on–chip amplifier which drives the N counter. This signal is normally sourced from an external voltage–controlled oscillator (VCO), and is ac–coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 22.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 13)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

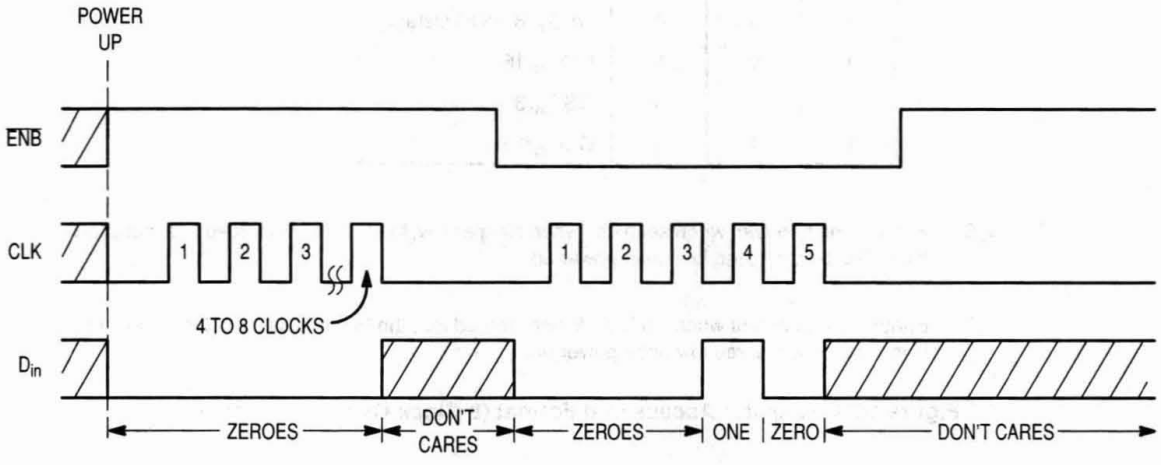
V_{DD}
Most Positive Supply Potential (Pin 16)

This pin may range from + 2.7 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

V_{SS}
Most Negative Supply Potential (Pin 12)

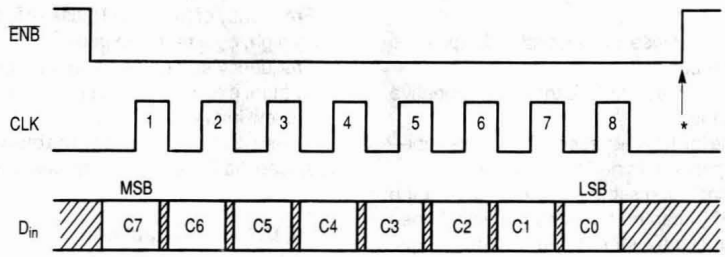
This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.



NOTE: This initialization sequence is usually not necessary because the on–chip power–on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (pin 7) toggles or floats upon power up, use the above sequence to reset the device.

Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on–chip power–on reset is only activated when the supply ramps up from a voltage below approximately 1 V.

Figure 13. Reset Sequence



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 — f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0 — f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)

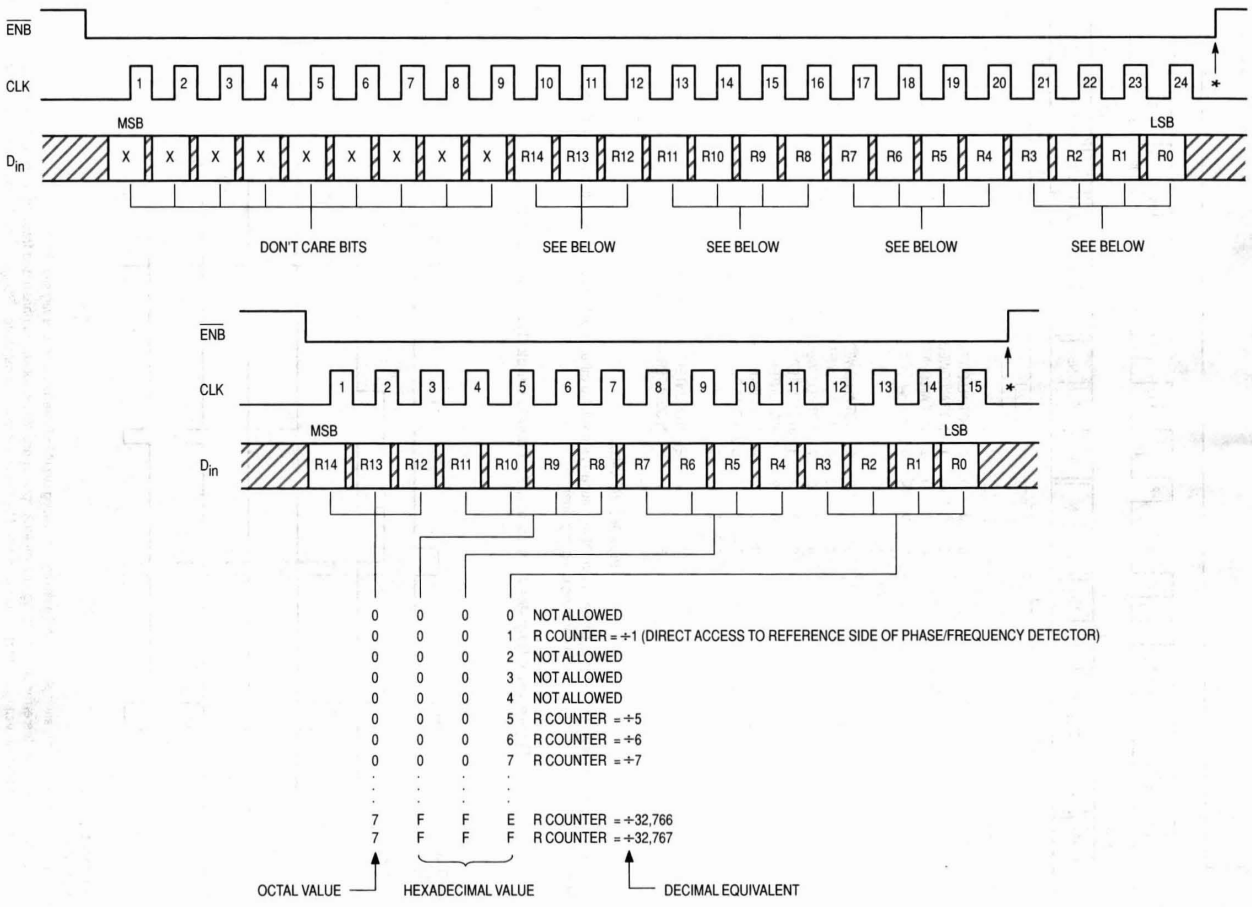
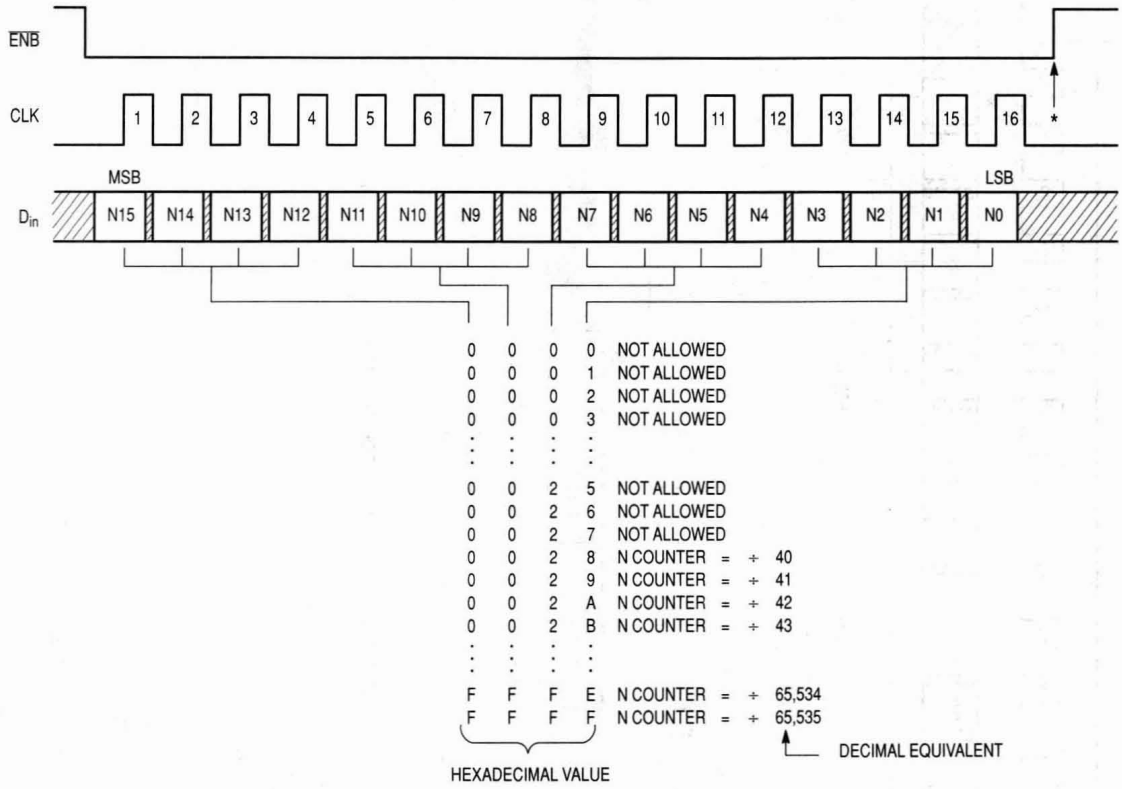

ENB
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 *
MSB
LSB
Din
X X X X X X X X X R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
DON'T CARE BITS
SEE BELOW
SEE BELOW
SEE BELOW
SEE BELOW
ENB
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 *
MSB
LSB
Din
R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
0 0 0 0 NOT ALLOWED
0 0 0 1 R COUNTER = ÷1 (DIRECT ACCESS TO REFERENCE SIDE OF PHASE/FREQUENCY DETECTOR)
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 0 4 NOT ALLOWED
0 0 0 5 R COUNTER = ÷5
0 0 0 6 R COUNTER = ÷6
0 0 0 7 R COUNTER = ÷7
7 F F E R COUNTER = ÷32,766
7 F F F R COUNTER = ÷32,767
OCTAL VALUE
HEXADECIMAL VALUE
DECIMAL EQUIVALENT

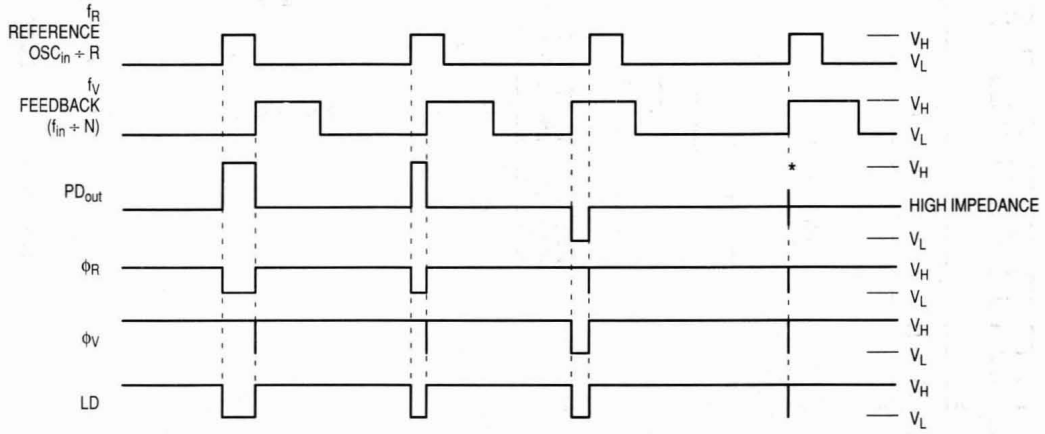
Figure 15. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)

* At this point, the new data is transferred to the R register and stored. No other registers are affected.


ENB
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 *
MSB
LSB
Din
N15 N14 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3 N2 N1 N0
0 0 0 0 NOT ALLOWED
0 0 0 1 NOT ALLOWED
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 2 5 NOT ALLOWED
0 0 2 6 NOT ALLOWED
0 0 2 7 NOT ALLOWED
0 0 2 8 N COUNTER = ÷ 40
0 0 2 9 N COUNTER = ÷ 41
0 0 2 A N COUNTER = ÷ 42
0 0 2 B N COUNTER = ÷ 43
F F F E N COUNTER = ÷ 65,534
F F F F N COUNTER = ÷ 65,535
DECIMAL EQUIVALENT
HEXADECIMAL VALUE

* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam–loaded and begin counting down together.

Figure 16. N Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figures 8a and 8b).

For additional information about TCXOs, visit *motorola.com* on the world wide web.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

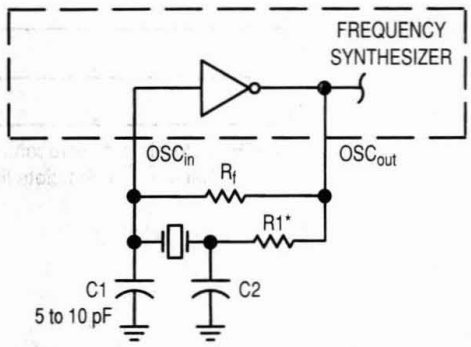
The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

A good design practice is to pick a small value for C1, such as 5 to 10 pF. Next, C2 is calculated. C1 < C2 results in a more robust circuit for start–up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

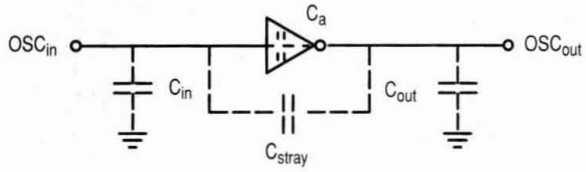
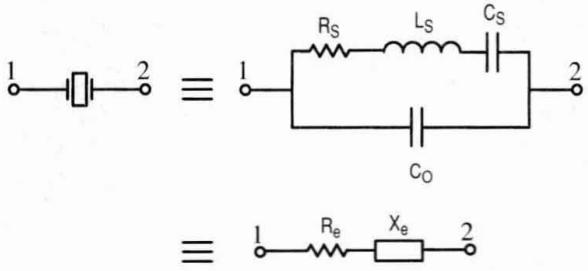


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

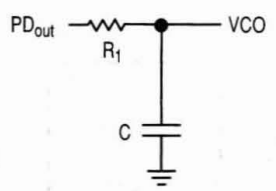
Table 2. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN

(A)

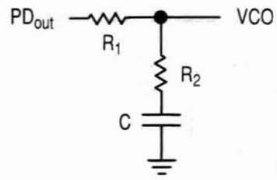


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

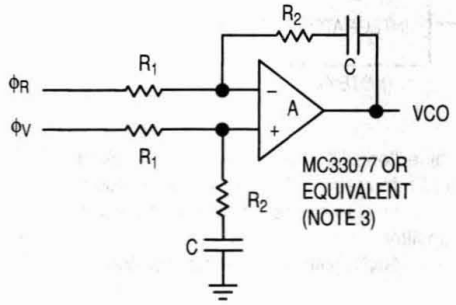


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTES:

4. For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.
5. The ϕR and ϕV outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.
6. For the latest information on MC33077 or equivalent, see the Motorola Analog IC web site at *http://www.mot–sps.com/analog.*

DEFINITIONS:

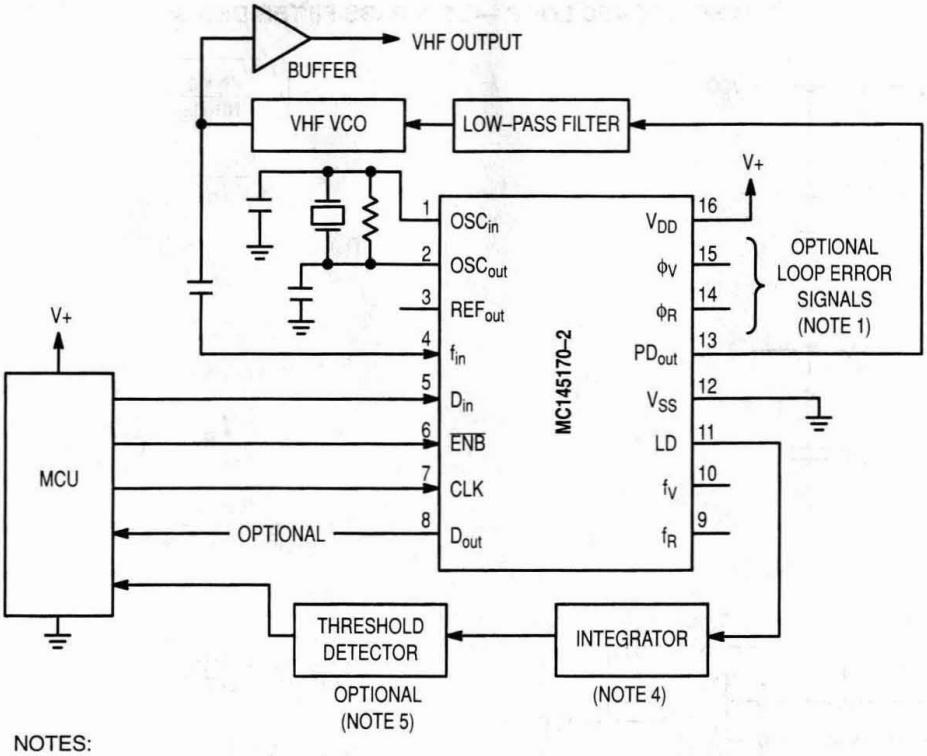
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ volts per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ volts per radian for ϕ_V and ϕ_R

$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

RECOMMENDED READING:

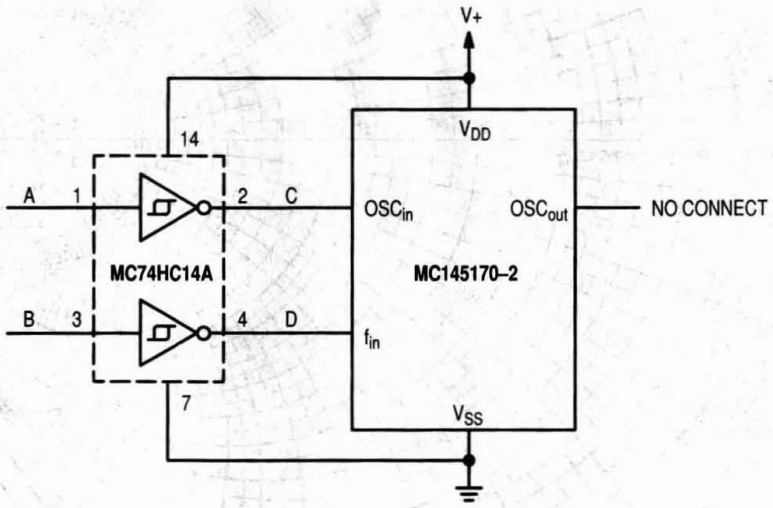
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.



NOTES:

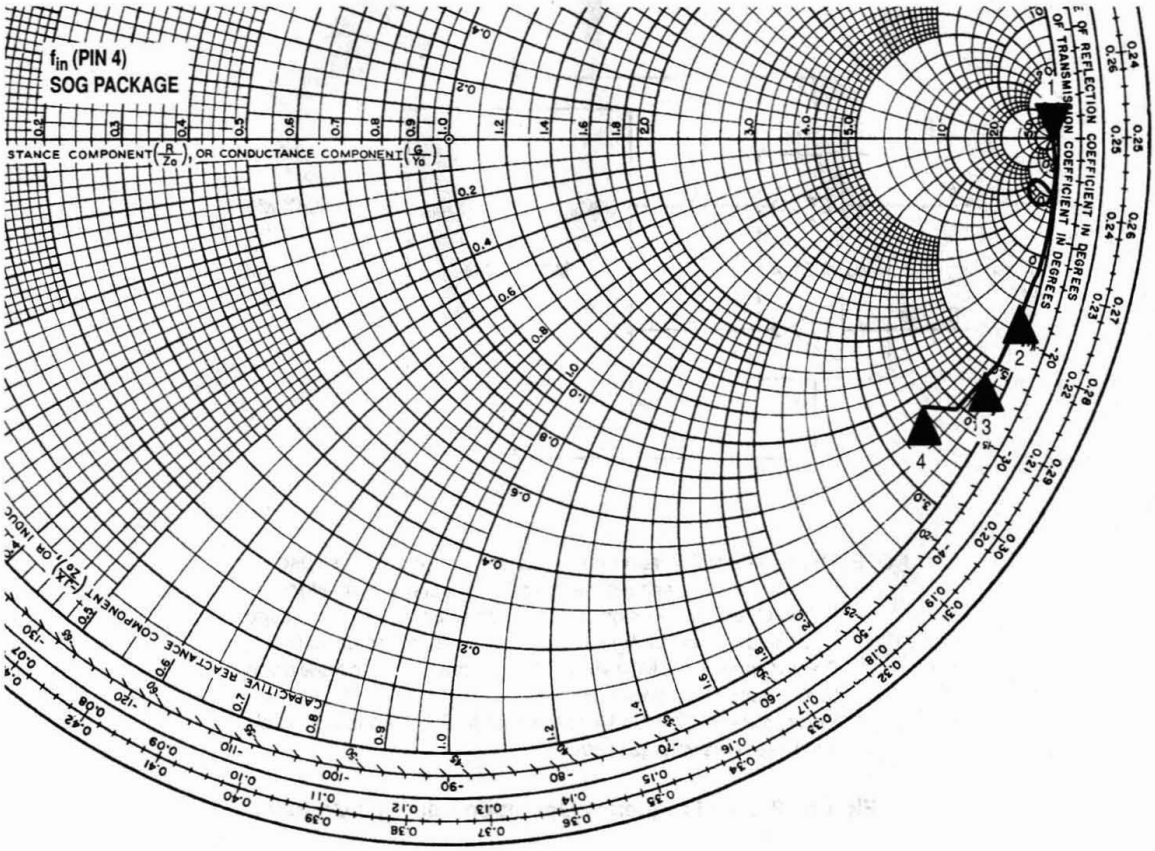
1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low–inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.
4. May be an R–C low–pass filter.
5. May be a bipolar transistor.

Figure 21. Example Application



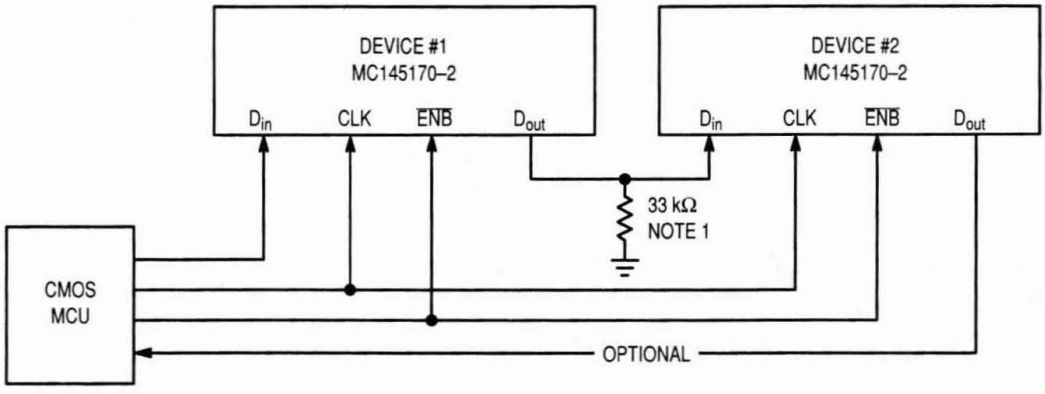
NOTE: The signals at Points A and B may be low–frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail–to–rail signal swings. With signals as described at Points C and D, the MC145170–2 is guaranteed to operate down to a frequency as low as dc.
Refer to the MC74HC14A data sheet for input switching levels and hysteresis voltage range.

Figure 22. Low Frequency Operation Using dc Coupling



Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	– 5900	5.39
2	100	39.2	– 347	4.58
3	150	25.8	– 237	4.48
4	185	42.6	– 180	4.79

Figure 23. Input Impedance at f_{in} — Series Format (R + jX) (5 MHz to 185 MHz)



NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. See related Figures 25, 26, and 27.

Figure 24. Cascading Two MC145170–2 Devices

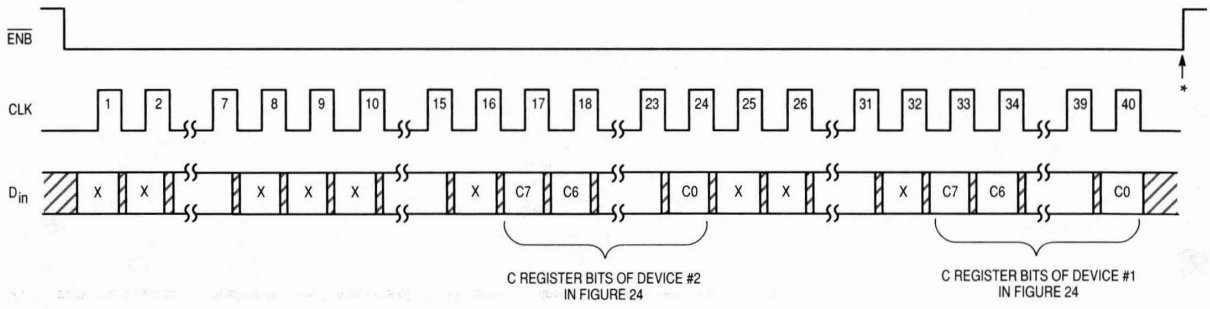


Figure 25. Accessing the C Registers of Two Cascaded MC145170–2 Devices

*At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

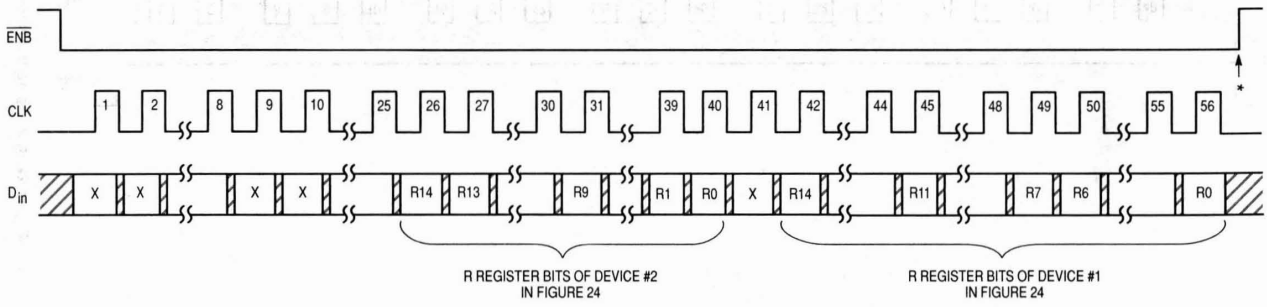


Figure 26. Accessing the R Registers of Two Cascaded MC145170–2 Devices

*At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

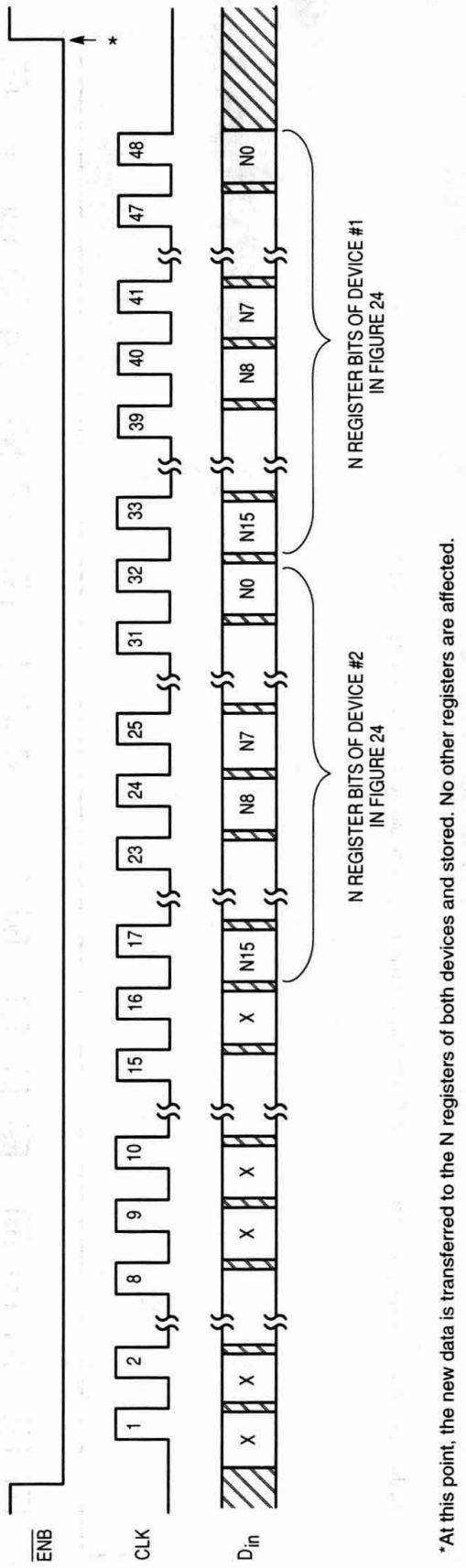
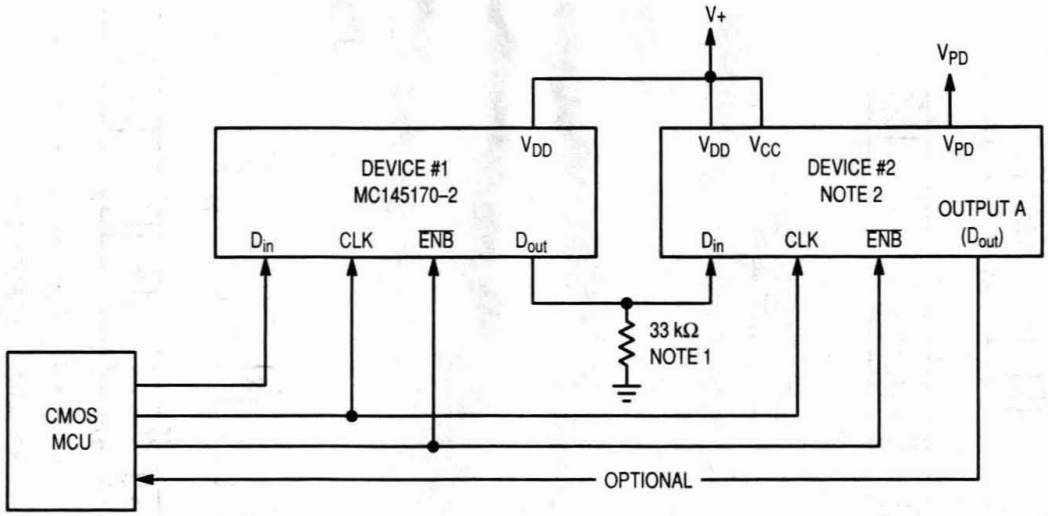


Figure 27. Accessing the N Registers of Two Cascaded MC145170–2 Devices



NOTES:

1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3. See related Figures 29, 30, and 31.

Figure 28. Cascading Two Different Device Types

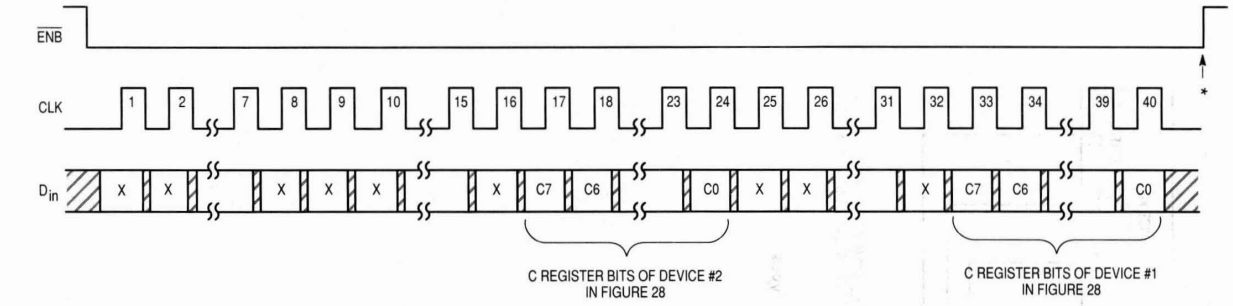


Figure 29. Accessing the C Registers of Two Different Device Types

*At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

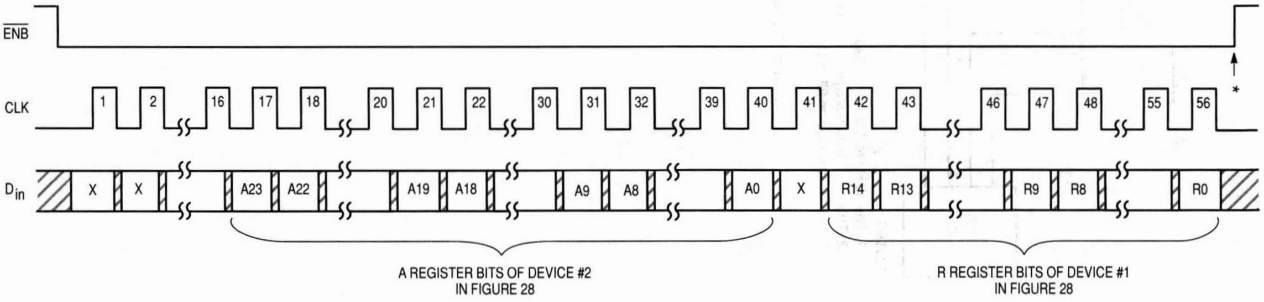
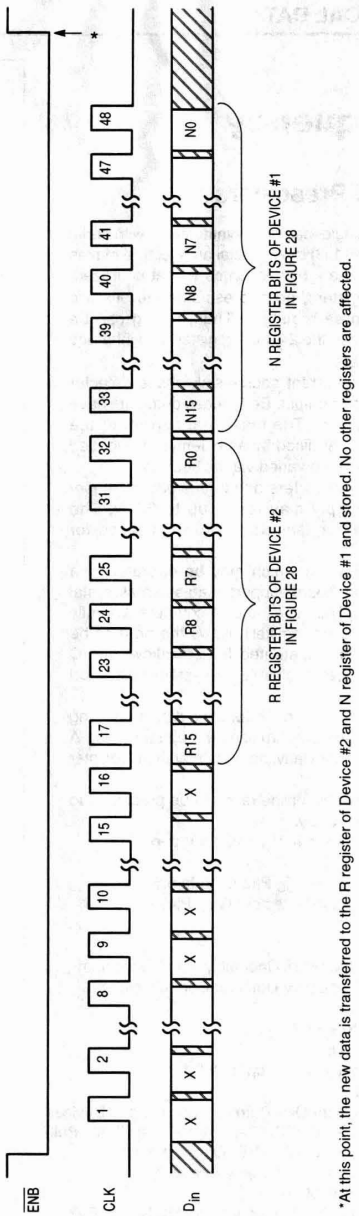


Figure 30. Accessing the A and R Registers of Two Different Device Types

*At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.



*At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

Figure 31. Accessing the R and N Registers of Two Different Device Types

1.1 GHz PLL Frequency Synthesizers

Include On–Board 64/65 Prescalers

MC145190
MC145191

The MC145190 and MC145191 are single–package synthesizers with serial interfaces capable of direct usage up to 1.1 GHz. A special architecture makes these PLLs very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

Each device features a single–ended current source/sink phase detector output and a double–ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

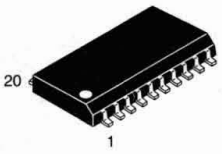
The MC145190 features logic–level converters and high–voltage phase/frequency detectors; the detector supply may range up to 9.5 V. The MC145191 has lower–voltage phase/frequency detectors optimized for single–supply systems of 5 V ±10%.

Each part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the parts to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

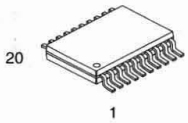
In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 7 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin) —
  MC145190: 8.0 to 9.5 V
  MC145191: 4.5 to 5.5 V
- Current Source/Sink Phase Detector OUTPUT Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: (1 and) 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull)
  OUTPUT B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- Evaluation Kit Available (Part Numbers MC145190EVK and MC145191EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping



F SUFFIX
SOG PACKAGE
CASE 751J

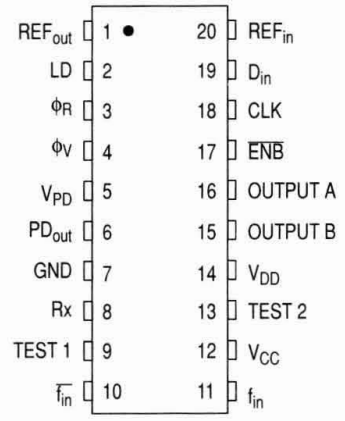


DT SUFFIX
TSSOP
CASE 948D

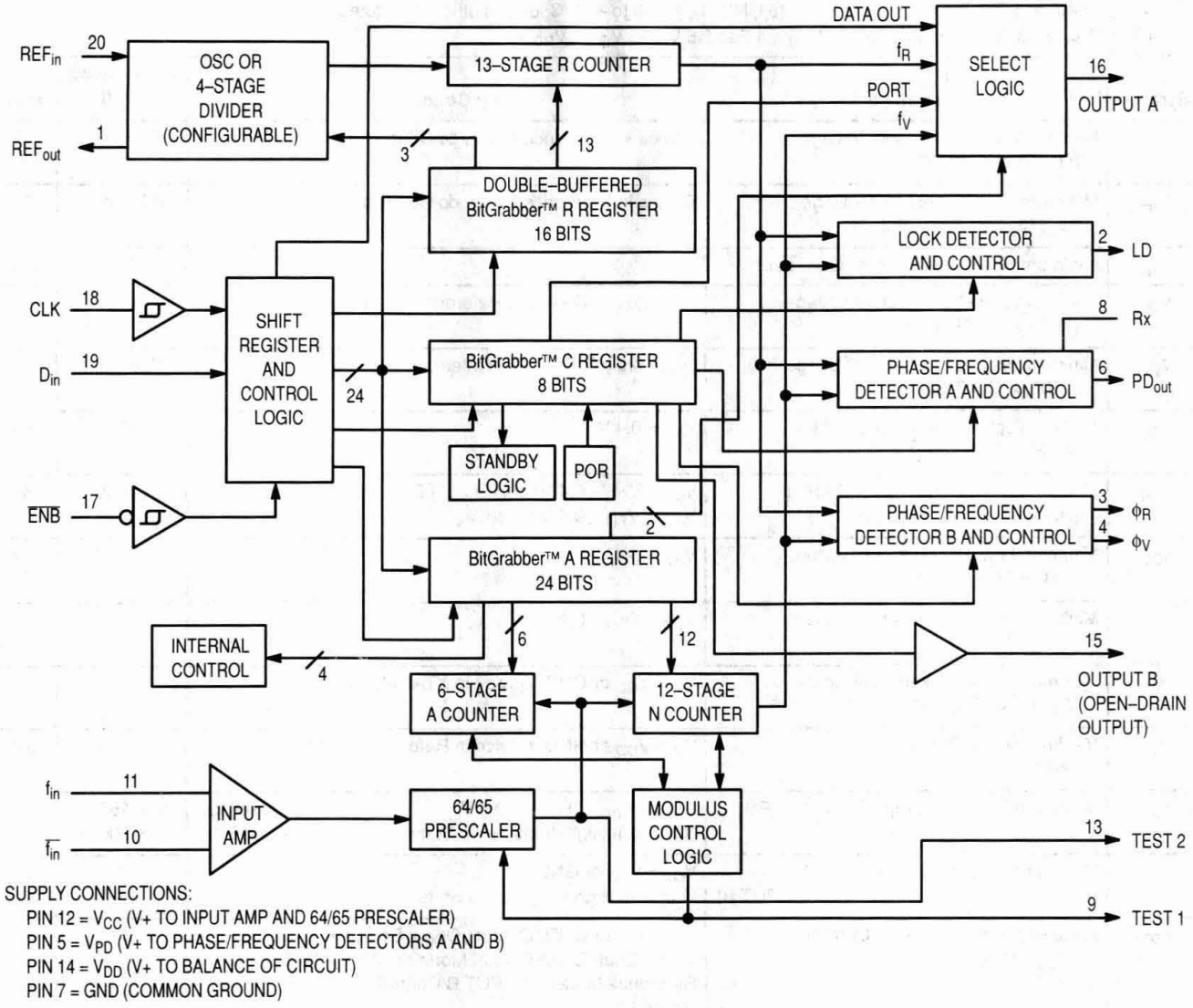
ORDERING INFORMATION

MC145190F	SOG Package
MC145191F	SOG Package
MC145190DT	TSSOP
MC145191DT	TSSOP

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5) MC145190 MC145191	V_{DD} – 0.5 to + 9.5 V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = −40 to +85°C, unless otherwise stated; MC145190: V_{PD} = 8.0 to 9.5 V; MC145191: V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$.)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.3 × V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.7 × V_{DD}	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 μA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = –20 μA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = V_{DD} – 0.4 V for REF_{out}, LD V_{out} = V_{PD} – 0.4 V for ϕ_R, ϕ_V	– 0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A, Only)	V_{out} = V_{DD} – 0.4 V	– 0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 V or 0.5 V, Output in High–Impedance State — MC145190 MC145191	± 150 ± 200	nA
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	V_{out} = V_{PD} or GND, Output in High–Impedance State	± 10	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 22	30	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 μA	600	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 V p–p; OUTPUT A = Inactive and No Connect; REF_{out} ÷ 8; ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	*	mA

* The nominal value = 7 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \leq V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	MC145190: $V_{out} = 0.5 \times V_{PD}$	8.0	± 20	%
		9.5	± 20	
	MC145191: $V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–vs–Source Mismatch (Note 3)	MC145190: $V_{out} = 0.5 \times V_{PD}$	8.0	12	%
		9.5	12	
	MC145191: $V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	MC145190: I_{out} Variation ≤ 20%	8.0	0.5 to 7.5	V
		9.5	0.5 to 9.0	
	MC145191: I_{out} Variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40° to + 85°C.

AC INTERFACE CHARACTERISTICS ($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to + 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; MC145190: $V_{PD} = 8.0$ to 9.5 V; MC145191: $V_{PD} = 4.5$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} ONLY, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF

TIMING REQUIREMENTS

($V_{DD} = V_{CC} = 4.5$ to 5.5 V, $T_A = -40$ to + 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times – CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

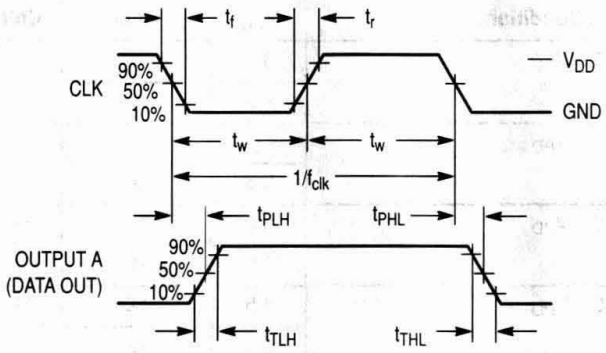


Figure 1.

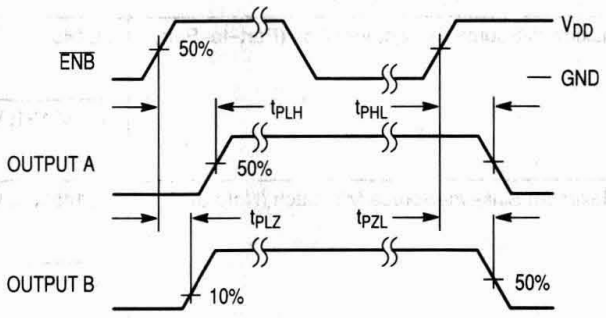


Figure 2.

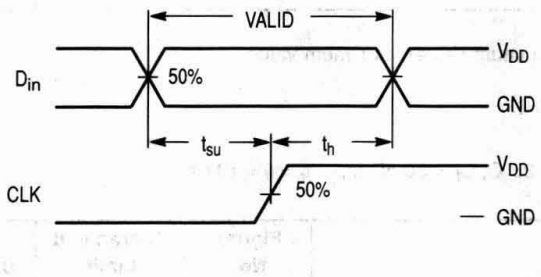


Figure 3.

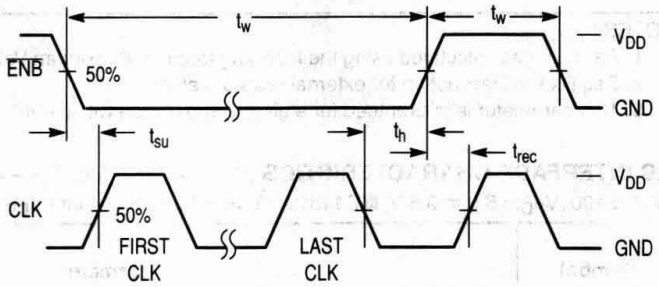
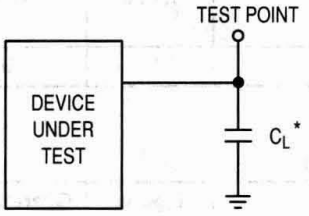
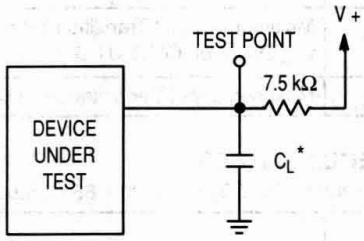


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = – 40 to + 85°C)

Symbol	Parameter		Test Condition	Figure No.	Guaranteed Operating Range		Unit
					Min	Max	
V_{in}	Input Voltage Range, f_{in}		100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	7	400 200	1500 1500	mV p–p
f_{ref}	Input Frequency Range, REF_{in} Externally Driven in Reference Mode	MC145190 MC145191	V_{in} ≥ 400 mV p–p V_{in} ≥ 1 V p–p V_{in} ≥ 400 mV p–p V_{in} ≥ 1 V p–p	8	13 6* 12 4.5*	27 27 27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode		C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}		C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors				dc	2	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, LD	MC145190 MC145191	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	17	85	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, ϕ_R — MC145191		C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance, REF_{in}				—	5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

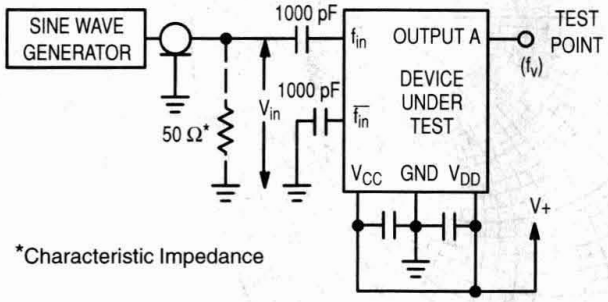


Figure 7. Test Circuit

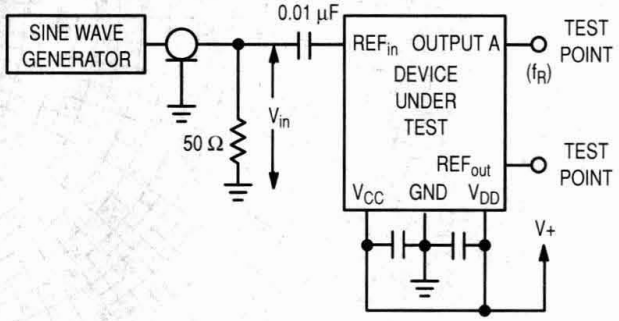


Figure 8. Test Circuit — Reference Mode

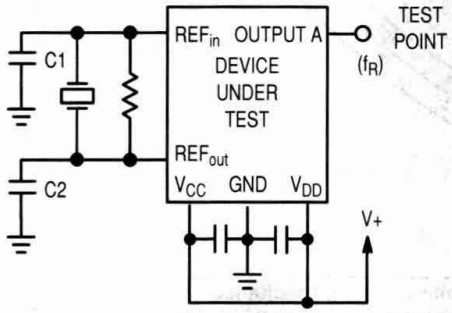


Figure 9. Test Circuit — Crystal Mode

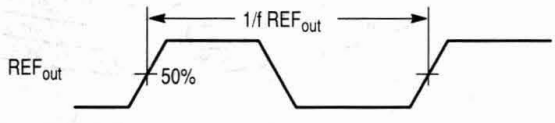


Figure 10. Switching Waveform

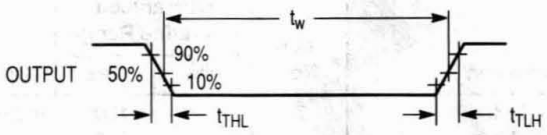


Figure 11. Switching Waveform

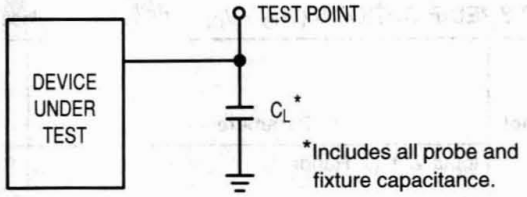
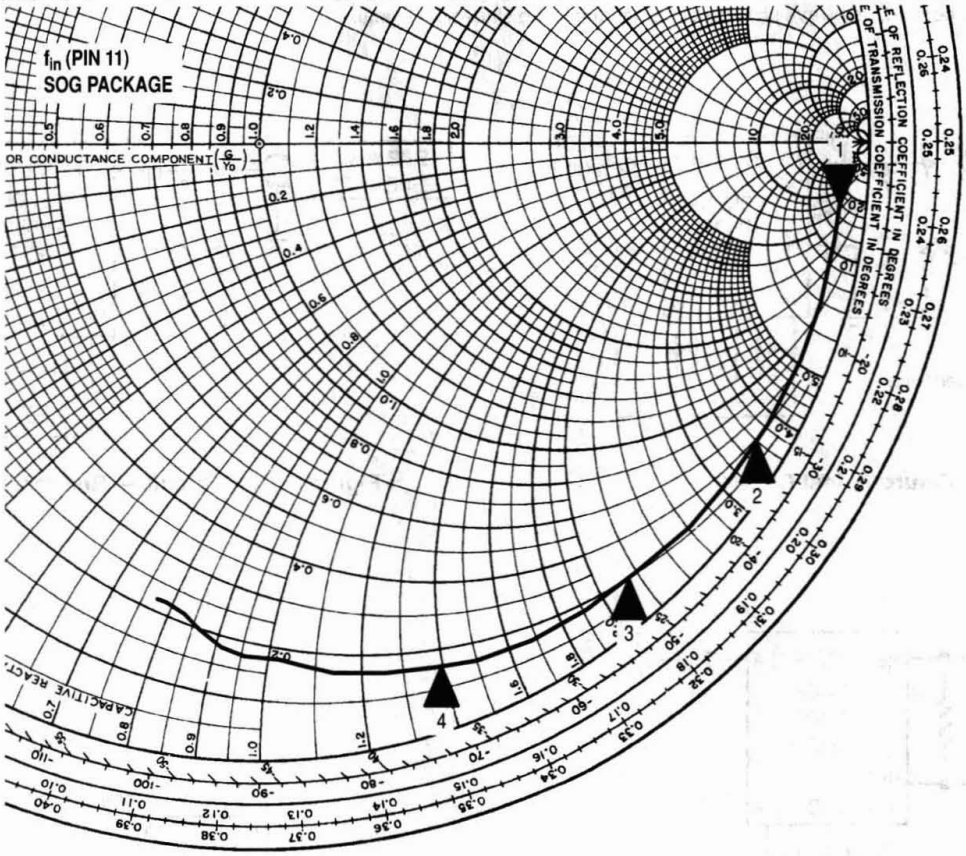


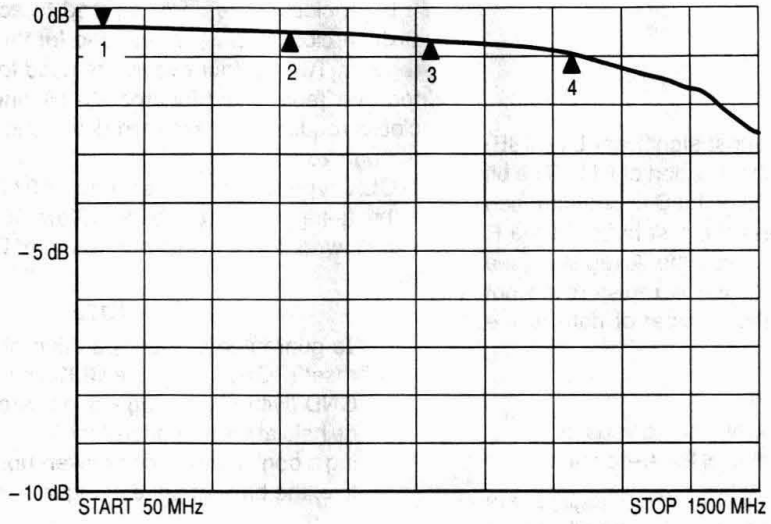
Figure 12. Test Circuit

NORMALIZED INPUT IMPEDANCE AT f_{in} — SERIES FORMAT (R + jX)
(100 MHz to 1.1 GHz)

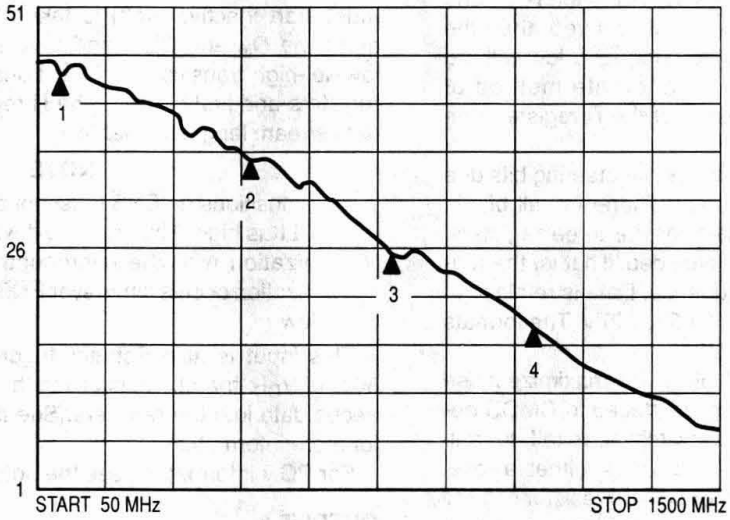


Marker	Frequency (MHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	100	338	– 785	2.03
2	500	20.2	– 183	1.74
3	800	11.5	– 109	1.83
4	1100	8.2	– 70.2	2.06

RETURN LOSS AT f_{in}



STANDING WAVE RATIO AT f_{in}



Marker	Frequency (MHz)	SWR	Return Loss (dB)
1	100	43.7	0.40
2	500	34.7	0.48
3	800	25.3	0.68
4	1100	17.9	0.98

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 17).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 15, 16, and 17.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	See Figure 13	
Values > 32	See Figures 22 – 25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 24 through 26.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. As an alternative, the bit sequence of Figure 13 may be used.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler,

A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 9.5 V for the MC145190 and 5.5 V for the MC145191.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 17) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one–to–one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function (no dead zone). The operation of the phase/frequency detector is described below and is shown in Figure 18.

- POL bit (C7) in the C register = low (see Figure 15)
  - Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
  - Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
  - Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter
- POL bit (C7) = high
  - Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
  - Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
  - Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the

floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)

Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD

Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 18).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx

External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 47 kΩ when V_{PD} is 9 V or about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1

Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

TEST 2

Prescaler Output (Pin 13)

This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD}

Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}

Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +4.5 to +5.5 V with respect to the GND pin. In the standby mode, the VCC pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 22.

For optimum performance, VCC should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{PD}

Positive Power Supply (Pin 5)

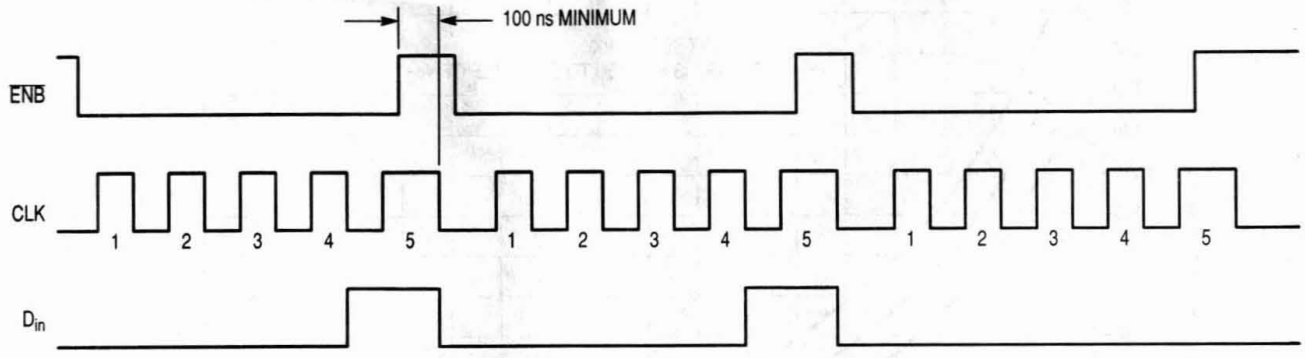
This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be +9.5 V with respect to the GND pin for the MC145190 and +5.5 V for the MC145191.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND

Ground (Pin 7)

Common ground.



NOTE: It may not be convenient to control the $\overline{ENB}$ or CLK pins during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the CLK must remain high at least 100 ns after $\overline{ENB}$ is brought high. Note that 3 groups of 5 bits are needed.

Figure 13. Initializing the PLL through the Serial Port

MC145190
Nominal PD_{out} Spurious Current vs f_R Frequency
(1 V < PD_{out} < V_{PD} – 1 V)

f_R (kHz)	Current (RMS nA)
10	1.6
20	5.3
50	22
100	95
200	320

MC145191
Nominal PD_{out} Spurious Current vs f_R Frequency
(1 V < PD_{out} < V_{PD} – 1 V)

f_R (kHz)	Current (RMS nA)
10	3.6
20	4.6
50	17
100	75
200	244

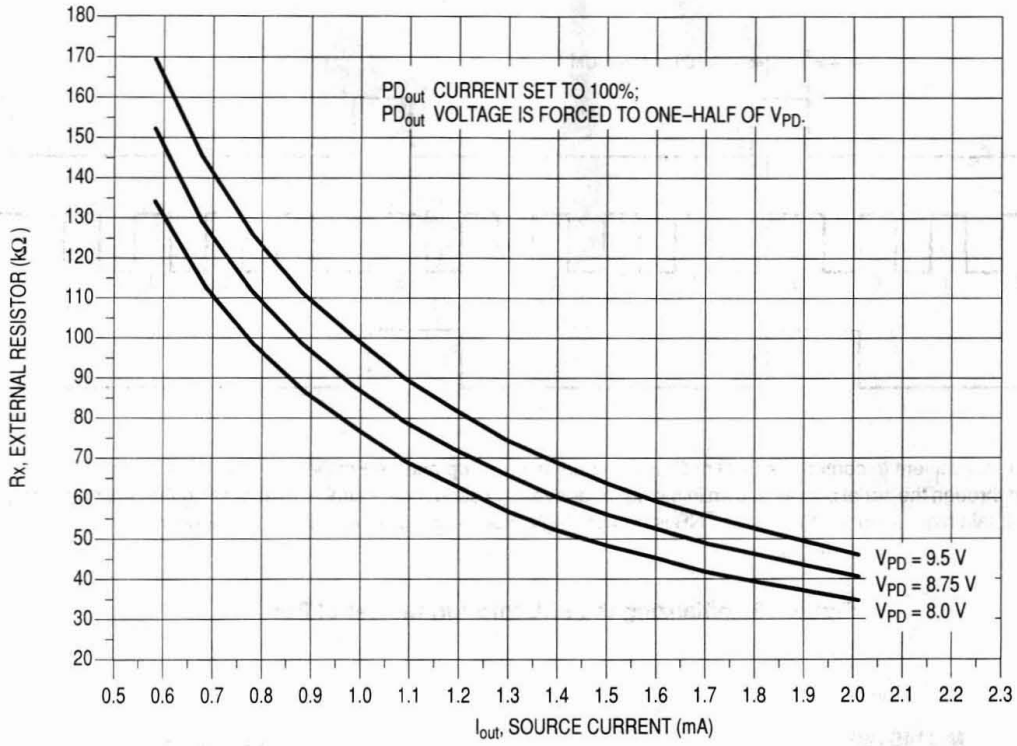
NOTE: For information on spurious current measurement see AN1253/D, "An Improved PLL Design Method Without ω_n and ζ".

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

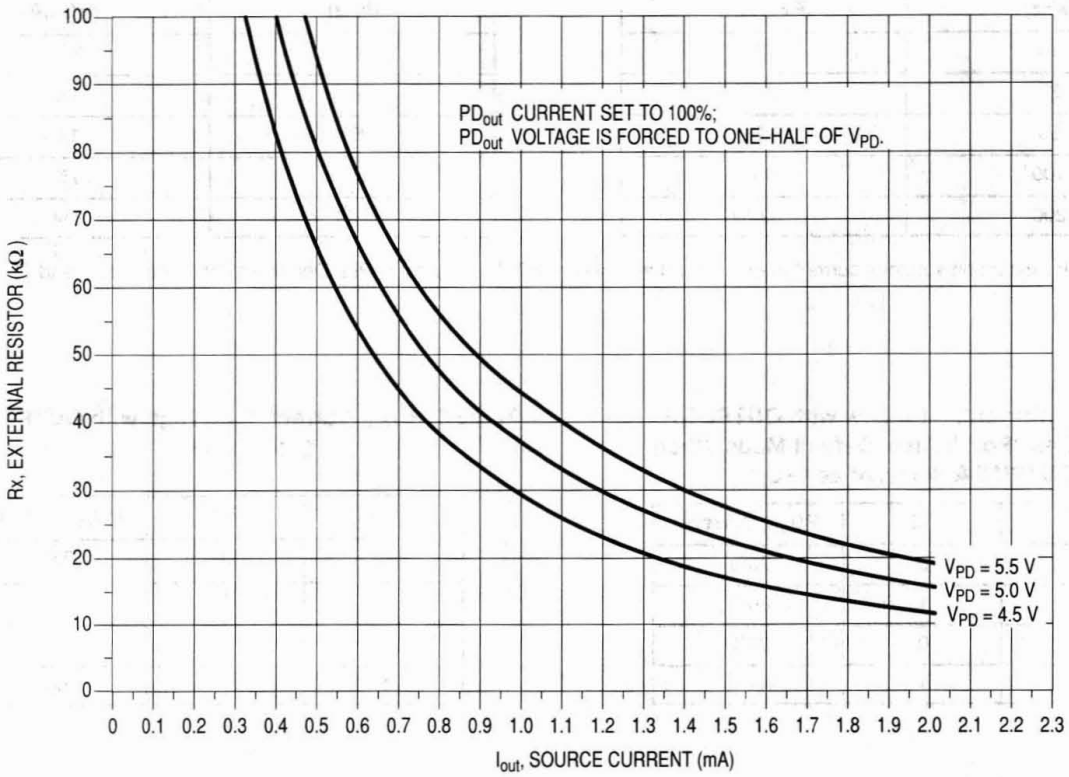
C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%


PDout CURRENT SET TO 100%;
PDout VOLTAGE IS FORCED TO ONE–HALF OF VPD.
VPD = 9.5 V
VPD = 8.75 V
VPD = 8.0 V
Rx, EXTERNAL RESISTOR (kΩ)
Iout, SOURCE CURRENT (mA)

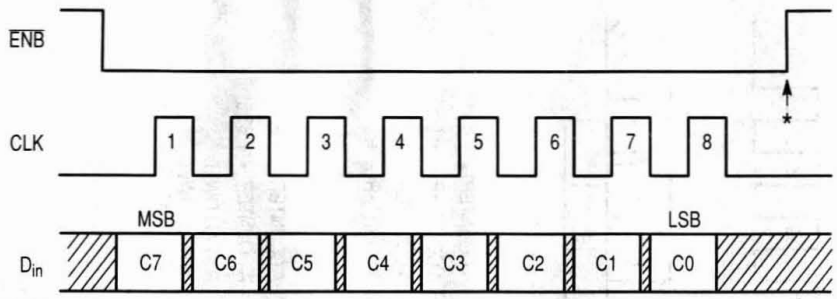
Nominal MC145190 PD_{out} Source Current vs Rx Resistance


PDout CURRENT SET TO 100%;
PDout VOLTAGE IS FORCED TO ONE–HALF OF VPD.
VPD = 5.5 V
VPD = 5.0 V
VPD = 4.5 V
Rx, EXTERNAL RESISTOR (kΩ)
Iout, SOURCE CURRENT (mA)

Nominal MC145191 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145191 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts the polarity of PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 18. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles are Used)

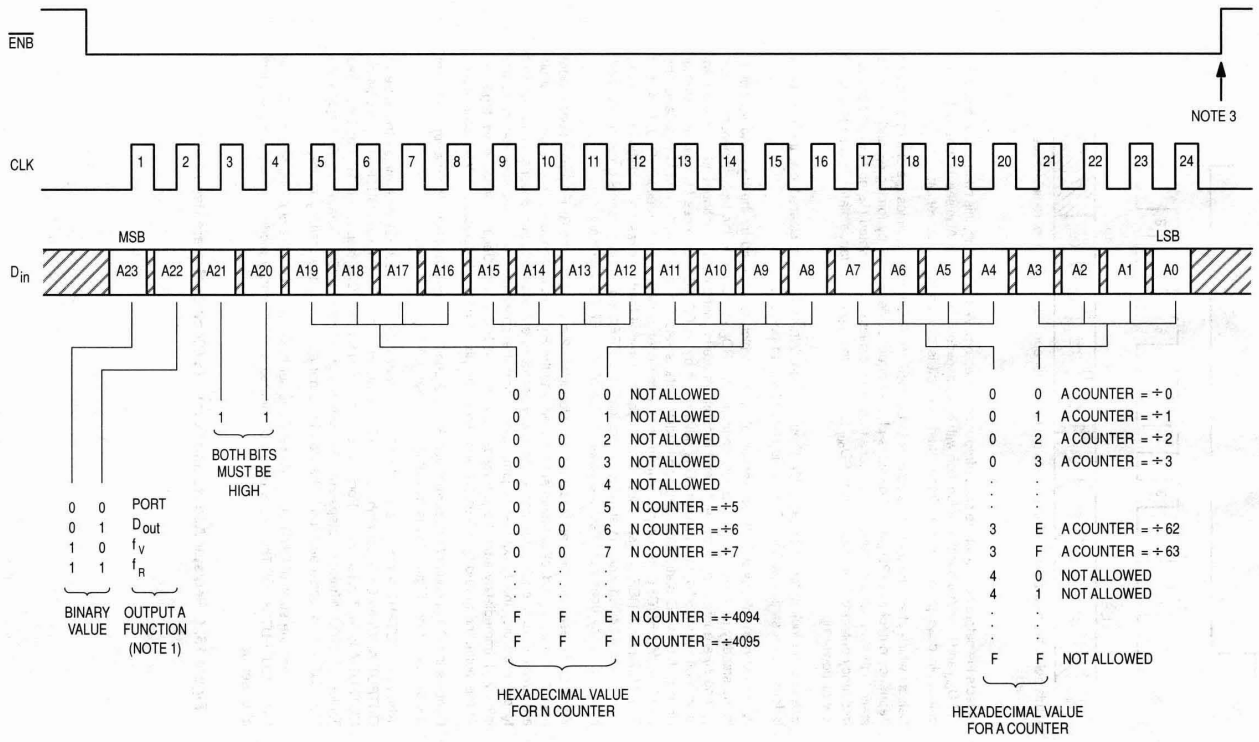
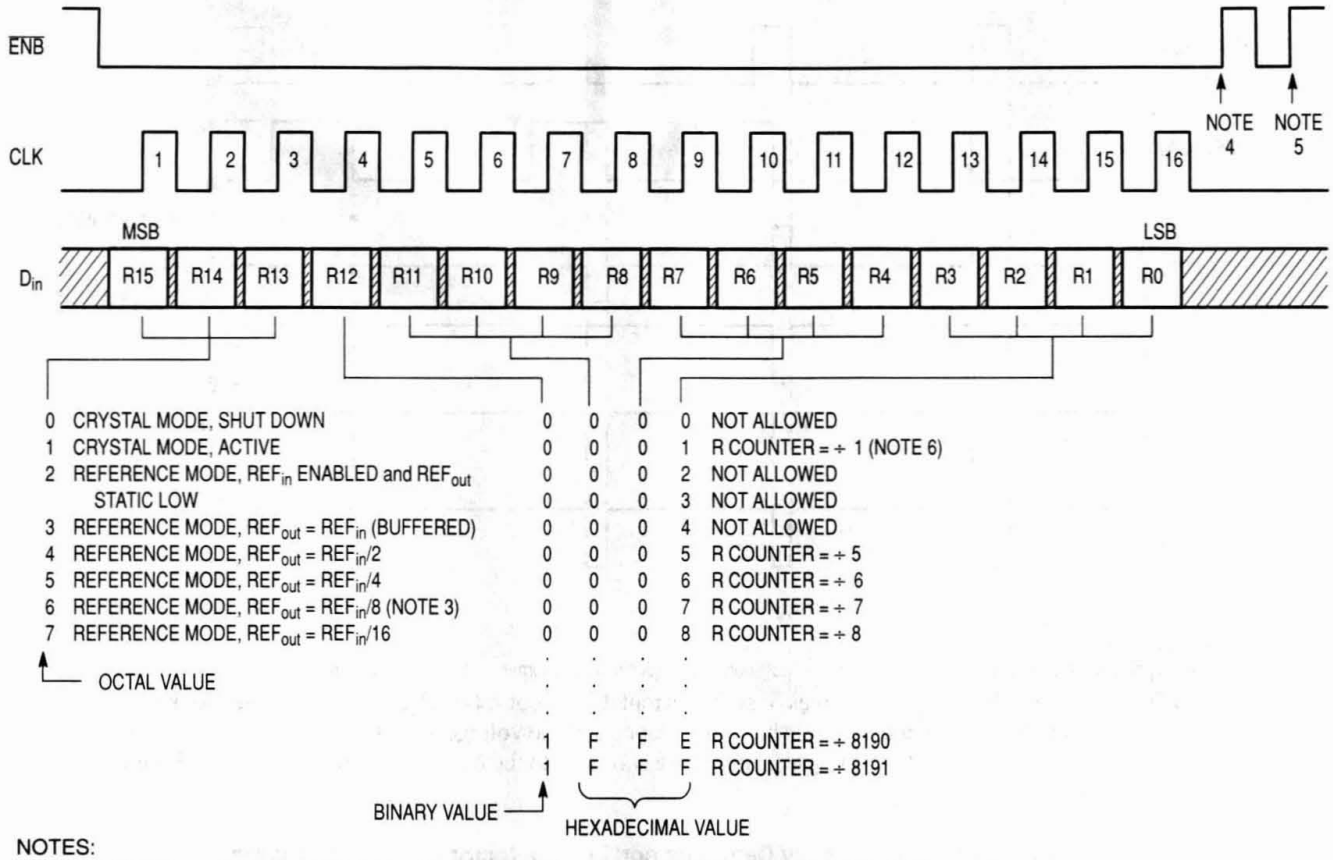

ENB
NOTE 3
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
MSB
LSB
Din
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 0 PORT Dout
0 1 fV
1 0 fR
1 1
BINARY VALUE
OUTPUT A FUNCTION (NOTE 1)
1 1
BOTH BITS MUST BE HIGH
0 0 0 NOT ALLOWED
0 0 1 NOT ALLOWED
0 0 2 NOT ALLOWED
0 0 3 NOT ALLOWED
0 0 4 NOT ALLOWED
0 0 5 N COUNTER = ÷5
0 0 6 N COUNTER = ÷6
0 0 7 N COUNTER = ÷7
F F E N COUNTER = ÷4094
F F F N COUNTER = ÷4095
HEXADECIMAL VALUE FOR N COUNTER
0 0 A COUNTER = ÷0
0 1 A COUNTER = ÷1
0 2 A COUNTER = ÷2
0 3 A COUNTER = ÷3
3 E A COUNTER = ÷62
3 F A COUNTER = ÷63
4 0 NOT ALLOWED
4 1 NOT ALLOWED
F F NOT ALLOWED
HEXADECIMAL VALUE FOR A COUNTER

Figure 16. A Register Access and Format (24 Clock Cycles are Used)

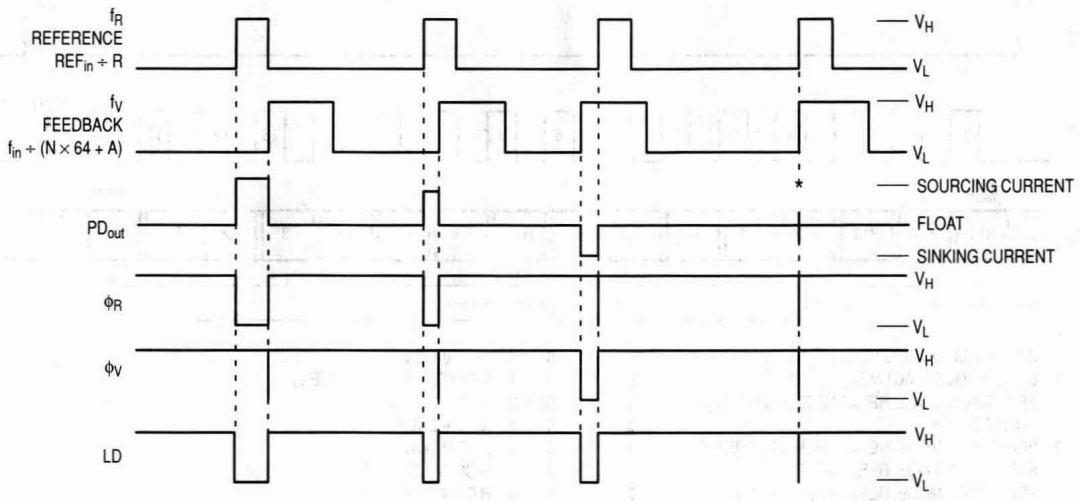
NOTES:
1. A power–on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.


ENB
CLK
NOTE 4
NOTE 5
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
MSB
LSB
Din
R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
0 CRYSTAL MODE, SHUT DOWN
1 CRYSTAL MODE, ACTIVE
2 REFERENCE MODE, REFin ENABLED and REFout STATIC LOW
3 REFERENCE MODE, REFout = REFin (BUFFERED)
4 REFERENCE MODE, REFout = REFin/2
5 REFERENCE MODE, REFout = REFin/4
6 REFERENCE MODE, REFout = REFin/8 (NOTE 3)
7 REFERENCE MODE, REFout = REFin/16
OCTAL VALUE
0 0 0 0 NOT ALLOWED
0 0 0 1 R COUNTER = ÷ 1 (NOTE 6)
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 0 4 NOT ALLOWED
0 0 0 5 R COUNTER = ÷ 5
0 0 0 6 R COUNTER = ÷ 6
0 0 0 7 R COUNTER = ÷ 7
0 0 0 8 R COUNTER = ÷ 8
1 F F E R COUNTER = ÷ 8190
1 F F F R COUNTER = ÷ 8191
BINARY VALUE
HEXADECIMAL VALUE

NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.

NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 18. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 19.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 20)
C_{out} = 6 pF (see Figure 20)
C_a = 1 pF (see Figure 20)
C1 and C2 = external capacitors (see Figure 19)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 21. The maximum drive level specified

by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 19 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

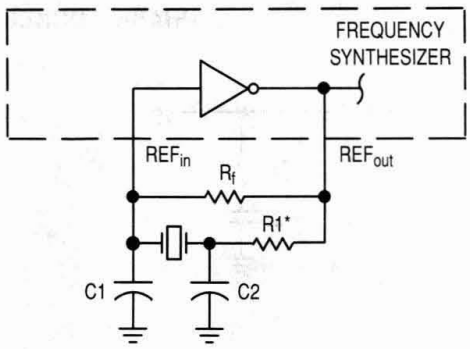
E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.



* May be needed in certain cases. See text.

Figure 19. Pierce Crystal Oscillator Circuit

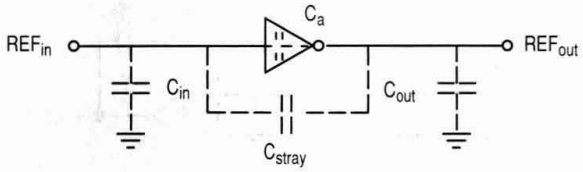
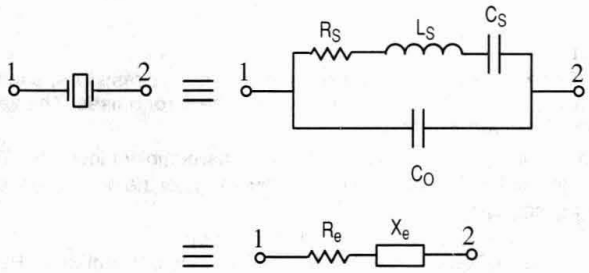


Figure 20. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 21. Equivalent Crystal Networks

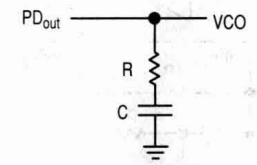
Table 4. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP—LOW PASS FILTER DESIGN

(A)



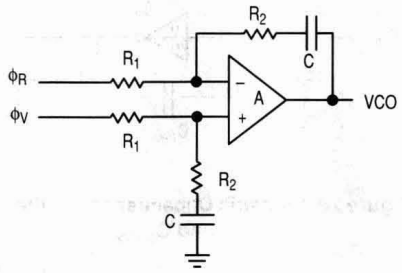
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/ filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

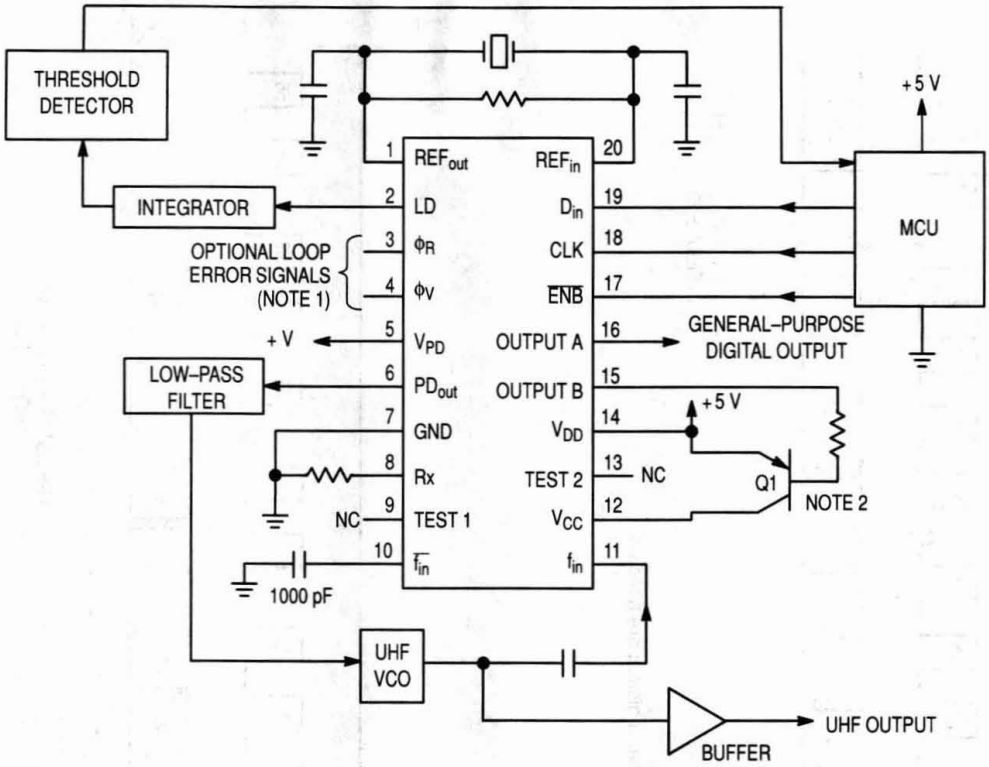
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

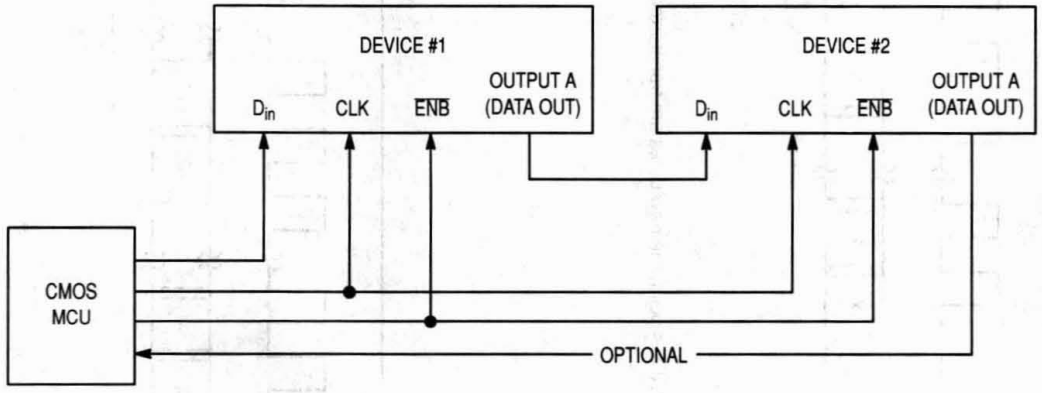
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 22. Example Application



NOTE: See related Figures 24 through 26; these bit streams apply to the MC145190, MC145191, MC145200, and MC145201.

Figure 23. Cascading Two Devices

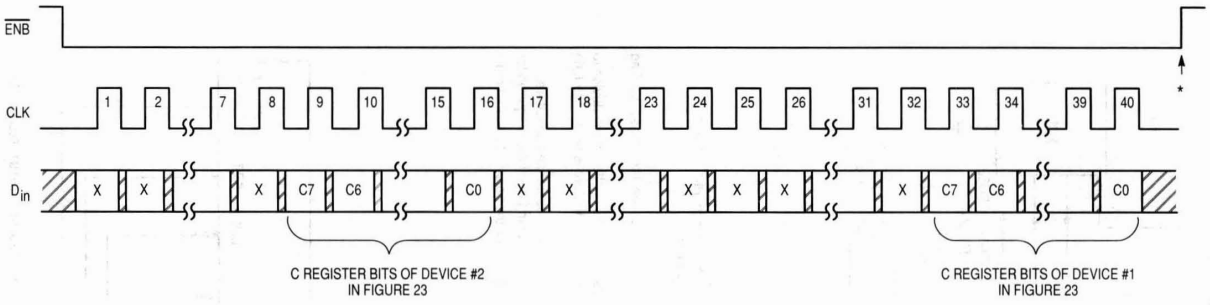


Figure 24. Accessing the C Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

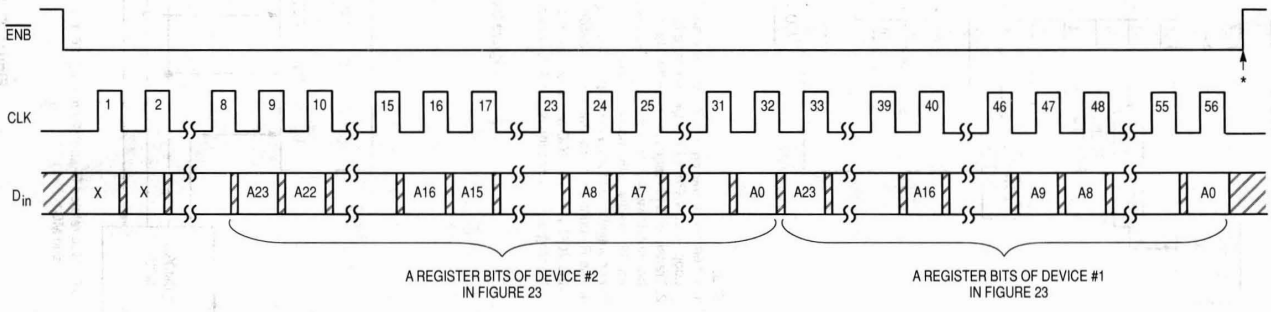


Figure 25. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

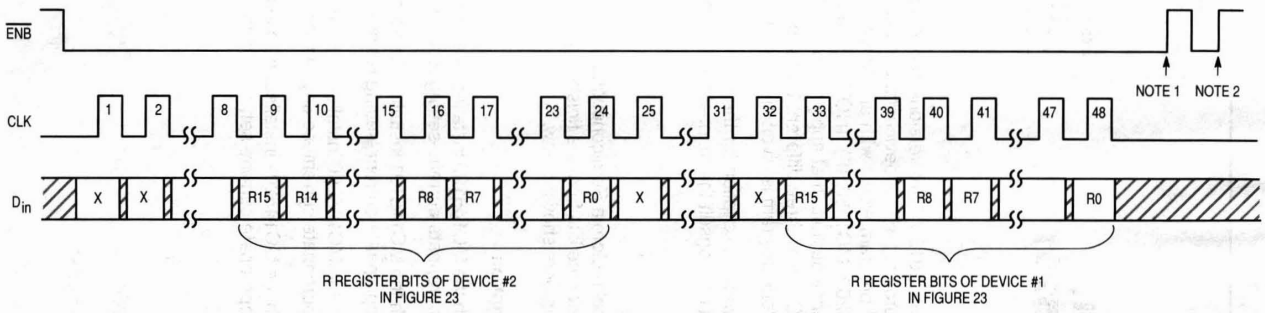


Figure 26. Accessing the R Registers of Two Cascaded Devices

NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{\text{ENB}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

MC145190EVK
MC145191EVK
MC145200EVK
MC145201EVK

Technical Summary

MC145190, MC145191, MC145200 and MC145201 Evaluation Boards

INTRODUCTION

The MC145190EVK, '191EVK, '200EVK, and '201EVK are versions of one board with a few component changes. They allow users to exercise features of the four devices and to build PLLs which meet individual performance requirements. The control program works with any board and can be used with other Motorola PLL devices (MC145192, MC145202, MC145220*). (NOTE: The MC145220 is not available with Rev. 3.0 software.) It will select frequency defaults that apply to each. All board functions are controlled through the printer port of an IBM PC. Up to three different EVKs may be controlled at the same time from one printer port. The functional block diagram is given in Figure 1.

This technical summary contains the hardware description for the evaluation board and a summary of the software section. For complete information, consult the manual that is provided in the evaluation kit.

ORDERING INFORMATION

These kits may be ordered through your local Motorola Semiconductor sales office or authorized distributor. Ask your Motorola representative to order the kits from the finished goods warehouse, not the literature distribution center. Request the part numbers shown below.

Part Number	Description
MC145190EVK	Kit with the MC145190 installed. Also includes a MC145191 device and appropriate current–setting resistor.
MC145191EVK	Kit with the MC145191 installed. Also includes a MC145190 device and appropriate current–setting resistor.
MC145200EVK	Kit with the MC145200 installed. Also includes a MC145201 device and appropriate current–setting resistor.
MC145201EVK	Kit with the MC145201 installed. Also includes a MC145200 device and appropriate current–setting resistor.

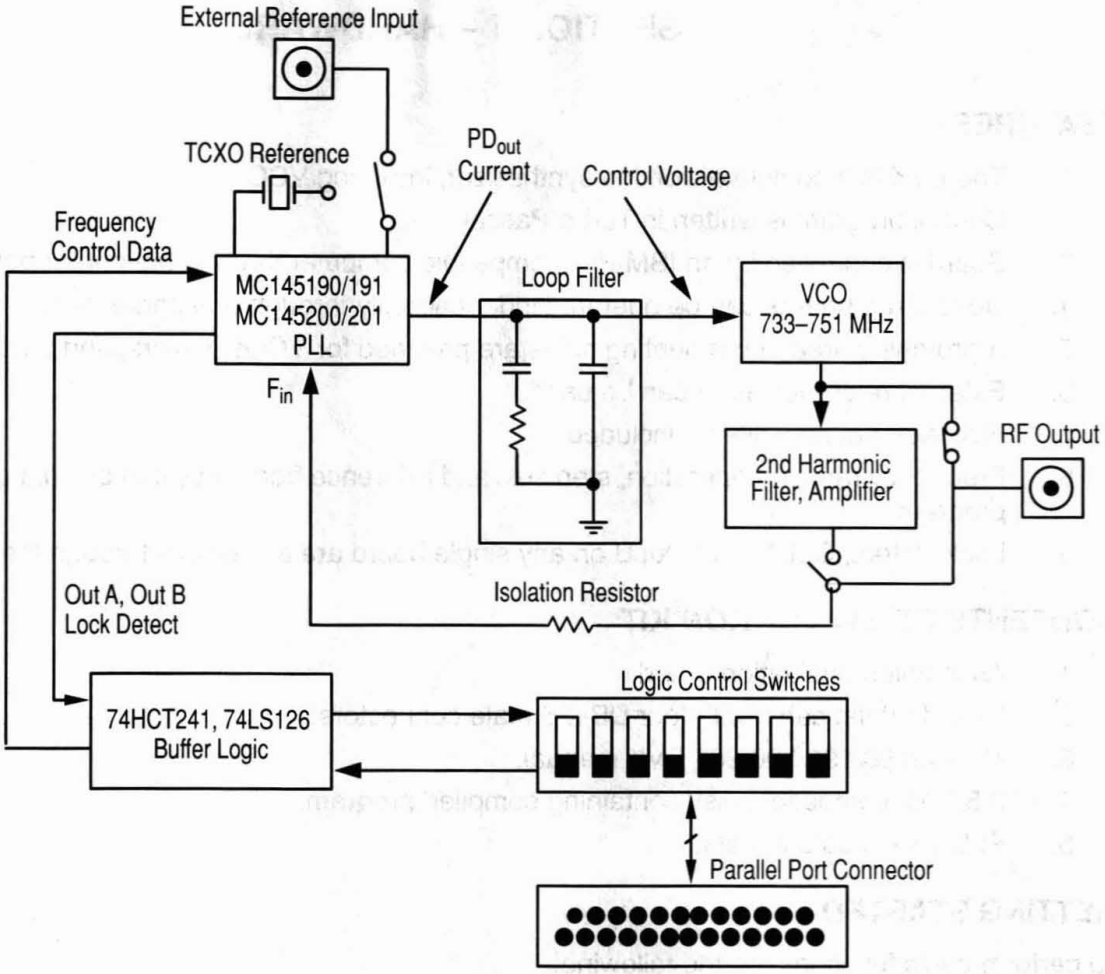


Figure 1. Evaluation Kit Block Diagram

SECTION 1 – HARDWARE

FEATURES

1. The EVK is a complete working synthesizer, including VCO.
2. Control program is written in Turbo Pascal.
3. Board is controlled by an IBM PC–compatible computer through the printer port.
4. Up to three boards can be operated independently through one printer port.
5. A prototype area and mounting holes are provided for VCOs, mixers, and amplifiers.
6. External reference input can be used.
7. Five element loop filter is included.
8. Frequency range of operation, step size and reference frequency can be changed in the control program.
9. Lock Detect, Out A, and Out B on any single board are accessible through the printer port.

CONTENTS OF EVALUATION KIT

1. Assembled evaluation board.
2. Nine–foot flat cable with four DB–25 male connectors.
3. MC145190/191/200/201 EVK manual.
4. 3.5″ PC–compatible disk containing compiled program.
5. PLL device data sheets.

GETTING STARTED

To perform basic functions, do the following:

1. Plug in 12 volts at J6, observing the polarity marked on the board.
2. Short circuit section 1 of the DIP switch (S1) and open circuit all other sections.
3. Connect the supplied flat cable between the computer printer port and the DB–25 connector on the board (J5).
4. Type PLLDEMO at the DOS prompt. Then press enter.
5. Type the number that corresponds with the type of board given in the on–screen menu. Then press Q.

You should now see the main menu displayed. There should be a signal present at J8 on the current output frequency given in the main menu. If the signal is not on the correct frequency, check to see if your printer card address is $278 (hexadecimal 278). If not, then select the P menu item and enter the correct address. After returning to the main menu, select the I menu item to send data to the board. You should now be on frequency.

MODIFICATIONS

The user may modify the hardware, such as utilizing a different VCO, by using the prototyping area of the board. After such modifications are made, the default values in the software may need to be changed. This is facilitated from screen #2 'Select from the available options' screen.

Note that the on–board voltage regulators allow for maximum control voltage to the VCO of approximately 7.8 V for the MC145190EVK and MC145200EVK. The maximum VCO control voltage is approximately 4.3 V for the MC145191EVK and MC145201EVK. The minimum voltage for all four devices is 0.5 V.

TYPICAL PERFORMANCE

Common to all four kits, unless noted.

Supply Voltage (J6)	11.5 – 12.5 V
Supply Current (J6) (Note 1)	120 mA
Available Current (Note 2)	60 mA
Frequency Range ('190)	741 – 751 MHz
Frequency Range ('191)	733 – 743 MHz
Frequency Range ('200)	1482 – 1502 MHz
Frequency Range ('201)	1466 – 1486 MHz
Reference Frequency	14.4 MHz
Temperature Stability (– 30°C to + 85°C)	< ± 2 ppm
TCXO Aging	< ± 1 ppm / year
Step Size ('190, '191)	100 kHz
Step Size ('200, '201)	200 kHz
Power Output	5 – 8 dBm
2nd Harmonic Level ('190, '191)	< – 18 dB
Fundamental Level ('200, '201)	< – 28 dB
3rd Harmonic Level	< – 18 dB
Frequency Accuracy ('190, '191)	± 1.5 kHz
Frequency Accuracy ('200, '201)	± 3.0 kHz
Reference Sidebands	– 70 dB
Phase Noise (100 Hz, '190, '191)	– 69 dBc/Hz
Phase Noise (100 Hz, '200, '201)	– 64 dBc/Hz
Phase Noise (10 kHz, '190, '191) (Note 3)	– 99 dBc/Hz
Phase Noise (10 kHz, '200, '201) (Note 3)	– 92 dBc/Hz
Switching Time (Note 4)	2.6 ms

NOTES:

1. Supply current is current the board requires without user modifications.
2. Available current is the sum of currents available to the user (in the prototype area) from the 5 V and 8.5 V supply. The 12 V supply is not regulated. Current at 12 V is limited by the external power supply. If the on–board VCO and amplifier are disconnected from the power bus, more current can be drawn in the prototype area. The current flowing into U3 (the 8.5 V regulator) should not exceed 180 mA. This will limit temperature rise in U3.
3. 10 kHz phase noise is limited by the PLL device noise. For low noise designs, the loop bandwidth is made more narrow and the VCO is relied upon to provide the 10 kHz phase noise. This can be seen on the EVKs since the VCO has much lower noise.
4. 10 MHz step, within ± 1 kHz of final frequency ('190, '191).
   20 MHz step, within ± 2 kHz of final frequency ('200, '201).

SUPPORT MATERIAL

To provide further information, the following documents are included:

1. Schematic diagram of '190/191/200/201EVK.
2. Separate Bill of Materials for each board.
3. Parts layout diagram.
4. Mechanical drawing of board.
5. MC145190/191 and MC145200/201 data sheets.
6. Printer port diagram.
7. Typical signal plots for each type of EVK.

PRODUCTION TEST

After assembly is complete, the following alignment and test is performed on '190 and '191EVK ('200 and '201EVK):

1. The control program is started in single board '190EVK ('200EVK) mode.
2. L menu item is selected.
3. Power is applied to the board. DIP switch section 1 is closed circuit with all others being open circuit.
4. After attaching computer cable, menu item I is selected.
5. Trim resistor VR1 is adjusted to obtain an output frequency at J8 of 740.999 – 741.001 MHz (1481.998 – 1482.002 MHz).
6. Voltage at the control voltage test point is measured. It must be 2.8 – 3.6 V.
7. When testing more than 1 board, steps 3 – 6 are repeated.

If in step 5 it isn't possible to obtain a signal on frequency, menu item P should be selected and the correct printer port address entered. Menu item I would then be selected to reload the data.

BOARD OPERATION

A computer is connected to the DB–25 connector J5. Data is output from the printer port. The printer card is in slot 0 using the default address in the control program. Data is sent to the PLL device (U1) through the DIP switch (S1), and 74HCT241 buffer (U5). A '190/191/200/201 PLL has three output lines which are routed through a 74LS126 line driver (U2) to the computer.

U5, the 74HCT241, provides isolation, logic translation and a turn–on delay for PLL input lines. Logic translation is needed from the TTL levels on the printer port to the CMOS levels on the '190/191 inputs. Turn–on delay is used to ensure the power–on reset functions properly. The clock line to the PLL must be held low during power up.

A 12 V power supply should be used to power the board at J6 (Augat 2SV–02 connector). The 2SV–02 will accept 18–24 AWG bare copper power leads. No tools are needed for connection. If power is properly connected, LED D2 will be lit.

Power passes from J6 to U3 (78M08 regulator) configured as an 8.5 V regulator. D1 increases output voltage of the regulator by 0.6 V. In the '190 and '200 boards, 8.5 V is routed through J3 to the charge pump supply, VCO, and RF amplifier. The '191 and '201 boards use 8.5 V to power the VCO and RF amplifier. J3 is a cut–trace and jumper. If it is desired to power the 8.5 V circuits directly, the trace under J3 can be cut, J3's shorting plug is removed, and 8.5 V is applied through J7 (2SV03 power connector).

Power for the 5 V logic is provided by U4 (78M05). U4 steps down the 8.5 V from U3. Output voltage from U4 passes through J4, the 5 V cut–trace and jumper. To supply separate power to logic, the trace under J4 is cut, J4 shorting plug is removed, and 5 V is applied to J7. U3 and U4 are cascaded to lower their individual voltage drops. This lowers the power dissipated in the regulators.

The PLL loop is composed of the PLL device (U1), 733 – 751 MHz VCO (M1), passive loop filter (R11, R12, C4, C5, C6) and second harmonic filter amplifier (U6). A passive loop filter was used to keep the design simple, reduce noise, and reduce the quantity of traces susceptible to stray pickup. About 56 dB rejection of fundamental and 23 dB gain is provided by the harmonic filter amplifier. This allows the '200 or '201 to lock at 1466 – 1502 MHz. The harmonic filter amplifier is bypassed on the '190 and '191.

A single VCO model is used for all boards. It is an internal Motorola part which is not sold for other applications. The '190 and '191 have different frequency ranges. This is due to the lower charge pump supply voltage of the '191. A common 10 MHz tune range allows the same loop filter components to be used. For the same reason, the '200 and '201 tune range is 20 MHz with double the step size of the '190 or '191. RF is fed to the PLL chip F_{in} input through a voltage divider. These two resistors terminate the PLL chip RF input with 50 ohms and provide isolation.

All boards use a phase detector current of 2 mA. J1 and J2 are removable jumpers and cut traces. They are used as connection points for a current measurement of V_{PD} or V_{CC}. J11 and J12 are wire jumpers that select 5 V or 8.5 V for V_{PD}. A potentiometer VR1 is used to set M2 (14.4 MHz TCXO) on frequency.

COMPONENTS UNIQUE TO EACH EVK

Components that are not the same on all EVKs are given in the following table:

	'190 EVK	'191 EVK	'200 EVK	'201 EVK
U1	MC145190	MC145191	MC145200	MC145201
R2	47 kΩ	22 kΩ	47 kΩ	22 kΩ
R8	0 Ω	0 Ω	not used	not used
C22	not used	not used	1.0 pF	1.0 pF
J11	connected	not used	connected	not used
J12	not used	connected	not used	connected

EXTERNAL REFERENCE INPUT

As shipped, all boards are configured for a 14.4 MHz TCXO (supplied). To use an external reference, disconnect J13 and connect J9. Use a reference signal at J10 which complies with data sheet requirements. Then modify the reference frequency in the program main menu to reflect the changes made ([F] menu item).

DATA TRANSFER FROM COMPUTER TO EVK

To control the serial input EVK with the parallel printer port, a conversion is done. Printer cards are designed to output 8 bits through eight lines. A bit mask is used to obtain the bit combination for the three required output lines (Data, Clock, Load). As bytes are sent to the printer card in sequence, it appears to be a serial transfer. The printer port was used because data transfer using the serial port would have been much slower. A standard IBM PC can support a parallel port data rate of 4.77 MHz.

IBM PCs and compatibles can accept up to three printer port cards. These ports are called LPT1, LPT2 and LPT3. Each printer card has jumpers or DIP switches on it to set a unique address. Two sets of addresses are in common use. One set applies to IBM PC XT, AT, and clones. The other is for the PS 2 line. To load data into the EVK, the correct address must be selected. The program default is $278, which is LPT1 in a clone. If $278 is not the address in use, it must be modified by entering the O menu item in the main menu. All allowed addresses given in hexadecimal are as follows:

Label	IBM PC and Clones	PS 2
LPT1	278	3BC
LPT2	378	378
LPT3	3BC	278

Up to three EVK boards can operate independently from one printer port. All lines on the printer port are connected to every EVK. Even with three boards operating, only three output lines (Clock, Data and Load) from the printer card are used. If two boards are controlled together, data for the second board is received from the Output A of the first. Output A is a configurable output on 190/191/200/201 devices, which in this case is used to shift data through chip 1 into chip 2. Output A and Data are connected using a printer port input line. This was done to avoid connecting extra wires. Fortunately not all port input lines are needed for computer input. Load and Clock are common to both boards.

A three–board cascade is handled similarly to a two–board cascade. Out A on the first board is fed to Data on the second. Out A on the second connects to Data on the third. Instructing the program on the quantity of boards connected together allows it to modify the number of bits sent.

All boards have a DIP switch S1 which gives each a unique address. The configuration menu is used to tell the program what type of board is connected at a board address. Switch positions for all possible addresses are given in Figure 2.

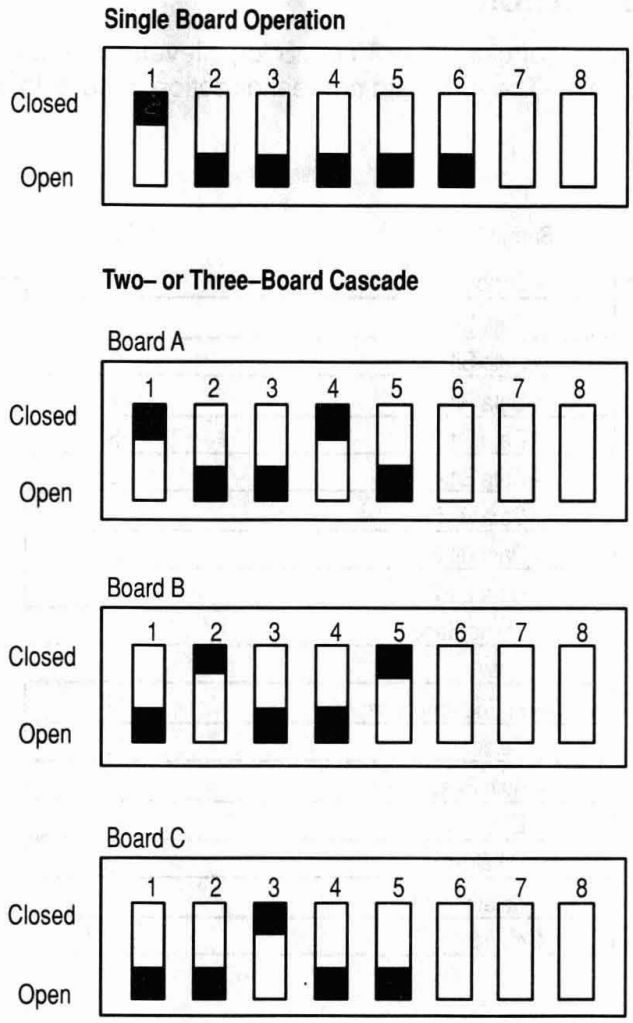


Figure 2. Switch Positions

In Figure 2, DIP switch sections 6, 7, and 8 allow the computer to read Out A, Out B or Lock Detect from the PLL device. Each of the inputs can only be read on one board at a time. But each item could be read on a different board. In a three–board cascade, Out A could be read from the first board, Out B from the second, and Lock Detect from the third. There is no way to determine in software the board address of a particular input. The control program doesn't make use of these inputs. Pin assignment on the printer port connector is:

Label	Pin Number
Out A	12
Out B	13
Lock Detect	15

PRINTER PORT CONFIGURATION

Printer port outputs on an IBM PC or clone use TTL–LS logic levels. Inputs are one TTL–LS load. Signal lines can be used for any purpose. The standard names, direction of data flow, true and inverted data are shown in Figure 3.

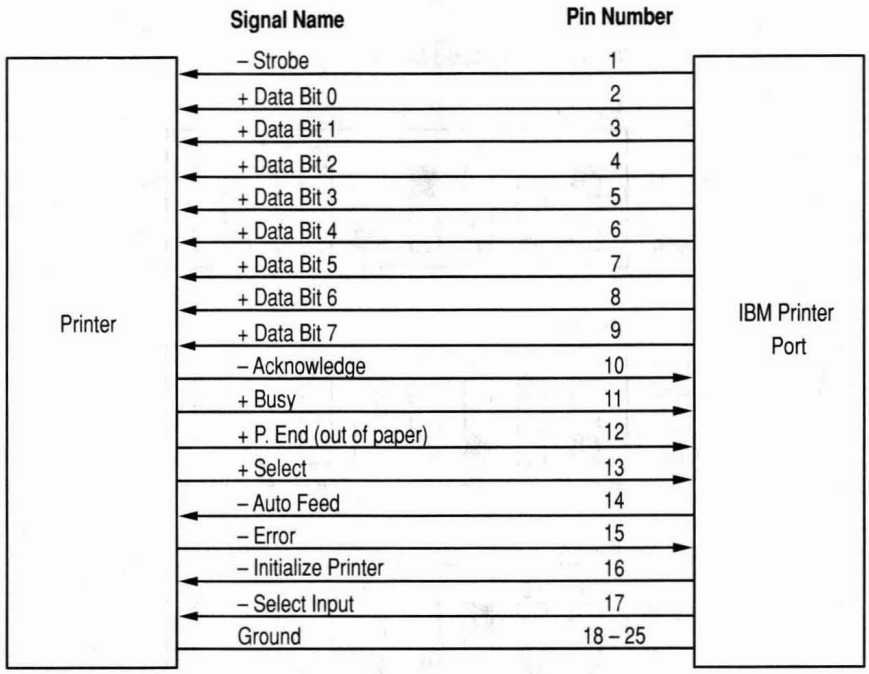


Figure 3. Printer Port Data Lines

Pin numbers for the port connector are shown in Figure 4.

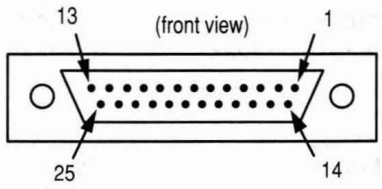


Figure 4. DB–25 Male Connector

SECTION 2 – SOFTWARE SUMMARY

The MC145xxx EVK control program is used to program all PLL evaluation kits. It will simultaneoulsy control up to three different boards independently from one printer port. All features of the PLL device may be accessed. Default frequencies can be modified to allow use of different channel spacings and VCOs.

User input errors are detected and appropriate messages are displayed.

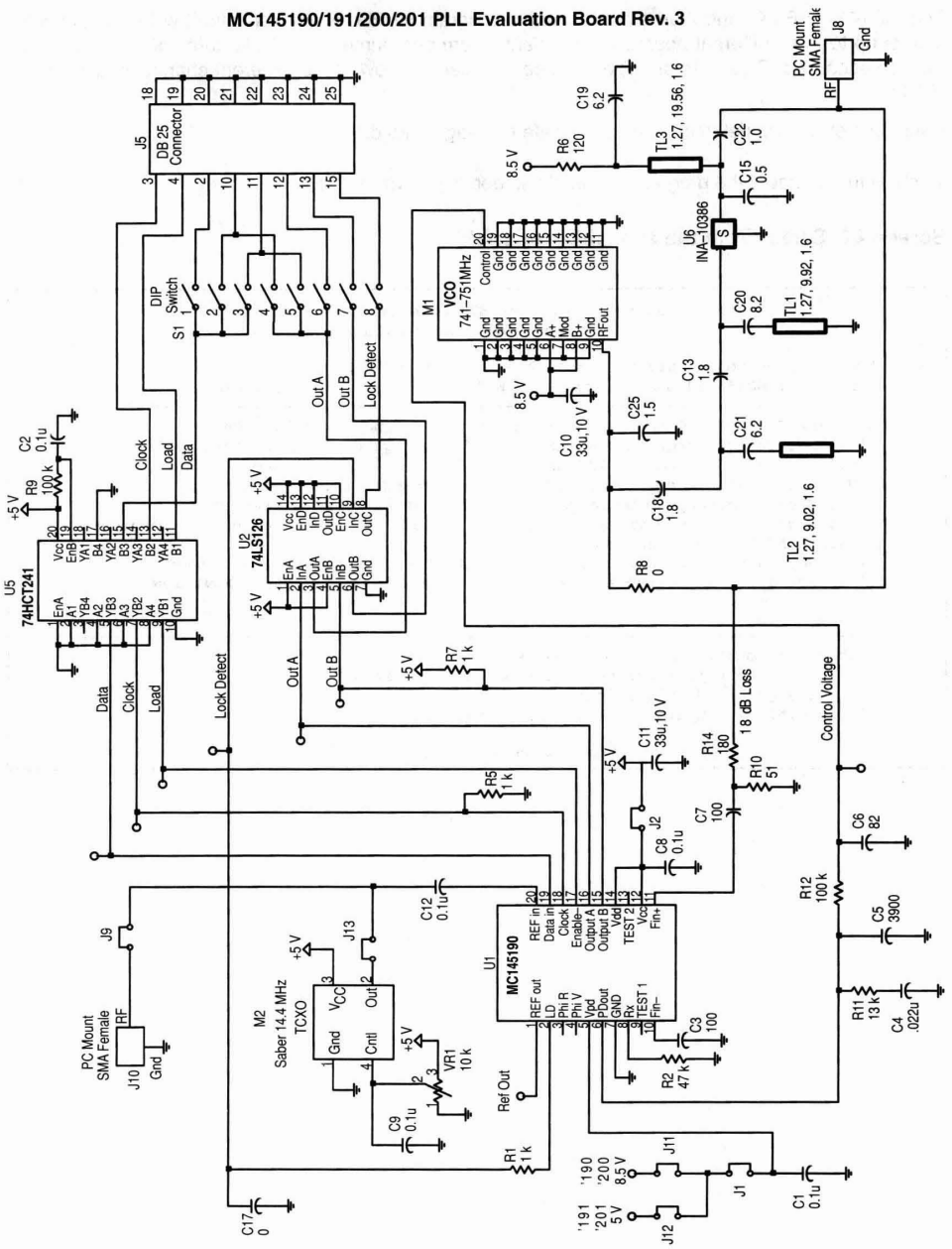
To show the format of the program, a sample screen is shown below:

Screen #2 'Select from the available options'

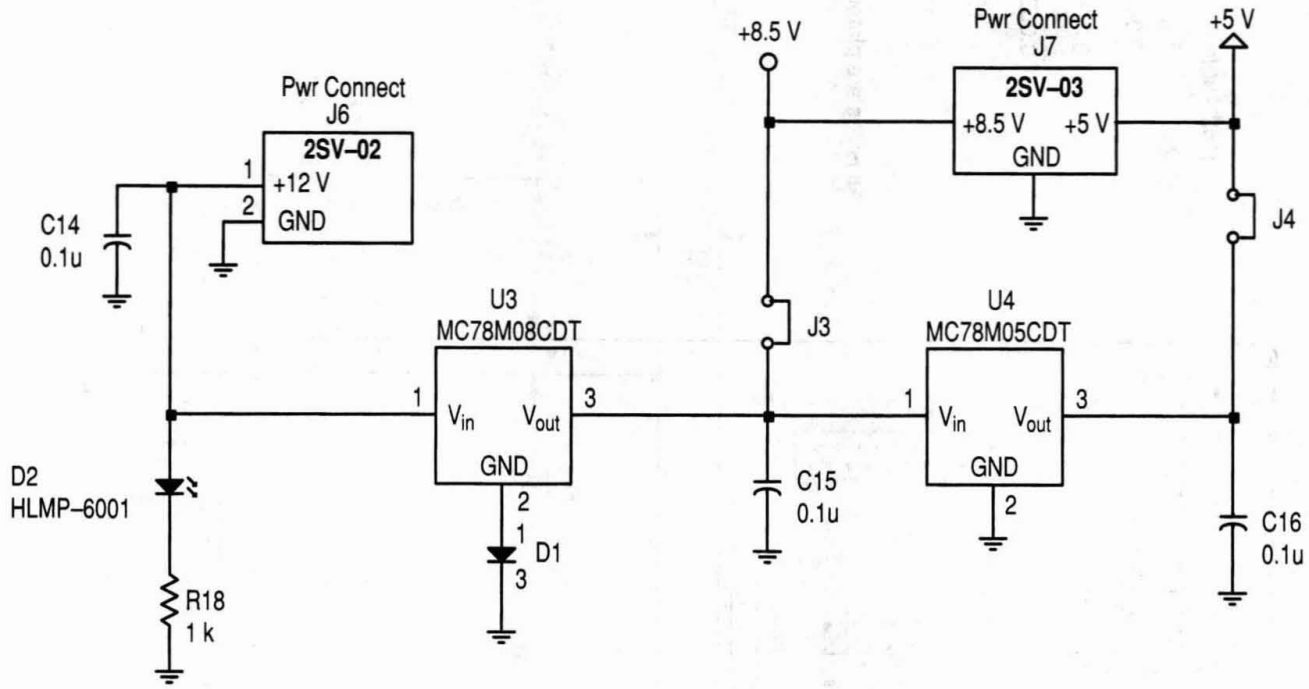
```
                Welcome to MC145xxx EVK Demonstration Program, rev 3.0
                          Select from the available options

Available Boards - Current target board is: A, MC145190 EVK
 Brd [A]!: MC145190 EVK    Brd [-]!: N/A            Brd [-]!: N/A
-------------------------------------------------------------------------------
MC145xxx Frequency Commands - Current Output Frequency is 746 MHz
 [L]! Set to low freq      741 MHz      [W] Change default low freq.
 [M]! Set to med. freq     746 MHz      [Y] Change default med. freq.
 [H]! Set to high freq.    751 MHz      [Z] Change default high freq.
 [U]! Step frequency up by step size    [O] Set PLL output frequency
 [D]! Step frequency down by step size  [F] Set REFin freq. & channel spacing
MC145xxx Additional Commands
 [E]  Set function of output A          [N] Change C register and Prescale
 [R]  Set crystal/reference mode - Current mode is Ref. mode, REFout low


-------------------------------------------------------------------------------
Initialization/System Setup Commands:
 [P]  Set output port address - Current address is $278
 [G]  Change board definitions
 [I]  Initialize board(s), Write all registers

              [X]! Terminate demonstration program. [?]! View help screen.
```

APPENDIX

MC145190/191/200/201 PLL Evaluation Board Rev. 3



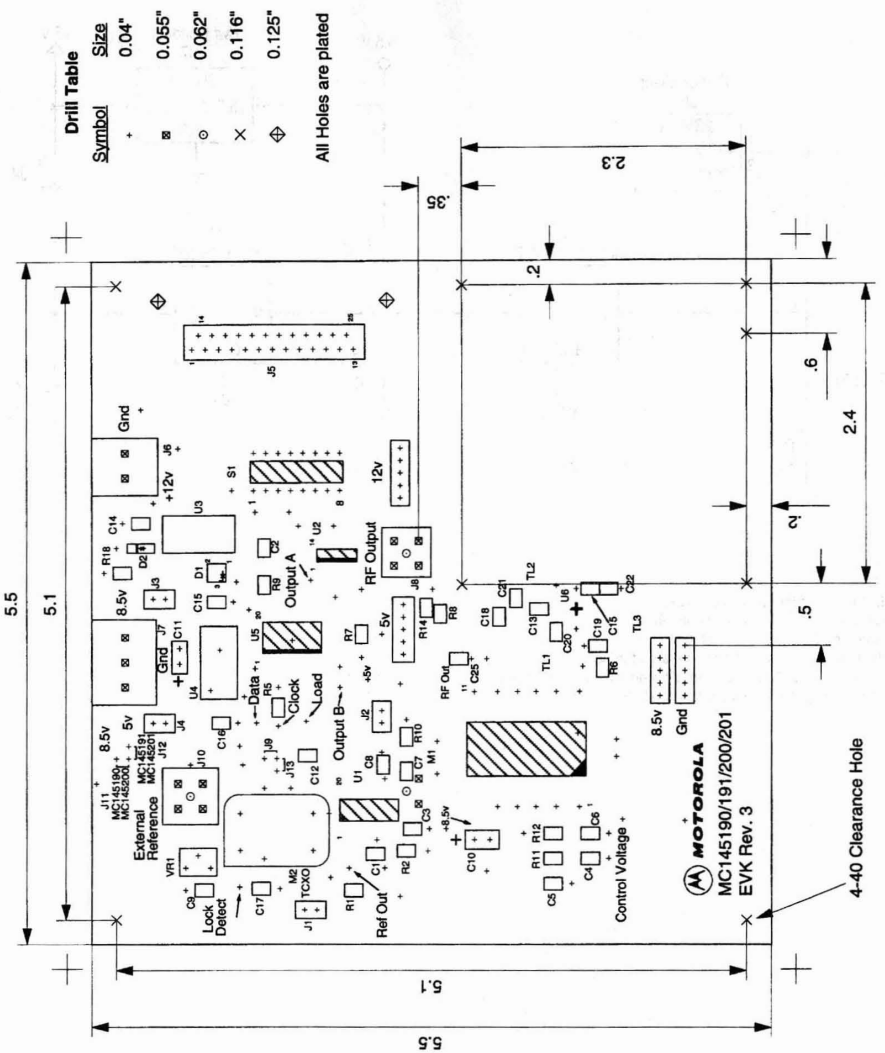
MC145190/191/200/201 Power Supply Rev. 3



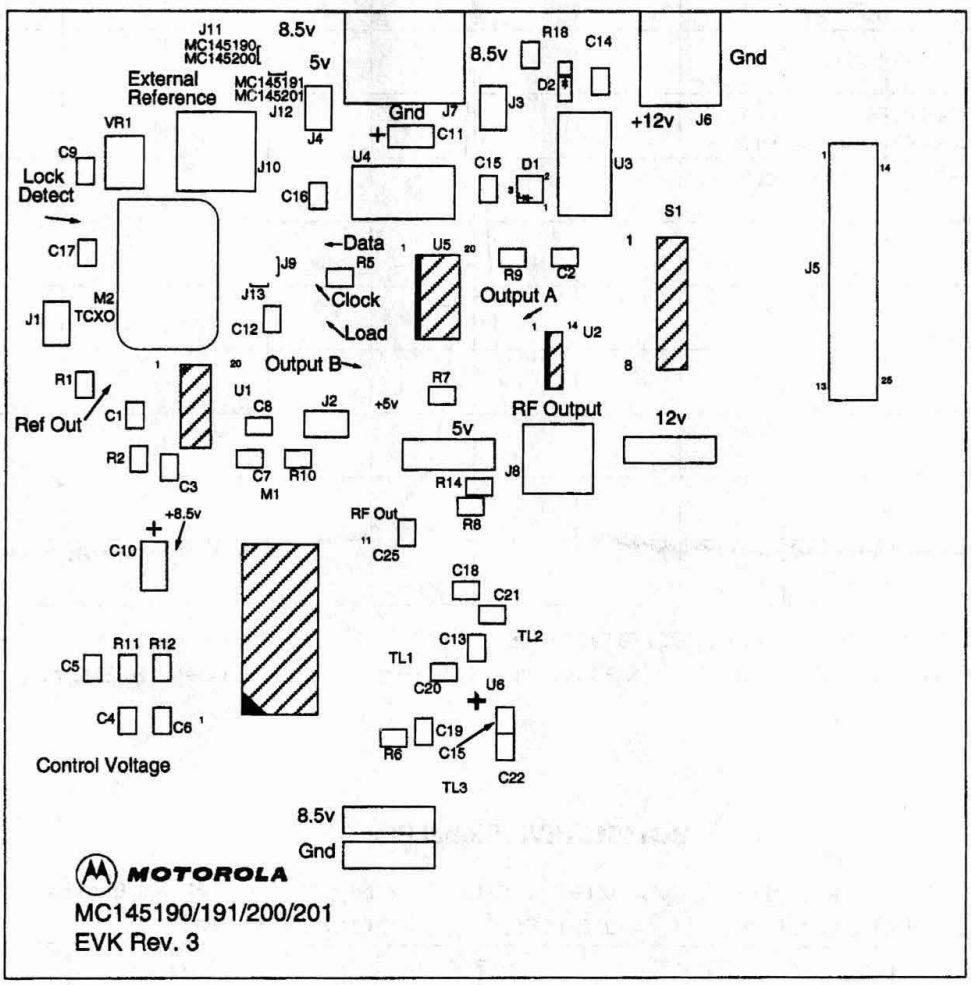
NOTES:

1. Default unit for capacitance is pF.
2. Default unit for resistance is ohms.
3. Board material is 1/16″ thick G10.
4. Test points are 0.04″ diameter plated through holes.
5. U1, R2, R8, C22, J11, J12 are different on each type of EVK. See the manual section titled "Components Unique to Each EVK".

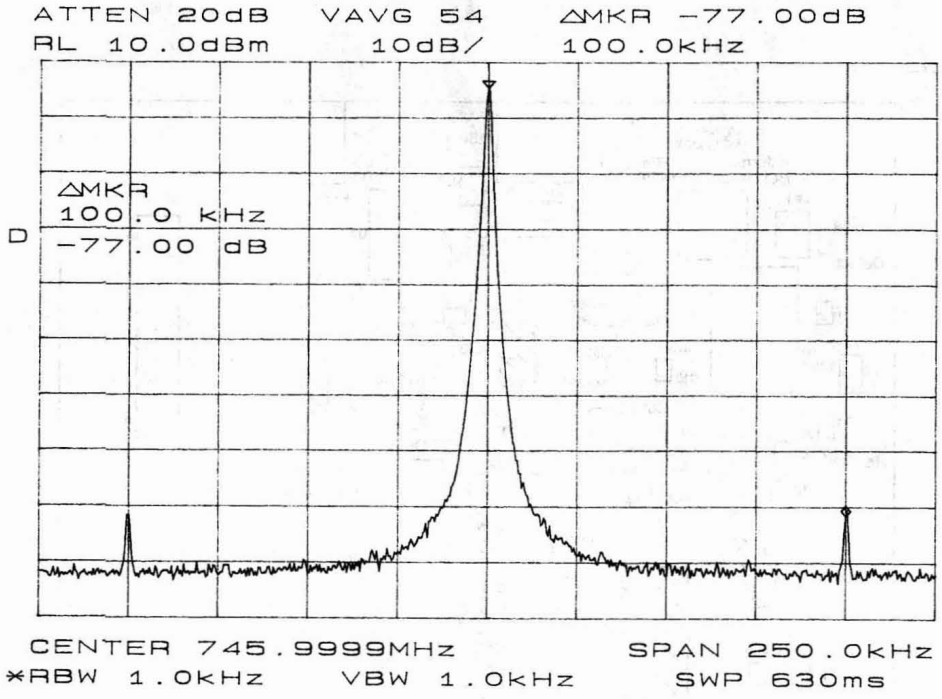
Drill Layer with Silkscreen (Top View)
Dimensions are in Inches



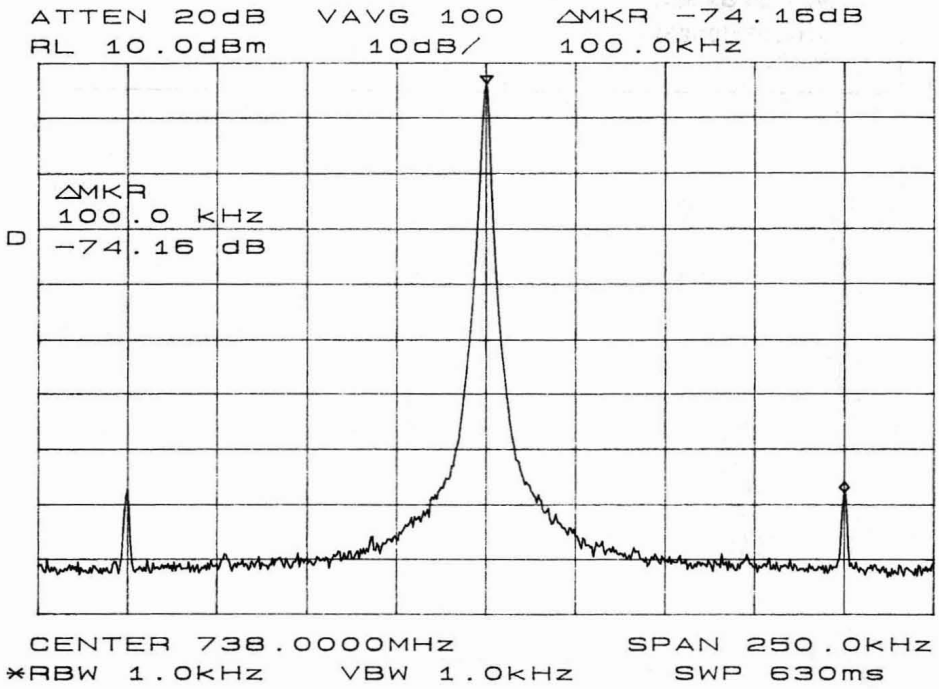
Silkscreen Layer (Top View)



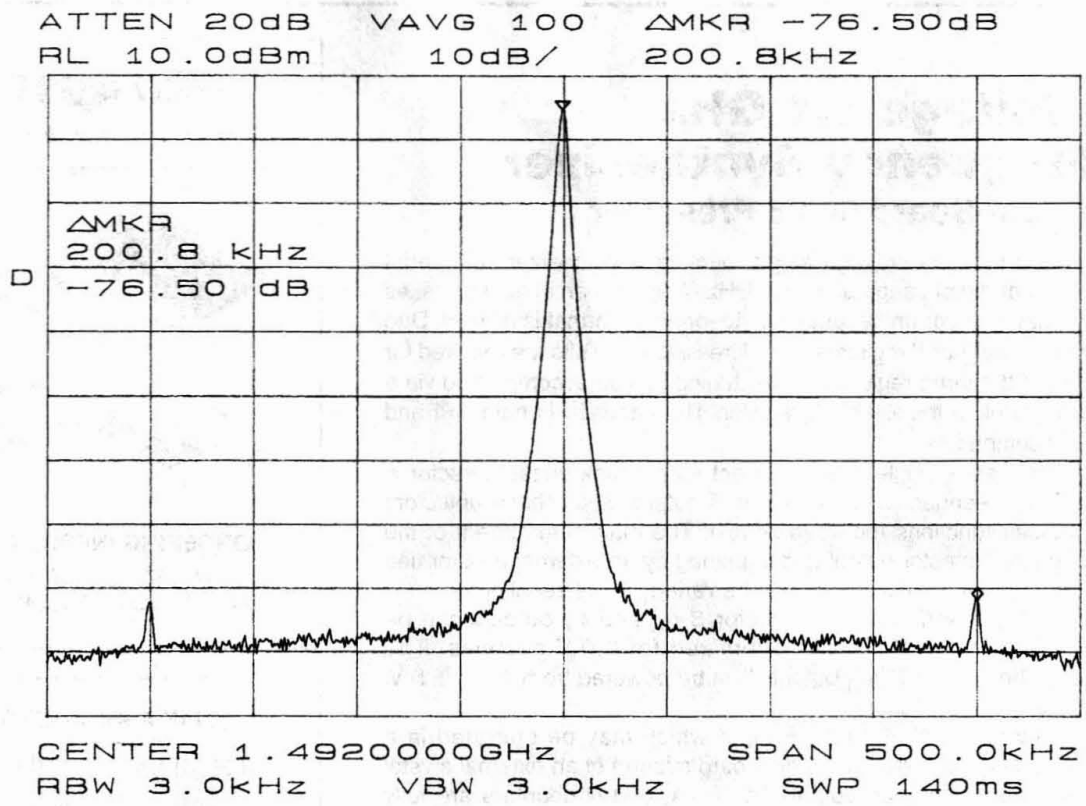
MC145190EVK Signal Plot



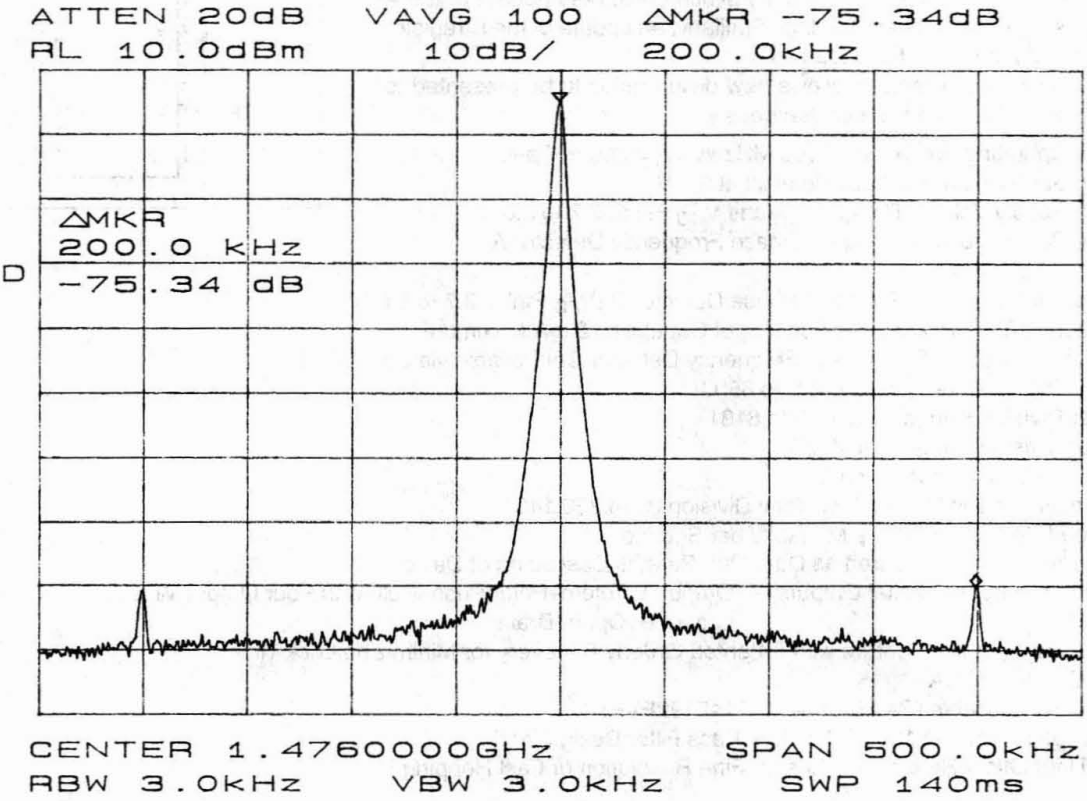
MC145191EVK Signal Plot



MC145200EVK Signal Plot



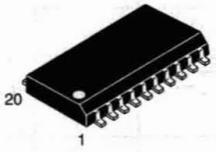
MC145201EVK Signal Plot



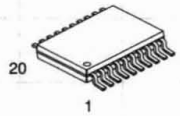
MC145192

Low-Voltage 1.1 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler



F SUFFIX
SOG PACKAGE
CASE 751J

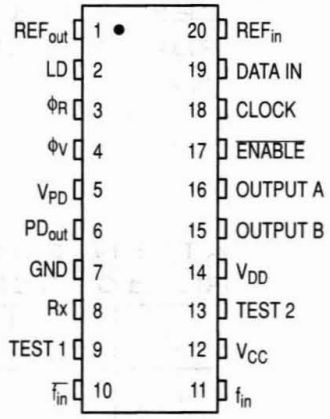


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145192F	SOG Package
MC145192DT	TSSOP

PIN ASSIGNMENT



The MC145192 is a low–voltage single–package synthesizer with serial interface capable of direct usage up to 1.1 GHz. A special architecture makes this PLL very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

The MC145192 phase/frequency detector B ϕ_R and ϕ_V outputs can be powered from 2.7 to 5.5 V. This is optimized for 3.0 V systems. The phase/frequency detector A PD_{out} output must be powered from 4.5 to 5.5 V, and is optimized for a 5 volt supply.

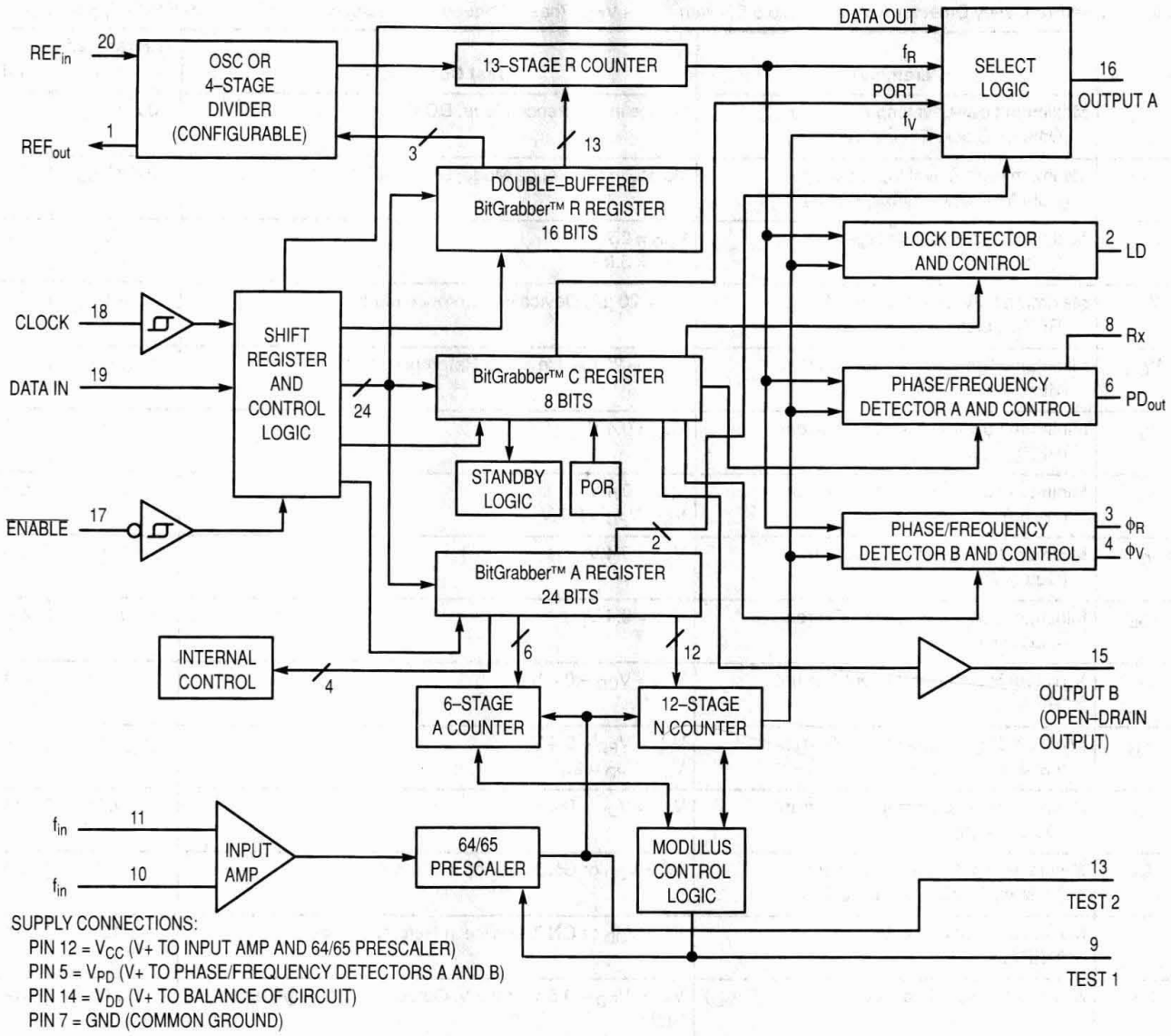
This part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 6 mA Nominal at 2.7 V
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 2.7 to 5.0 V
- Operating Supply Voltage Range of Phase Frequency Detector A (V_{PD} Pin) = 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detector B (V_{PD} Pin) = 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40° to 85°C
- R Counter Division Range: (1 and) 5 to 8191
- N Counter Division Range: 5 to 4095
- A Counter Division Range: 0 to 63
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 2 Megabits per Second
- Output A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — Output A: Totem–Pole (Push–Pull) with Four Output Modes
  Output B: Open–Drain
- Power–Saving Standby Feature with Patented Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- Evaluation Kit Available (Part Number MC145192EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage, except Output B, PD_{out}, ϕ_R, ϕ_V Output B, PD_{out}, ϕ_R, ϕ_V	 – 0.5 to V_{DD} + 0.5 – 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{DD} = V_{CC} = 2.7 to 5.0 V, Voltages Referenced to GND, T_A = – 40° to 85°C, unless otherwise stated; Phase/Frequency Detector A V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$; Phase/Frequency Detector B V_{PD} = 2.7 to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	Device in Reference Mode, DC Coupled	0.2 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	Device in Reference Mode, DC Coupled	0.8 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (Clock, $\overline{\text{Enable}}$)	V_{DD} = 2.7 V V_{DD} = 5.0 V	100 300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, Output A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, Output A)	I_{out} = – 20 µA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD)	V_{out} = 0.4 V	0.25	mA
I_{OL}	Minimum Low–Level Output Current (ϕ_R, ϕ_V)	V_{out} = 0.4 V V_{DD}, V_{PD} = 2.7 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (Output A)	V_{out} = 0.4 V	0.6	mA
I_{OL}	Minimum Low–Level Output Current (Output B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD)	V_{out} = V_{DD} – 0.4 V	– 0.25	mA
I_{OH}	Minimum High–Level Output Current (ϕ_R, ϕ_V)	V_{out} = V_{PD} – 0.4 V V_{DD}, V_{PD} = 2.7 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (Output A Only)	V_{out} = V_{DD} – 0.4 V	– 0.35	mA
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 V or 0.5 V, Output in High–Impedance State	± 200	nA
	(Output B)	Output in High–Impedance State	± 10	µA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; Output B Controlling V_{CC} per Figure 22	30	µA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is NOT Standby, I_{Rx} = 113 µA, V_{PD} = 5.5 V	600	µA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is NOT Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 V p–p; Output A = Inactive and No Connect; V_{DD} = V_{CC}, REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; Data In, $\overline{\text{Enable}}$, Clock = V_{DD} or GND, Phase Detector A Off	*	mA

* The nominal values are:
6 mA at V_{DD} = 2.7 V and V_{PD} = 2.7 V
9 mA at V_{DD} = 5.0 V and V_{PD} = 5.5 V
These are not guaranteed limits.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 2.7$ to 5.0 V, Voltages Referenced to GND, $V_{DD} = V_{CC} \leq V_{PD}$)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part	$V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–versus–Source Mismatch (Note 3)	$V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40° to 85°C.

AC INTERFACE CHARACTERISTICS

($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40°$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns, $V_{PD} = 2.7$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Figure 1) NOTE: Refer to Clock t_w below	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Output A (Selected as Data Out) (Figures 1 and 5)	200	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{\text{Enable}}$ to Output A (Selected as Port) (Figures 2 and 5)	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{\text{Enable}}$ to Output B (Figures 2 and 6)	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Output A and Output B; t_{THL} only, on Output B (Figures 1, 5, and 6)	200	ns
C_{in}	Maximum Input Capacitance — Data In, Clock, $\overline{\text{Enable}}$	10	pF

TIMING REQUIREMENTS ($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40°$ to 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	100	ns
t_w	Minimum Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	*	cycles
t_w	Minimum Pulse Width, Clock (Figure 1)	250	ns
t_r, t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

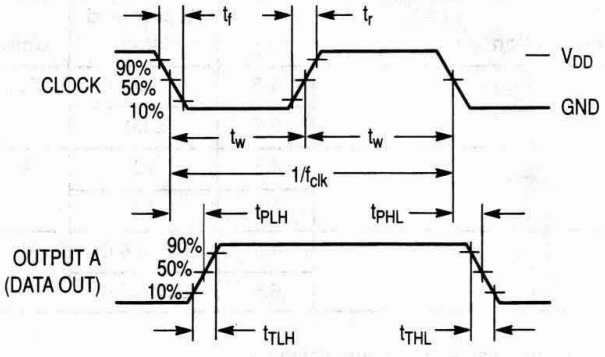


Figure 1.

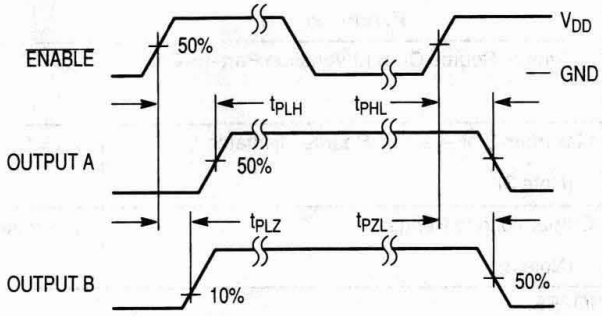


Figure 2.

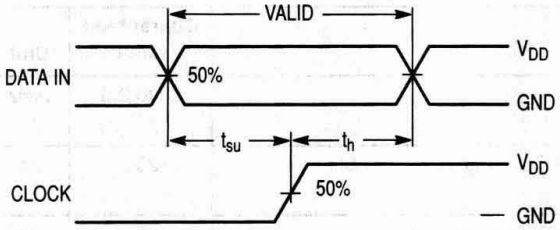


Figure 3.

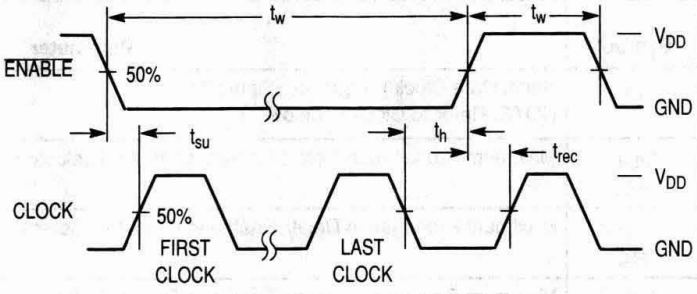
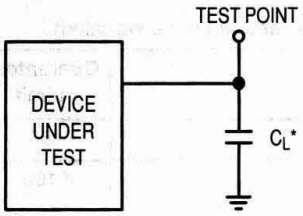
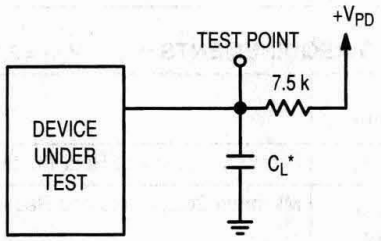


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 2.7 to 5.0 V unless otherwise indicated, T_A = – 40° to 85°C)

Symbol	Parameter	Test Condition	Guaranteed Operating Range		Unit
			Min	Max	
V_{in}	Input Voltage Range, f_{in} (Figure 7)	100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	400 200	1500 1500	mV p–p
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode (Figure 8)	V_{in} ≥ 400 mV p–p V_{DD} = 2.7 V V_{DD} = 3.0 V V_{DD} = 3.5 V V_{DD} = 4.5 to 5 V	 1 4.5 5.5 12	 20 20 20 27	MHz
		V_{in} ≥ 1 V p–p V_{DD} = 2.7 V V_{DD} = 3.0 V V_{DD} = 3.5 V V_{DD} = 4.5 to 5 V	 1 1.5 2 4.5	 20 20 20 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	2	10	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 30 pF	dc	5	MHz
f	Operating Frequency of the Phase Detectors		dc	1	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD (Figures 11 and 12)	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	20	140	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, and ϕ_R (Figures 11 and 12)	C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	—	80	ns
C_{in}	Input Capacitance, REF_{in}		—	5	pF

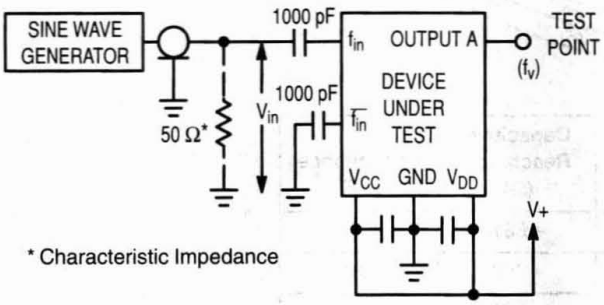


Figure 7. Test Circuit

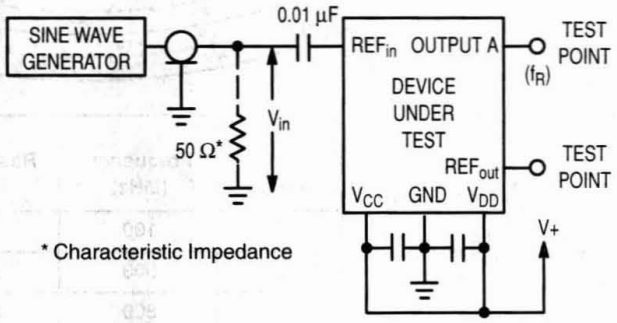


Figure 8. Test Circuit–Reference Mode

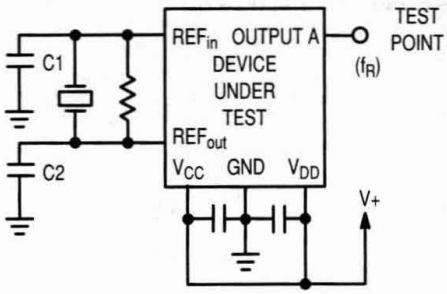


Figure 9. Test Circuit–Crystal Mode

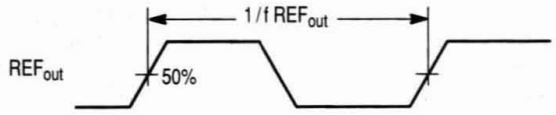


Figure 10. Switching Waveform

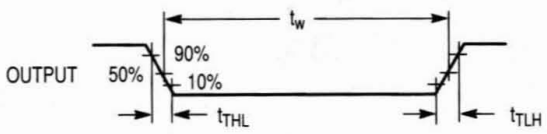


Figure 11. Switching Waveform

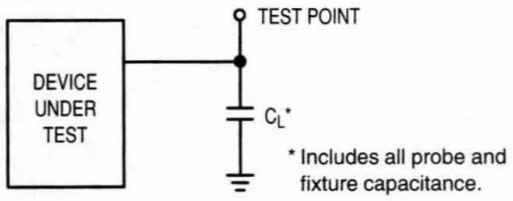
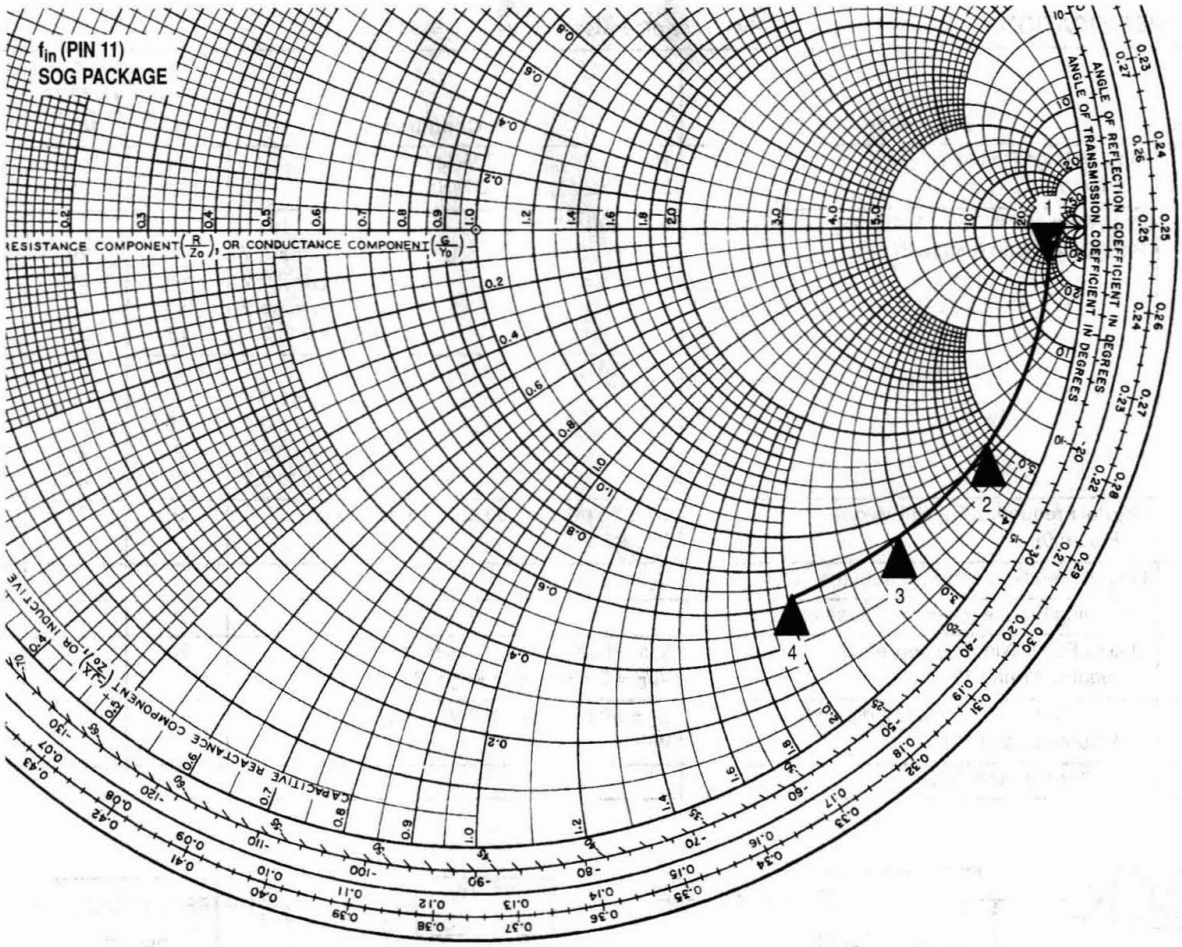


Figure 12. Test Circuit



Marker	Frequency (MHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	100	574	– 881	1.81
2	500	57.9	– 242	1.31
3	800	38.3	– 148	1.34
4	1100	31.6	– 103	1.40

Figure 13. Normalized Input Impedance at f_{in} — Series Format (R + jX) (100 MHz to 1100 MHz)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

Data In (Pin 19)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clock. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{\text{Enable}}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 LSBs of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{\text{Enable}}$ low with no signal on the Clock pin. This is an alternate method of transferring data to the second buffer of the R register. See Figure 17.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 2.7 to 5.0 V. The formats are shown in Figures 15, 16, and 17.

Data In typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first, C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 24 to 27	

Clock (Pin 18)

Serial Data Clock Input. Low–to–high transitions on Clock shift bits available at the Data pin, while high–to–low transitions shift bits from Output A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 25 through 27.

Clock typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow Clock rise and fall times are allowed. See the last paragraph of **Data In** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the Clock pin must be held at GND (with $\overline{\text{Enable}}$ being a don't care) or $\overline{\text{Enable}}$ must be held at the potential of the V+ pin (with Clock being a don't care) during power–up. As an alternative, the bit sequence of Figure 18 may be used.

$\overline{\text{Enable}}$ (Pin 17)

Active–Low Enable Input. This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{\text{Enable}}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which must start inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken back high. The low–to–high transition on $\overline{\text{Enable}}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high. This will put the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{\text{Enable}}$ is high and Clock is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **Data In** for more information.

For POR information, see the note for the **Clock pin**.

Output A (Pin 16)

Configurable Digital Output. Output A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, Output A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high. The f_R signal can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0 through R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of one. See Figure 17. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R should not exceed 1 MHz.

If A23 = high and A22 = low, Output A is configured as f_V. This signal is the buffered output of the 12–stage N counter.

The f_V signal appears as normally low and pulses high. The f_V signal can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V should not exceed 1 MHz.

If A23 = low and A22 = high, Output A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the Clock input. Upon power up, Output A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, Output A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

Output B (Pin 15)

Open–Drain Digital Output. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, Output B assumes the high–impedance state. Output B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. Note: the maximum voltage allowed on the V_{PD} pin is 5.5 V for the MC145192.

Upon power–up, power–on reset circuitry forces Output B to a low level.

REFERENCE PINS

REF_{in} and REF_{out} (Pins 20 and 1)

Configurable Pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 10 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode shown in Figure 17, and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 20 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. The ac–coupled signal must be at least 400 mV p–p. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for V_{DD} to V_{SS} swing. Therefore, for REF_{in} frequencies above 5 MHz, the one–to–one ratio may not be used for large signal swing requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$ (Pins 11 and 10)

Frequency Input from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they are usually used in a single–ended configuration as shown in Figure 7. Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out} (Pin 6)

Single–Ended Phase/Frequency Detector Output. This is a 3–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 15)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state

Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)

Double–Ended Phase/Frequency Detector Outputs. These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 15)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD (Pin 2)

Lock Detector Output. This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V. See Figure 19.

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false lock signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx (Pin 8)

External Resistor. A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Figure 15 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 22 kΩ when V_{PD} is 5 V.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

Test 1 (Pin 9)

Modulus Control Signal. This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin may be attached to an isolated pad with no trace.

Test 2 (Pin 13)

Prescaler Output. This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin may be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD} (Pin 14)

Positive Supply Potential. This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 2.7 to + 5.0 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC} (Pin 12)

Positive Supply Potential. This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is + 2.7 to + 5.0 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 23.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

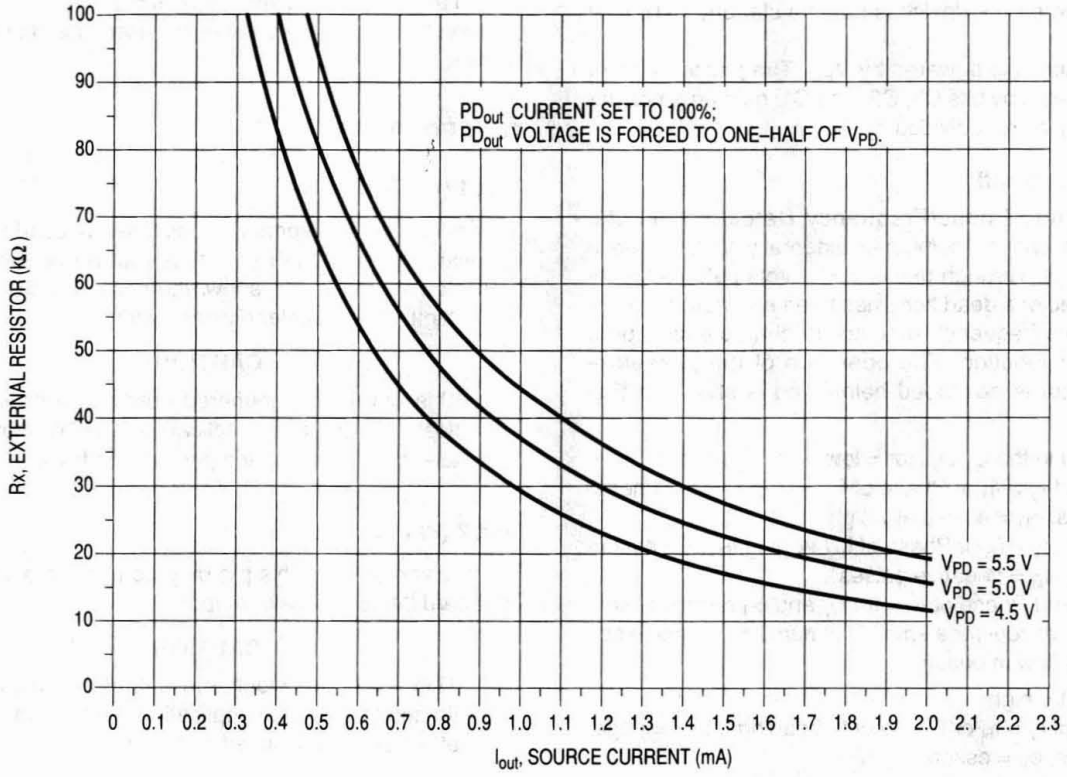
V_{PD} (Pin 5)

Positive Supply Potential. This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be ≥ V_{DD} but not more than 5.5 V. The voltage range for V_{PD} is 4.5 to 5.5 V with respect to the GND pin when using PD_{OUT} and 2.7 to 5.5 V when using ϕ_R, ϕ_V outputs.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND (Pin 7)

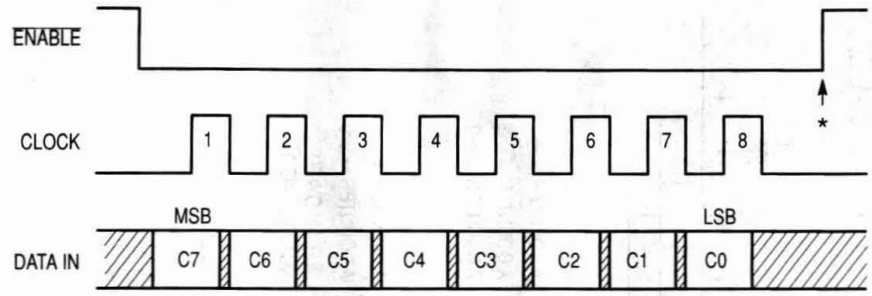
Common ground.



Nominal MC145192 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145192 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 19. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.
When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. This is a patented feature.

C3, C2 – I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx) is available. Also, see C1 bit description.

C1 – Port: When the Output A pin is selected as "Port" via bits A22 and A23, C1 determines the state of Output A. When C1 is set high, Output A is forced high; C1 low forces Output A low. When Output A is not selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when Output A is selected as "Port." The Port bit is not affected by the standby mode.

C0 – Out B: Determines the state of Output B. When C0 is set high, Output B is high–impedance; C0 low forces Output B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles Are Used)

Table 2. PD_{out} Current, C1 = Low with Output A NOT Selected as "Port"; Also, Default Mode When Output A Selected as "Port"

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with Output A NOT Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%

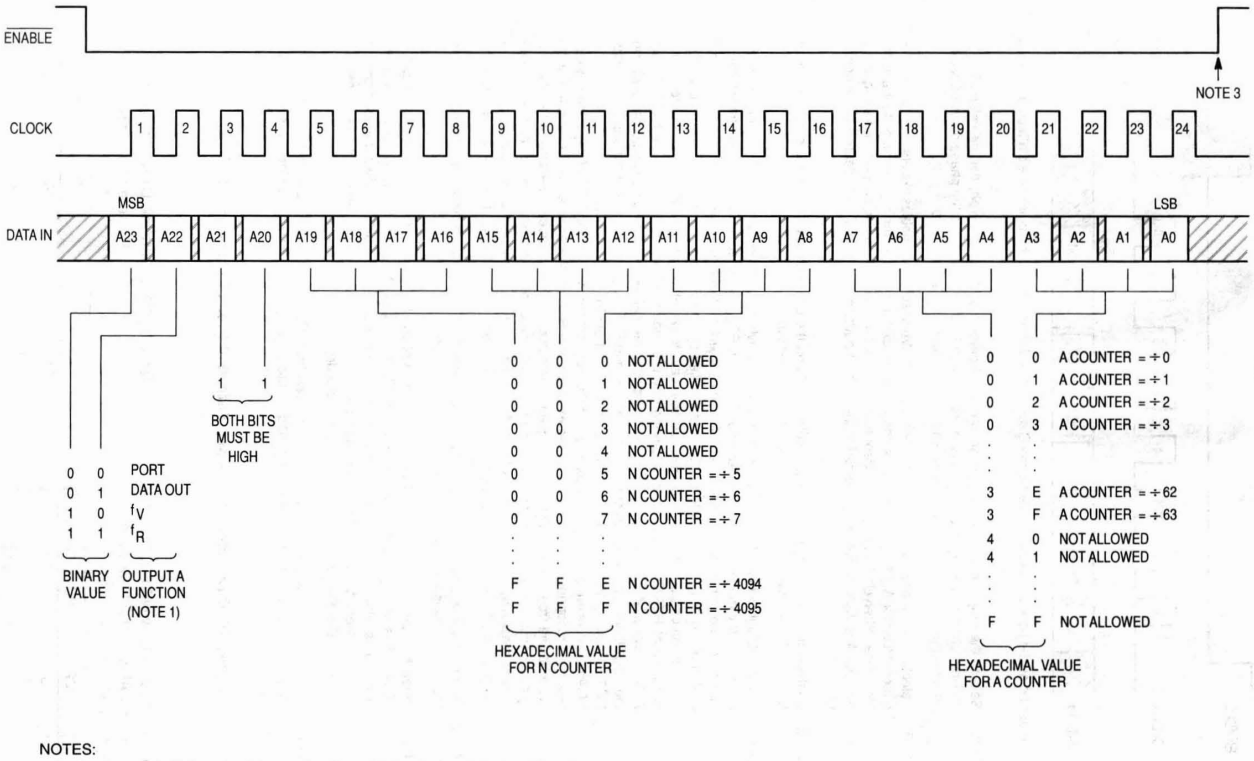
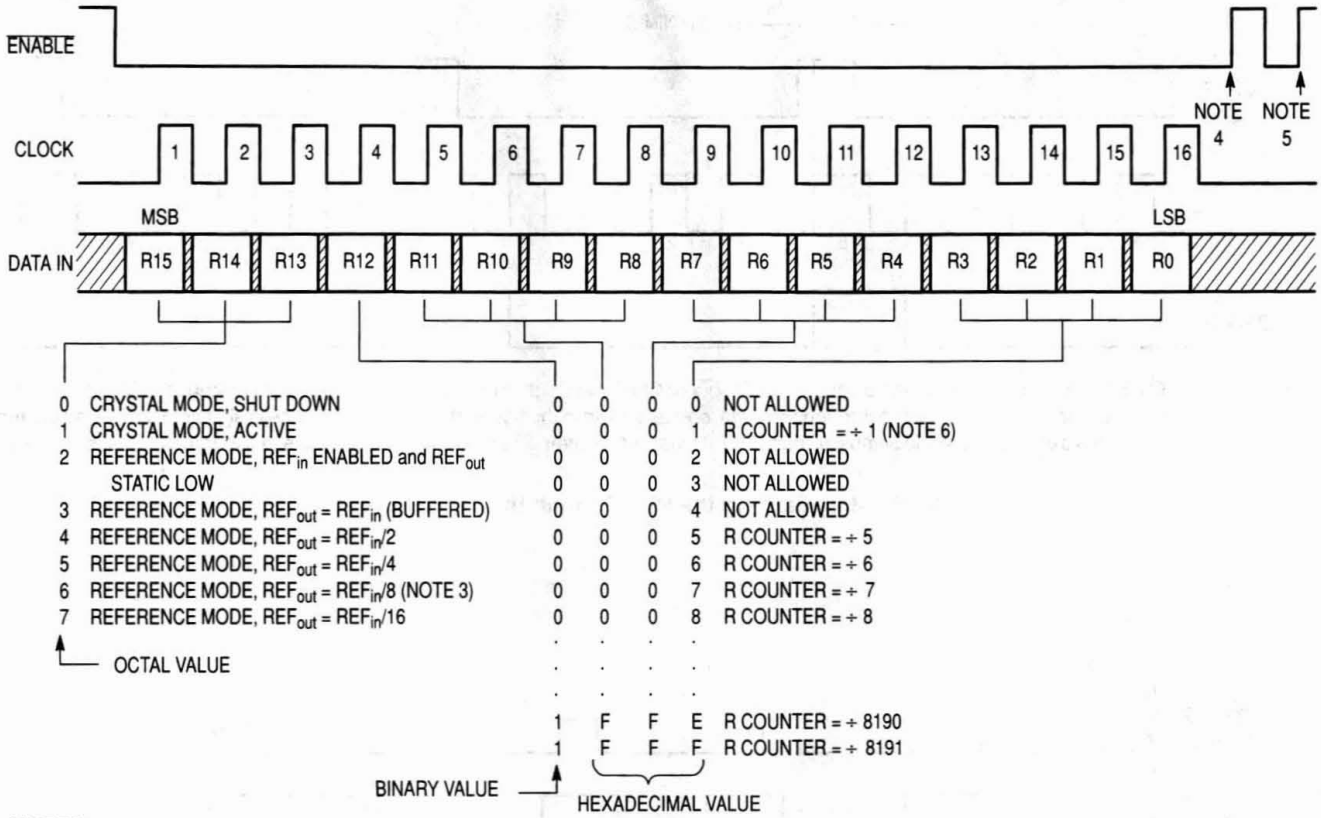

ENABLE
NOTE 3
CLOCK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
MSB
LSB
DATA IN
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 0 PORT DATA OUT
0 1 fV
1 0 fR
1 1
BINARY VALUE
OUTPUT A FUNCTION (NOTE 1)
1 1
BOTH BITS MUST BE HIGH
0 0 0 NOT ALLOWED
0 0 1 NOT ALLOWED
0 0 2 NOT ALLOWED
0 0 3 NOT ALLOWED
0 0 4 NOT ALLOWED
0 0 5 N COUNTER = ÷ 5
0 0 6 N COUNTER = ÷ 6
0 0 7 N COUNTER = ÷ 7
F F E N COUNTER = ÷ 4094
F F F N COUNTER = ÷ 4095
HEXADECIMAL VALUE FOR N COUNTER
0 0 A COUNTER = ÷ 0
0 1 A COUNTER = ÷ 1
0 2 A COUNTER = ÷ 2
0 3 A COUNTER = ÷ 3
3 E A COUNTER = ÷ 62
3 F A COUNTER = ÷ 63
4 0 NOT ALLOWED
4 1 NOT ALLOWED
F F NOT ALLOWED
HEXADECIMAL VALUE FOR A COUNTER

Figure 16. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

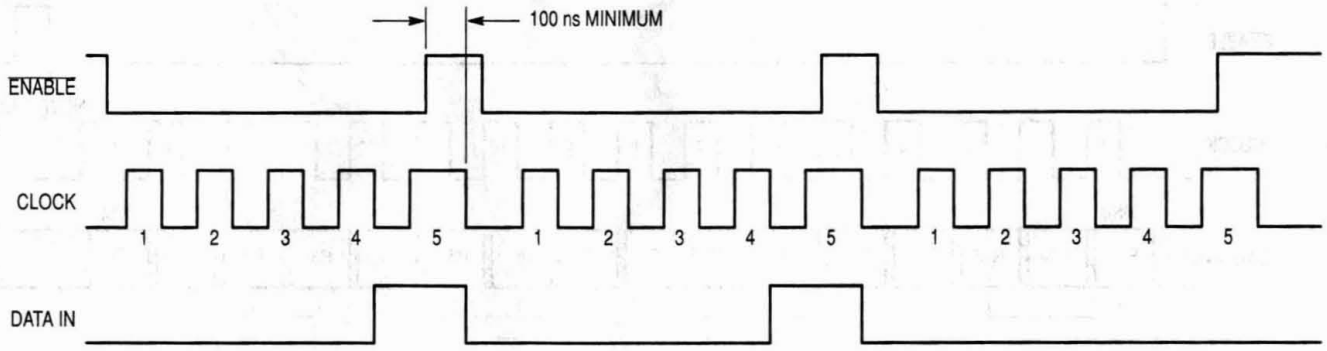
1. A power–on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.


ENABLE
NOTE 4
NOTE 5
CLOCK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
MSB
LSB
DATA IN
R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
0 CRYSTAL MODE, SHUT DOWN
1 CRYSTAL MODE, ACTIVE
2 REFERENCE MODE, REFin ENABLED and REFout STATIC LOW
3 REFERENCE MODE, REFout = REFin (BUFFERED)
4 REFERENCE MODE, REFout = REFin/2
5 REFERENCE MODE, REFout = REFin/4
6 REFERENCE MODE, REFout = REFin/8 (NOTE 3)
7 REFERENCE MODE, REFout = REFin/16
OCTAL VALUE
0 0 0 0 NOT ALLOWED
0 0 0 1 R COUNTER = ÷ 1 (NOTE 6)
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 0 4 NOT ALLOWED
0 0 0 5 R COUNTER = ÷ 5
0 0 0 6 R COUNTER = ÷ 6
0 0 0 7 R COUNTER = ÷ 7
0 0 0 8 R COUNTER = ÷ 8
1 F F E R COUNTER = ÷ 8190
1 F F F R COUNTER = ÷ 8191
BINARY VALUE
HEXADECIMAL VALUE

NOTES:

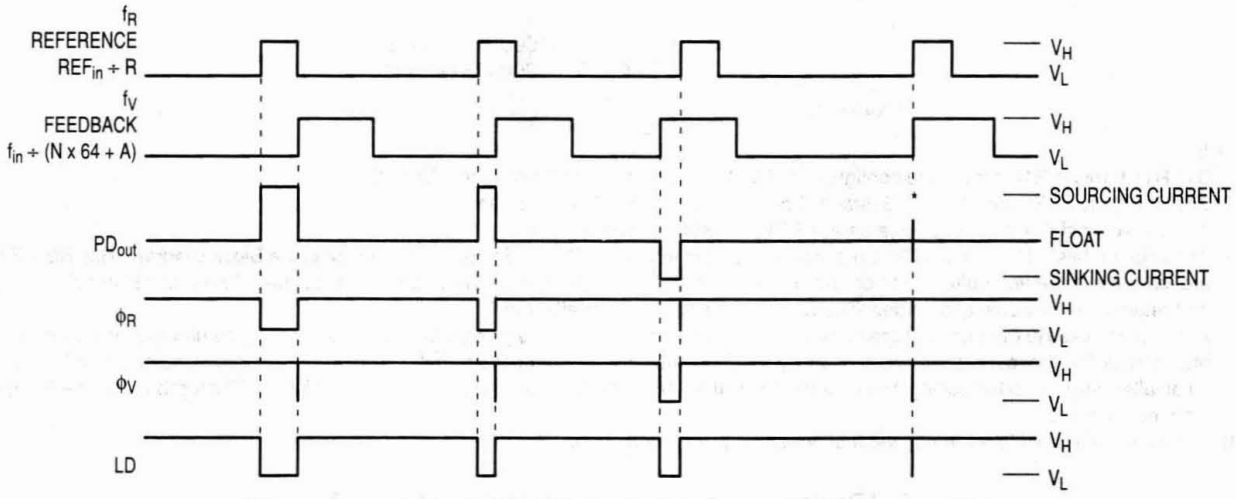
1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. Clock must be low during the $\overline{\text{Enable}}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



NOTE: It may not be convenient to control the $\overline{\text{Enable}}$ or Clock pins high during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the Clock must remain high at least 100 ns after $\overline{\text{Enable}}$ is brought high. Note that 3 groups of 5 bits are needed.

Figure 18. Initializing the PLL through the Serial Port



V_H = High voltage level
V_L = Low voltage level
* At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 15 for POL.

Figure 19. Phase/Frequency Detectors and Lock Detector Output Waveforms

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used. See Figure 8.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

DESIGN AN OFF–CHIP REFERENCE

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

USE OF THE ON–CHIP OSCILLATOR CIRCUITRY

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 20.

The crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 20 pF when used at the highest operating frequency of 10 MHz. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1+C2}$$

where

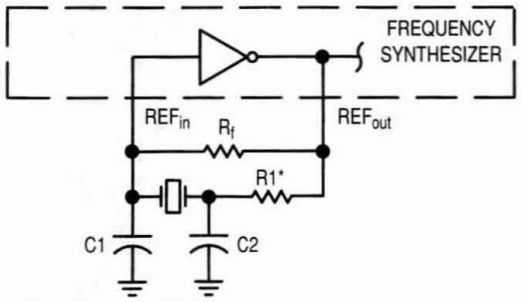
C_{in} = 5 pF (see Figure 21)
C_{out} = 6 pF (see Figure 21)
C_a = 1 pF (see Figure 21)
C1 and C2 = external capacitors (see Figure 20)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making either a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 22. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 20 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven; monitor the output frequency (f_R) at Output A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. Note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 4.



* May be needed in certain cases. See text.

Figure 20. Pierce Crystal Oscillator Circuit

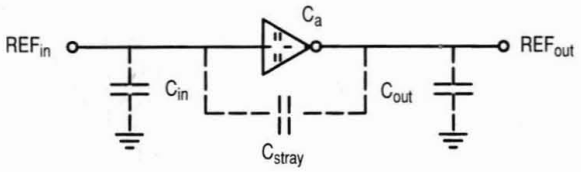
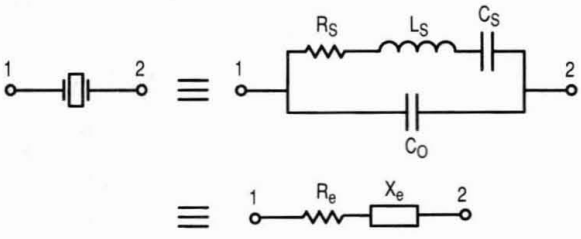


Figure 21. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 22. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

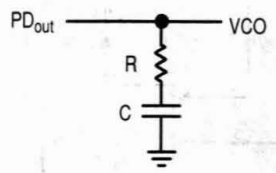
Table 4. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

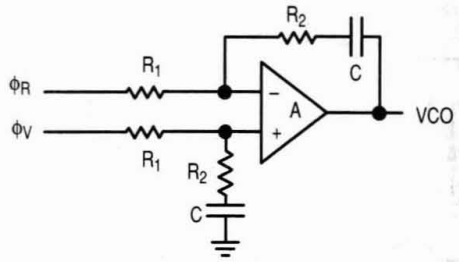
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

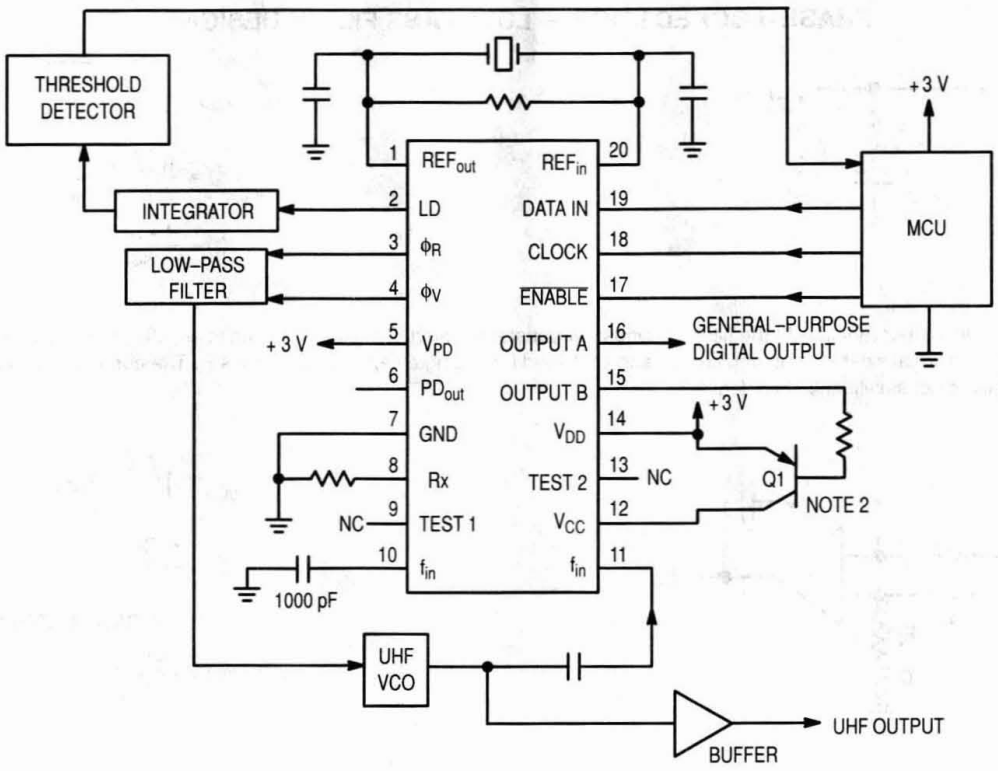
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

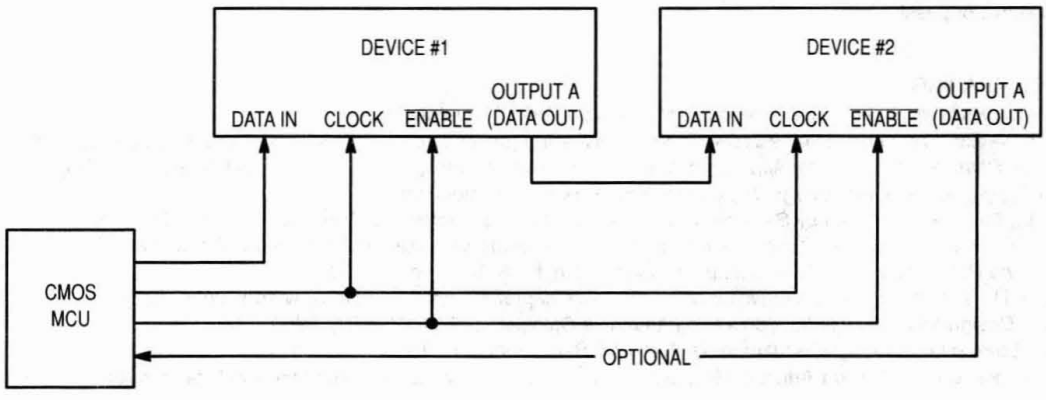
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

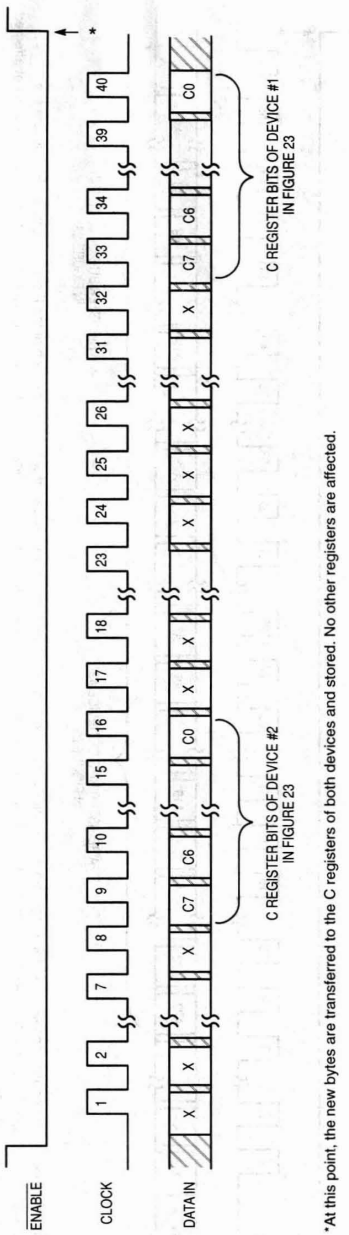
1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, Output B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in} / f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 23. Example Application



NOTE: See related Figures 25, 26, and 27.

Figure 24. Cascading Two Devices



*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

Figure 25. Accessing the C Registers of Two Cascaded Devices

Figure 26. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

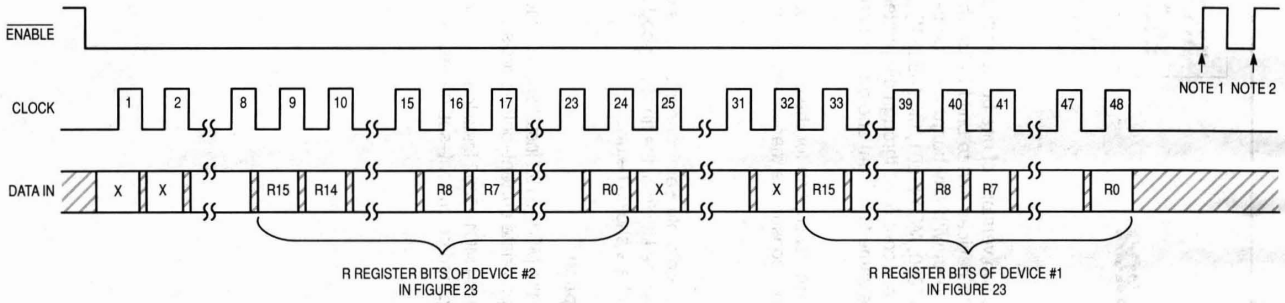


Figure 27. Accessing the R Registers of Two Cascaded Devices

NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. Clock must be low during the $\overline{\text{Enable}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

MC145192EVK
MC145202EVK

Technical Summary

MC145192 and MC145202 Evaluation Boards

INTRODUCTION

The MC145192EVK and MC145202EVK are two versions of one board with a few component changes. They allow users to exercise features of both devices and to build PLLs which meet individual performance requirements. The control program works with any board and can be used with other Motorola PLL devices (MC145190, MC145191, MC145200, MC145201, MC145220*). It will select frequency defaults that apply to each. All board functions are controlled through the printer port of an IBM PC. Up to three different EVKs may be controlled at the same time from one printer port. The functional block diagram is given in Figure 1.

This technical summary contains the hardware description for the evaluation board and a summary of the software section. For complete information, consult the manual that is provided in the evaluation kit.

ORDERING INFORMATION

These kits may be ordered through your local Motorola Semiconductor sales office or authorized distributor. Ask your Motorola representative to order the kits from the finished goods warehouse, not the literature distribution center. Request the part numbers shown below.

Part Number	Description
MC145192EVK	Kit with the MC145192 installed. Also includes a MC145202 device and appropriate current–setting resistor.
MC145202EVK	Kit with the MC145202 installed. Also includes a MC145192 device and appropriate current–setting resistor.

* The MC145220 is not available with Rev. 2.5 software.

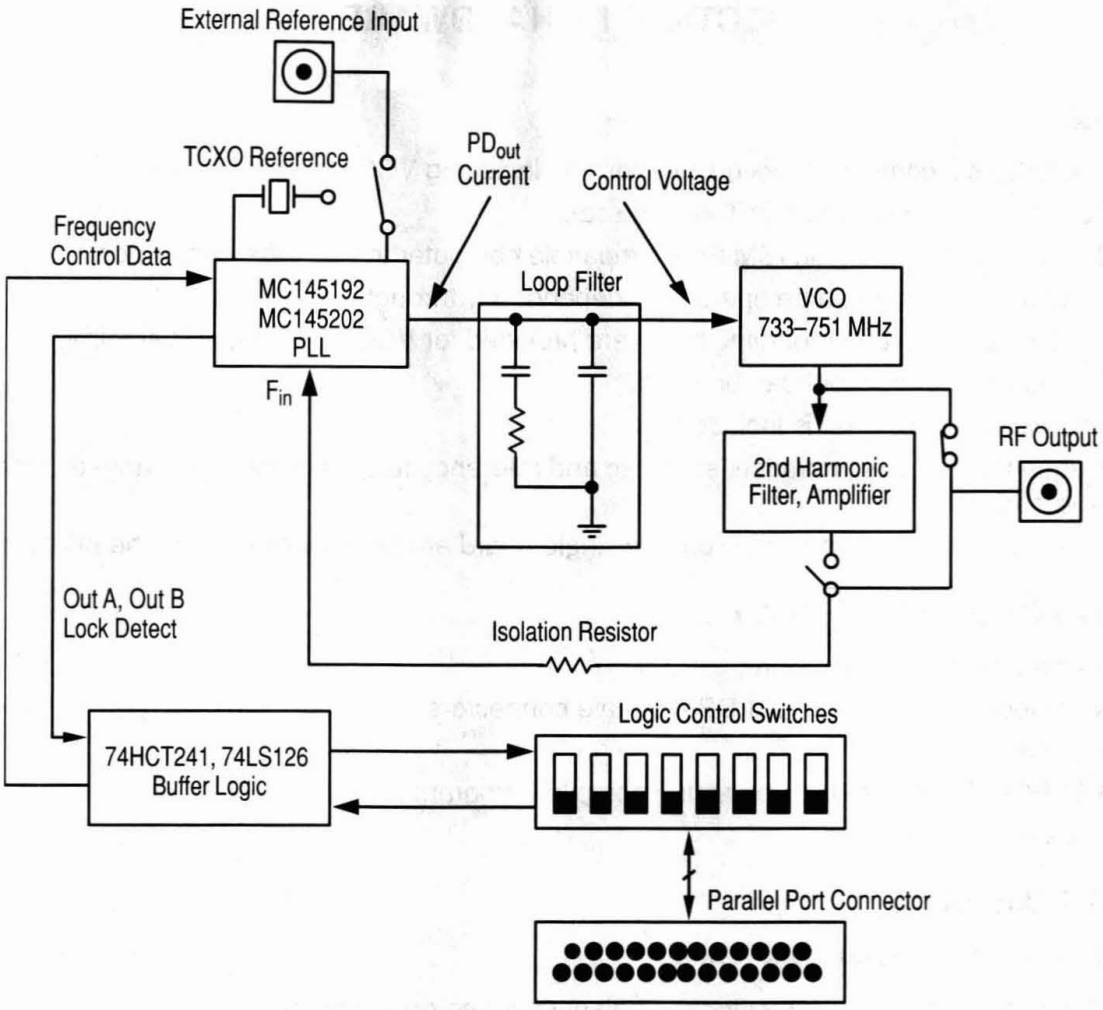


Figure 1. Evaluation Kit Block Diagram

SECTION 1 – HARDWARE

FEATURES

5. The EVK is a complete working synthesizer, including VCO.
6. Control program is written in Turbo Pascal.
7. Board is controlled by an IBM PC–compatible computer through the printer port.
8. Up to three boards can be operated independently through one printer port.
9. A prototype area and mounting holes are provided for VCOs, mixers, and amplifiers.
10. External reference input can be used.
11. Five element loop filter is included.
12. Frequency range of operation, step size and reference frequency can be changed in the control program.
13. Lock Detect, Out A, and Out B on any single board are accessible through the printer port.

CONTENTS OF EVALUATION KIT

1. Assembled evaluation board.
2. Nine–foot flat cable with four DB–25 male connectors.
3. MC145192/202 EVK manual.
4. 3.5″ PC–compatible disk containing compiled program.
5. PLL device data sheets.

GETTING STARTED

To perform basic functions, do the following:

1. Plug in 12 volts at J6, observing the polarity marked on the board.
2. Short circuit section 1 of the DIP switch (S1) and open circuit all other sections.
3. Connect the supplied flat cable between the computer printer port and the DB–25 connector on the board (J5).
4. Type PLL at the DOS prompt. Then press enter.
5. Type the number that corresponds with the type of board given in the on–screen menu. Then press Q.

You should now see the main menu displayed. There should be a signal present at J8 on the current output frequency given in the main menu. If the signal is not on the correct frequency, check to see if your printer card address is $278 (hexadecimal 278). If not, then select the P menu item and enter the correct address. After returning to the main menu, select the I menu item to send data to the board. You should now be on frequency.

MODIFICATIONS

The user may modify the hardware, such as utilizing a different VCO, by using the prototyping area of the board. After such modifications are made, the default values in the software may need to be changed. This is facilitated from screen #2 'Select from the available options' screen.

Note that the on–board voltage regulators allow for maximum control voltage range of 0.5 to 4.5 V.

TYPICAL PERFORMANCE

Common to both kits, unless noted. Typical performance applies only to the configuration as shipped. The MC145192EVK is shipped with V_{CC} = 3 V and V_{PD} = 5 V. The MC145202EVK is shipped with V_{CC} = 5 V and V_{PD} = 5 V.

Supply Voltage (J6)	11.5 – 12.5 V
Supply Current (J6) (Note 1)	120 mA
Available Current (Note 2)	60 mA
Frequency Range ('192) (Note 3)	733 – 743 MHz
Frequency Range ('202) (Note 3)	1466 – 1486 MHz
Reference Frequency	14.4 MHz
Temperature Stability (– 30°C to + 85°C)	< ± 2 ppm
TCXO Aging	< ± 1 ppm / year
Step Size ('192)	100 kHz
Step Size ('202)	200 kHz
Power Output	4.5 – 7.5 dBm
2nd Harmonic Level ('192)	< – 18 dB
Fundamental Level ('202)	< – 23 dB
3rd Harmonic Level	< – 18 dB
Frequency Accuracy ('192)	± 1.5 kHz
Frequency Accuracy ('202)	± 3.0 kHz
Reference Sidebands	– 70 dB
Phase Noise (100 Hz, '192)	– 70 dBc/Hz
Phase Noise (100 Hz, '202)	– 69 dBc/Hz
Phase Noise (10 kHz, '192) (Note 4)	– 86 dBc/Hz
Phase Noise (10 kHz, '202) (Note 4)	– 90 dBc/Hz
Switching Time (Note 5)	2.6 ms

NOTES:

1. Supply current is current the board requires without user modifications.
2. Available current is the sum of currents available to the user (in the prototype area) from the 5 V and 8.5 V supply. The 12 V supply is not regulated. Current at 12 V is limited by the external power supply. If the on–board VCO and amplifier are disconnected from the power bus, more current can be drawn in the prototype area. The current flowing into U3 (the 8.5 V regulator) should not exceed 180 mA. This will limit temperature rise in U3.
3. Frequency ranges require use of the 5 V default charge pump supply voltage.
4. 10 kHz phase noise is limited by the PLL device noise. For low noise designs, the loop bandwidth is made more narrow and the VCO is relied upon to provide the 10 kHz phase noise. This can be seen on the EVKs since the VCO has much lower noise.
5. 10 MHz step, within ± 1 kHz of final frequency ('192).
   20 MHz step, within ± 2 kHz of final frequency ('202).

SUPPORT MATERIAL

To provide further information, the following documents are included:

1. Schematic diagram of '192/202EVK.
2. Separate Bill of Materials for each board.
3. Parts layout diagram.
4. Mechanical drawing of board.
5. MC145192 and MC145202 data sheets.
6. Printer port diagram.
7. Typical signal plots for each type of EVK.

PRODUCTION TEST

After assembly is complete, the following alignment and test is performed on '192EVK (or '202EVK):

1. The control program is started in single board '190EVK ('200EVK) mode.
2. L menu item is selected.
3. Power is applied to the board. DIP switch section 1 is closed circuit with all others being open circuit.
4. After attaching computer cable, menu item I is selected.
5. Trim resistor VR1 is adjusted to obtain an output frequency at J8 of 740.999 – 741.001 MHz (1481.998 – 1482.002 MHz).
6. Voltage at the control voltage test point is measured. It must be 2.5 – 3.1 V.
7. When testing more than 1 board, steps 3 – 6 are repeated.

If in step 5 it isn't possible to obtain a signal on frequency, menu item P should be selected and the correct printer port address entered. Menu item I would then be selected to reload the data.

BOARD OPERATION

A computer is connected to the DB–25 connector J5. Data is output from the printer port. The printer card is in slot 0 using the default address in the control program. Data is sent to the PLL device (U1) through the DIP switch (S1), and 74HCT241 buffer (U5). D2, D3, D4, R19, R20, and R21 are in the data path between the 74HCT241 and PLL devices. This limits the high level output voltage of the buffer. Voltage on the PLL device inputs must not be greater than 0.5 V above V_{CC}. A '192/202 PLL has three output lines which are routed through a 74LS126 line driver (U2) to the computer.

U5, the 74HCT241, provides isolation, logic translation and a turn–on delay for PLL input lines. Logic translation is needed from the TTL levels on the printer port to the CMOS levels on the '192/202 inputs. Turn–on delay is used to ensure the power–on reset functions properly. The enable line to the PLL must be held low during power–up.

A 12 V power supply should be used to power the board at J6 (Augat 2SV–02 connector). The 2SV–02 will accept 18–24 AWG bare copper power leads. No tools are needed for connection. If power is properly connected, LED D2 will be lit.

Power passes from J6 to U3 (LM317 regulator) configured as an 8.5 V regulator. Both boards use 8.5 V to power the VCO and RF amplifier. Regulators U4 and U7 use the 8.5 V supply to produce 3 V and 5 V. The '192 always uses 3 V to power logic and 5 V to power the charge pump, while the '202 can have either power both the logic and charge pump. J3 and J4 are jumpers which select voltages for the logic and charge pump supplies. U4 and U7 are cascaded with U3 to equalize their individual voltage drops.

The PLL loop is composed of the PLL device (U1), 733 – 743 MHz VCO (M1), passive loop filter (R11, R12, C4, C5, C6) and second harmonic filter amplifier (U6). A passive loop filter was used to keep the

design simple, reduce noise, and reduce the quantity of traces susceptible to stray pickup. About 56 dB rejection of fundamental and 23 dB gain is provided by the harmonic filter amplifier. This allows the '202 to lock at 1466 – 1486 MHz.

A single VCO model is used for both boards. It is an internal Motorola part which is not sold for other applications. The '192 operates at half the output frequency and step size of the '202. This allows the same loop filter components to be used. RF is fed to the PLL chip F_{in} input through voltage dividers R14 and R10. These two resistors terminate the PLL chip RF input with 50 ohms and provide isolation.

Both boards use a phase detector current of 2 mA. J1 and J2 are removable jumpers and cut traces. They are used as connection points for a current measurement of V_{PD} or V_{CC}. A potentiometer VR1 is used to set M2 (14.4 MHz TCXO) on frequency.

COMPONENTS UNIQUE TO EACH EVK

Components that are not the same on all EVKs are given in the following table:

	'192EVK	**'202EVK**
U1	MC145192	MC145202
R2	18 kΩ	3.9 kΩ
R8	0 Ω	Not Used
C22	Not Used	1.0 pF
J3	3 V	5 V

EXTERNAL REFERENCE INPUT

As shipped, all boards are configured for a 14.4 MHz TCXO (supplied). To use an external reference, disconnect J13 and connect J9. Use a reference signal at J10 which complies with data sheet requirements. Then modify the reference frequency in the program main menu to reflect the changes made ([F] menu item).

DATA TRANSFER FROM COMPUTER TO EVK

To control the serial input EVK with the parallel printer port, a conversion is done. Printer cards are designed to output eight bits through eight lines. A bit mask is used to obtain the bit combination for the three required output lines (Data, Clock, Load). As bytes are sent to the printer card in sequence, it appears to be a serial transfer. The printer port is used because data transfer using the serial port is much slower. A standard IBM PC can support a parallel port data rate of 4.77 MHz.

IBM PCs and compatibles can accept up to three printer port cards. These ports are called LPT1, LPT2, and LPT3. Each printer card has jumpers or DIP switches on it to set a unique address. Two sets of addresses are in common use. One set applies to IBM PC XT, AT, and clones. The other is for the PS 2 line. To load data into the EVK, the correct address must be selected. The program default is $278, which is LPT1 in a clone. If $278 is not the address in use, it must be modified by entering the O menu item in the main menu. All allowed addresses given in hexadecimal are as follows:

Label	**IBM PC and Clones**	**PS 2**
LPT1	278	3BC
LPT2	378	378
LPT3	3BC	278

Up to three EVK boards can operate independently from one printer port. All lines on the printer port are connected to every EVK. Even with three boards operating, only three output lines (Clock, Data and Load) from the printer card are used. If two boards are controlled together, data for the second board is received from the Output A of the first. Output A is a configurable output on '192/202 devices, which in this case is used to shift data through chip 1 into chip 2. Output A and Data are connected using a printer port input line. This was done to avoid connecting extra wires. Fortunately not all port input lines are needed for computer input. Load and Clock are common to both boards.

A three–board cascade is handled similarly to a two–board cascade. Out A on the first board is fed to Data on the second. Out A on the second connects to Data on the third. Instructing the program on the quantity of boards connected together allows it to modify the number of bits sent.

All boards have a DIP switch S1 which gives each a unique address. The configuration menu is used to tell the program what type of board is connected at a board address. Switch positions for all possible addresses are given in Figure 2.

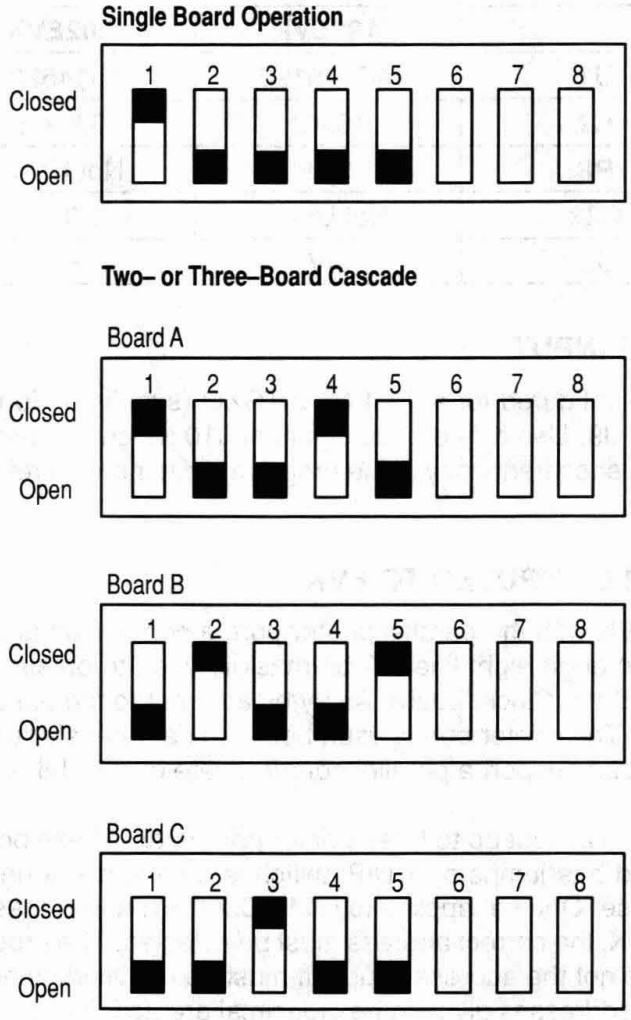


Figure 2. Switch Positions

In Figure 2, DIP switch sections 6, 7, and 8 allow the computer to read Out A, Out B or Lock Detect from the PLL device. Each of the inputs can only be read on one board at a time, but each item could be read on a different board. In a three–board cascade, Out A could be read from the first board, Out B from the second, and Lock Detect from the third. There is no way to determine in software the board address of a particular input. The control program does not make use of these inputs. Pin assignment on the printer port connector is:

Label	Pin Number
Out A	12
Out B	13
Lock Detect	15

PRINTER PORT CONFIGURATION

Printer port outputs on an IBM PC or clone use TTL–LS logic levels. Inputs are one TTL–LS load. Signal lines can be used for any purpose. The standard names, direction of data flow, true and inverted data are shown in Figure 3.

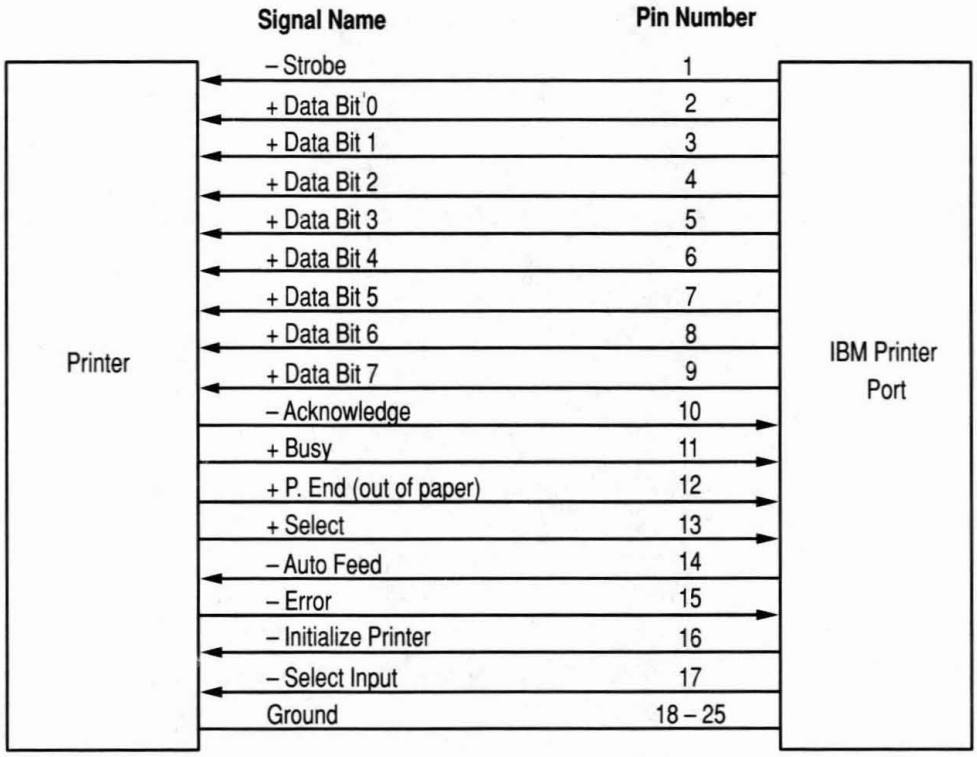


Figure 3. Printer Port Data Lines

Pin numbers for the port connector are shown in Figure 4.

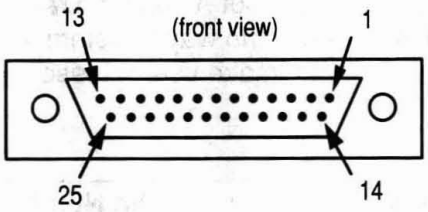


Figure 4. DB–25 Male Connector

SECTION 2 – SOFTWARE SUMMARY

INTRODUCTION

The MC145xxx EVK control program is used to program all PLL evaluation kits. It will simultaneoulsy control up to three different boards independently from one printer port. All features of the PLL device may be accessed. Default frequencies can be modified to allow use of different channel spacings and VCOs.

User input errors are detected and appropriate messages are displayed.

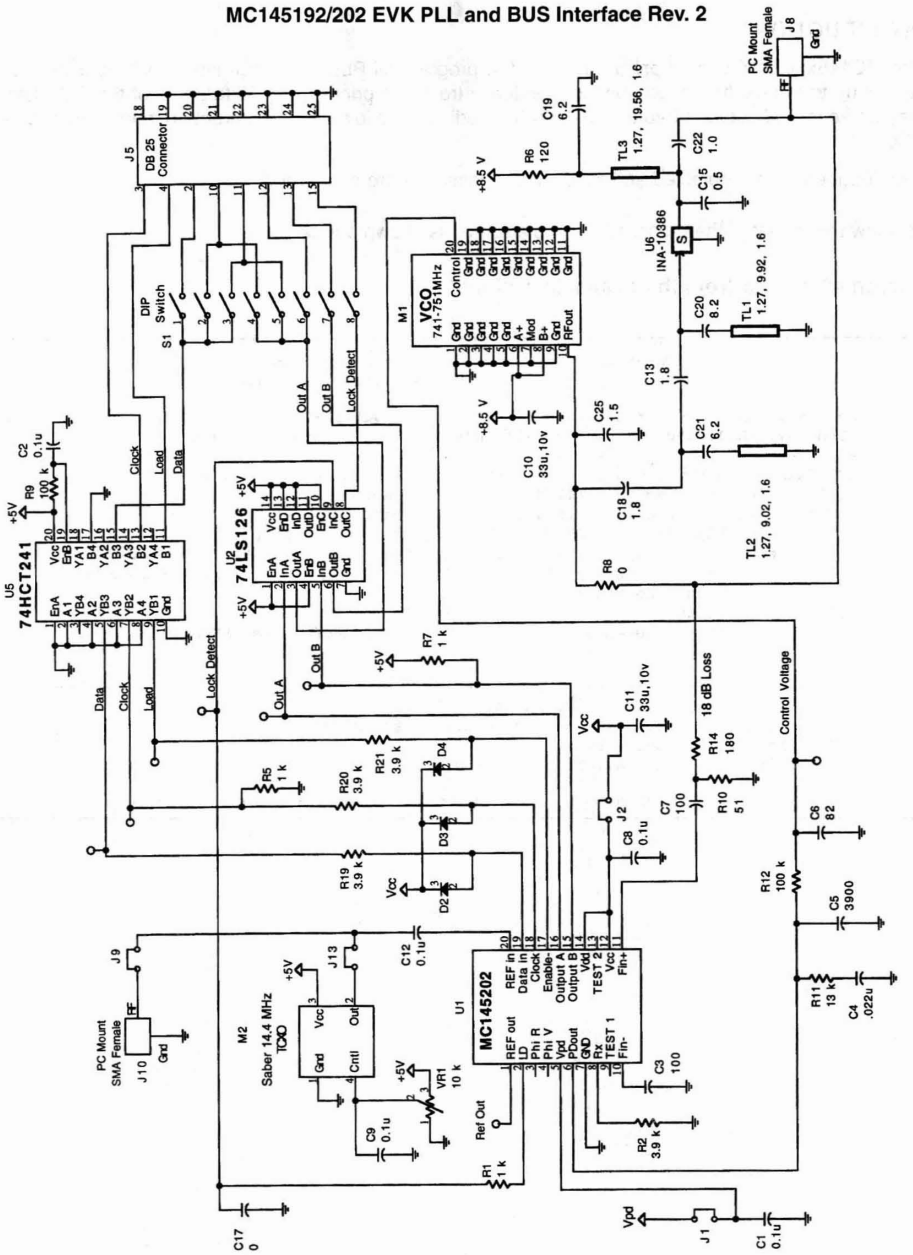
To show the format of the program, a sample screen is shown below:

Screen #2 'Select from the available options'

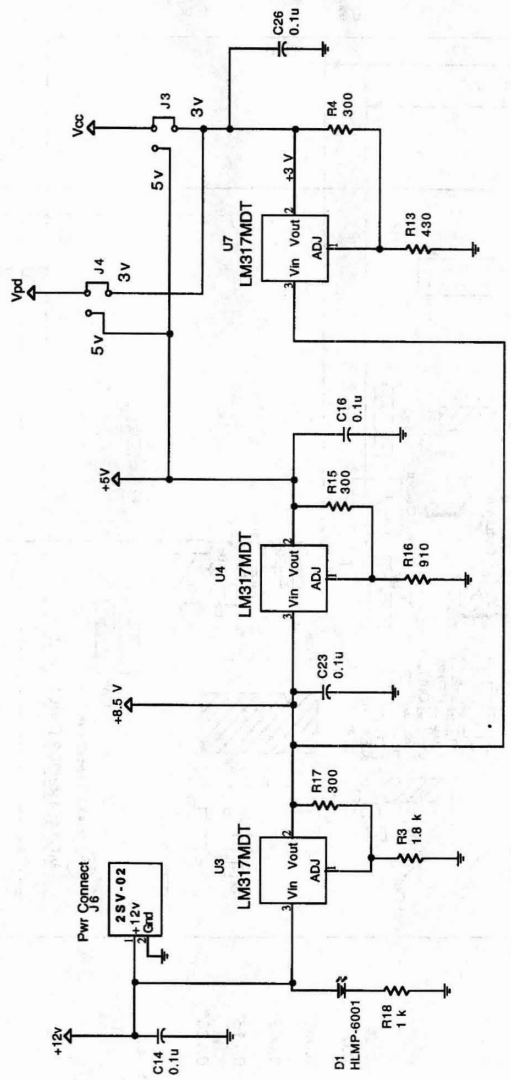
```
                Welcome to MC145xxx EVK Demonstration Program, rev 2.5
                          Select from the available options

Available Boards - Current target board is: A, MC145190
 Brd [A]!: MC145190        Brd [-]!: N/A            Brd [-]!: N/A
-------------------------------------------------------------------------------
MC145xxx Frequency Commands - Current Output Frequency is 746 MHz
 [L]! Set to low freq      741 MHz      [W] Change default low freq.
 [M]! Set to med. freq     746 MHz      [Y] Change default med. freq.
 [H]! Set to high freq.    751 MHz      [Z] Change default high freq.
 [U]! Step frequency up by step size    [O] Set PLL output frequency
 [D]! Step frequency down by step size  [F] Set REFin freq. & channel spacing
MC145xxx Additional Commands
 [E]  Set function of output A          [N] Change C Register
 [R]  Set crystal/reference mode - Current mode is Ref. mode, REFout low


-------------------------------------------------------------------------------
Initialization/System Setup Commands:
 [P]  Set output port address - Current address is $278
 [G]  Change board definitions
 [I]  Initialize board(s), Write all registers

             [X]! Terminate demonstration program. [?]! View help screen.
```

APPENDIX

MC145192/202 EVK PLL and BUS Interface Rev. 2



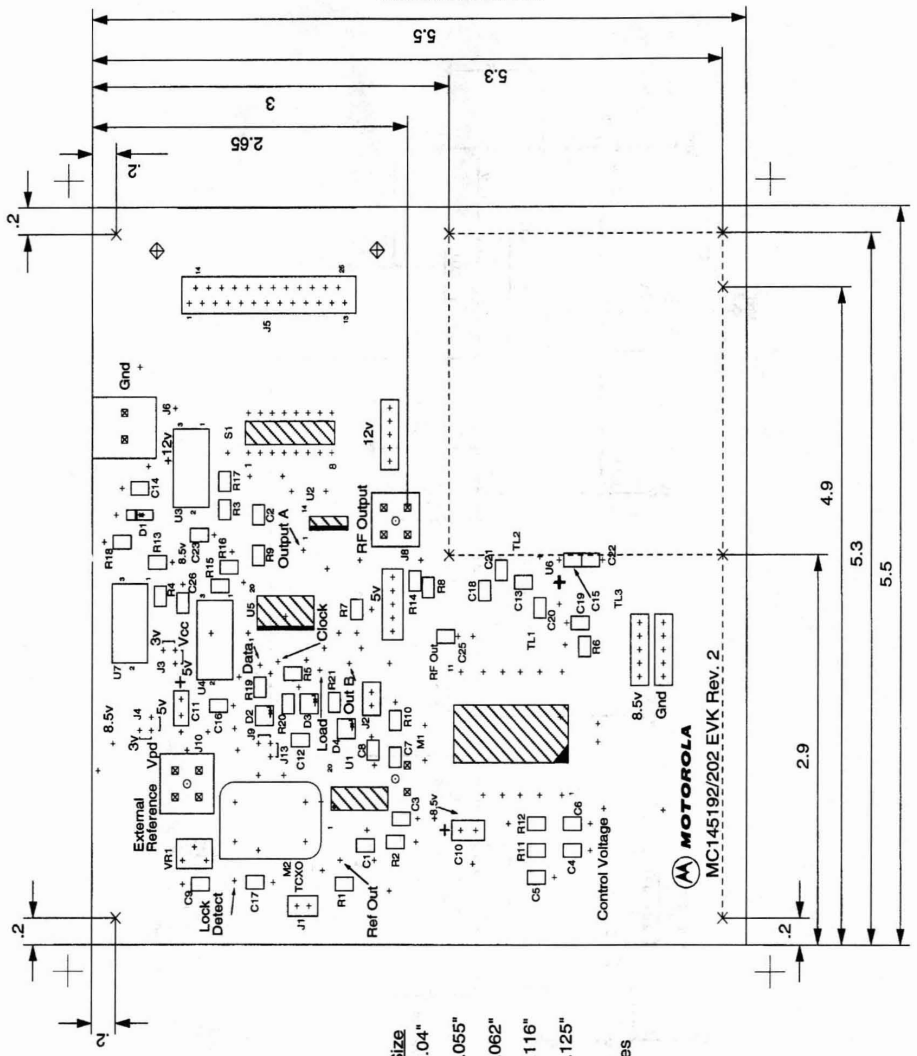
MC145192/202 EVK Power Supply Rev. 2



NOTES:
1. Default unit for capacitance is pF.
2. Default unit for resistance is ohms.
3. Board material is 1/16" thick G10.
4. Test points are 0.04" diameter plated through holes.
5. U1, R2, R8, C22, J3, and J4 are different on each type of EVK.
   See the manual section titled "Components Unique to Each EVK".

Drill Layer with Silkscreen (Top View)

Dimensions are in Inches

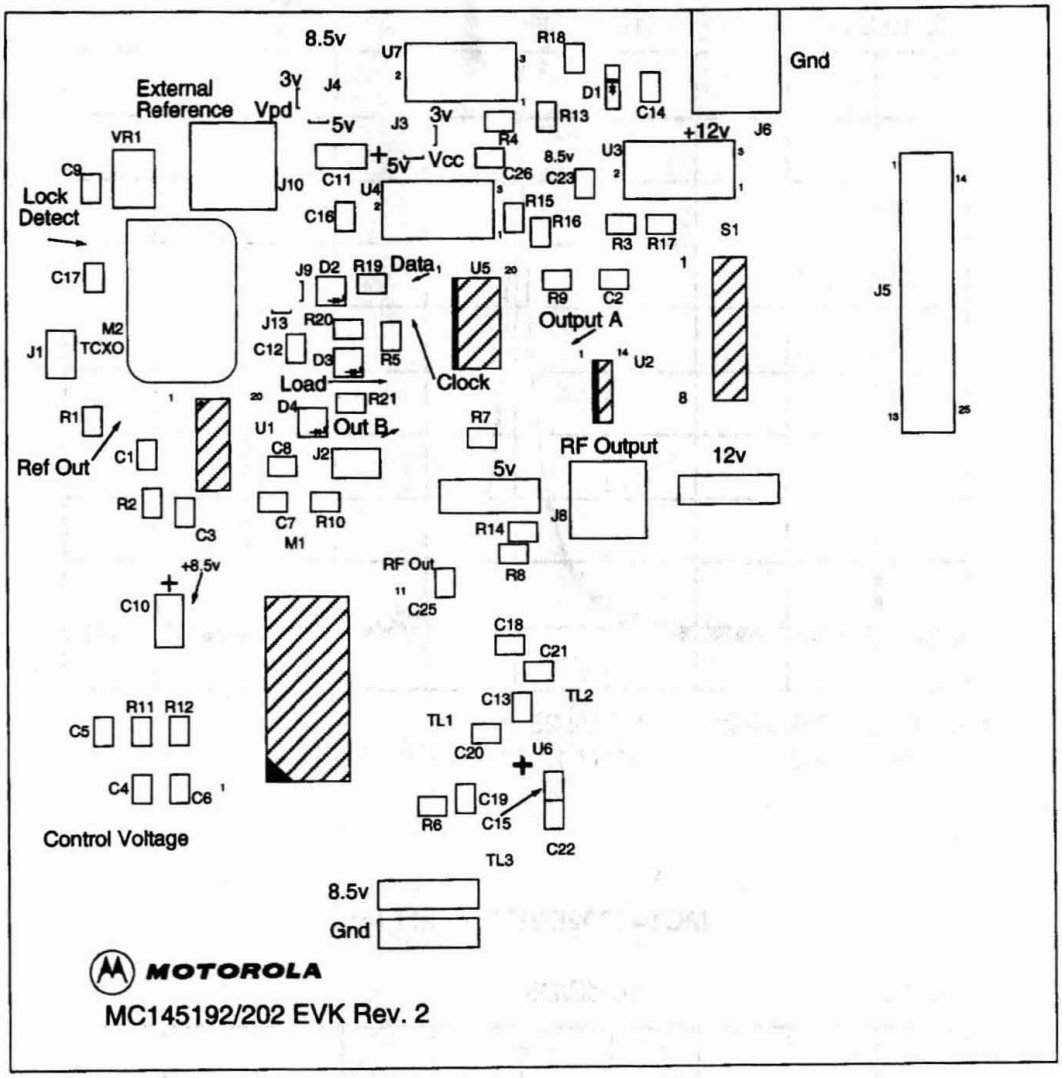


Drill Table:

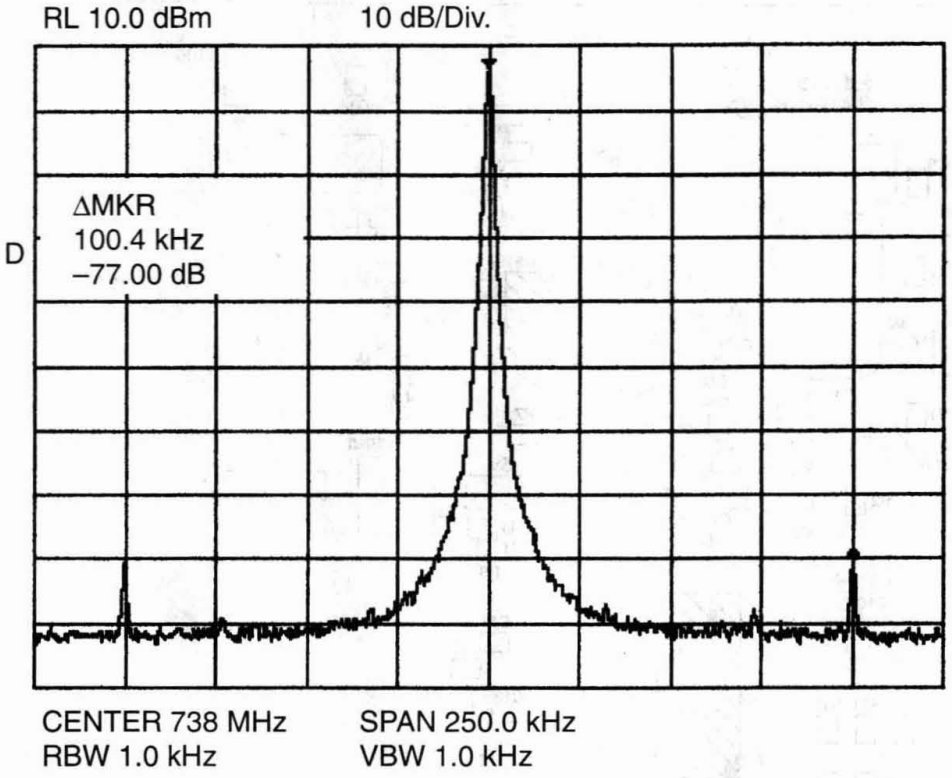
Symbol	Size
+	0.04"
⊠	0.055"
⊙	0.062"
×	0.116"
⌖	0.125"

Dimensions are in inches

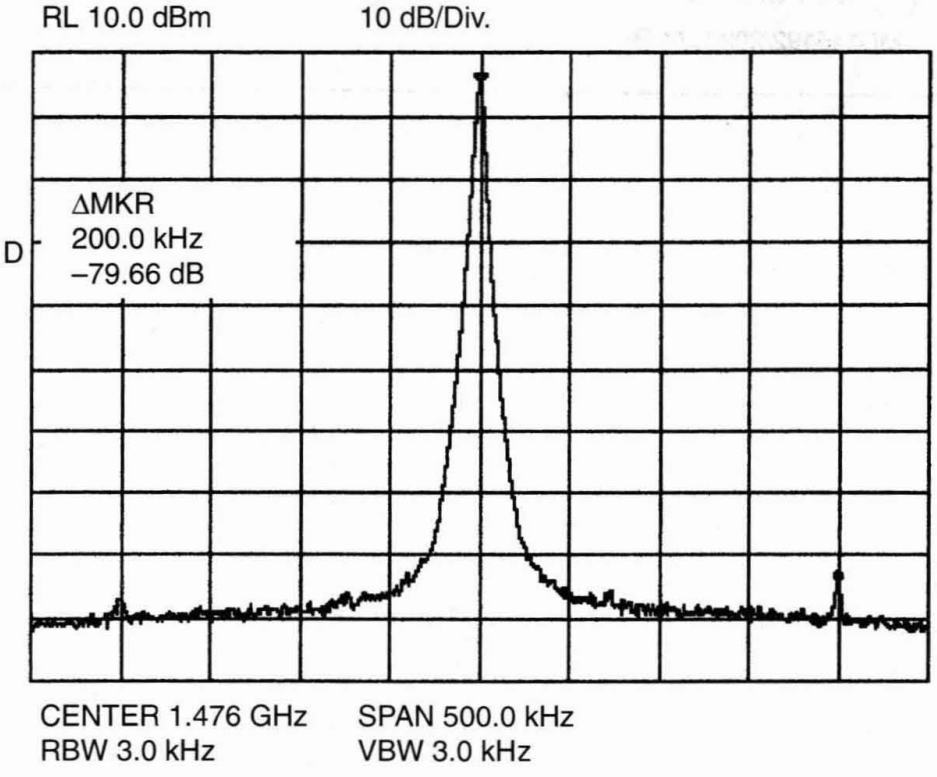
Silkscreen Layer (Top View)



MC145192EVK Signal Plot



MC145202EVK Signal Plot



MC145200
MC145201

2.0 GHz PLL Frequency Synthesizers
Include On–Board 64/65 Prescalers

The MC145200 and MC145201 are single–package synthesizers with serial interfaces capable of direct usage up to 2.0 GHz. A special architecture makes these PLLs very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

Each device features a single–ended current source/sink phase detector output and a double–ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

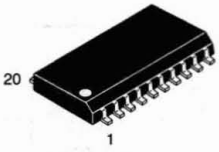
The MC145200 features logic–level converters and high–voltage phase/frequency detectors; the detector supply may range up to 9.5 V. The MC145201 has lower–voltage phase/frequency detectors optimized for single–supply systems of 5 V ±10%.

Each part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the parts to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

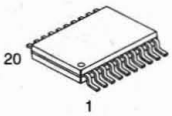
In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 12 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin) —
  MC145200: 8.0 to 9.5 V
  MC145201: 4.5 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to +85°C
- R Counter Division Range: (1 and) 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull)
  OUTPUT B: Open–Drain
- Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 µA
- Evaluation Kit Available (Part Numbers MC145200EVK and MC145201EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping



F SUFFIX
SOG PACKAGE
CASE 751J

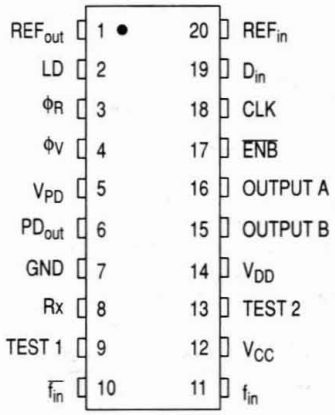


DT SUFFIX
TSSOP
CASE 948D

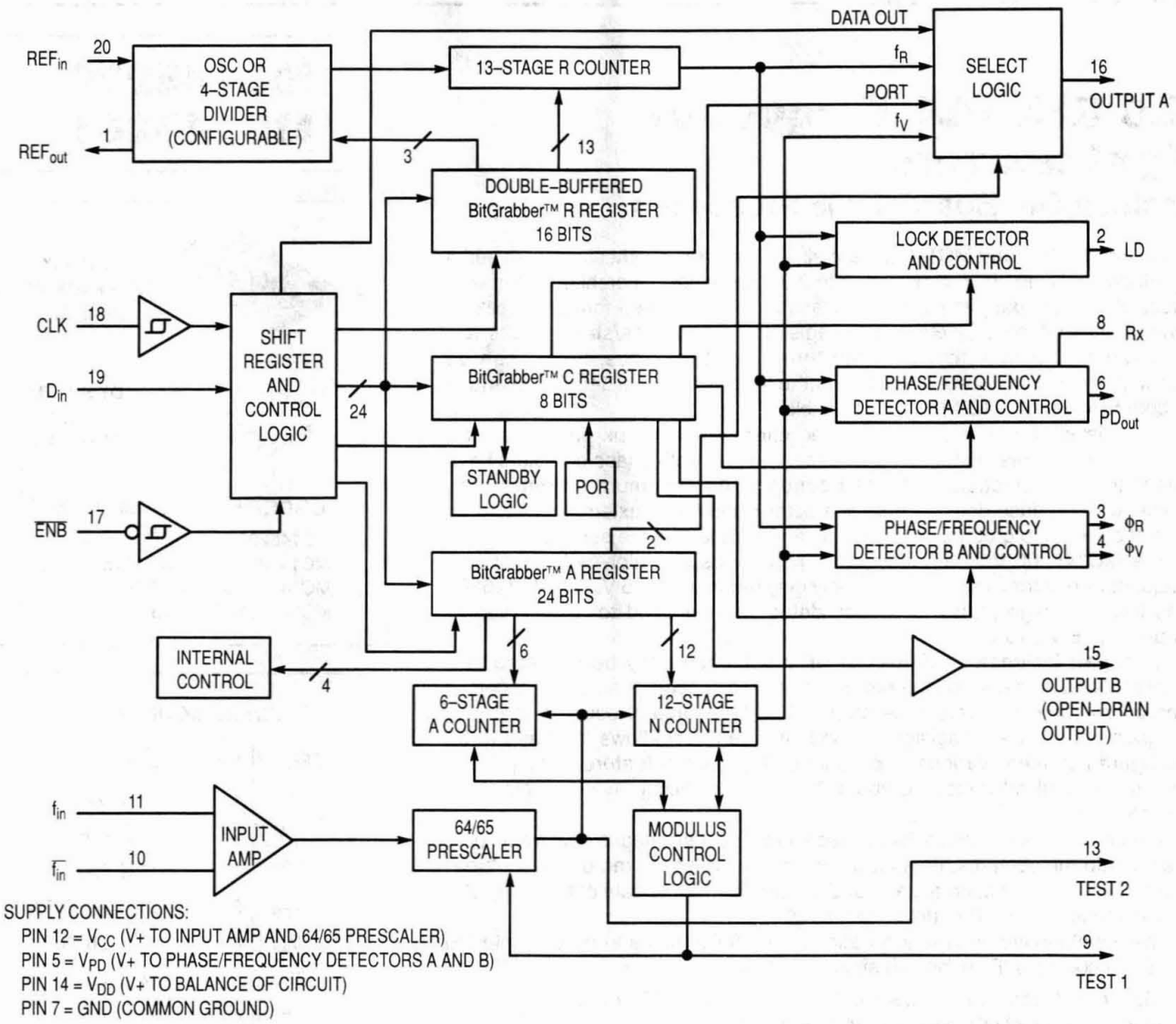
ORDERING INFORMATION

MC145200F	SOG Package
MC145201F	SOG Package
MC145200DT	TSSOP
MC145201DT	TSSOP

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	−0.5 to +6.0	V
V_{PD}	DC Supply Voltage (Pin 5) MC145200 MC145201	V_{DD} −0.5 to +9.5 V_{DD} −0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	−0.5 to V_{PD} +0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = −40 to +85°C, unless otherwise stated; MC145200: V_{PD} = 8.0 to 9.5 V; MC145201: V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$.)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, DC Coupled	$0.3 \times V_{DD}$	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, DC Coupled	$0.7 \times V_{DD}$	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 μA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = –20 μA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = V_{DD} – 0.4 V for REF_{out}, LD V_{out} = V_{PD} – 0.4 V for ϕ_R, ϕ_V	–0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A Only)	V_{out} = V_{DD} – 0.4 V	– 0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 or 0.5 V MC145200 Output in High–Impedance State MC145201	± 150 ± 200	nA
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	V_{out} = V_{PD} or GND, Output in High–Impedance State	± 10	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 22	30	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 μA	600	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 2.0 GHz; REF_{in} = 13 MHz @ 1 V p–p; OUTPUT A = Inactive and No Connect; REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Enabled (Bit C6 = Low)	*	mA

* The nominal value = 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \leq V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation	MC145200: $V_{out} = 0.5 \times V_{PD}$	8.0	±20	%
		9.5	±20	
	MC145201: $V_{out} = 0.5 \times V_{PD}$	4.5	±20	%
		5.5	±20	
Maximum Sink–vs–Source Mismatch (Note 3)	MC145200: $V_{out} = 0.5 \times V_{PD}$	8.0	12	%
		9.5	12	
	MC145201: $V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	MC145200: I_{out} variation ≤ 20%	8.0	0.5 to 7.5	V
		9.5	0.5 to 9.0	
	MC145201: I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within –40 to +85°C.

AC INTERFACE CHARACTERISTICS

($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; MC145200: $V_{PD} = 8.0$ to 9.5 V; MC145201: $V_{PD} = 4.5$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} only, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK,		10	pF

TIMING REQUIREMENTS

($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

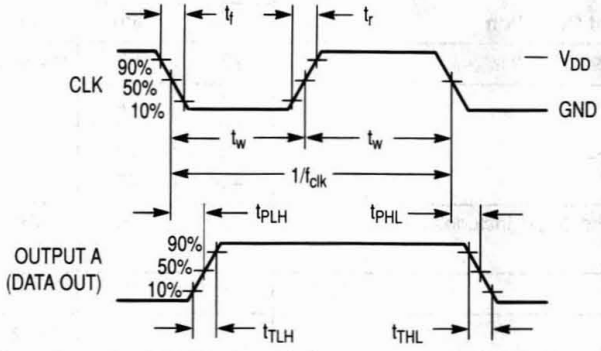


Figure 1.

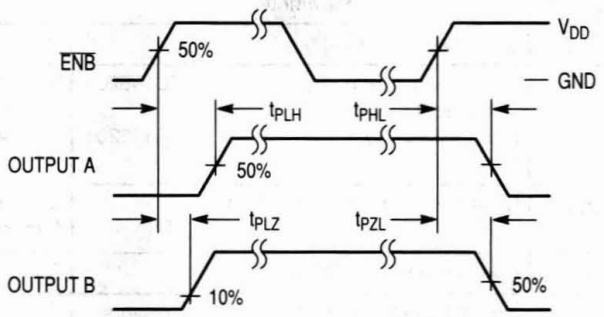


Figure 2.

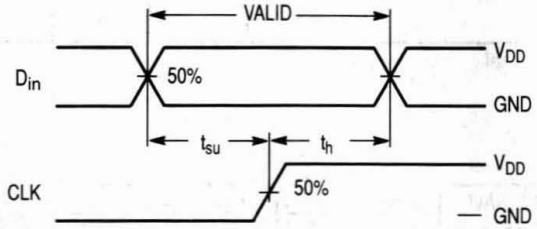


Figure 3.

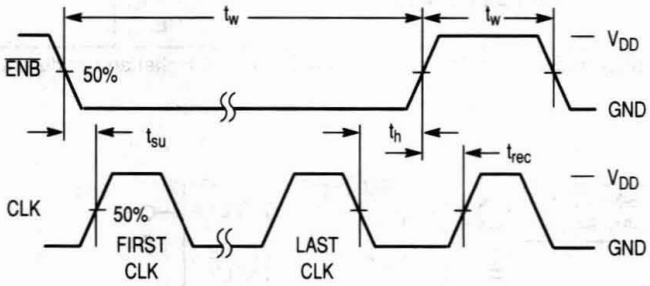
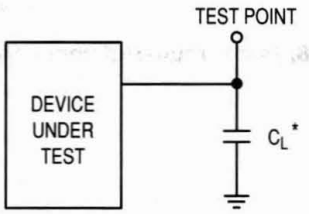
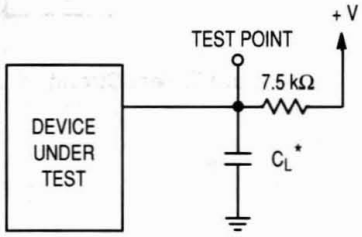


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Figure No.	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	500 MHz ≤ f_{in} ≤ 2000 MHz	7	200	1500	mV p–p
f_{ref}	Input Frequency, REF_{in} MC145200 Externally Driven in Reference Mode MC145201	V_{in} ≥ 400 mV p–p V_{in} ≥ 1 V p–p V_{in} ≥ 400 mV p–p V_{in} ≥ 1 V p–p	8	13 6* 12 4.5*	27 27 27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width, LD, ϕ_R, and ϕ_V, — MC145200, MC145201	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	17	85	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, and ϕ_R — MC145201	C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance f_{in} REF_{in}			— —	TBD 5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

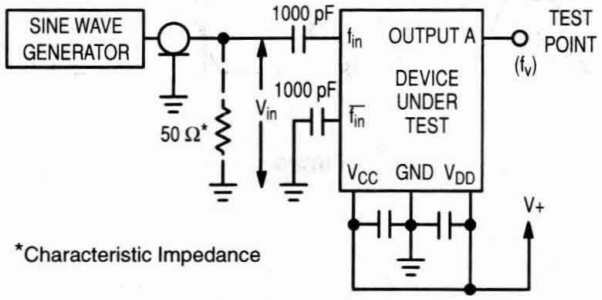


Figure 7. Test Circuit

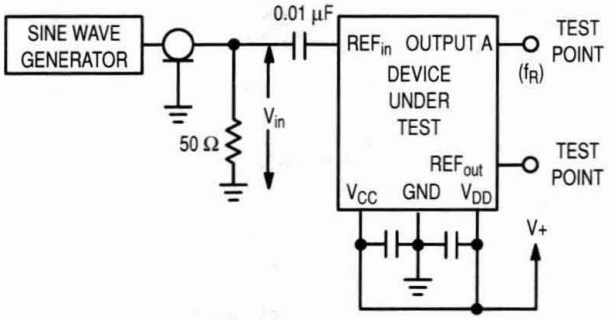


Figure 8. Test Circuit–Reference Mode

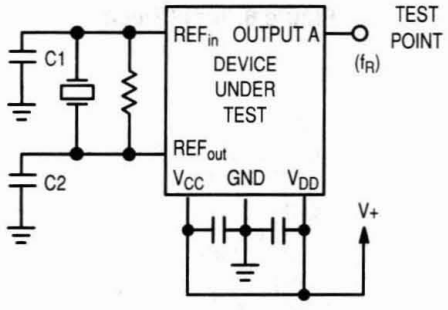


Figure 9. Test Circuit–Crystal Mode

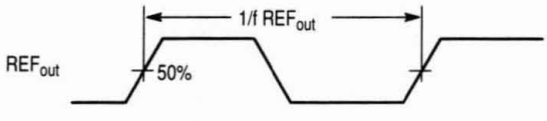


Figure 10. Switching Waveform

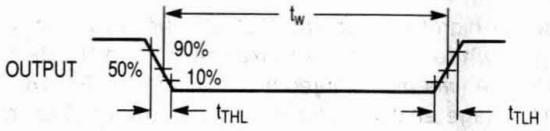


Figure 11. Switching Waveform

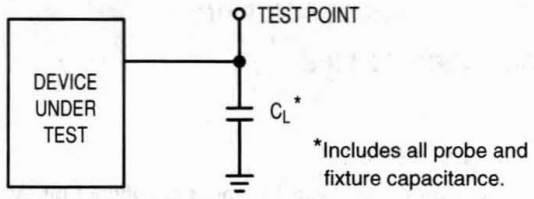
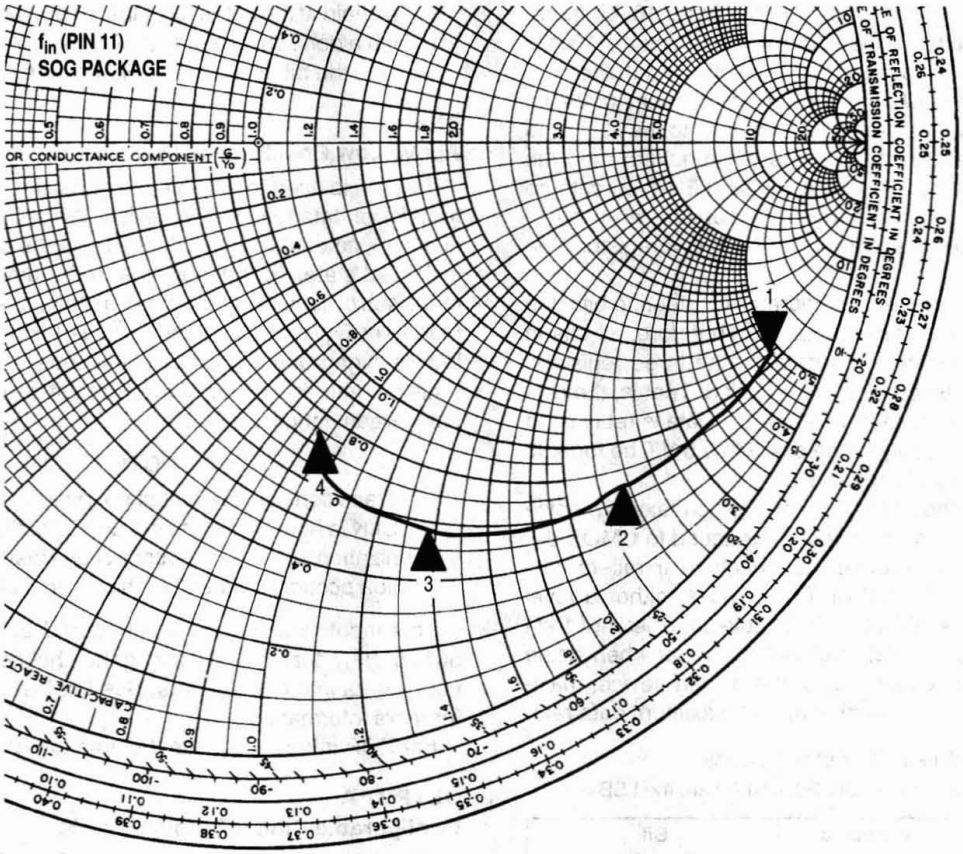


Figure 12. Test Circuit

MC145200/MC145201
NORMALIZED INPUT IMPEDANCE AT f_{in} — SERIES FORMAT (R + jX)
(500 MHz to 2 GHz)



Marker	Frequency (GHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	0.5	59.0	– 240	1.33
2	1	34.7	– 118	1.35
3	1.5	28.3	– 68.7	1.54
4	2	37.4	– 45.7	1.74

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 17).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 15, 16, and 17.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	See Figure 13	
Values > 32	See Figures 22–25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 24 through 26.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. As an alternative, the bit sequence of Figure 13 may be used.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0 through R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 9.5 V for the MC145200 and 5.5 V for the MC145201.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 8. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 17) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one–to–one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Freq. Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function (no dead zone). The operation of the phase/ frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state

Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to a floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 18).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 47 kΩ when V_{PD} is 9 V or about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +4.5 to +5.5 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 22.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

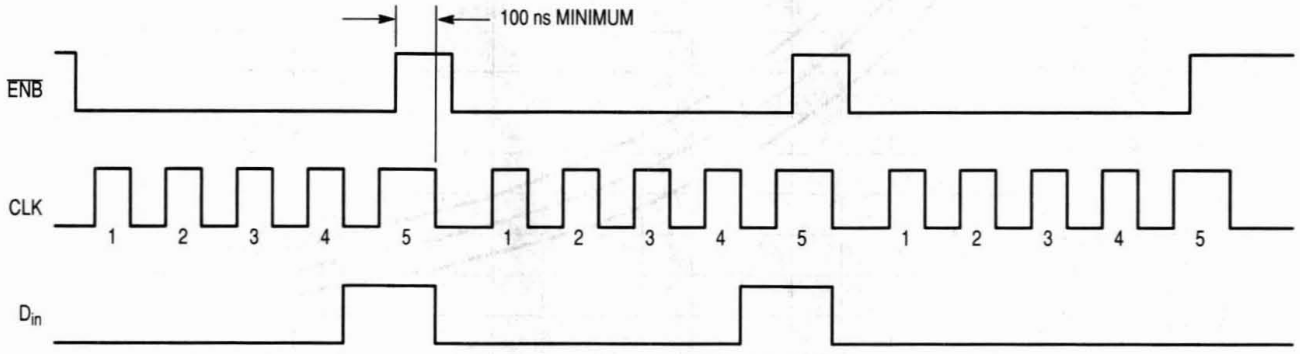
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be +9.5 V with respect to the GND pin for the MC145200 and +5.5 V for the MC145201.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



NOTE: It may not be convenient to control the $\overline{ENB}$ or CLK pins during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the CLK must remain high at least 100 ns after $\overline{ENB}$ is brought high. Note that 3 groups of 5 bits are needed.

Figure 13. Initializing the PLL through the Serial Port

MC145200
Nominal PD_{out} Spurious Current vs f_R Frequency
(1 V < PD_{out} < V_{PD} – 1V)

f_R (kHz)	Current (RMS nA)
10	1.6
20	5.3
50	22
100	95
200	320

MC145201
Nominal PD_{out} Spurious Current vs f_R Frequency
(1 V < PD_{out} < V_{PD} – 1V)

f_R (kHz)	Current (RMS nA)
10	3.6
20	4.6
50	17
100	75
200	244

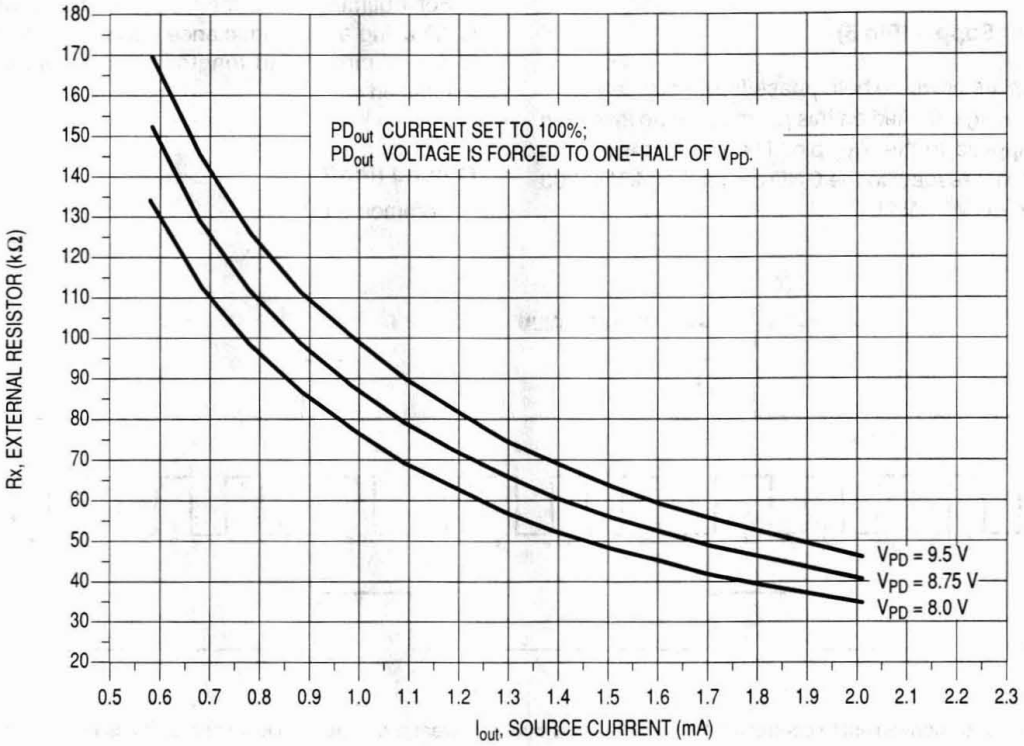
NOTE: For information on spurious current measurement see AN1253/D, "An Improved PLL Design Method Without ω_n and ζ".

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

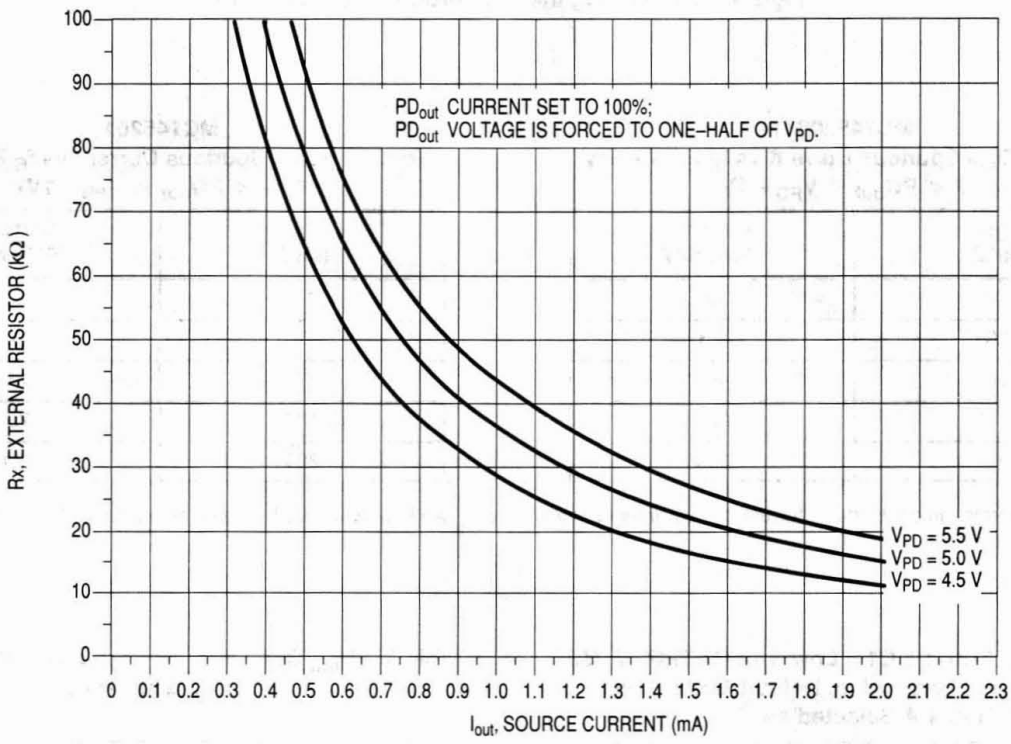
C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%


PDout CURRENT SET TO 100%;
PDout VOLTAGE IS FORCED TO ONE–HALF OF VPD.
VPD = 9.5 V
VPD = 8.75 V
VPD = 8.0 V
Rx, EXTERNAL RESISTOR (kΩ)
Iout, SOURCE CURRENT (mA)

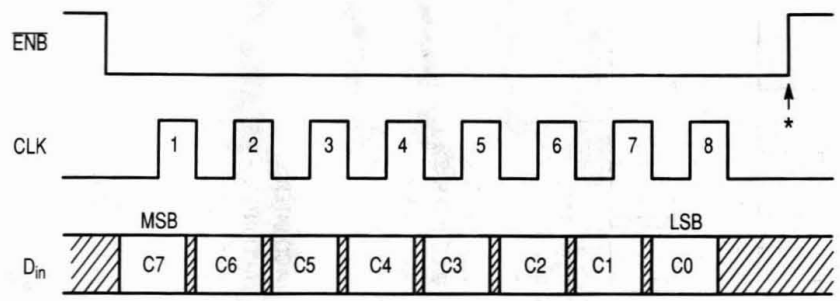
Nominal MC145200 PD_{out} Source Current vs Rx Resistance


PDout CURRENT SET TO 100%;
PDout VOLTAGE IS FORCED TO ONE–HALF OF VPD.
VPD = 5.5 V
VPD = 5.0 V
VPD = 4.5 V
Rx, EXTERNAL RESISTOR (kΩ)
Iout, SOURCE CURRENT (mA)

Nominal MC145201 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145201 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts the polarity of PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 18. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles are Used)

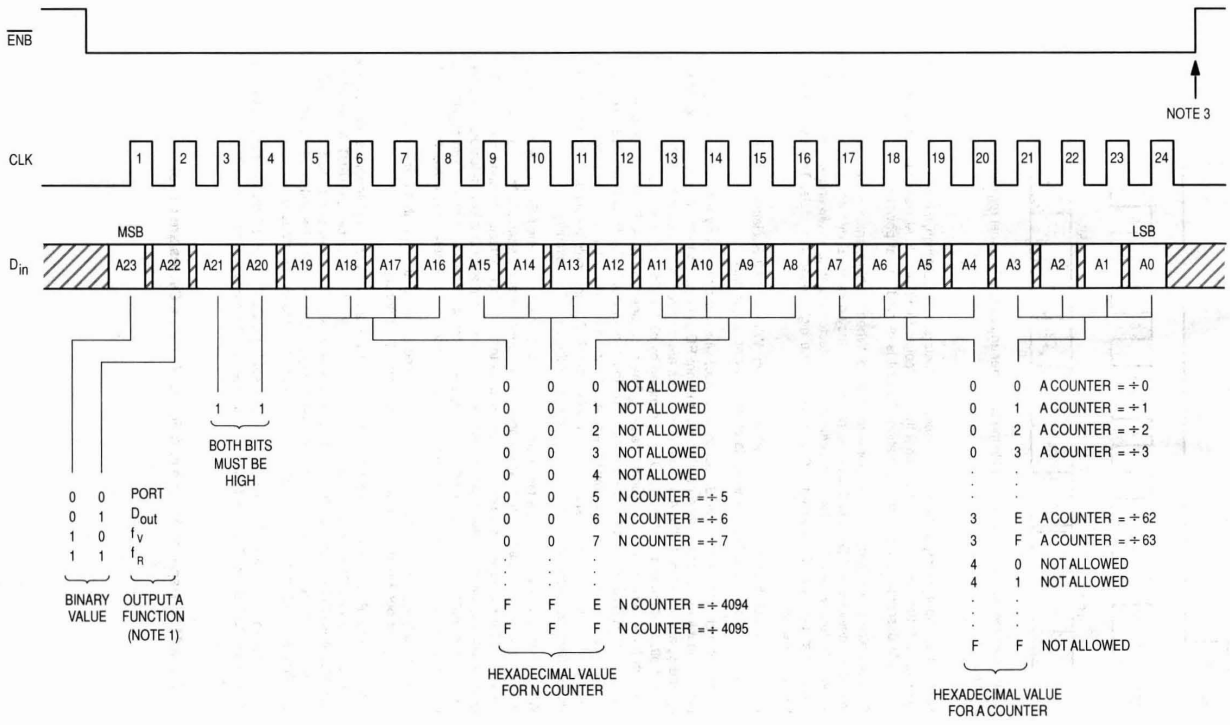
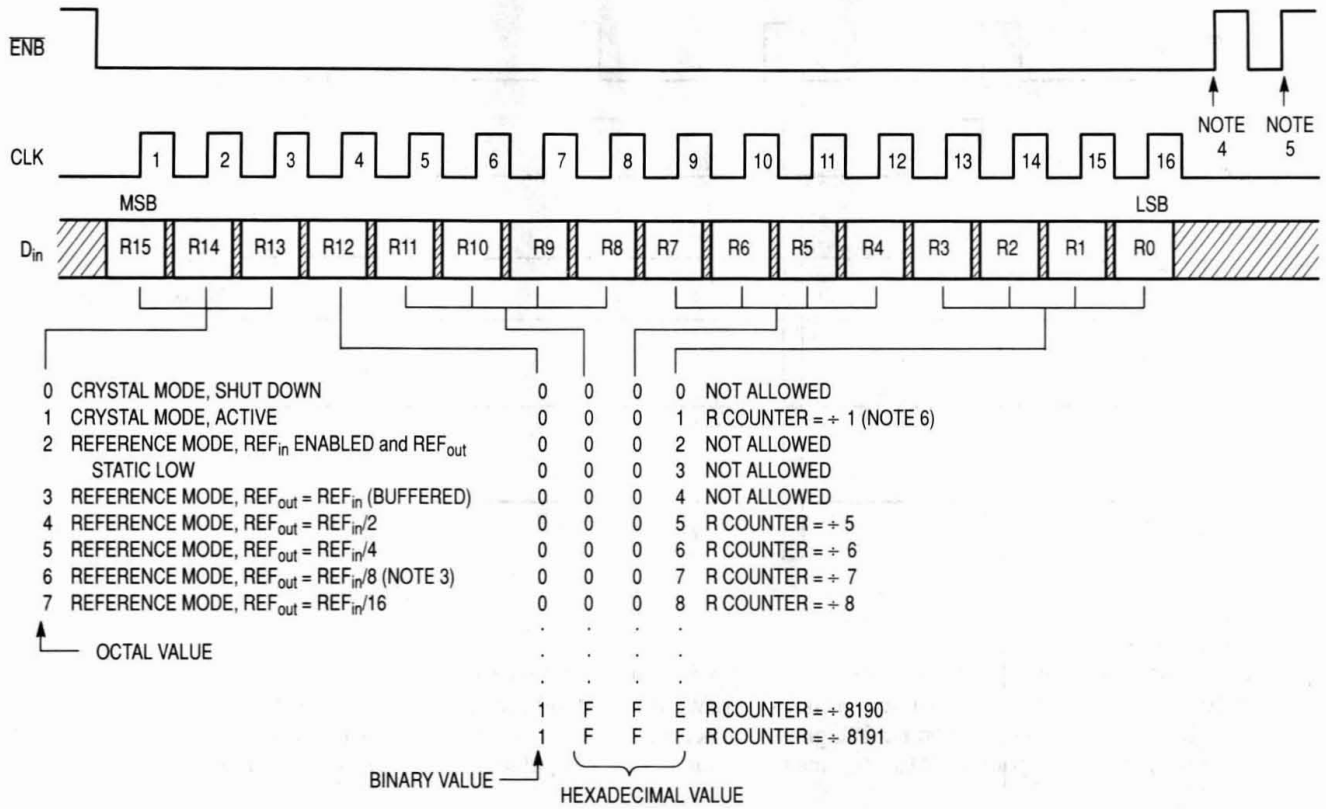

ENB
NOTE 3
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
MSB
LSB
Din
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 0 PORT
0 1 Dout
1 0 fV
1 1 fR
BINARY VALUE
OUTPUT A FUNCTION (NOTE 1)
1 1
BOTH BITS MUST BE HIGH
0 0 0 NOT ALLOWED
0 0 1 NOT ALLOWED
0 0 2 NOT ALLOWED
0 0 3 NOT ALLOWED
0 0 4 NOT ALLOWED
0 0 5 N COUNTER = ÷ 5
0 0 6 N COUNTER = ÷ 6
0 0 7 N COUNTER = ÷ 7
F F E N COUNTER = ÷ 4094
F F F N COUNTER = ÷ 4095
HEXADECIMAL VALUE FOR N COUNTER
0 0 A COUNTER = ÷ 0
0 1 A COUNTER = ÷ 1
0 2 A COUNTER = ÷ 2
0 3 A COUNTER = ÷ 3
3 E A COUNTER = ÷ 62
3 F A COUNTER = ÷ 63
4 0 NOT ALLOWED
4 1 NOT ALLOWED
F F NOT ALLOWED
HEXADECIMAL VALUE FOR A COUNTER

Figure 16. A Register Access and Format (24 Clock Cycles are Used)

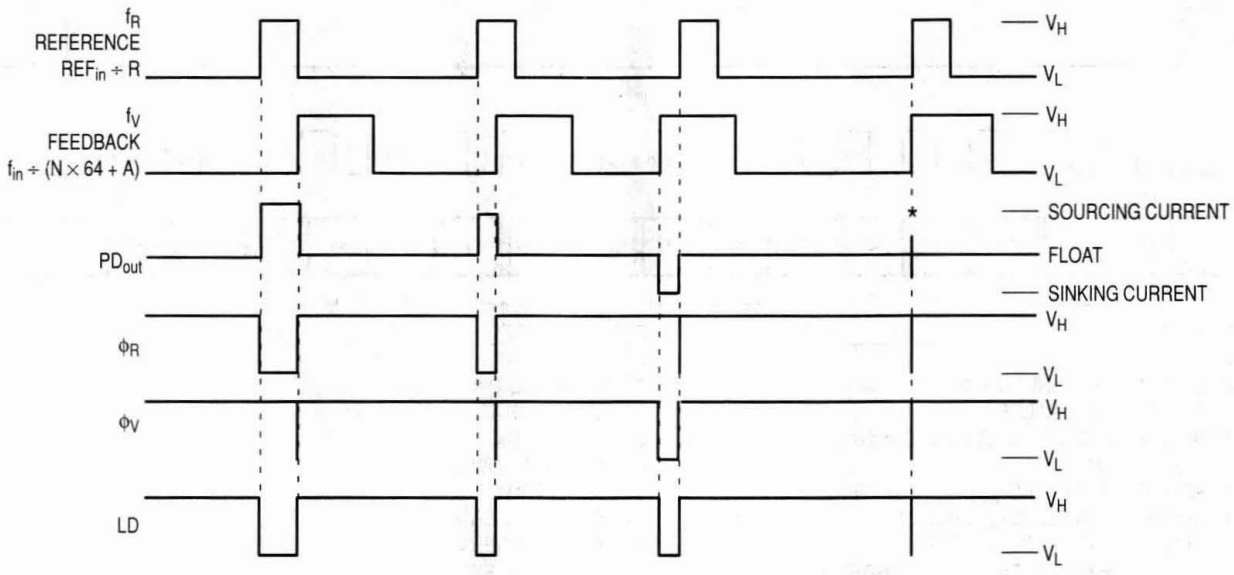
NOTES:
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.


ENB
NOTE 4
NOTE 5
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
MSB
LSB
Din
R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
0 CRYSTAL MODE, SHUT DOWN
1 CRYSTAL MODE, ACTIVE
2 REFERENCE MODE, REFin ENABLED and REFout STATIC LOW
3 REFERENCE MODE, REFout = REFin (BUFFERED)
4 REFERENCE MODE, REFout = REFin/2
5 REFERENCE MODE, REFout = REFin/4
6 REFERENCE MODE, REFout = REFin/8 (NOTE 3)
7 REFERENCE MODE, REFout = REFin/16
OCTAL VALUE
0 0 0 0 NOT ALLOWED
0 0 0 1 R COUNTER = ÷ 1 (NOTE 6)
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 0 4 NOT ALLOWED
0 0 0 5 R COUNTER = ÷ 5
0 0 0 6 R COUNTER = ÷ 6
0 0 0 7 R COUNTER = ÷ 7
0 0 0 8 R COUNTER = ÷ 8
1 F F E R COUNTER = ÷ 8190
1 F F F R COUNTER = ÷ 8191
BINARY VALUE
HEXADECIMAL VALUE

NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.

NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 18. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 19.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 20)
C_{out} = 6 pF (see Figure 20)
C_a = 1 pF (see Figure 20)

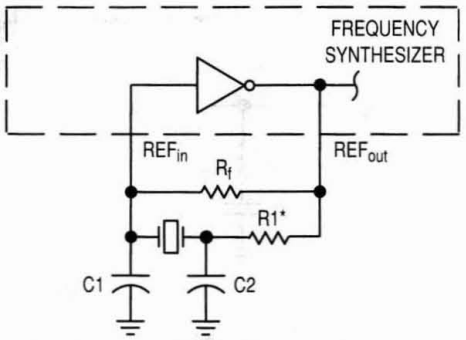
C1 and C2 = external capacitors (see Figure 19)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 21. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 19 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).



* May be needed in certain cases. See text.

Figure 19. Pierce Crystal Oscillator Circuit

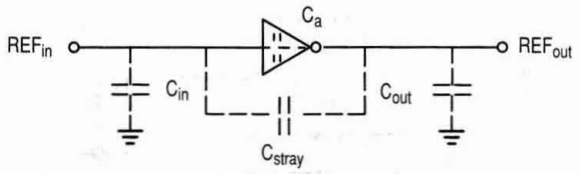
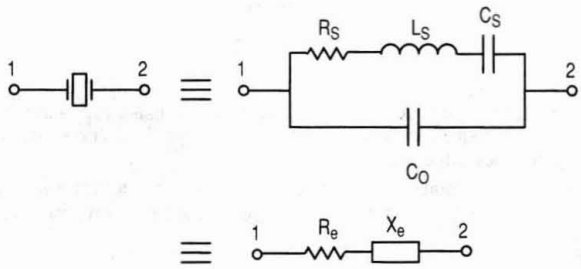


Figure 20. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 21. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

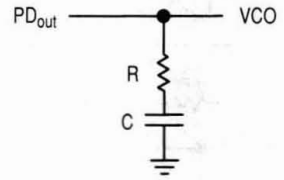
Table 4. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



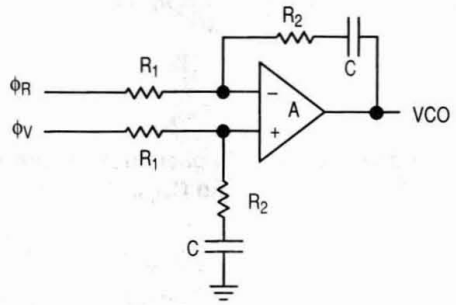
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

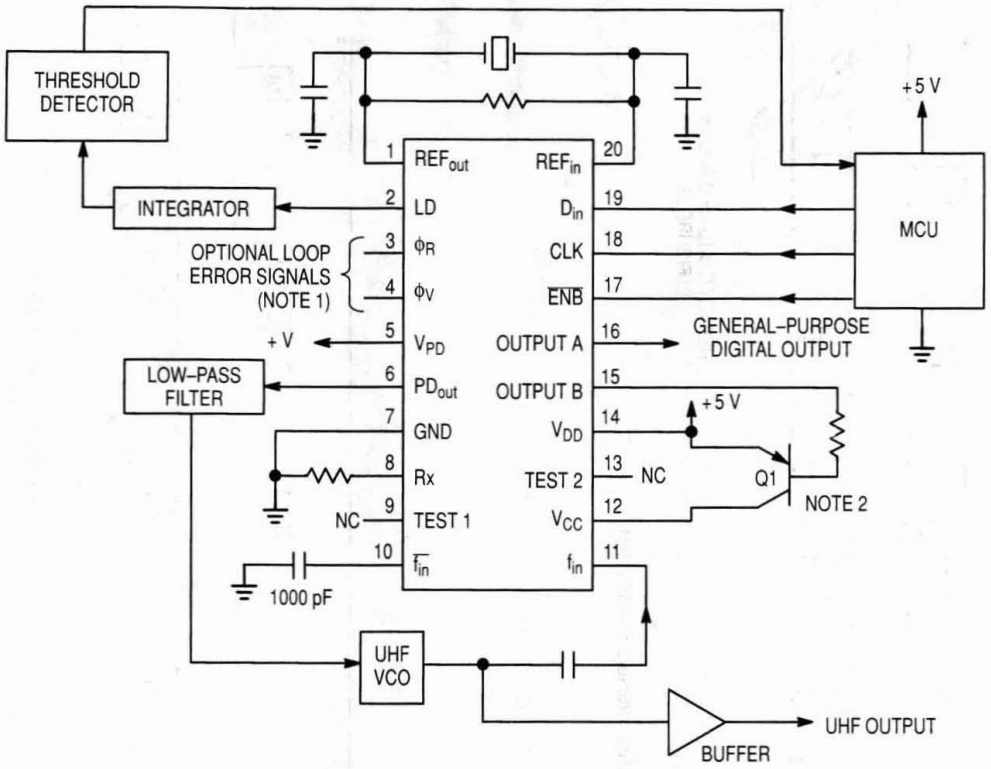
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

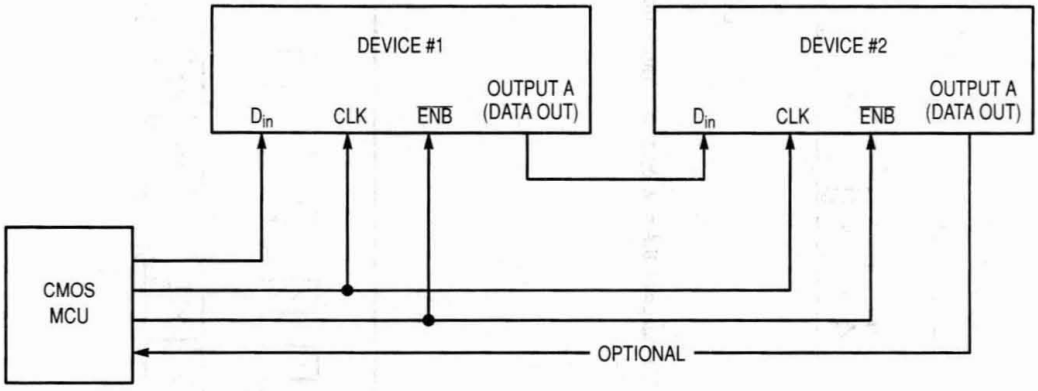
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 22. Example Application



NOTE: See related Figures 24 through 26; these bit streams apply to the MC145190, MC145191, MC145200, and MC145201.

Figure 23. Cascading Two Devices

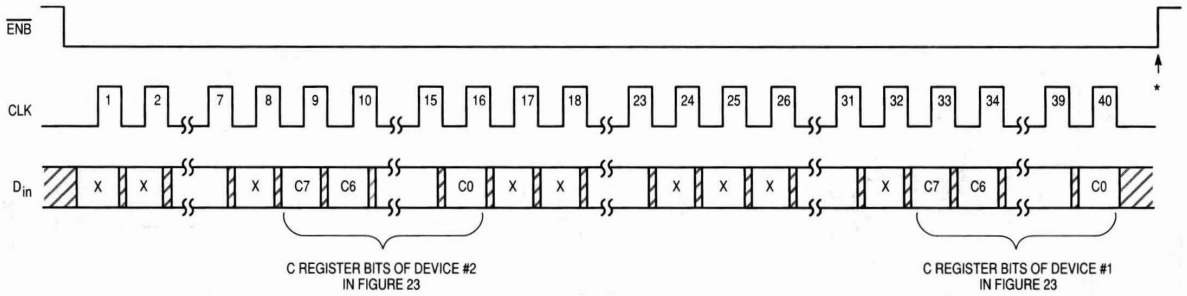

ENB
CLK
1 2 7 8 9 10 15 16 17 18 23 24 25 26 31 32 33 34 39 40
*
Din
X X X C7 C6 C0 X X X X X X C7 C6 C0
C REGISTER BITS OF DEVICE #2
IN FIGURE 23
C REGISTER BITS OF DEVICE #1
IN FIGURE 23

Figure 24. Accessing the C Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

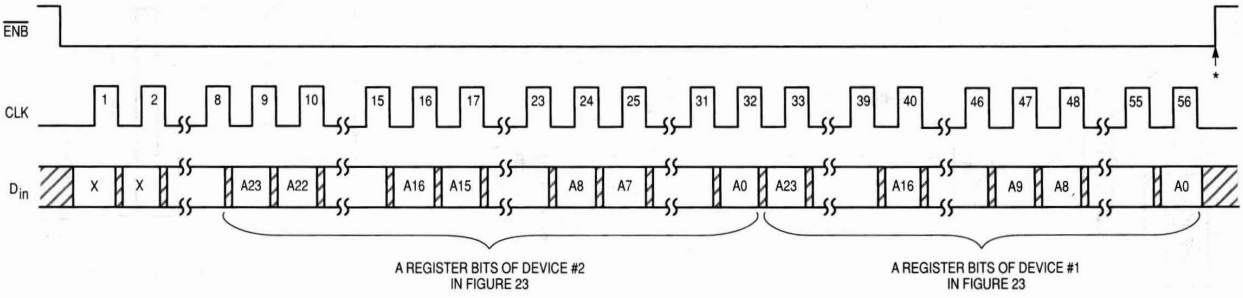

ENB
CLK
1 2 8 9 10 15 16 17 23 24 25 31 32 33 39 40 46 47 48 55 56
*
Din
X X A23 A22 A16 A15 A8 A7 A0 A23 A16 A9 A8 A0
A REGISTER BITS OF DEVICE #2
IN FIGURE 23
A REGISTER BITS OF DEVICE #1
IN FIGURE 23

Figure 25. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

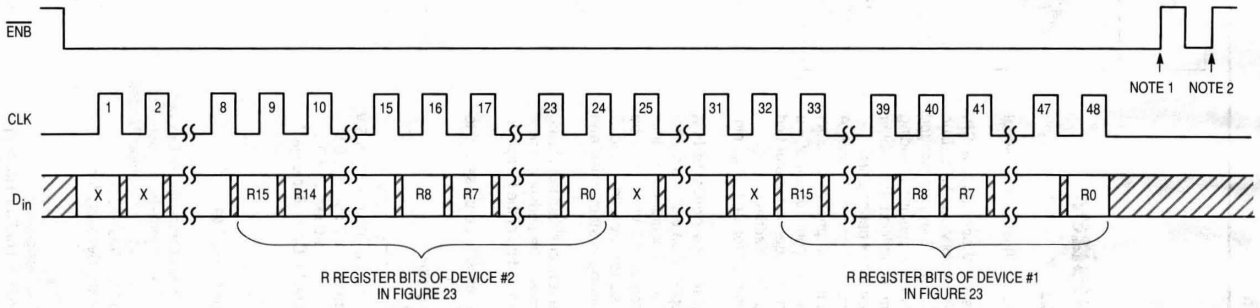


Figure 26. Accessing the R Registers of Two Cascaded Devices

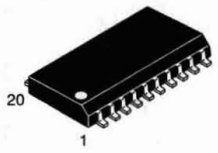
NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{\text{ENB}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

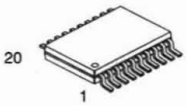
MC145202

Low-Voltage 2.0 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler



F SUFFIX
SOG PACKAGE
CASE 751J

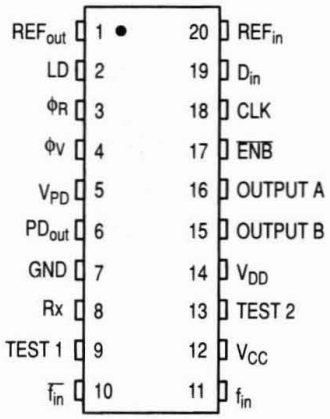


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145202F	SOG Package
MC145202DT	TSSOP

PIN ASSIGNMENT



The MC145202 is a low–voltage single–package synthesizer with serial interface capable of direct usage up to 2.0 GHz.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte-oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145202 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals.

The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

Slew–rate control is provided by a special driver designed for the REF_{out} pin. This minimizes interference caused by REF_{out}.

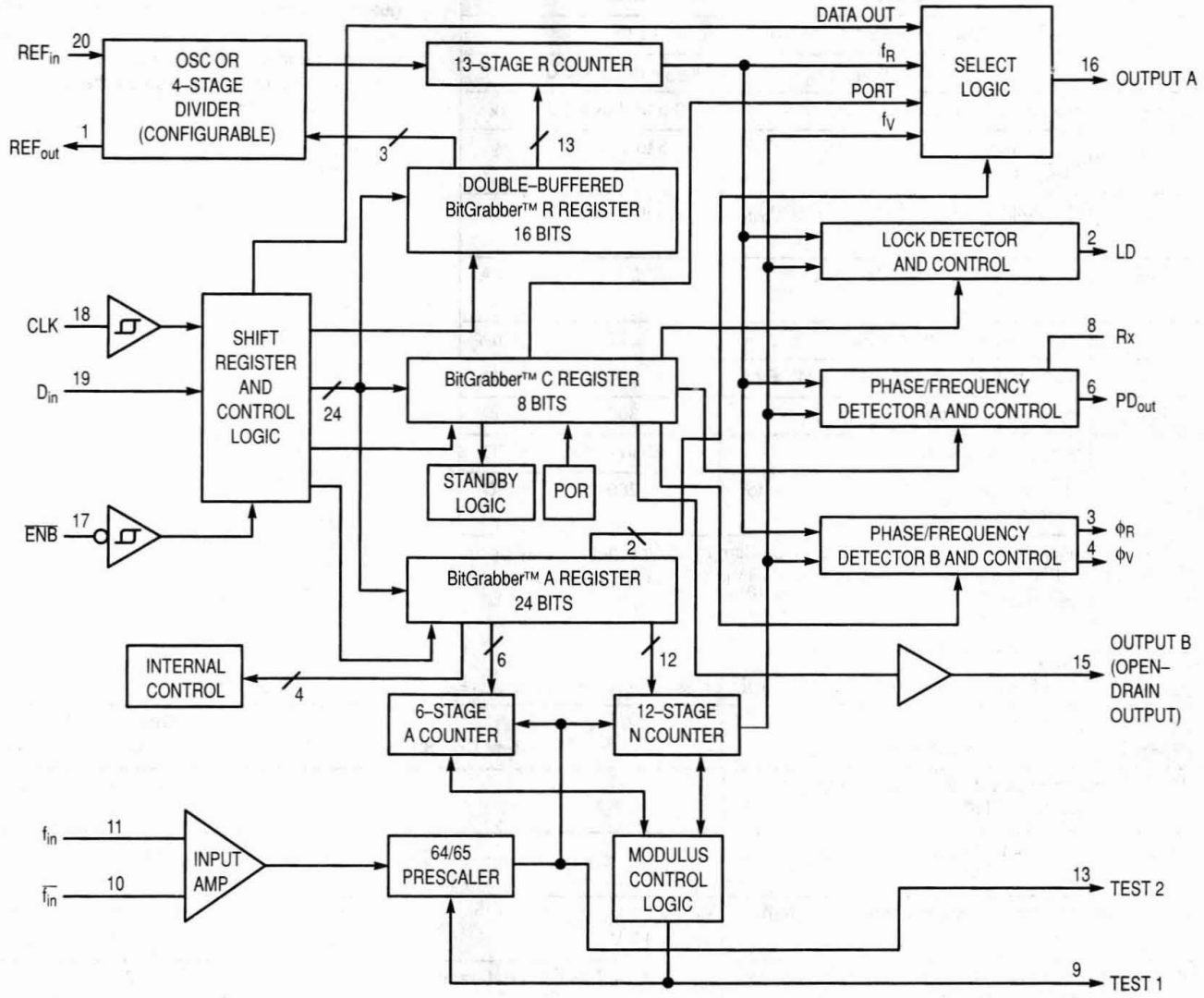
This part includes a differential RF input that may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ – 10 dBm
- Operating Supply Current: 4 mA Nominal at 3.0 V
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 2.7 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin): 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 1.7 mA @ 5.0 V
  1.0 mA @ 3.0 V
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: 1 and 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull) with Four Output Modes
  OUTPUT B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- Evaluation Kit Available (Part Number MC145202EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

BLOCK DIAGRAM



SUPPLY CONNECTIONS:

PIN 12 = V_{CC} (V+ TO INPUT AMP AND 64/65 PRESCALER)

PIN 5 = V_{PD} (V+ TO PHASE/FREQUENCY DETECTORS A AND B)

PIN 14 = V_{DD} (V+ TO BALANCE OF CIRCUIT)

PIN 7 = GND (COMMON GROUND)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, Voltages Referenced to GND, unless otherwise stated; V_{PD} = 2.7 to 5.5 V, T_A = – 40 to 85°C)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.3 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.7 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)	V_{DD} = 2.7 V V_{DD} = 4.5 V	100 250	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = – 20 µA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD)	V_{out} = 0.3 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (ϕ_R, ϕ_V)	V_{out} = 0.3 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A)	V_{out} = 0.4 V V_{DD} = 4.5 V	1.0	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD)	V_{out} = V_{DD} – 0.3 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (ϕ_R, ϕ_V)	V_{out} = V_{PD} – 0.3 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A Only)	V_{out} = V_{DD} – 0.4 V V_{DD} = 4.5 V	– 0.6	mA

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	$V_{in} = V_{DD}$ or GND, Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	$V_{in} = V_{DD}$ or GND, Device in Reference Mode	± 100	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	$V_{out} = V_{PD}$ or GND, Output in Floating State	± 130	nA
	(OUTPUT B)	$V_{out} = V_{PD}$ or GND, Output in High–Impedance State	± 1	µA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	$V_{in} = V_{DD}$ or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 21	30	µA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static State, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 170 µA, V_{PD} = 5.5 V	750	µA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 2.0 GHz; REF_{in} = 13 MHz @ 1 Vp–p; OUTPUT A = Inactive and No Connect; $V_{DD} = V_{CC}$, REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	*	mA

* The nominal values are:
4 mA at V_{DD} = 3.0 V and V_{PD} = 3.0 V
6 mA at V_{DD} = 5.0 V and V_{PD} = 5.0 V
These are not guaranteed limits.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — PD_{out}

($I_{out} \leq 1$ mA @ V_{DD} = 2.7 V and $I_{out} \leq 1.7$mA @ $V_{DD} \geq 4.5$ V, $V_{DD} = V_{CC}$ = 2.7 to 5.5 V, Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	$V_{out} = 0.5 \times V_{PD}$	2.7	± 15	%
		4.5	± 15	
		5.5	± 15	
Maximum Sink–vs–Source Mismatch (Note 3)	$V_{out} = 0.5 \times V_{PD}$	2.7	11	%
		4.5	11	
		5.5	11	
Output Voltage Range (Note 3)	I_{out} Variation ≤ 15%	2.7	0.5 to 2.2	V
	I_{out} Variation ≤ 20%	4.5	0.5 to 3.7	
	I_{out} Variation ≤ 22%	5.5	0.5 to 4.7	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40 to + 85°C.

AC INTERFACE CHARACTERISTICS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, T_A = – 40 to + 85°C, C_L = 25 pF, Input t_r = t_f = 10 ns; V_{PD} = 2.7 to 5.5 V)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	100	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	150	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	150	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL}only, on OUTPUT B	1, 5, 6	50	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF

TIMING REQUIREMENTS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, T_A = – 40 to + 85°C, Input t_r = t_f = 10 ns, unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

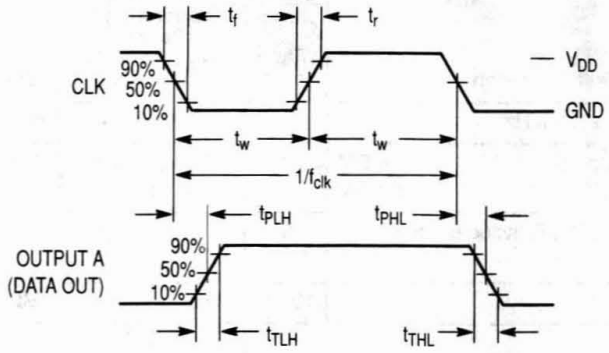


Figure 1.

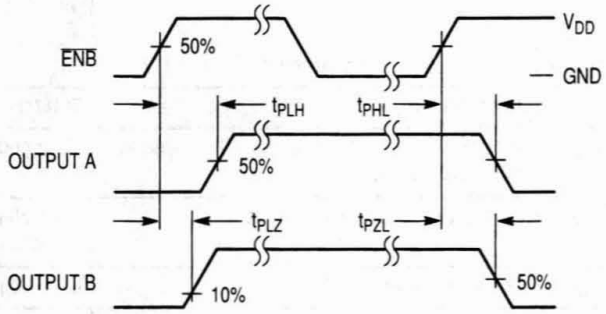


Figure 2.

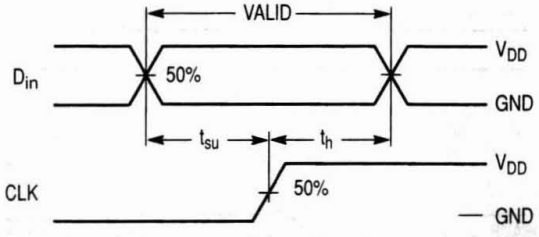


Figure 3.

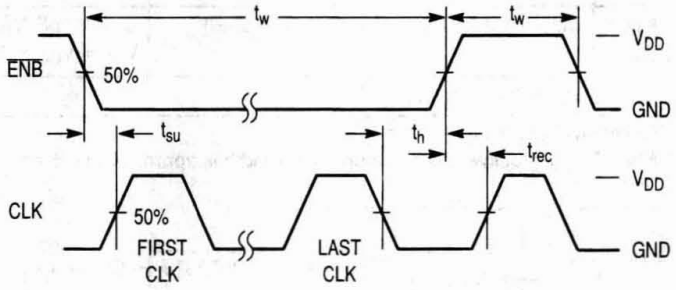
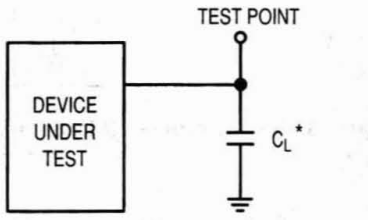
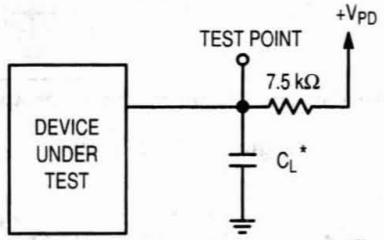


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5.



* Includes all probe and fixture capacitance.

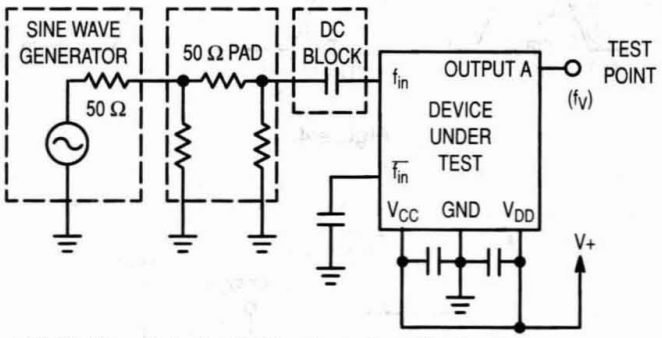
Figure 6.

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 2.7 to 5.5 V unless otherwise indicated, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	Fig. No.	Guaranteed Operating Range		Unit
				Min	Max	
P_{in}	Input Sensitivity Range, f_{in}	500 MHz ≤ f_{in} ≤ 2000 MHz	7	– 10	4	dBm*
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode	V_{in} ≥ 400 mV p–p 2.7 ≤ V_{DD} < 4.5 V 4.5 ≤ V_{DD} ≤ 5.5 V	8	1.5 1.5	20 30	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 20 pF, V_{out} ≥ 1 V p–p	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width (ϕ_R, ϕ_V, and LD)	f_R in Phase with f_V, C_L = 20 pF, ϕ_R and ϕ_V active for LD measurement, ** V_{PD} = 2.7 to 5.5 V V_{DD} = 2.7 V V_{DD} = 4.5 V V_{DD} = 5.5 V	11, 12	 40 18 14	 120 60 50	ns
t_{TLH}, t_{THL}	Output Transition Times (LD, ϕ_V, and ϕ_R)	C_L = 20 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	11, 12	—	80	ns
C_{in}	Input Capacitance, REF_{in}			—	7	pF

* Power level at the input to the dc block.

** When PD_{out} is active, LD minimum pulse width is approximately 5 ns.



NOTE: Alternately, the 50 Ω pad may be a T network.

Figure 7. Test Circuit

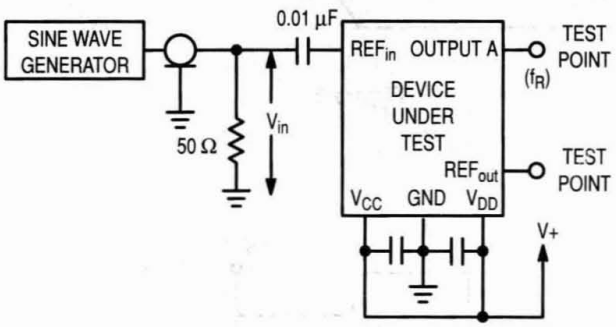


Figure 8. Test Circuit — Reference Mode

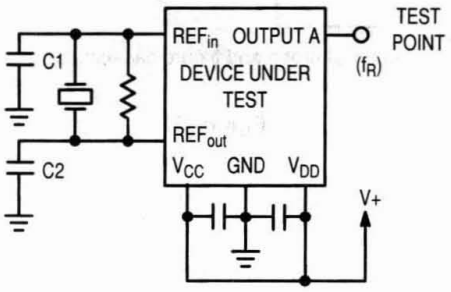


Figure 9. Test Circuit — Crystal Mode

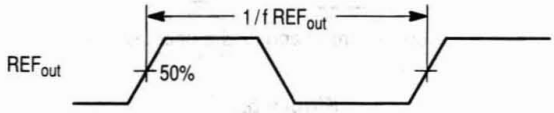


Figure 10. Switching Waveform

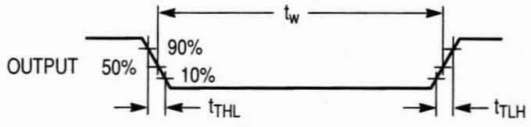


Figure 11. Switching Waveform

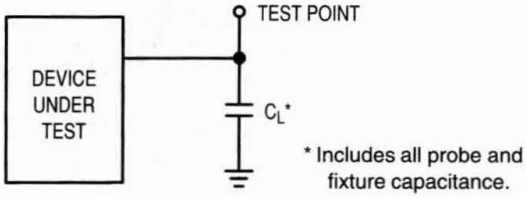


Figure 12. Test Circuit

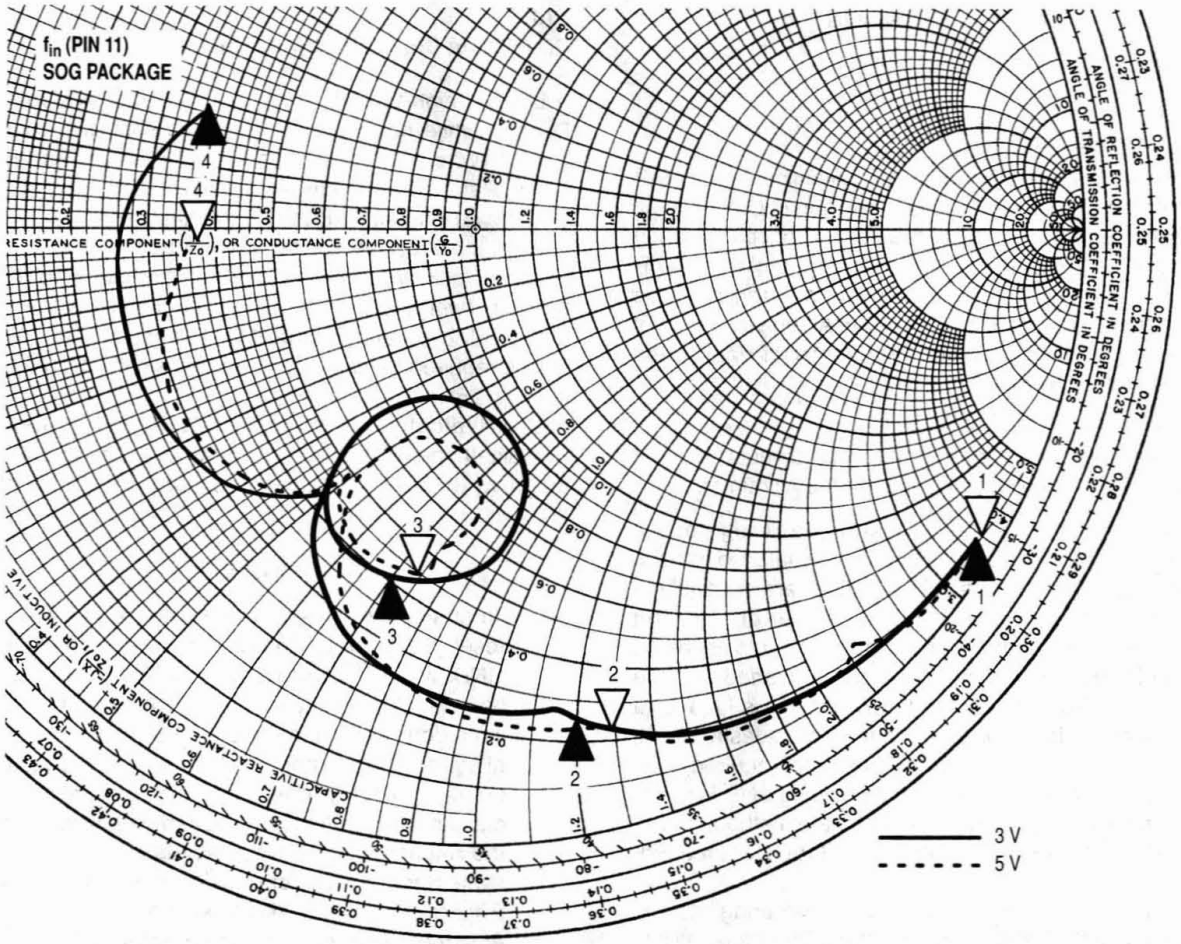


Figure 13. Normalized Input Impedance at f_{in} — Series Format (R + jx)

Table 1. Input Impedence at f_{in} — Series Format (R + jx), V_{CC} = 3 V

Marker	Frequency (GHz)	Resistance (Ω)	Reactance (Ω)	Capacitance/ Inductance
1	0.5	11.4	– 168	1.9 pF
2	1	12.4	– 59.4	2.68 pF
3	1.5	19.8	– 34.9	3.04 pF
4	2	18.1	9.43	751 pH

Table 2. Input Impedence at f_{in} — Series Format (R + jx), V_{CC} = 5 V

Marker	Frequency (GHz)	Resistance (Ω)	Reactance (Ω)	Capacitance/ Inductance
1	0.5	11.8	–175	1.82 pF
2	1	11.5	– 64.4	2.47 pF
3	1.5	22.2	– 36.5	2.91 pF
4	2	18.4	1.14	90.4 pH

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 3). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 16).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber Plus registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 3. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 22 – 25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 3 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 23 through 25.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. Floating, toggling, or having these pins in the wrong state during power–up does not harm the chip, but causes two potentially undesirable effects. First, the outputs of the device power up in an unknown state. Second, if two devices are cascaded, the A Registers must be written twice after power up. After these two accesses, the two cascaded chips perform normally.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 3.

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 15.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high. The f_R signal can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 16). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high. The f_V signal can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 15. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 5.5 V.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 16) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is listed in the Loop Specifications table for an output swing of 1 V p–p and 20 pF loads. Therefore, for higher REF_{in} frequencies, the one–to–one ratio may not be used for this magnitude of signal swing and loading requirements. Likewise, for REF_{in} frequencies above two times the highest rated frequency, the ratio must be more than two.

The output has a special on–board driver that has slew–rate control. This feature minimizes interference in the application.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption.

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they are usually used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the high–impedance state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 17).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 4 and 5 for other current values. The recommended value for Rx is 3.9 kΩ. A value of 3.9 kΩ provides current at the PD_{out} pin of approximately 1 mA @ V_{DD} = 3 V and approximately 1.7 mA @ V_{DD} = 5 V in the 100% current mode. Note that V_{DD}, not V_{PD}, is a factor in determining the current.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

Table 4. PD_{out} Current*, C1 = Low with OUTPUT A *not* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

Bit C3	Bit C2	PD_{out} Current*
0	0	70%
0	1	80%
1	0	90%
1	1	100%

* At the time the data sheet was printed, only the 100% current mode was guaranteed. The reduced current modes were for experimentation only.

Table 5. PD_{out} Current*, C1 = High with OUTPUT A *not* Selected as "Port"

Bit C3	Bit C2	PD_{out} Current*
0	0	25%
0	1	50%
1	0	75%
1	1	100%

* At the time the data sheet was printed, only the 100% current mode was guaranteed. The reduced current modes were for experimentation only.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. Also, this pin, in conjunction with the Rx resistor, determines the internal reference current for the PD_{out} pin. The voltage range is +2.7 to +5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +2.7 to +5.5 V with respect to the GND pin. In standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 21.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

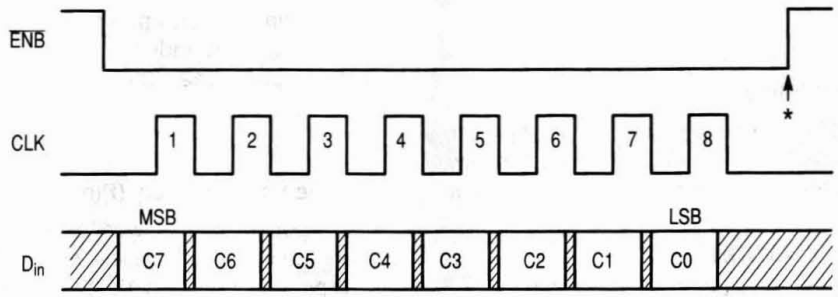
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin may be more or less than the potential applied to the V_{DD} and V_{CC} pins. The voltage range for V_{PD} is 2.7 to 5.5 V with respect to the GND pin.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – STBY: When set, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in two steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 – I2, I1: Controls the PD_{out} source/sink current per Tables 4 and 5. With both bits high, the maximum current is available. Also, see C1 bit description.

C1 – Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is ***not*** selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 4 and 5.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 – Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)

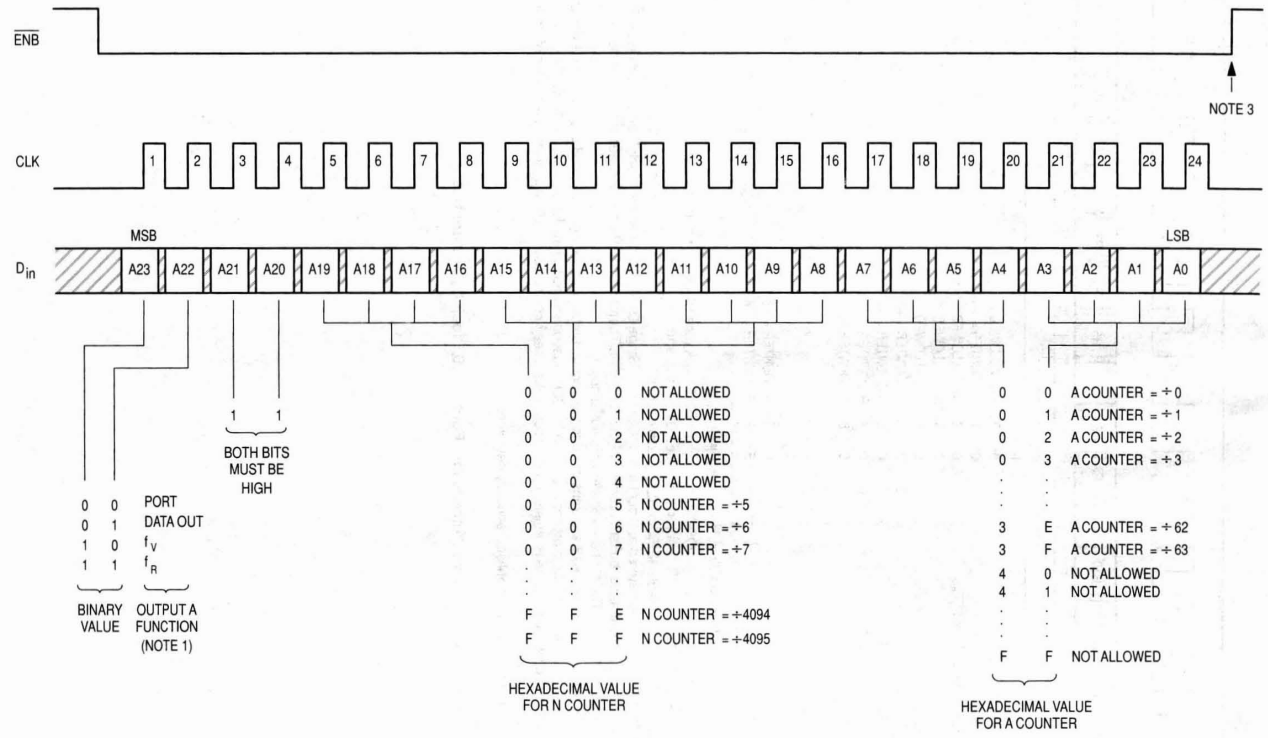
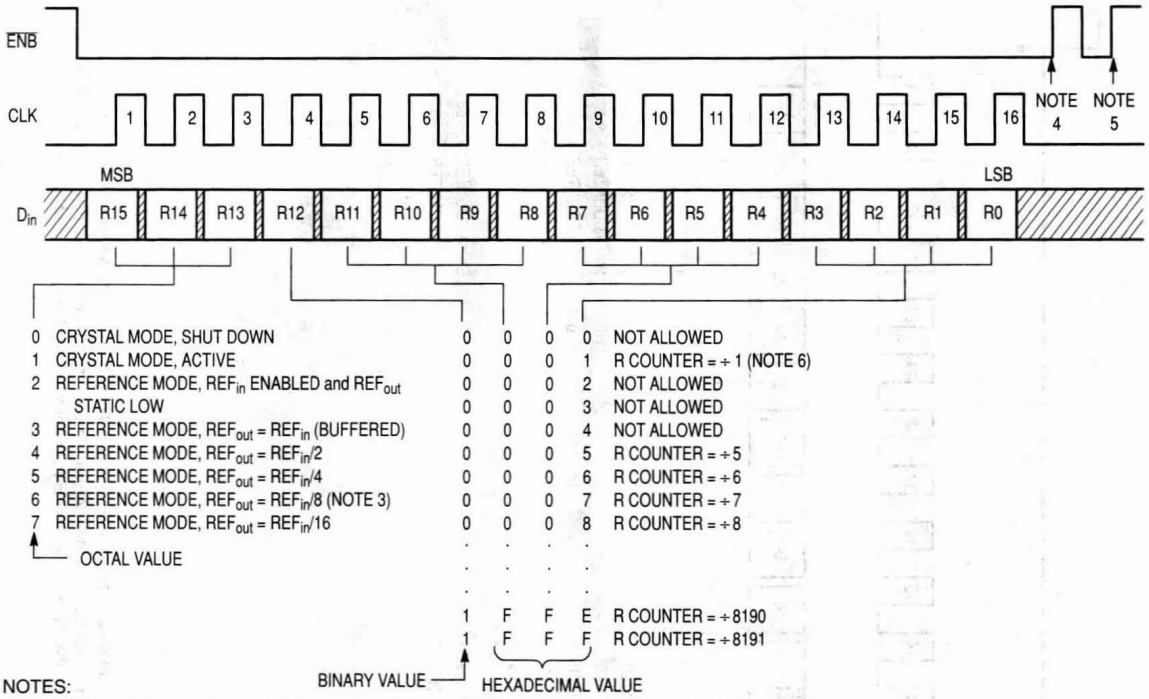

ENB
NOTE 3
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
MSB
LSB
Din
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 0 PORT DATA OUT
0 1 fV
1 0 fR
1 1
BINARY VALUE
OUTPUT A FUNCTION (NOTE 1)
1 1
BOTH BITS MUST BE HIGH
0 0 0 NOT ALLOWED
0 0 1 NOT ALLOWED
0 0 2 NOT ALLOWED
0 0 3 NOT ALLOWED
0 0 4 NOT ALLOWED
0 0 5 N COUNTER = ÷5
0 0 6 N COUNTER = ÷6
0 0 7 N COUNTER = ÷7
F F E N COUNTER = ÷4094
F F F N COUNTER = ÷4095
HEXADECIMAL VALUE FOR N COUNTER
0 0 A COUNTER = ÷0
0 1 A COUNTER = ÷1
0 2 A COUNTER = ÷2
0 3 A COUNTER = ÷3
3 E A COUNTER = ÷62
3 F A COUNTER = ÷63
4 0 NOT ALLOWED
4 1 NOT ALLOWED
F F NOT ALLOWED
HEXADECIMAL VALUE FOR A COUNTER

Figure 15. A Register Access and Format (24 Clock Cycles are Used)

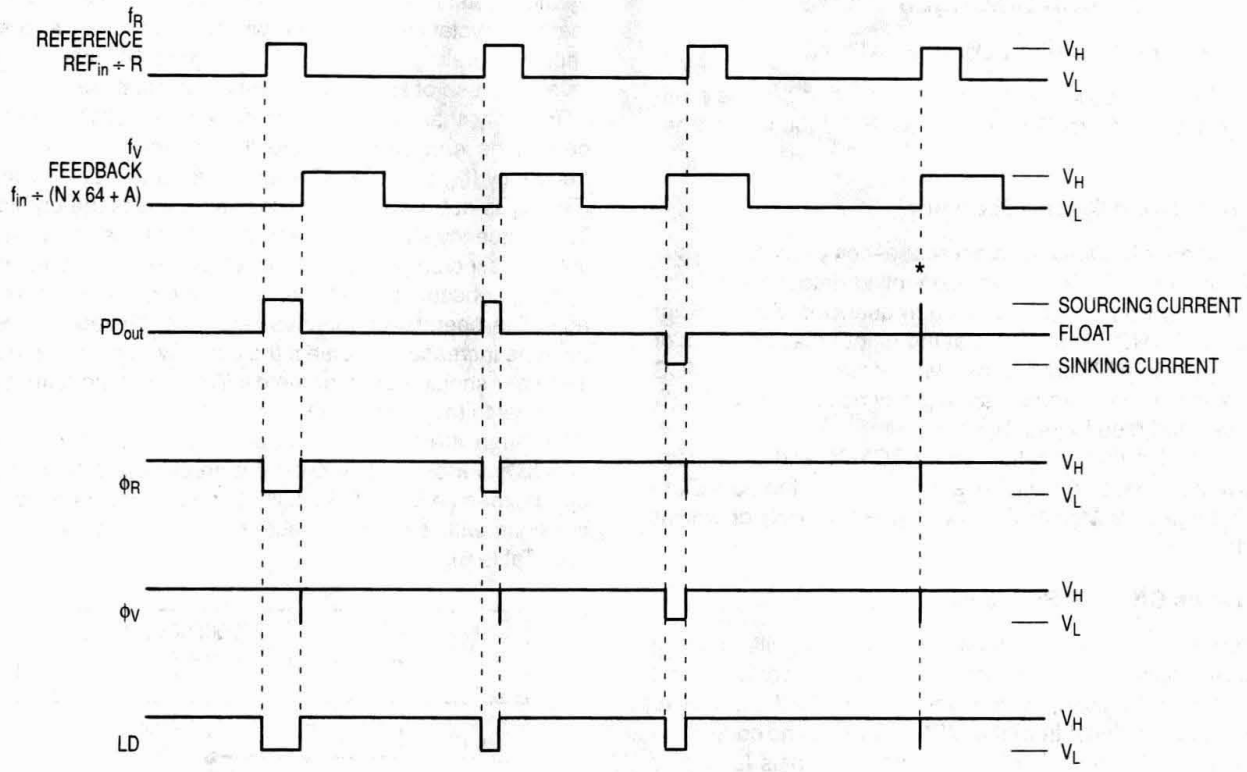
NOTES:
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.


ENB
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
NOTE 4
NOTE 5
MSB
LSB
Din
R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
0 CRYSTAL MODE, SHUT DOWN
1 CRYSTAL MODE, ACTIVE
2 REFERENCE MODE, REFin ENABLED and REFout STATIC LOW
3 REFERENCE MODE, REFout = REFin (BUFFERED)
4 REFERENCE MODE, REFout = REFin/2
5 REFERENCE MODE, REFout = REFin/4
6 REFERENCE MODE, REFout = REFin/8 (NOTE 3)
7 REFERENCE MODE, REFout = REFin/16
OCTAL VALUE
0 0 0 0 NOT ALLOWED
0 0 0 1 R COUNTER = ÷ 1 (NOTE 6)
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 0 4 NOT ALLOWED
0 0 0 5 R COUNTER = ÷5
0 0 0 6 R COUNTER = ÷6
0 0 0 7 R COUNTER = ÷7
0 0 0 8 R COUNTER = ÷8
1 F F E R COUNTER = ÷8190
1 F F F R COUNTER = ÷8191
BINARY VALUE
HEXADECIMAL VALUE

NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. Optional load pulse. At this point, bits R0 – R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. The C and A registers are not affected. The first buffer of the R register is not affected. Also, see note 3 of Figure 15 for an alternate method of loading the second buffer in the R register.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.

NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is in the floating condition and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequencies listed in the Loop Specifications table. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

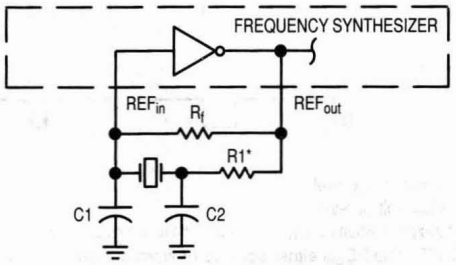
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 6).



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

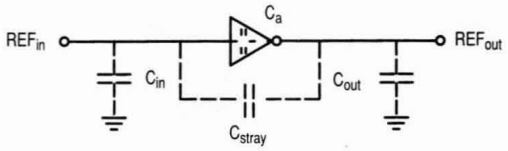
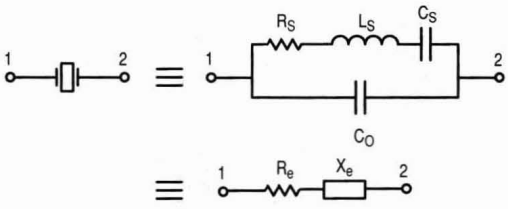


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

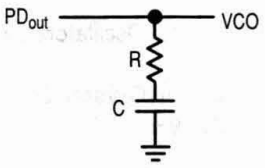
Table 6. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

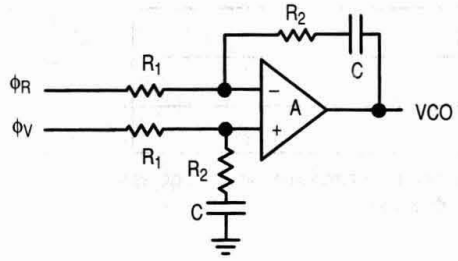
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

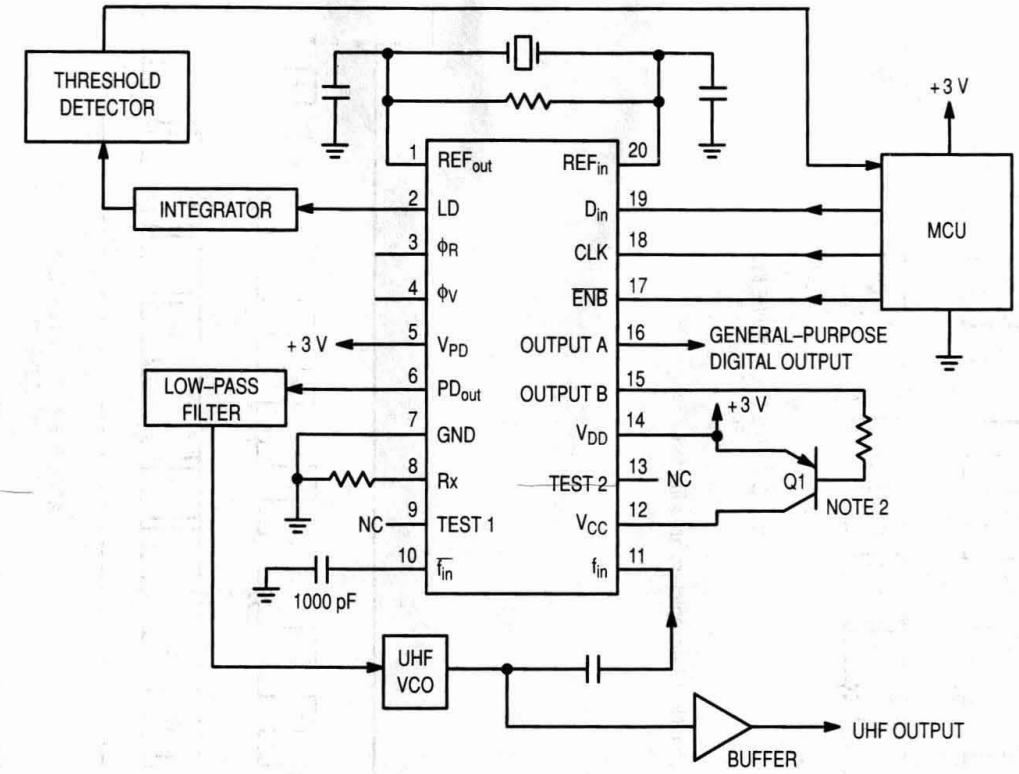
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

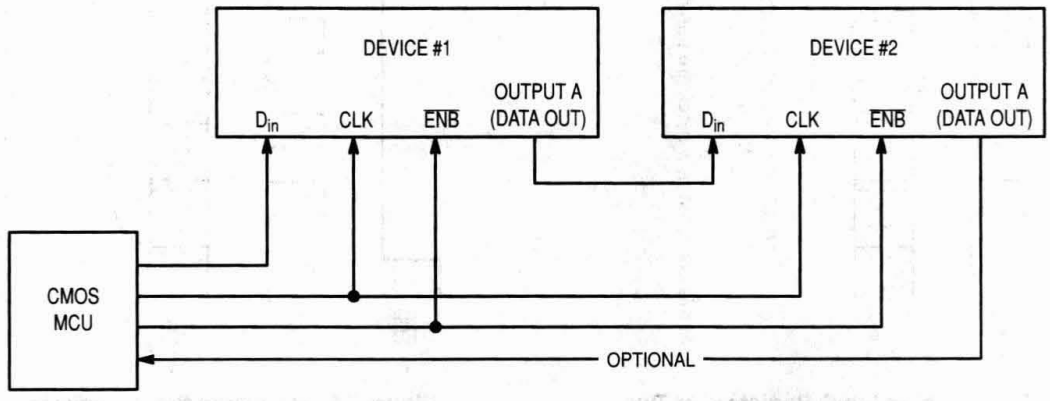
AN1253, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 21. Example Application



NOTE: See related Figures 23, 24, and 25.

Figure 22. Cascading Two Devices

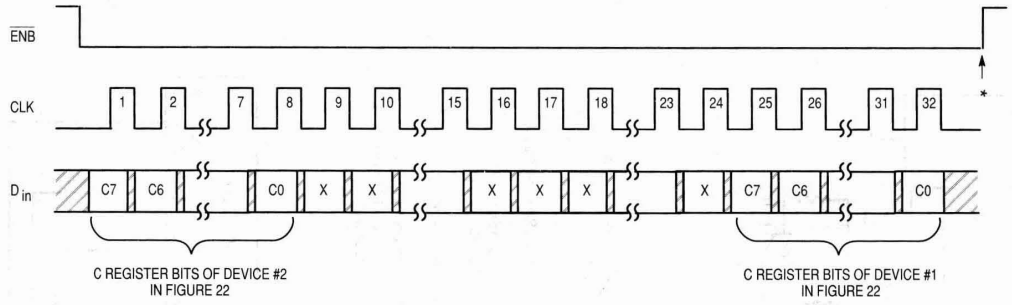


Figure 23. Accessing the C Registers of Two Cascaded MC145202 Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

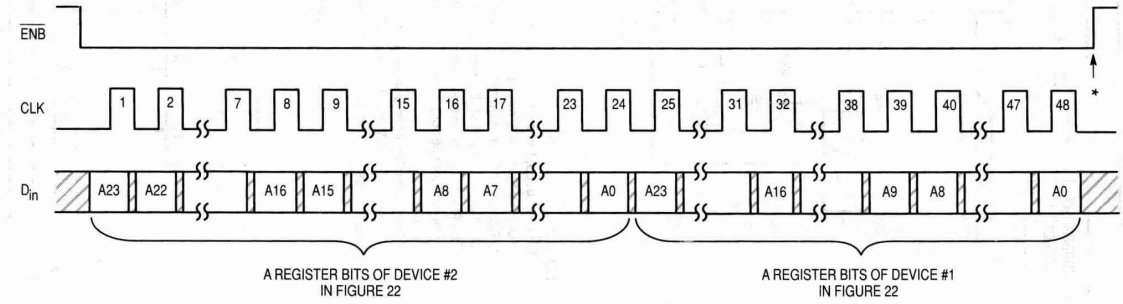


Figure 24. Accessing the A Registers of Two Cascaded MC145202 Devices

* At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counter can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

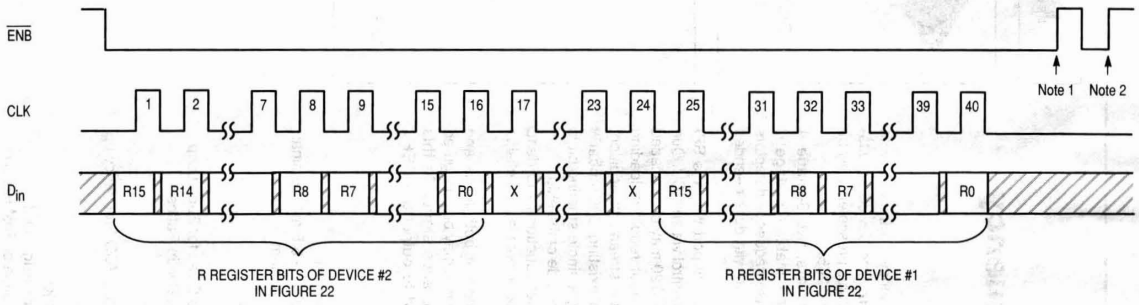


Figure 25. Accessing the R Registers of Two Cascaded MC145202 Devices

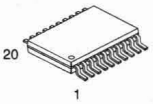
NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14 and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therfore, the R counter divide is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. Optional load pulse. At this point, the bits R0 through R12 are transfered to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{\text{ENB}}$ pulse, as shown. The C and A registers are not affected. The first buffer of the R register is not affected. Also, see note of Figure 24 for an alternate method of loading the second buffer in the R register.

MC145220

Dual 1.1 GHz PLL Frequency Synthesizer
BiCMOS

F SUFFIX
SOG PACKAGE
CASE 803C

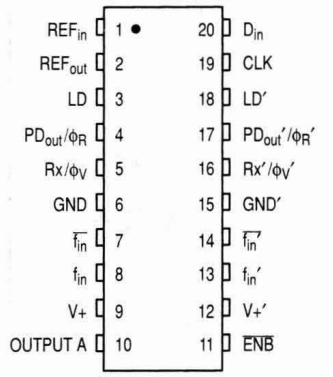


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145220F	SOG Package
MC145220DT	TSSOP

PIN ASSIGNMENT



The MC145220 is a low–voltage, single–chip frequency synthesizer with serial interface capable of direct usage up to 1.1 GHz. The device simultaneously supports two loops. The two on–chip dual–modulus prescalers may be independently programmed to divide by either 32/33 or 64/65.

The device consists of two dual–modulus prescalers, two 6–stage A counters, two 12–stage N counters, two fully programmable 13–stage R (reference) counters, and two lock detectors. Four phase/frequency detectors are included: two with current source/sink outputs and two with double–ended outputs.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte–oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145220 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or multiple address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals. Because this device is a dual synthesizer, a single steering bit is used in the serial data stream to direct the data to either side of the chip.

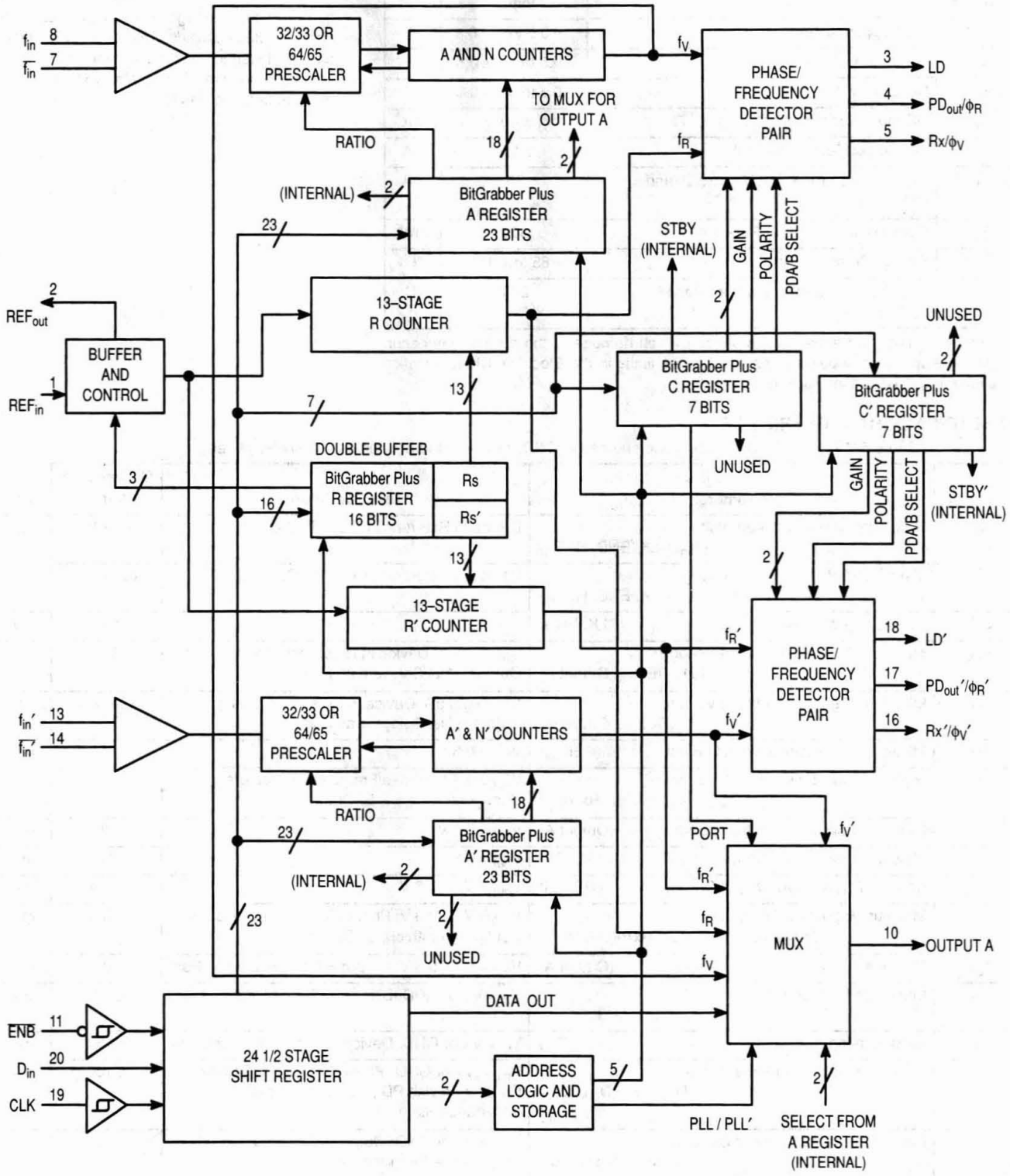
The phase/frequency detectors have linear transfer functions (no dead zones). The current delivered by the current source/sink outputs is controllable via the serial port.

Also featured are low–power standby for either one or both loops and on–board support of an external crystal. In addition, the part may be configured such that the REF_{in} pin accepts an external reference signal. In this configuration, the REF_{out} pin may be programmed to output the REF_{in} frequency divided by 1, 2, 4, 8, or 16.

- Operating Frequency: 40 to 1100 MHz
- Operating Supply Voltage Range: 2.7 to 5.5 V
- Supply Current: Both PLLs Operating — 12 mA Nominal
  One PLL Operating, One on Standby — 6.5 mA Nominal
  Both PLLs on Standby — 30 μA Maximum
- Phase Detector Output Current: Up to 2 mA @ 5 V
  Up to 1 mA @ 3 V
- Operating Temperature Range: – 40 to 85°C
- Independent R Counters Allow Use of Different Step Sizes for Each Loop
- Double–Buffered R Register — Reference and Loop Divide Ratios Updated Simultaneously
- R Counter Division Range: 1 and 10 to 8,191
- Dual–Modulus Capability Provides Total Division of the VCO Frequency up to 262,143
- Direct Interface to Motorola SPI Data Port
- Evaluation Kit Available (Part Number MC145220EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

NOTE: This product has been evaluated for operation over a wider range than 40 MHz to 1.1 GHz. If your design requires a wider frequency range, contact your local Motorola representative for further information.

BLOCK DIAGRAM



PIN 9 = V+ (Positive Power to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 6 = GND (Ground to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 12 = V+′ (Positive Power to PLL′ and a portion of the Serial Port)
PIN 15 = GND′ (Ground to PLL′ and a portion of the Serial Port)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V+, V+′	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V+ + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V+ + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I	DC Supply Current, V+, V+′, GND, and GND′ Pins	30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, Voltages Referenced to GND, T_A = – 40 to 85°C, unless otherwise stated)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.3 x V+	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.7 x V+	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		100	mV
V_{OL}	Maximum Low–Level Output Voltage (LD, LD', REF_{out}, Output A)	I_{out} = 20 µA, Device in Reference Mode; Output A Not Selected as Port	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, Output A)	I_{out} = – 20 µA, Device in Reference Mode; Output A Not Selected as Port	V+ – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out})	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx'/ϕ_V')	V_{out} = 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	0.5	mA
I_{OL}	Minimum Low–Level Output Current (Output A)	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (LD, LD')	V_{out} = 0.3 V	0.5	mA
I_{OH}	Minimum High–Level Output Current (REF_{out})	V_{out} = V+ – 0.3 V	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx'/ϕ_V')	V_{out} = V+ – 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (Output A)	V_{out} = V+ – 0.3 V; Output A Not Selected as Port	– 0.4	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V+ or GND; Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V+ or GND; Device in Reference Mode	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R')	V_{out} = V+ or GND; Phase/Frequency Detectors Configured with PD_{out} Output, Output in High–Impedance State	± 150	nA
I_{OZ}	Maximum Output Leakage Current (Output A, LD, LD′)	V_{out} = V+ or GND; Output A Selected as Port; Output in High–Impedance State	± 5	µA
I_{STBY}	Maximum Standby Supply Current	V_{in} = V+ or GND; Outputs Open; Both PLLs in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode	30	µA
I_T	Total Operating Supply Current	$f_{in} = f_{in}'$ = 1.1 GHz; both loops active; REF_{in} = 13 MHz @ 1 V p–p; Output A = Inactive; All Outputs = No Connect; D_{in}, $\overline{ENB}$, CLK = V+ or GND; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	*	mA

* The nominal value is 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUTS — PD_{out}/ϕ_R AND PD_{out}'/ϕ_R'

(Phase/Frequency Detectors Configured with PD_{out} Outputs, $I_{out} \leq 2$ mA @V+ = V+′ = 4.5 to 5.5 V, $I_{out} \leq 1$ mA @V+ = V+′ = 2.7 to 4.4 V, GND = GND′, Voltages Referenced to GND)

Parameter		Test Condition	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part	(Notes 3 and 4)	V_{out} = 0.5 x V+	± 20	%
Maximum Sink–versus–Source Mismatch	(Note 3)	V_{out} = 0.5 x V+	12	%
Output Voltage Range	(Note 3)	I_{out} variation ≤ 20%	0.5 to V+ – 0.5 V	V

NOTES:

5. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
6. See Rx Pin Description for external resistor values.
7. This parameter is guaranteed for a given temperature within – 40 to 85°C and given supply voltage within 2.7 to 5.5 V.
8. Applicable for the Rx/ϕ_V or Rx'/ϕ_V' reference pin tied to the GND or GND′ pin through a resistor. See Pin Descriptions for suggested resistor values.

AC INTERFACE CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, C_L = 25 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter		Guaranteed Limit	Unit
f_{clk}	Serial Data CLK Frequency NOTE: Refer to Clock t_w below	(Figure 1)	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to Output A (Selected as Data Out)	(Figures 1 and 5)	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to Output A (Selected as Port)	(Figures 2 and 6)	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Output A; t_{THL} only, on Output A when Selected as Port	(Figures 1, 5, and 6)	200	ns
C_{in}	Maximum Input Capacitance — D_{in}, CLK, $\overline{ENB}$		10	pF

TIMING REQUIREMENTS (V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter		Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} versus CLK	(Figure 3)	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ versus CLK	(Figure 4)	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	(Figure 4)	*	cycles
t_w	Minimum Pulse Width, CLK	(Figure 1)	250	ns
t_r, t_f	Maximum Input Rise and Fall Times — CLK	(Figure 1)	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} or f_{in}' cycles with selection of a 64/65 prescale ratio or 99 f_{in} or f_{in}' cycles with selection of a 32/33 prescale ratio, whichever is greater.

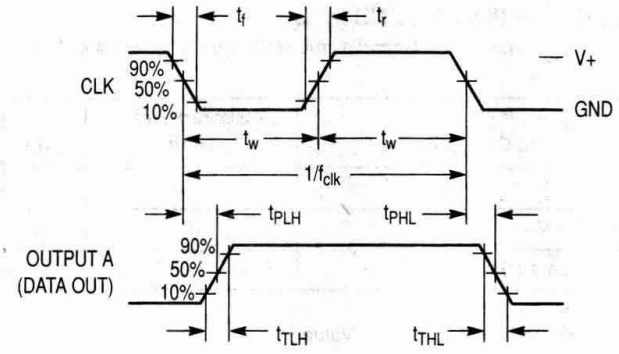


Figure 1.

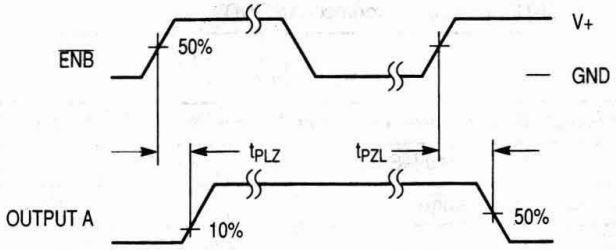


Figure 2.

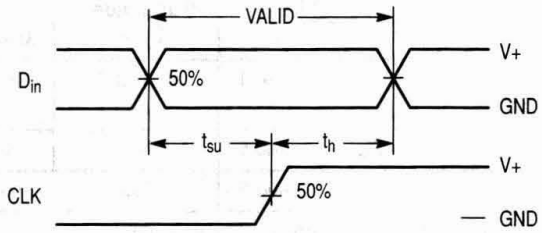


Figure 3.

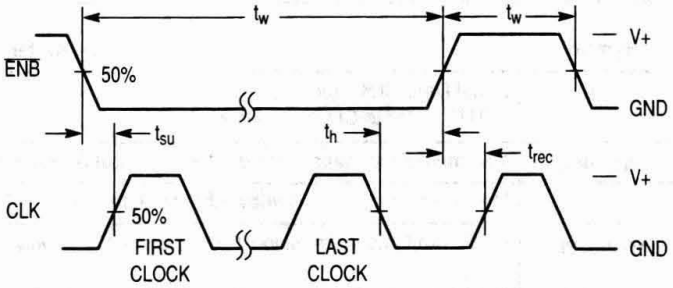
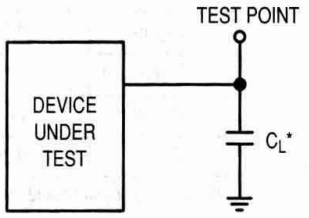
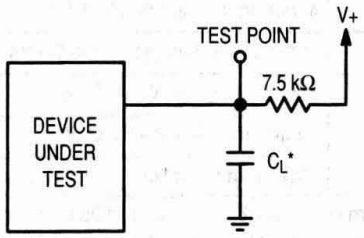


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5.



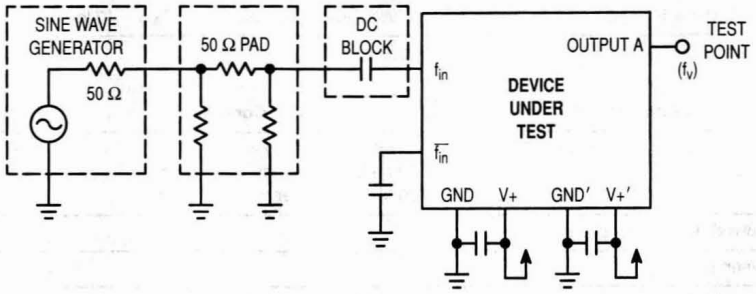
* Includes all probe and fixture capacitance.

Figure 6.

LOOP SPECIFICATIONS (V+ = V+′ = 2.7 to 5.5 V unless otherwise indicated, GND = GND′, T_A = – 40 to 85°C)

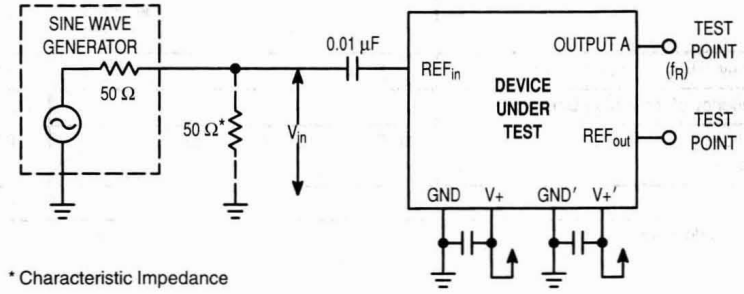
Symbol	Parameter	Test Condition	Guaranteed Operating Range		Unit
			Min	Max	
P_{in}	Input Sensitivity Range, f_{in} or f_{in}' (Figure 7)	40 MHz ≤ frequency < 300 MHz 300 MHz ≤ frequency < 700 MHz 700 MHz ≤ frequency < 1100 MHz	– 2 – 5 – 16	8 6 4	dBm*
ΔP_{in}	Difference Allowed Between f_{in} and f_{in}'			10	dB
—	Isolation Between f_{in} and f_{in}'		15		dB
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode (Figure 8)	V_{in} ≥ 400 mV p–p, R Counter set to divide ratio such that f_R ≤ 1 MHz, REF Counter set to divide ratio such that REF_{out} ≤ 5 MHz	4	27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance; R Counter and REF Counter same as above V+ = 2.7 V V+ = 3.5 V V+ = 4.5 V V+ = 5.5 V	 2 2 2 2	 10 13 15 15	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 25 pF	dc	5	MHz
f	Operating Frequency of the Phase Detectors		dc	1	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, ϕ_R', ϕ_V' (Figures 11 and 12)	f_R in Phase with f_V, C_L = 25 pF	16	125	ns
C_{in}	Input Capacitance, REF_{in}		—	5	pF

* Power level at the input to the dc block.



NOTE: Alternately, the 50 Ω pad may be a T network.

Figure 7. Test Circuit



* Characteristic Impedance

Figure 8. Test Circuit — Reference Mode

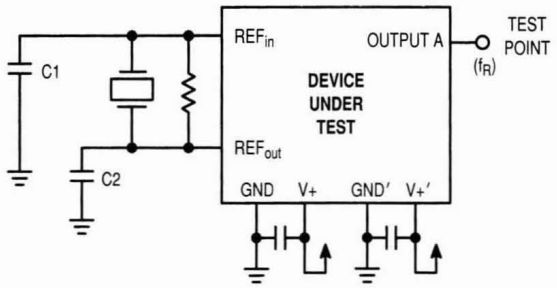


Figure 9. Test Circuit — Crystal Mode

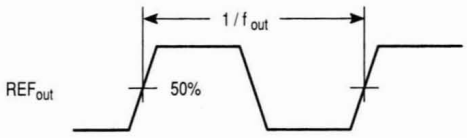


Figure 10. Switching Waveform

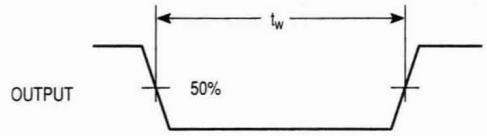
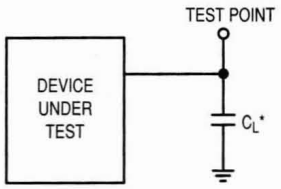
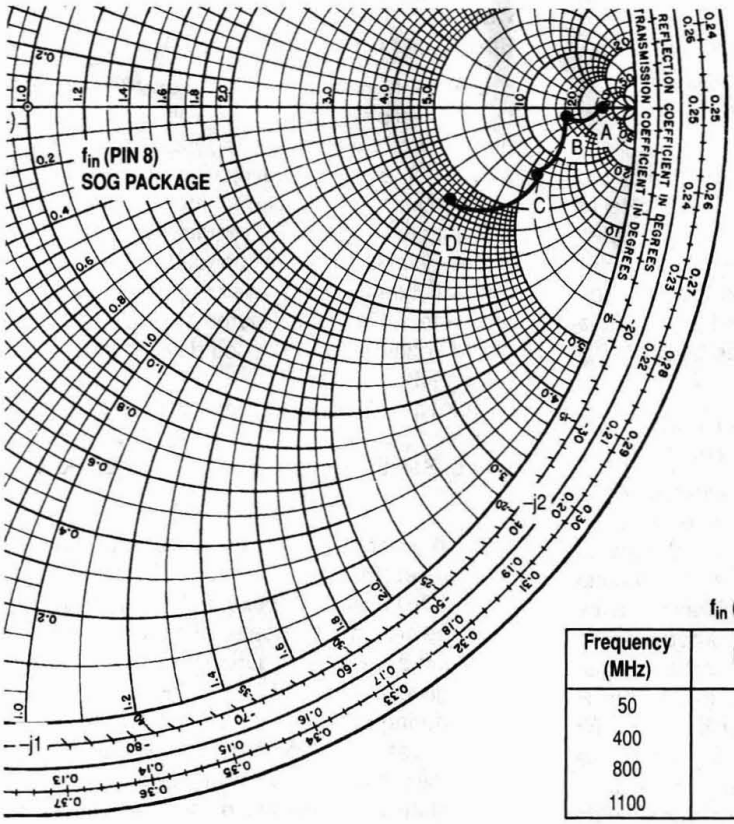


Figure 11. Switching Waveform



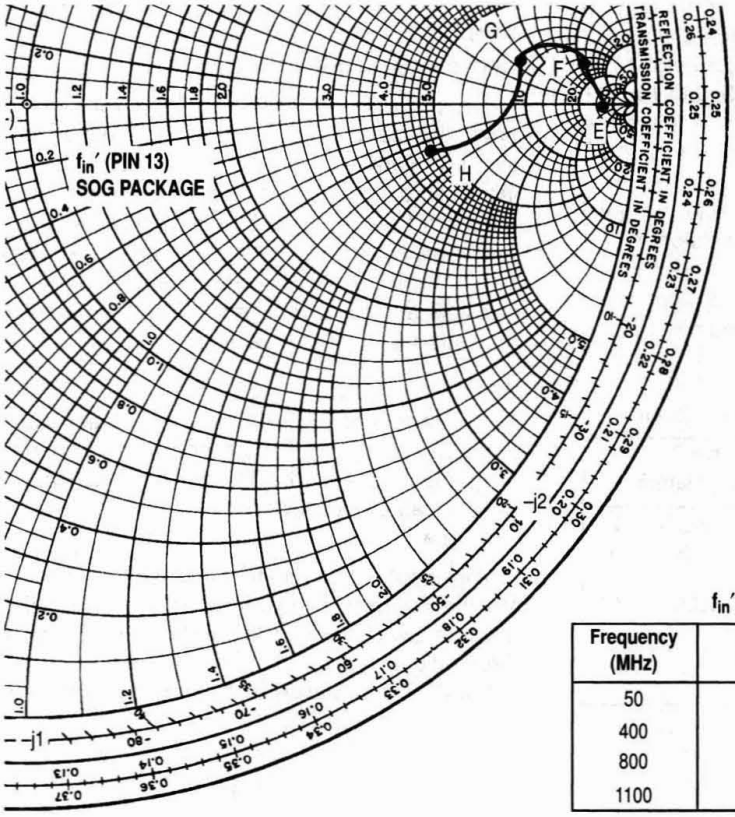
* Includes all probe and fixture capacitance.

Figure 12. Test Circuit



f_{in} (PIN 8) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	A	1900 – j 157	1970 – j 102
400	B	1440 – j 228	1510 + j 19
800	C	552 – j 380	671 – j 334
1100	D	196 – j 141	223 – j 147



f_{in}' (PIN 13) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	E	1900 + j 149	1930 + j 214
400	F	878 + j 703	746 + j 741
800	G	705 + j 208	626 + j 327
1100	H	215 – j 69.3	243 – j 61.3

Figure 13. Nominal Input Impedance of f_{in} and f_{in}' — Series Format (R + jX) (50 – 1100 MHz)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 20)

The bit stream begins with the MSB and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration registers, 2 bytes (16 bits) to access the first buffer of the R registers, or 3 bytes (24 bits) to access the A registers (see Table 1). The values in the registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

NOTE

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 LSBs of the R registers are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The two second buffers of the R register contain the two 13–bit divide ratios for the R counters. These second buffers are loaded with the contents of the first buffer as follows. Whenever the A register is loaded, the Rs (second) buffer is loaded from the R (first) buffer. Similarly, whenever the A′ register is loaded, the Rs′ (second) buffer is updated from the R (first) buffer. This allows presenting new values to the R, A, and N counters simultaneously. Note that two different R counter divide ratios may be established: one for the main PLL and another for PLL′.

The bit stream does not need address bits due to the innovative BitGrabber Plus registers. A steering bit is used to direct data to either the main PLL or PLL′ section of the chip. Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 14, 15, and 16.

D_{in} typically switches near 50% of V+ to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Registers	C7, C6, C5, . . ., C0
16	R Register, First Buffer	R15, R14, R13, . . ., R0
24	A Registers	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 24 to 27	

CLK
Serial Data Clock Input (Pin 19)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from Output A (when configured as Data Out, see Pin 10). The 24–1/2 stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C registers. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A registers. See Table 1 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 25 through 27.

CLK typically switches near 50% of V+ and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. Floating, toggling, or having these pins in the wrong state during power–up does not harm the chip, but causes two potentially undesirable effects. First, the outputs of the device power up in an unknown state. Second, if two devices are cascaded, the A Registers must be written twice after power up. After these two accesses, the two cascaded chips perform normally.

$\overline{ENB}$
Active–Low Enable Input (Pin 11)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{ENB}$ is high and CLK is low.

This input is Schmitt–triggered and switches near 50% of V+, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 10)

Output A is selectable as f_R, f_V, f_R', f_V', Data Out, or Port. Bits A21 and A22 and the steering bit (A23) control the selection; see Figure 15. When selected as Port, the pin becomes an open–drain N–channel MOSFET output. As such, a pullup device is needed for pin 10. With all other selections, the pin is a totem–pole (push–pull) output.

If A22 = A21 = high, Output A is configured as f_R when the steering bit is low and f_R' when the bit is high. These signals are the buffered outputs of the 13–stage R counters. The signals appear as normally low and pulse high. The signals can be used to verify the divide ratios of the R counters. These ratios extend from 10 to 8191 and are determined by the binary value loaded into bits R0 – R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of one. See Figure 16. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R and f_R' should not exceed 1 MHz.

If A22 = high and A21 = low, Output A is configured as f_V when the steering bit is low and f_V' when the bit is high. These signals are the buffered outputs of the 12–stage N counters. The signals appear as normally low and pulse high. The signals can be used to verify the operation of the prescalers, A counters, and N counters. The divide ratio between the f_{in} or f_{in}' input and the f_V or f_V' signal is N x P + A. N is the divide ratio of the N counter, P is 32 with a 32/33 prescale ratio or 64 with a 64/65 prescale ratio, and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A registers. See Figure 15. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V and f_V' should not exceed 1 MHz.

If A22 = low and A21 = high, Output A is configured as Data Out. This signal is the serial output of the 24–1/2 stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, Output A is automatically configured as Data Out to facilitate cascading devices.

If A22 = A21 = low, Output A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high impedance when the Port bit is high. See Figure 14.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Oscillator Input and Output (Pins 1 and 2)

Configurable Pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In the crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the crystal are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C or C′ register, the oscillator runs, but the R or R′ counter is stopped, respectively. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode shown in Figure 16, and can be engaged whether in standby or not.

In the reference mode, REF_{in} (pin 1) accepts a signal from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. The ac–coupled signal must be at least 400 mV p–p. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for large output swings (V_{OH} to V_{OL}) and 25 pF loads. Therefore, for REF_{in} frequencies above 5 MHz, the one–to–one ratio may not be used for these large signal swing and large C_L requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in}, $\overline{f_{in}}$ and f_{in}', $\overline{f_{in}'}$
Frequency Inputs (Pins 8, 7 and 13, 14)

These pins feed the onboard RF amplifiers which drive the prescalers. These inputs may be fed differentially. However, they usually are used in single–ended configurations (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ac ground (via capacitor). The signal sources driving these pins originate from external VCOs.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the **Loop Specifications** table.

PD_{out}/ϕ_R, PD_{out}'/ϕ_R'
Single–Ended Phase/Frequency Detector Outputs (Pins 4 and 17)

When the C2 bits in the C or C′ registers are low, these pins are independently configured as single–ended outputs PD_{out} or PD_{out}', respectively. As such, each pin is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

These outputs can be enabled, disabled, and inverted via the C and C′ registers. If desired, these pins can be forced to the floating state by utilization of the standby feature in the C or C′ registers (bit C6). This is a patented feature.

The phase detector gain is controllable by bits C4 and C5: gain (in amps per radian) = PD_{out} current in amps divided by 2π.

PD_{out}/ϕ_R, Rx/ϕ_V and PD_{out}'/ϕ_R', Rx'/ϕ_V'
Double–Ended Phase/Frequency Detector Outputs (Pins 4, 5 and 17, 16)

When the C2 bits in the C or C′ registers are high, these two pairs of pins are independently configured as double–ended outputs ϕ_R, ϕ_V or ϕ_R', ϕ_V', respectively. As such, these outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detectors are described below and are shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, or interchanged via C register bits C6 or C0. This is a patented feature. Note that when disabled in standby, these outputs are forced to their rest condition (high state). See Figure 14.

The ϕ_R and ϕ_V output signals swing from approximately GND to V+.

LD and LD′
Lock Detector Outputs (Pins 3 and 18)

Each output is essentially at a high–impedance state with very narrow low–going pulses of a few nanoseconds when the respective loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V, while LD′ is the logical ANDing of ϕ_R' and ϕ_V'. See Figure 17.

Upon power up, on–chip initialization circuitry forces LD and LD′ to the high–impedance state. These pins are low during standby. If unused, LD should be tied to GND and LD′ should be tied to GND′.

These outputs have open–drain N–channel MOSFET drivers. This facilitates a wired–OR function. See Figure 21.

Rx/ϕ_V and Rx'/ϕ_V'
External Current Setting Resistors (Pins 5 and 16)

When the C2 bits in the C or C′ registers are low, these two pins are independently configured as current setting pins Rx or Rx′, respectively. As such, resistors tied between each of these pins and GND and GND′, in conjunction with bits C4 and C5 in the C and C′ registers, determine the amount of current that the PD_{out} pins sink and source. When bits C4 and C5 are both set high, the maximum current is obtained; see Table 2 for other values of current.

Table 2. PD_{out} or PD_{out}' Current

C5	C4	Current
0	0	5%
0	1	50%
1	0	80%
1	1	100%

The formula for determining the value of Rx or Rx′ is as follows.

$$Rx = \frac{V1 - V2}{I}$$

where Rx is the value of external resistor in ohms, V1 is the supply voltage, V2 is 1.5 V for a reference current through Rx of 100 μA or 1.745 V for a reference current of 200 μA, and I is the reference current flowing through Rx or Rx′.

The reference current flowing through Rx or Rx′ is multiplied by a factor of approximately 10 (in the 100% current mode) and delivered by the PD_{out} or PD_{out}' pin, respectively. To achieve a maximum phase detector output current of 1 mA, the resistor should be about 15 kΩ when a 3 V supply is employed. See Table 3.

Table 3. Rx Values

Supply Voltage	Rx	PD_{out} or PD_{out}' Current in 100% Mode
3 V	15 kΩ	1 mA
5 V	16 kΩ	2 mA

Do not use a decoupling capacitor on the Rx or Rx′ pin. Use of a capacitor causes undesirable current spikes to appear on the phase detector output when invoking the standby mode.

POWER SUPPLY PINS

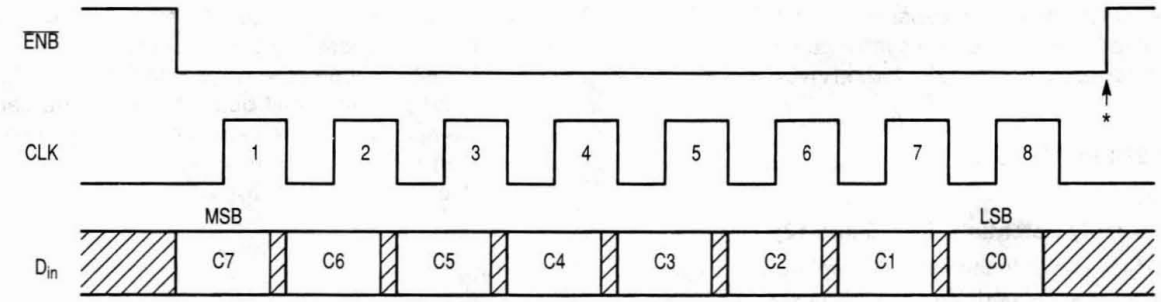
V+ and V+′
Positive Supply Potentials (Pins 9 and 12)

V+ supplies power to the main PLL, reference circuit, and a portion of the serial port. V+′ supplies power to PLL′ and a portion of the serial port. Both V+ and V+′ must be at the same voltage level and may range from 2.7 V to 5.5 V with respect to the GND and GND′ pins.

For optimum performance, V+ should be bypassed to GND and V+′ bypassed to GND′ using separate low–inductance capacitors mounted very close to the MC145220. Lead lengths and printed circuit board traces to the capacitors should be minimized. (The very fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

GND and GND′
Grounds (Pins 6 and 15)

The GND pin is the ground for the main PLL and GND′ is the ground for PLL′.



* At this point, the new byte is transferred to the C or C′ register and stored. No other registers are affected.

C7 – Steer: Used to direct the data to either the C or C′ register. A low level directs data to the C register; a high level is for the C′ register.

C6 – Standby: When set high, places both the main PLL and PLL′ (when C6 is set in the C register) or PLL′ only (when C6 is set in the C′ register) in the standby mode for reduced power consumption. The associated PD_{out} is forced to the floating state, the associated counters (A, N, and R) are inhibited from counting, the associated Rx current is shut off, and the associated prescaler stops counting and is placed in a low current mode. The associated double–ended phase/frequency detector outputs are forced to a high level. In standby, the associated LD output is placed in the low–state, thus indicating "not locked" (open loop). During standby, data is retained in all registers and any register may be accessed.

In standby, the condition of the REF/OSC circuitry is determined by bits R13, R14, and R15 in the R register per Figure 16. However, if REF_{out} = *static low* is selected, the internal feedback resistor is disconnected and the REF_{in} is inhibited when both PLL and PLL′ are placed in standby via the C register. Thus, the REF_{in} only presents a capacitive load. **Note**: PLL/PLL′ standby does not affect the other modes of the REF/OSC circuitry as determined by bits R13, R14, and R15 in the R register. The PLL′ standby mode (controlled from the C′ register) has no effect on the REF/OSC circuit.

When C6 is reset low, the associated PLL (or PLLs) is (are) taken out of standby in two steps. First, the REF_{in} (only in 1 mode, PLL/PLL′ in standby) resistor is reconnected, REF_{in} (only 1 mode) is gated on, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detectors. Second, when the appropriate f_R pulse occurs, the A and N counters are jam loaded, the prescaler is gated on, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C5, C4 – I2, I1: Independently controls the PD_{out} or PD_{out}' source/sink current per Table 2. With both bits high, the maximum current (as set by Rx or Rx′) is available. POR forces C5 and C4 to high levels.

C3 – Spare: Unused

C2 – PDA/B: Independently selects which phase/frequency detector is to be used. When set high, the double–ended detector is selected with outputs ϕ_R and ϕ_V or ϕ_R' and ϕ_V'. When reset low, the current source/sink detector is selected with outputs PD_{out} or PD_{out}'. In the second case, the appropriate Rx or Rx′ pin is tied to an external resistor. POR forces C2 low.

C1 – Port: When the Output A pin is selected as "Port" via bits A22 and A21, C1 of the C register determines the state of Output A. When C1 is set high, Output A is forced to the high–impedance state; C1 low forces Output A low. The Port bit is not affected by the standby mode. **Note**: C1 of the C′ register is not used in any mode.

C0 – POL: Selects the output polarity of the associated phase/frequency detectors. When set high, this bit inverts the associated current source/sink output and interchanges the associated double–ended output relative to the waveforms in Figure 17. Also, see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

Figure 14. C and C′ Register Accesses and Format (8 Clock Cycles are Used)

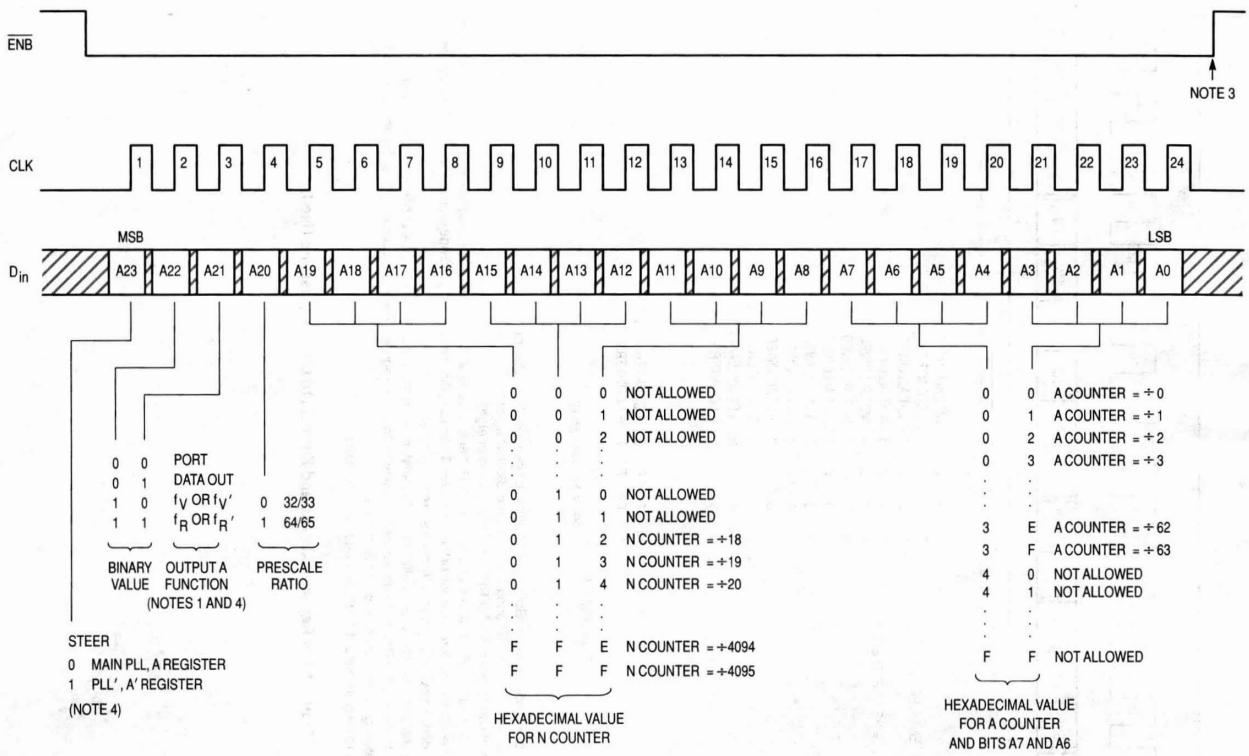
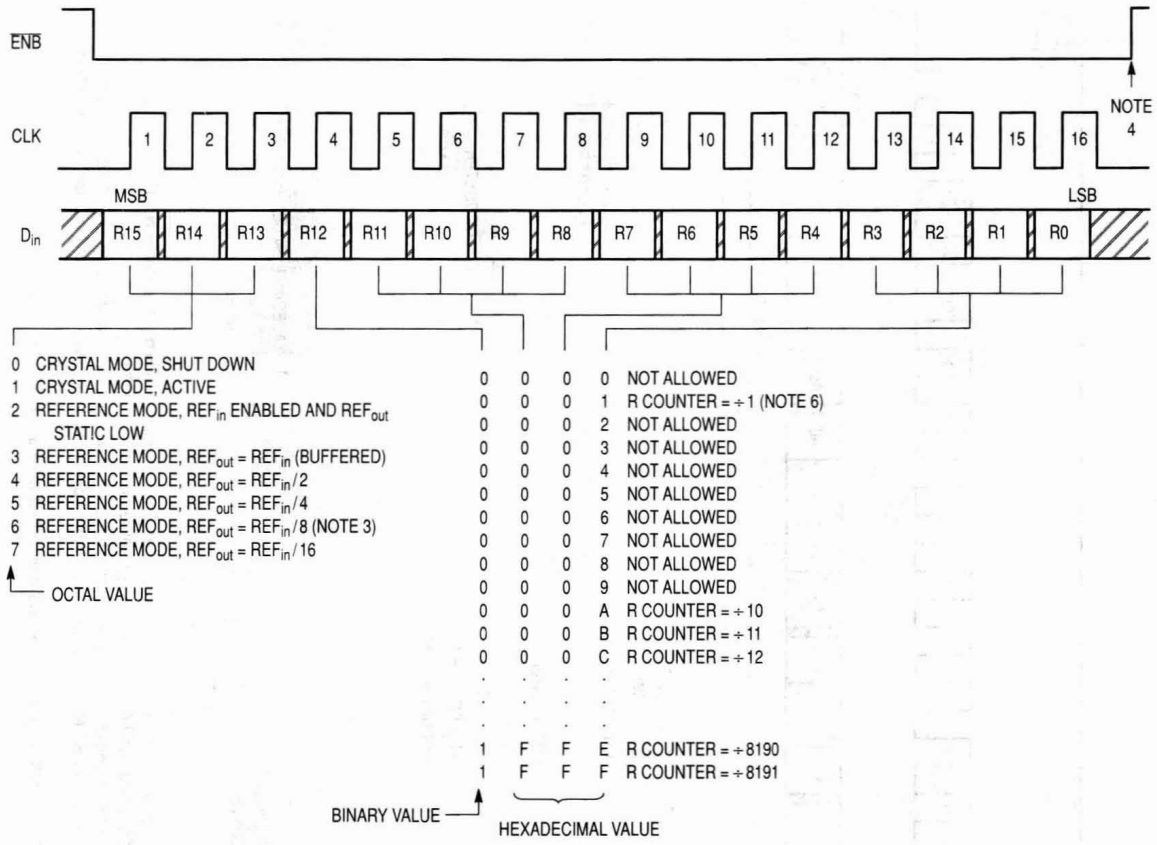

ENB
NOTE 3
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
MSB
LSB
Din
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 0 PORT DATA OUT
0 1 fV OR fV'
1 0 fR OR fR'
1 1
BINARY VALUE
OUTPUT A FUNCTION (NOTES 1 AND 4)
0 32/33
1 64/65
PRESCALE RATIO
STEER
0 MAIN PLL, A REGISTER
1 PLL', A' REGISTER
(NOTE 4)
0 0 0 NOT ALLOWED
0 0 1 NOT ALLOWED
0 0 2 NOT ALLOWED
0 1 0 NOT ALLOWED
0 1 1 NOT ALLOWED
0 1 2 N COUNTER = ÷18
0 1 3 N COUNTER = ÷19
0 1 4 N COUNTER = ÷20
F F E N COUNTER = ÷4094
F F F N COUNTER = ÷4095
HEXADECIMAL VALUE FOR N COUNTER
0 0 A COUNTER = ÷0
0 1 A COUNTER = ÷1
0 2 A COUNTER = ÷2
0 3 A COUNTER = ÷3
3 E A COUNTER = ÷62
3 F A COUNTER = ÷63
4 0 NOT ALLOWED
4 1 NOT ALLOWED
F F NOT ALLOWED
HEXADECIMAL VALUE FOR A COUNTER AND BITS A7 AND A6

Figure 15. A and A′ Register Accesses and Format (24 Clock Cycles are Used)

NOTES:

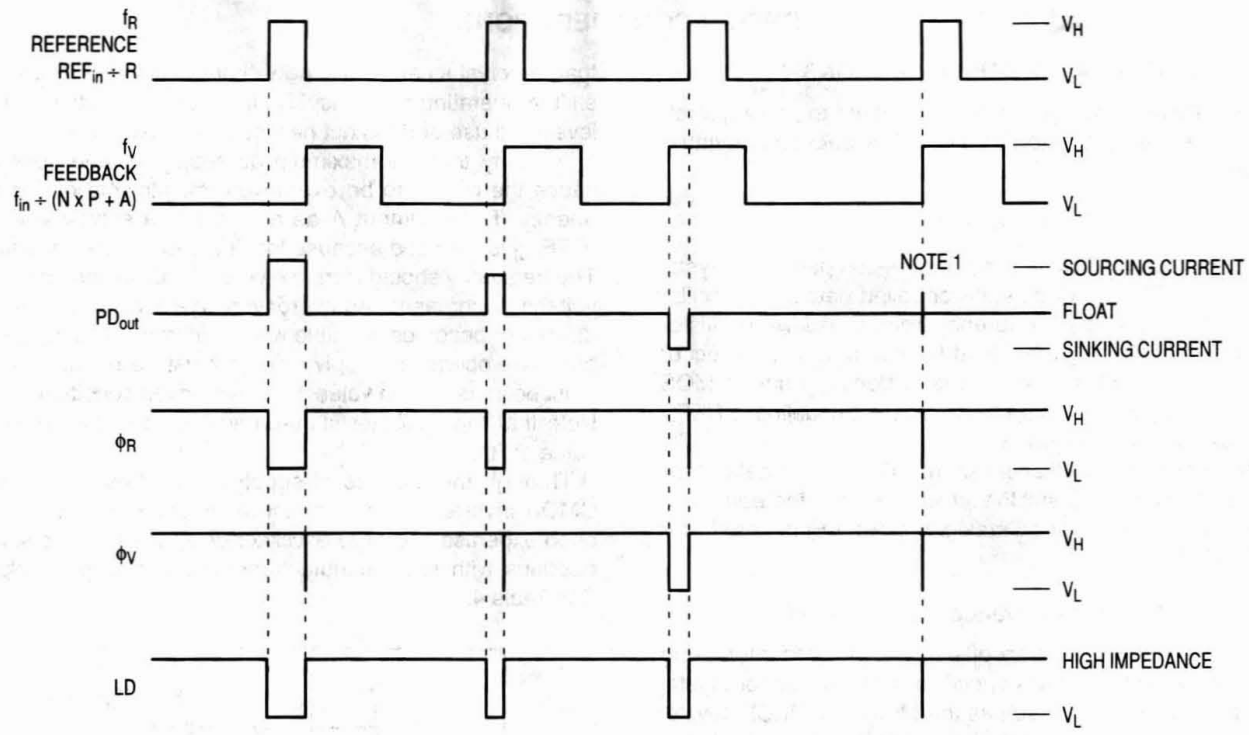
1. A power-on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x P + A where N is the value programmed for the N counter, P is 32 if bit A20 is low or 64 if A20 is high, and A is the value programmed for the A counter.
3. At this point, the three new bytes are transferred to the A register if bit A23 is a "0" or A′ register if A23 is a "1". In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's relative second buffer, Rs or Rs′. Thus, the R, N, and A (or R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C or C′ registers are not affected.
4. A "0" for the Steering bit allows selection of f_R, f_V, Data Out, or Port by bits A21 and A22. A "1" for the Steering bit allows selection of f_R', f_V', Data Out, or Port.


ENB
NOTE 4
CLK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
MSB
LSB
D_{in}
R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0
0 CRYSTAL MODE, SHUT DOWN
1 CRYSTAL MODE, ACTIVE
2 REFERENCE MODE, REF_{in} ENABLED AND REF_{out} STATIC LOW
3 REFERENCE MODE, $REF_{out} = REF_{in}$ (BUFFERED)
4 REFERENCE MODE, $REF_{out} = REF_{in}/2$
5 REFERENCE MODE, $REF_{out} = REF_{in}/4$
6 REFERENCE MODE, $REF_{out} = REF_{in}/8$ (NOTE 3)
7 REFERENCE MODE, $REF_{out} = REF_{in}/16$
OCTAL VALUE
0 0 0 0 NOT ALLOWED
0 0 0 1 R COUNTER = ÷1 (NOTE 6)
0 0 0 2 NOT ALLOWED
0 0 0 3 NOT ALLOWED
0 0 0 4 NOT ALLOWED
0 0 0 5 NOT ALLOWED
0 0 0 6 NOT ALLOWED
0 0 0 7 NOT ALLOWED
0 0 0 8 NOT ALLOWED
0 0 0 9 NOT ALLOWED
0 0 0 A R COUNTER = ÷10
0 0 0 B R COUNTER = ÷11
0 0 0 C R COUNTER = ÷12
1 F F E R COUNTER = ÷8190
1 F F F R COUNTER = ÷8191
BINARY VALUE
HEXADECIMAL VALUE

NOTES:

1. Bits R15 – R13 control the configurable "Buffer and Control" block (see Block Diagram).
2. Bits R12 – R0 control the "13–stage R counter" blocks (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "Buffer and Control" block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R or R′ counter divide ratio is not altered yet and retains the previous ratio loaded. The C, C′, A, and A′ registers are not affected.
5. Bits R0 – R12 are transferred to the second buffer of the R register (Rs in the Block Diagram) on a subsequent 24–bit write to the A register. The bits are transferred to Rs′ on a subsequent 24–bit write to the A′ register. The respective R counter begins dividing by the new ratio after completing the rest of its present count cycle.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles are Used)



NOTES:

1. At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
2. The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is mostly in a floating condition and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.
3. V_H = High voltage level, V_L = Low voltage level.
4. The waveforms are applicable to both the main PLL and PLL′.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} must be used. See Figure 8.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 20 pF when used near the highest operating frequency of the MC145220. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

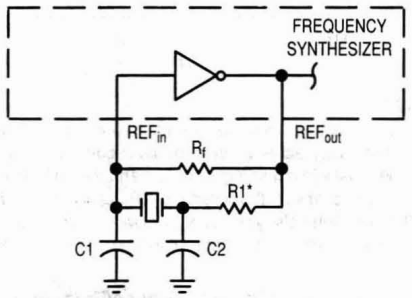
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making either a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at Output A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. Note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 4.



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

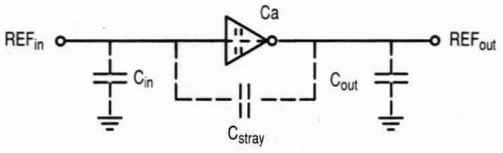
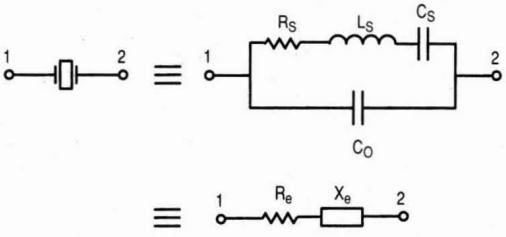


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

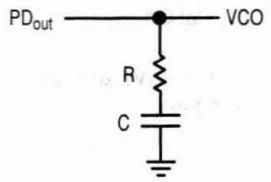
Table 4. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

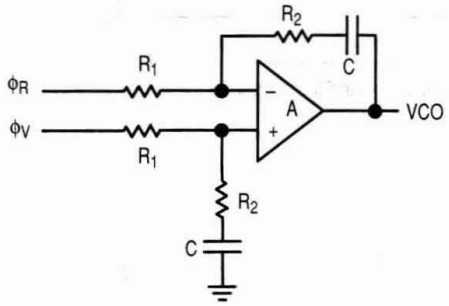
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$Z(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V+/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

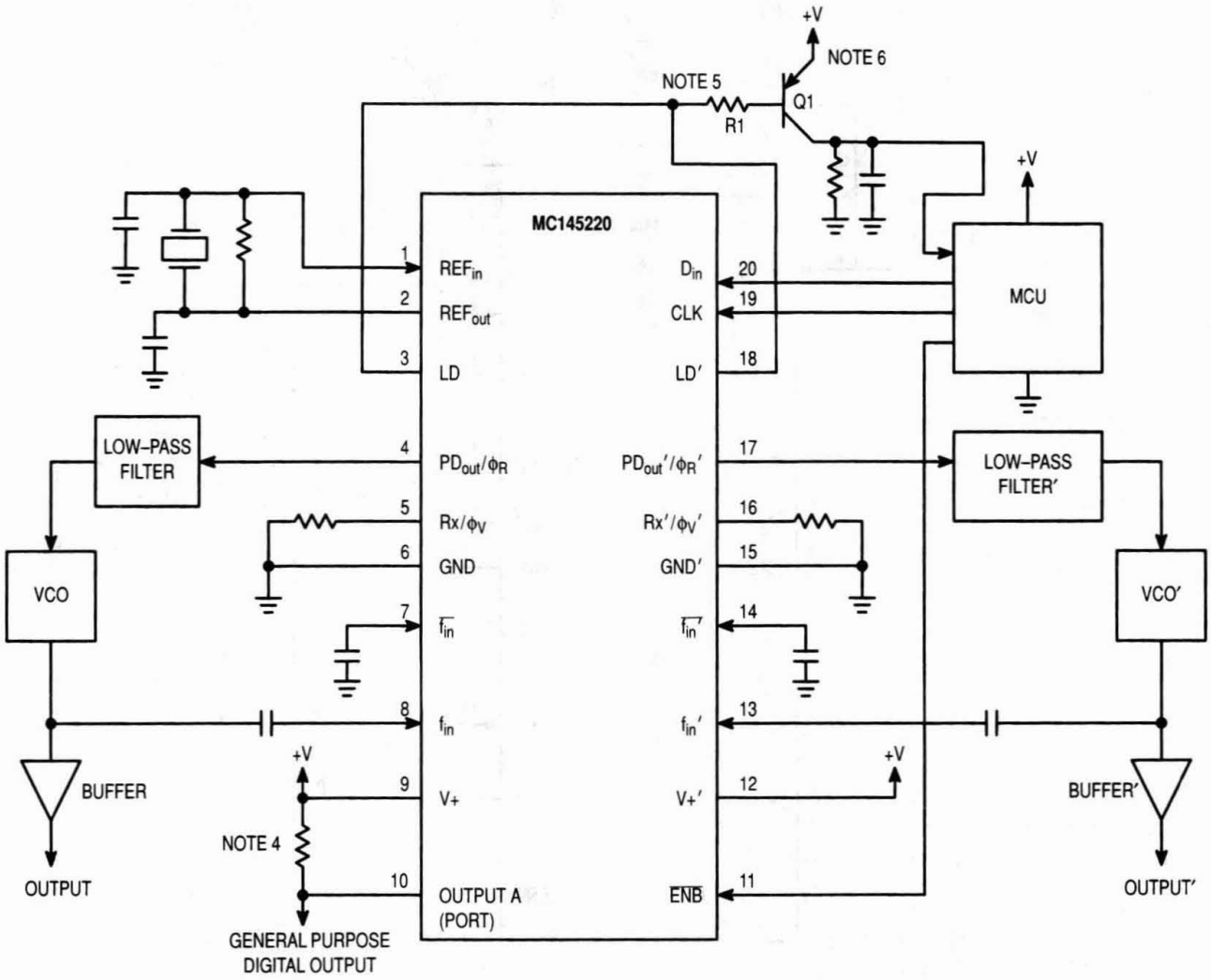
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

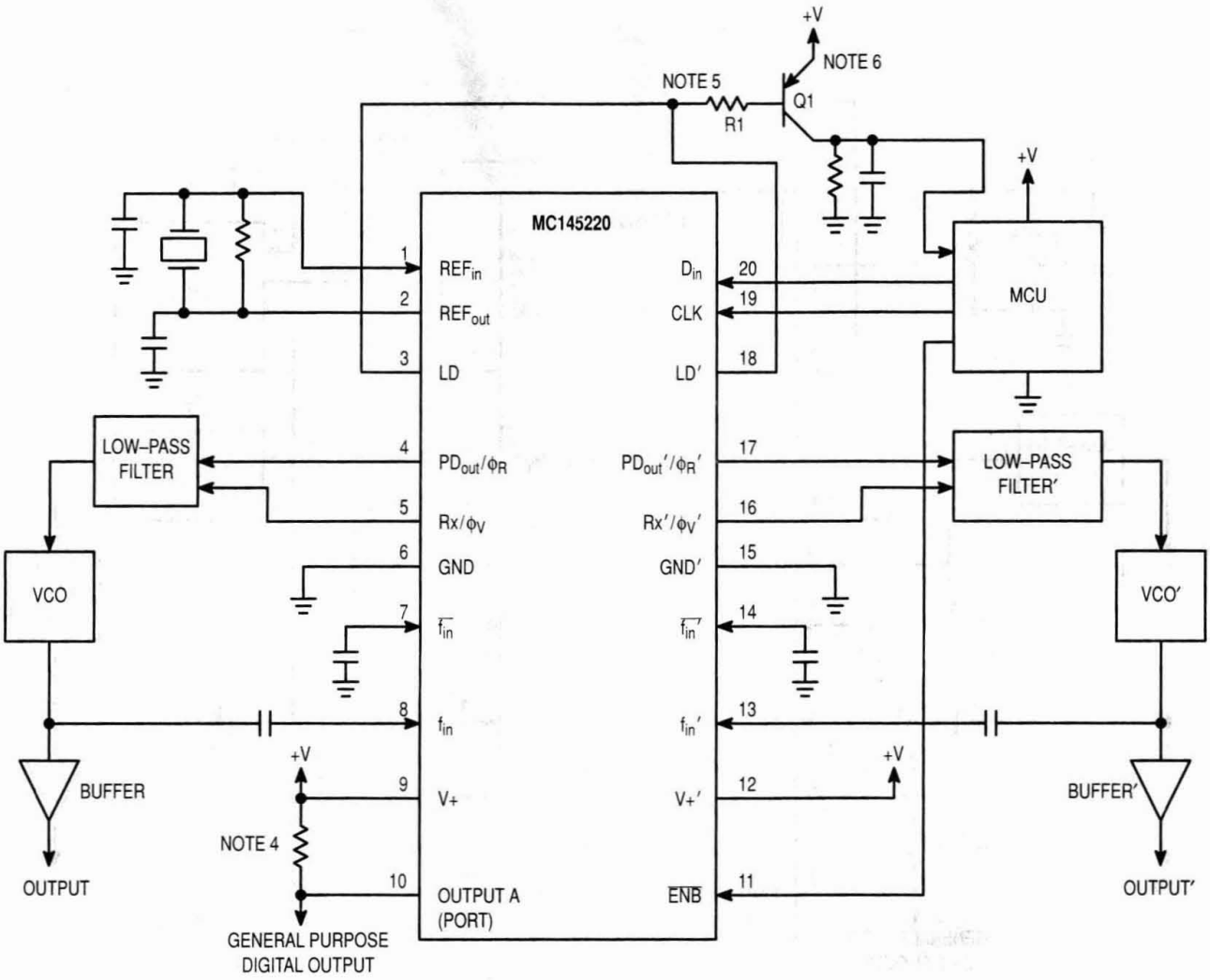
AN1253, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. The PD_{out} output is fed to an external loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R', f_V, f_V', DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the "pull–up device".
6. Use of Q1 is optional and depends on loading.

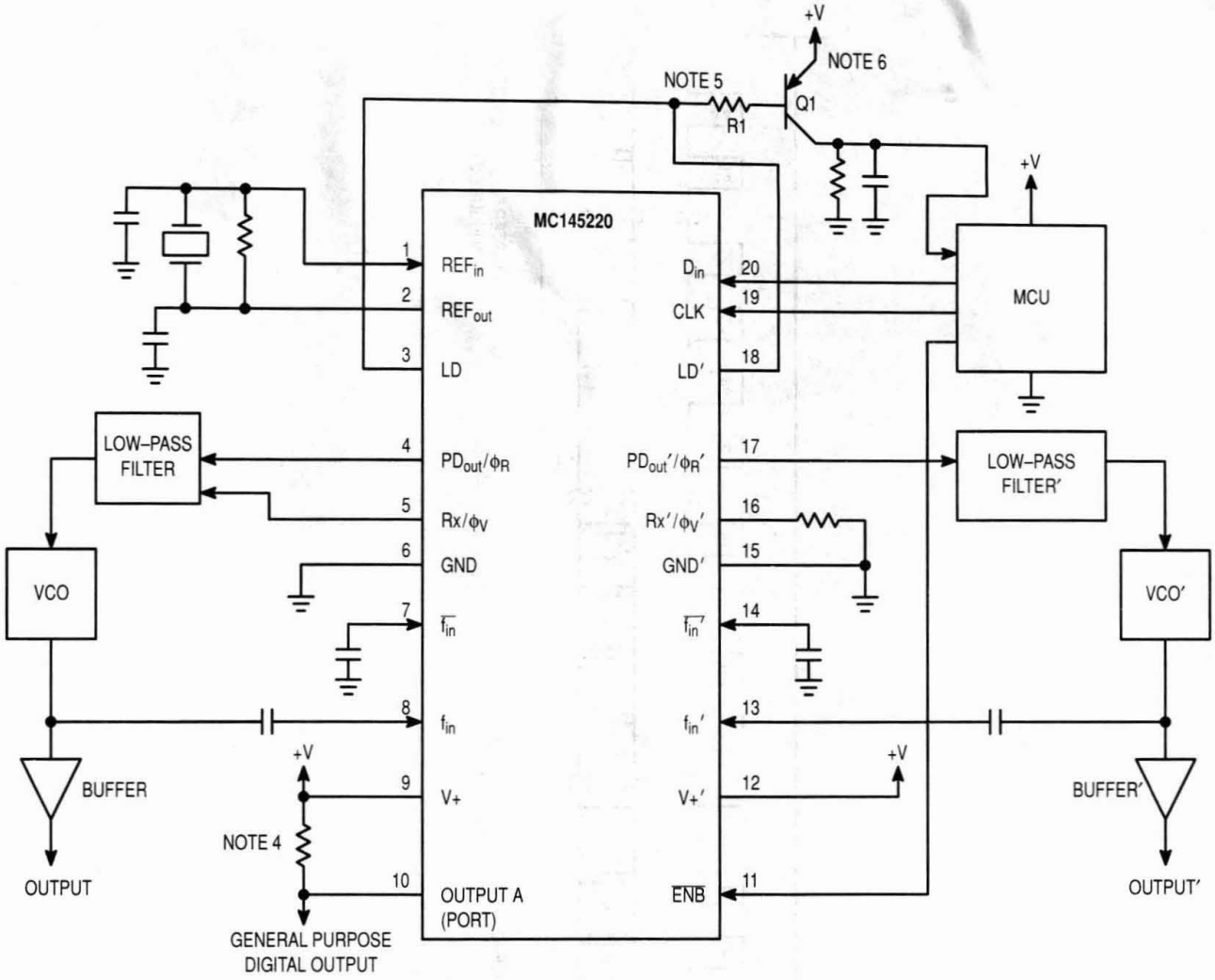
Figure 21. Application Showing Use of the Two Single–Ended Phase/Frequency Detectors



NOTES:

1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R′, f_V, f_V′, DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the "pull–up device".
6. Use of Q1 is optional and depends on loading.

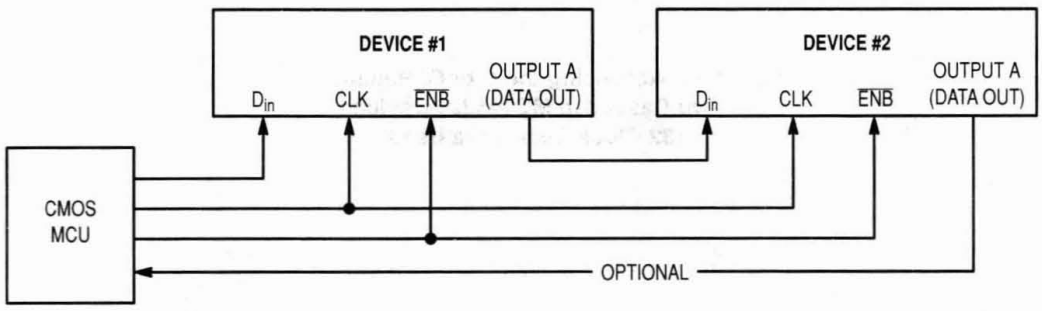
Figure 22. Application Showing Use of the Two Double–Ended Phase/Frequency Detectors



NOTES:

1. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R′, f_V, f_V′, DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the "pull–up device".
6. Use of Q1 is optional and depends on loading.

Figure 23. Application Showing Use of Both the Single– and Double–Ended Phase/Frequency Detectors



NOTE: See related Figures 25, 26, and 27.

Figure 24. Cascading Two Devices

Figure 25. Accessing the C or C′ Registers of Two Cascaded MC145220 Devices (32 Clock Cycles are Used)

*At this point, the new bytes are transferred to the C or C′ registers of both devices and stored. No other registers are affected.

Figure 26. Accessing the A or A′ Registers of Two Cascaded MC145220 Devices (48 Clock Cycles are Used)

*At this point, the new bytes are transferred to the A or A′ registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R Registers are transferred to the respective R register's second buffer. Thus, the R, N, and A (R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. None of the C or C′ registers are affected.

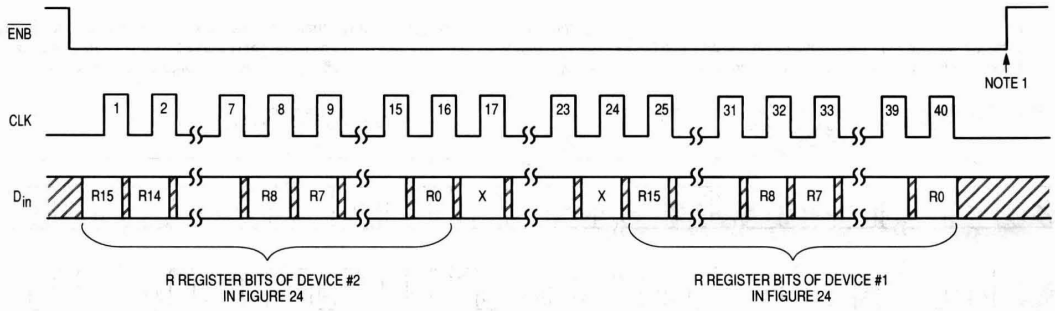


Figure 27. Accessing the R Registers of Two Cascaded MC145220 Devices (40 Clock Cycles are Used)

NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the Buffer and Control block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R and R′ counter divide ratios are not altered yet and retain the previous ratios loaded. The other registers are not affected.
2. See note of Figure 26 for the method of loading the second buffers in the R register to achieve new divide ratios.

MC145220EVK

Technical Summary

MC145220 Evaluation Board

INTRODUCTION

The MC145220EVK makes it easy to exercise features of the MC145220 and build PLLs which meet individual performance requirements. The EVK is controlled through menu driven software operating on an IBM PC or compatible. Other Motorola PLL EVKs (MC145190, MC145191, MC145192, MC145200, MC145201, MC145202) in up to three–board cascades can use the same program. Frequency defaults that apply to each are automatically selected. All board functions are controlled through the printer port of an IBM PC. Up to three different EVKs may be controlled at the same time from one printer port. The functional block diagram is given in Figure 1.

This technical summary contains the hardware description for the evaluation board and a summary of the software section. For complete information, consult the manual that is provided in the evaluation kit.

ORDERING INFORMATION

These kits may be ordered through your local Motorola Semiconductor sales office or authorized distributor. Ask your Motorola representative to order the kits from the finished goods warehouse, not the literature distribution center. Request the part number shown below.

Part Number	Description
MC145220EVK	Kit with the MC145220 installed.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SECTION 1 – HARDWARE

FEATURES

1. The EVK is a complete working synthesizer, including VCOs.
2. Board is controlled by an IBM PC–compatible computer through the printer port.
3. Up to three boards can be operated independently through one printer port.
4. A prototype area and mounting holes are provided for VCOs, mixers, and amplifiers.
5. External reference input can be used.
6. Five element loop filter is included.
7. Frequency range of operation, step size and reference frequency can be changed in the control program.
8. Lock Detect, Out A, and Out B on any single board are accessible through the printer port.

CONTENTS OF EVALUATION KIT

1. Assembled evaluation board.
2. Nine–foot flat cable with four DB–25 male connectors.
3. MC145220EVK manual.
4. 3.5″ PC–compatible disk containing compiled program.
5. PLL device data sheets.

GETTING STARTED

To perform basic functions, do the following:

1. Plug in 12 volts at J8, observing the polarity marked on the board.
2. Short circuit section 1 of the DIP switch (S1) and open circuit all other sections.
3. Connect the supplied flat cable between the computer printer port and the DB–25 connector on the board (J9).
4. Type PLL at the DOS prompt. Then press enter.
5. Type the number that corresponds with the type of board given in the on–screen menu. The MC145220 may operate in single loop or dual loop mode. Then press Q.

You should now see the main menu displayed. There should be a signal present at J5 if single loop, or J12 if dual loop. The frequency will be the current output frequency given in the main menu. If the signal is not on the correct frequency, check to see if your printer port address is $278 (hexadecimal 278). If not, then select the P menu item and enter the correct address. After returning to the main menu, select the I menu item to send data to the board. You should now be on frequency.

MODIFICATIONS

The user may modify the hardware, such as utilizing a different VCO, by using the prototyping area of the board. After such modifications are made, the default values in the software may need to be changed. This is facilitated from the 'Select from the available options' screen.

Note that the on–board voltage regulators allow for a maximum VCO control voltage range of 0.5 – 4.5 volts.

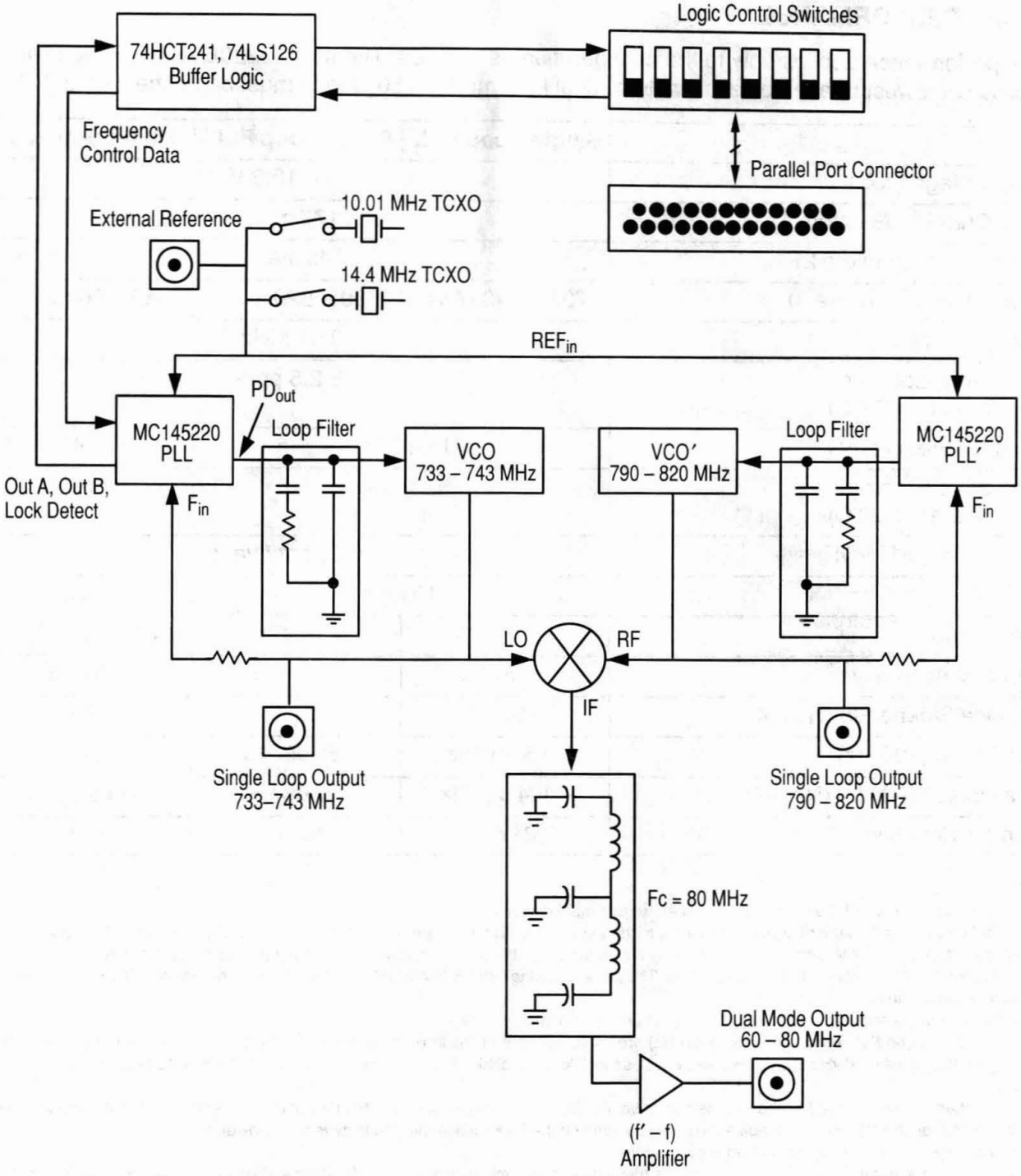


Figure 1. Evaluation Kit Block Diagram

TYPICAL PERFORMANCE

Typical performance applies only to the configuration as shipped. The MC145220EVK is shipped with V+ = 5 V. For lowest phase noise in single or dual loop mode, a 50 Ω load must be connected to J12.

	Single Loop PLL	Single Loop PLL′	Dual Loop PLL
Supply Voltage (J8)	11.5 – 12.5 V		
Supply Current (J8) (Note 1)	177 mA		
Available Current (Note 2)	45 mA		
Frequency Range (Note 3)	733 – 743 MHz	790 – 820 MHz	60 – 80 MHz
Reference Frequency (M1)	10.01 MHz		
Temperature Stability (M1, – 30°C to + 70°C)	< ± 2.5 ppm		
Reference Frequency (M5)	14.4 MHz		N/A
Temperature Stability (M5, – 30°C to + 85°C)	< ± 2 ppm		N/A
TCXO Aging (M1, M5)	< ± 1 ppm / year		
Step Size	10 kHz		10 Hz
Power Output	– 3.0 dBm	– 5.0 dBm	4.5 – 7.5 dBm
Frequency Accuracy	± 1.5 kHz	± 1.5 kHz	± 50 Hz
Reference Sidebands (Note 4)	– 57 dB	– 74 dB	– 57 dB
Phase Noise (100 Hz)	– 65 dBc/Hz	– 56 dBc/Hz	– 50 dBc/Hz
Phase Noise (10 kHz) (Note 5)	– 104 dBc/Hz	– 90 dBc/Hz	– 89 dBc/Hz
Switching Time (Note 6)	24 ms	40 ms	45 ms

NOTES:

1. Supply current is current the board requires without user modifications.
2. Available current is the sum of currents available to the user (in the prototype area) from the 5 V and 8.5 V supply. The 12 V supply is not regulated. Current at 12 V is limited by the external power supply. If the on–board VCO and amplifier are disconnected from the power bus, more current can be drawn in the prototype area. The current flowing into U5 (the 8.5 V regulator) should not exceed 180 mA. This will limit temperature rise in U5.
3. Frequency ranges require use of the 5 V default charge pump supply voltage.
4. VCO sidebands on PLL at low step sizes (10 kHz) are limited by control line leakage of the VCO. Up to 24 nA of leakage has been seen. At higher step sizes (100 kHz and above), this effect is much less noticable. This did not affect PLL′ because its VCO leakage was less than 10 pA.
5. 10 kHz phase noise is limited by the PLL device noise. For low noise designs, the loop bandwidth is made narrower and the VCO is relied upon to provide the 10 kHz phase noise. This can be seen on the EVKs since the VCOs have much lower noise.
6. 10 MHz step, within ± 1 kHz of final frequency ('220).
   Due to the software architecture, when the user is measuring the switching time of a single board in dual loop mode, it takes 20 ms to load the data as compared to single loop mode, which takes 8 ms to load the data. This is a limitation of the software, not the IC.
   To find the actual PLL switching time, subtract 8 or 20 ms from the switching time stated in the table.

SUPPORT MATERIAL

The following documents are included in the appendix:

1. Schematic diagram of MC145220EVK.
2. Bill of materials.
3. Parts layout diagram.
4. Mechanical drawing of board.
5. MC145220 data sheet.
6. Typical signal plots.

PRODUCTION TEST

After assembly is complete, the following alignment and test is performed:

1. The control program is started in '220 single loop mode.
2. [L]! is selected to set PLL frequency to 733 MHz.
3. Power is applied to the board. DIP switch section 1 is closed circuit with all others being open circuit.
4. After attaching computer cable, [I]! is selected.
5. Trim resistor VR1 is adjusted to obtain an output frequency at J5 of 733 MHz ± 500 Hz.
6. Voltage at the control voltage test point (TP2) is measured. It must be > 0.5 V.
7. [H]! is selected.
8. Voltage at the control voltage test point (TP2) is measured. It must be < 4.4 V.
9. [T]! is selected to toggle to PLL′.
10. [L]! is selected to set PLL′ frequency to 790 MHz.
11. Voltage at the control voltage test point (TP9) is measured. It must be > 0.5 V.
12. [H]! is selected to set PLL′ frequency to 820 MHz.
13. Voltage at the control voltage test point (TP9) is measured. It must be < 4.4 V.
14. [G] is selected and the board type is changed to '220 dual loop mode.
15. [Q]!, then [I]!, is selected to initialize the dual mode output (J12) to 70 MHz. The frequency should be 70 MHz ± 50 Hz.

If in step 5 it isn't possible to obtain a signal on frequency, the adjustment screw in M1 may be turned for further frequency adjustment range. If neither adjustment works, [P] should be selected and the correct printer port address entered. [I]! is then selected to reload the data.

BOARD OPERATION

A computer is connected to the DB–25 connector J9. Data is output from the printer port. The printer card is in slot 0 using the default address in the control program. Data is sent to the PLL device (U1) through the DIP switch (S1), and 74HCT241 buffer (U2). D1, D2, D3, R7, R8, and R12 are in the data path between the 'HCT241 and PLL device. This limits the high level output voltage of the buffer. Voltage on PLL device inputs must be no greater than 0.5 V above V+. A '220 PLL has three output lines which are routed through a 74LS126 line driver (U3) back to the computer.

U2, the 74HCT241, provides isolation and logic translation for PLL input lines. Logic translation is needed from the TTL levels on the printer port to the CMOS levels on the '220 inputs.

A 12 V power supply should be used to power the board at J8 (Augat 2SV–02 connector). The 2SV–02 will accept 18–24 AWG bare copper power leads. No tools are needed for connection. If power is properly connected, LED D4 will be lit.

Power passes from J8 to U5 (LM317 regulator) configured as an 8.5 V regulator. 8.5 V powers the VCOs. Regulators U6 and U7 use the 8.5 V supply to produce 3 V and 5 V. The '220 board can use either to power the logic and charge pump. V+ voltage is selected by J11. U6 and U7 are cascaded with U5 to equalize their individual voltage drops.

The '220 operates in both a single loop and dual loop mode. There are no component changes between the two modes. The differences are in the programming of the counters and the SMA connector that is used.

The PLL loop is composed of the MC145220 (U1), 733 – 743 MHz VCO (M2), and a passive loop filter (R4, R5, C6, C7, C8). In single loop mode, output is taken from J5. A passive loop filter was used to keep the design simple, reduce noise, and reduce the quantity of traces susceptible to stray pickup. The PLL′ loop is composed of the MC145220 (U1), 790 – 820 MHz VCO (M3), and a passive loop filter (R22, R25, C24, C26, C30). In single loop mode, output is taken from J10.

Dual mode output is the (f′ – f) frequency output from the mixer. It is low pass filtered (L1, L2, C15, C21, C22) then amplified (U4). The output is available at J12.

Phase detector current is 2 mA. J1 is a removable jumper used for current measurement of V+.

Two TCXOs, a Motorola Saber 14.4 MHz (M5), and Raltron 10.01 MHz (M1) are supplied. As shipped from the factory, the 10.01 MHz TCXO is in use. This allows both the 10 kHz and 10 Hz step sizes to be used with one TCXO. 10.01 MHz cannot be divided for larger step sizes such as 100 kHz. For larger step sizes use the Saber. Jumpers J3, J4, J13, and J14 determine which TCXO or the external reference input is in use.

DUAL MODE OUTPUT

The dual mode output (J12) is the difference frequency from mixing PLL and PLL′. By using a reference frequency of 10.01 MHz, PLL can be operated with a 10.01 kHz step size and PLL′ with a 10 kHz step size. If both PLL and PLL′ step down in frequency, the mixed output will step up by 10 Hz. More information on the offset reference technique is in **AN1277/D, Offset Reference PLLs for Fine Resolution or Fast Hopping**. The block diagram, formulas, and an example are shown in Figure 2.

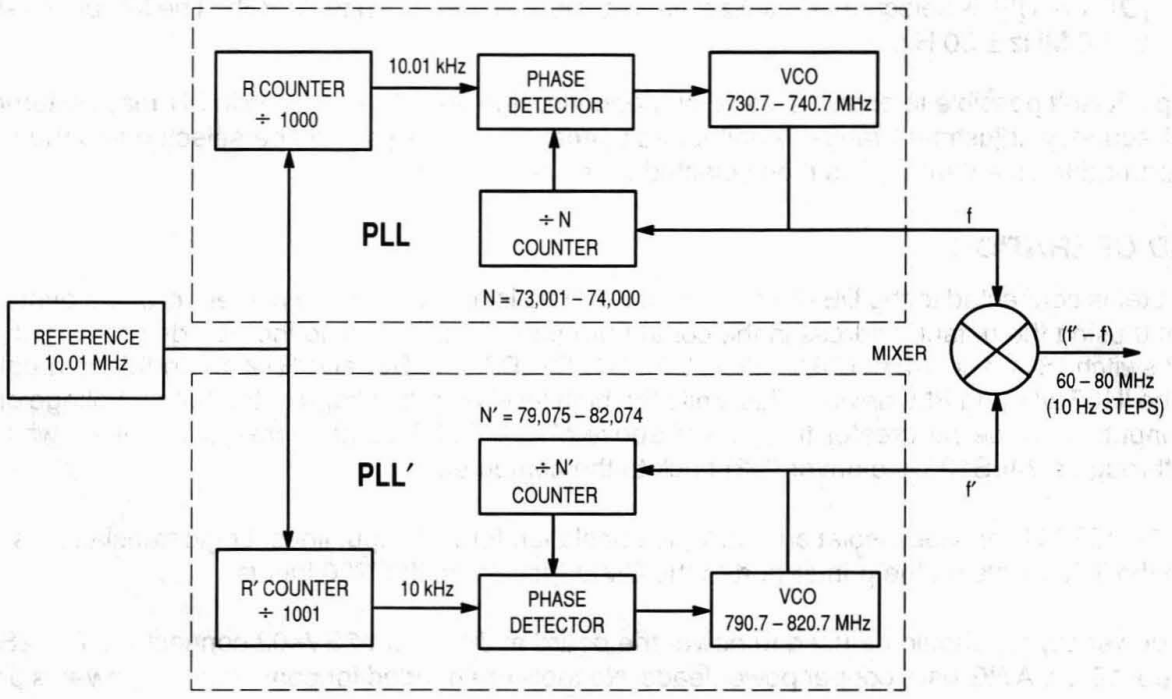


Figure 2. Dual Mode Block Diagram

PLL	PLL′
$f = N\ (10.01\ kHz)$	$f' = N'\ (10\ kHz)$
$f = 10.01\ kHz \left[74{,}000 - \frac{r(f' - f)}{10\ Hz}\right]$	$f' = 10\ kHz \left[\frac{w(f' - f) + 740\ kHz}{10\ kHz} + N\right]$
$N = 74{,}000 - \frac{r(f' - f)}{10\ Hz}$	$N' = N + 74 + \frac{w(f' - f)}{10\ kHz}$
$(f' - f) = w(f' - f) + r(f' - f)$	
$(f' - f)$ = Desired Output Frequency	
$w(f' - f)$ = Output Frequency Portion that Divides Evenly by 10 kHz	
$r(f' - f)$ = Remainder from Output Frequency Division by 10 kHz	

Dual Mode Formulas

Example: Synthesize 76.849 930 MHz

$r(f' - f) = 9.930\ kHz$, $w(f' - f) = 76.840\ MHz$

$$N = 74{,}000 - \frac{9.930\ kHz}{10\ Hz} = 73{,}007 \qquad f = 73{,}007\ (10.01\ kHz) = 730.800\ 070\ MHz$$

$$N' = 73{,}007 + 74 + \frac{76.840\ MHz}{10\ kHz} = 80{,}765 \qquad f' = 80{,}765\ (10\ kHz) = 807.650\ 000\ MHz$$

$(f' - f) = 807.650\ 000\ MHz - 730.800\ 070\ MHz = 76.849\ 930\ MHz$

EXTERNAL REFERENCE INPUT

To use an external reference, disconnect J3, J4, J13, and J14. Use a reference signal at J2 which complies with data sheet requirements. Then modify the reference frequency in the program main menu to reflect the changes made (F menu item).

DATA TRANSFER FROM COMPUTER TO EVK

To control the serial input EVK with the parallel printer port, a conversion is done. Printer cards are designed to output eight bits through eight lines. A bit mask is used to obtain the bit combination for the three required output lines (Data, Clock, Load). As bytes are sent to the printer card in sequence, it appears to be a serial transfer. The printer port is used because data transfer using the serial port would be much slower. A standard IBM PC can support a parallel port data rate of 4.77 MHz.

IBM PCs and compatibles can accept up to three printer port configurations. These ports are called LPT1, LPT2, and LPT3. Each printer port has a unique address. Two sets of addresses are in common use. One set applies to IBM PC XT, AT, and clones. The other is for the PS 2 line. To load data into the EVK, the correct address must be selected. The program default is $278. If $278 is not the address in use, it must be modified by entering the P menu item in the main menu. All allowed addresses given in hexadecimal are as follows:

Label	IBM PC and Clones	PS 2
LPT1	278	3BC
LPT2	378	378
LPT3	3BC	278

Up to three EVK boards can operate independently from one printer port. All lines on the printer port are connected to every EVK. Even with three boards operating, only three output lines (Clock, Data, and Load) from the printer card are used. If two boards are controlled together, data for the second board is received from the Output A of the first. Output A is a configurable output on '220 devices, which in this case is used to shift data through chip 1 into chip 2. Output A and Data are connected using a printer port input line. This was done to avoid connecting extra wires. Fortunately not all port input lines are needed for computer input. Load and Clock are common to both boards.

A three–board cascade is handled similarly to a two–board cascade. Out A on the first board is fed to Data on the second. Out A on the second connects to Data on the third. Instructing the program on the quantity of boards connected together allows it to modify the number of bits sent.

All boards have a DIP switch S1 which gives each a unique address. The configuration menu is used to tell the program what type of board is connected at a board address. Switch positions for all possible addresses are given in Figure 2.

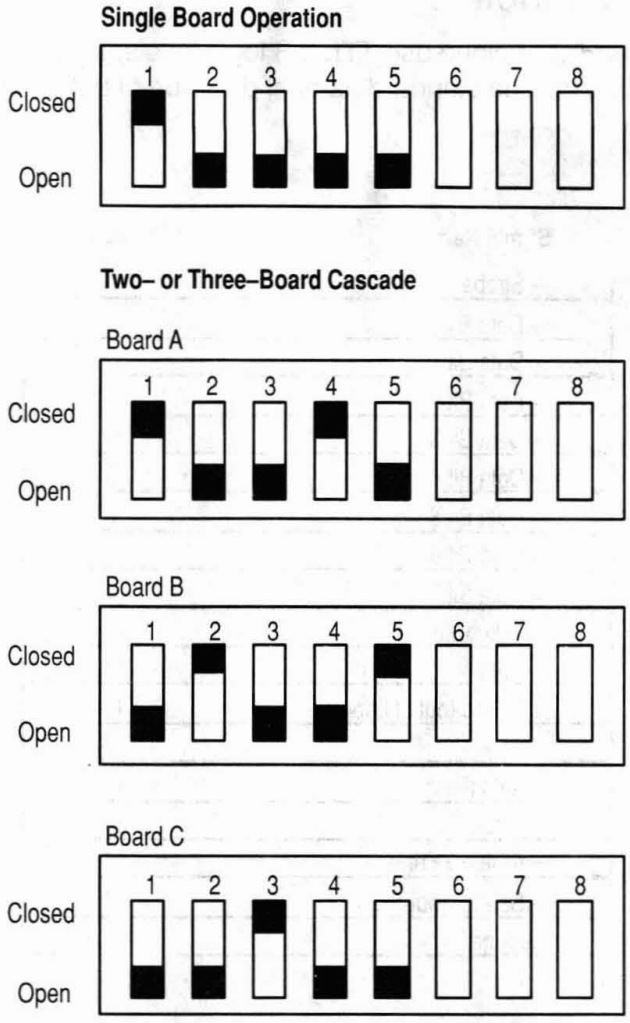


Figure 3. Switch Positions

In Figure 2, DIP switch sections 6, 7, and 8 allow the computer to read Out A, Lock Detect′, or Lock Detect from the PLL device. Each of the inputs can only be read on one board at a time, but each item could be read on a different board. In a three–board cascade, Out A could be read from the first board, Out B from the second, and Lock Detect from the third. There is no way to determine the board address of a particular input with software. The control program does not make use of these inputs; however, source code could be modified as required. Pin assignment on the printer port connector is:

Label	Pin Number
Out A	12
Out B	13
Lock Detect	15

PRINTER PORT CONFIGURATION

Printer port outputs on an IBM PC or clone use TTL–LS logic levels. Inputs are one TTL–LS load. Signal lines can be used for any purpose. The standard names, direction of data flow, true and inverted data are shown in Figure 3.

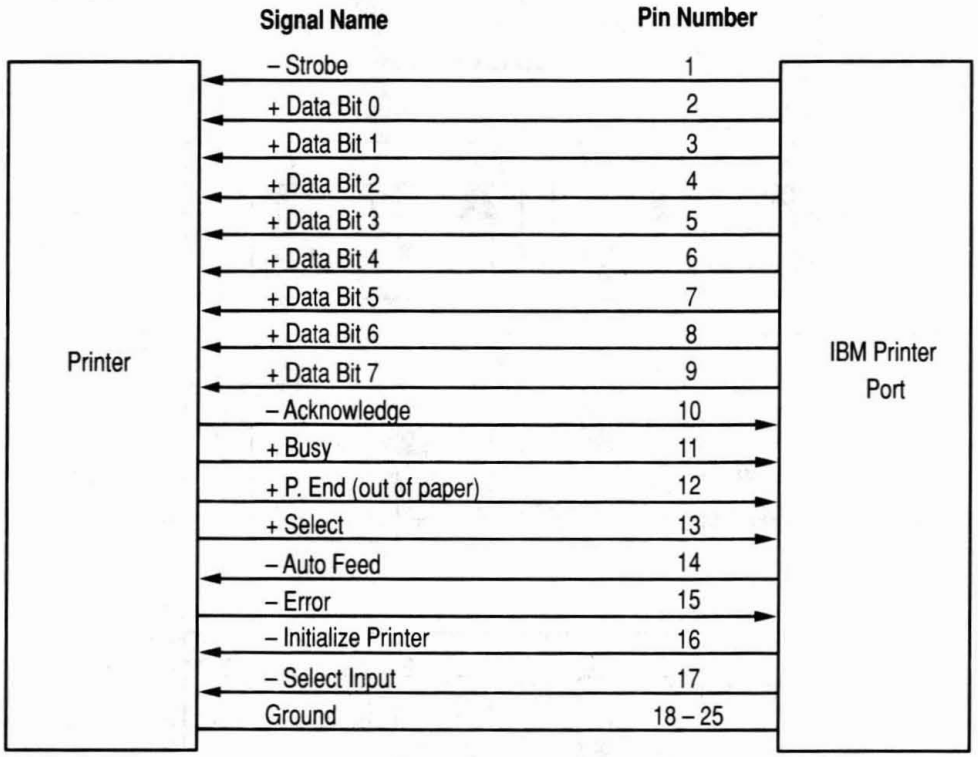


Figure 4. Printer Port Data Lines

Pin numbers for the port connector are shown in Figure 4.

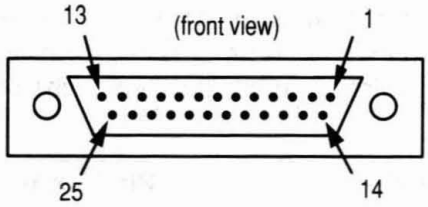


Figure 5. DB–25 Male Connector

SECTION 2 – SOFTWARE DESCRIPTIONS SUMMARY

INTRODUCTION

The MC145xxx EVK control program is used to program all PLL evaluation kits. It will simultaneoulsy control up to three different boards independently from one printer port. All features of the PLL device may be accessed. Default frequencies can be modified to allow use of different channel spacings and VCOs.

User input errors are detected and appropriate messages are displayed.

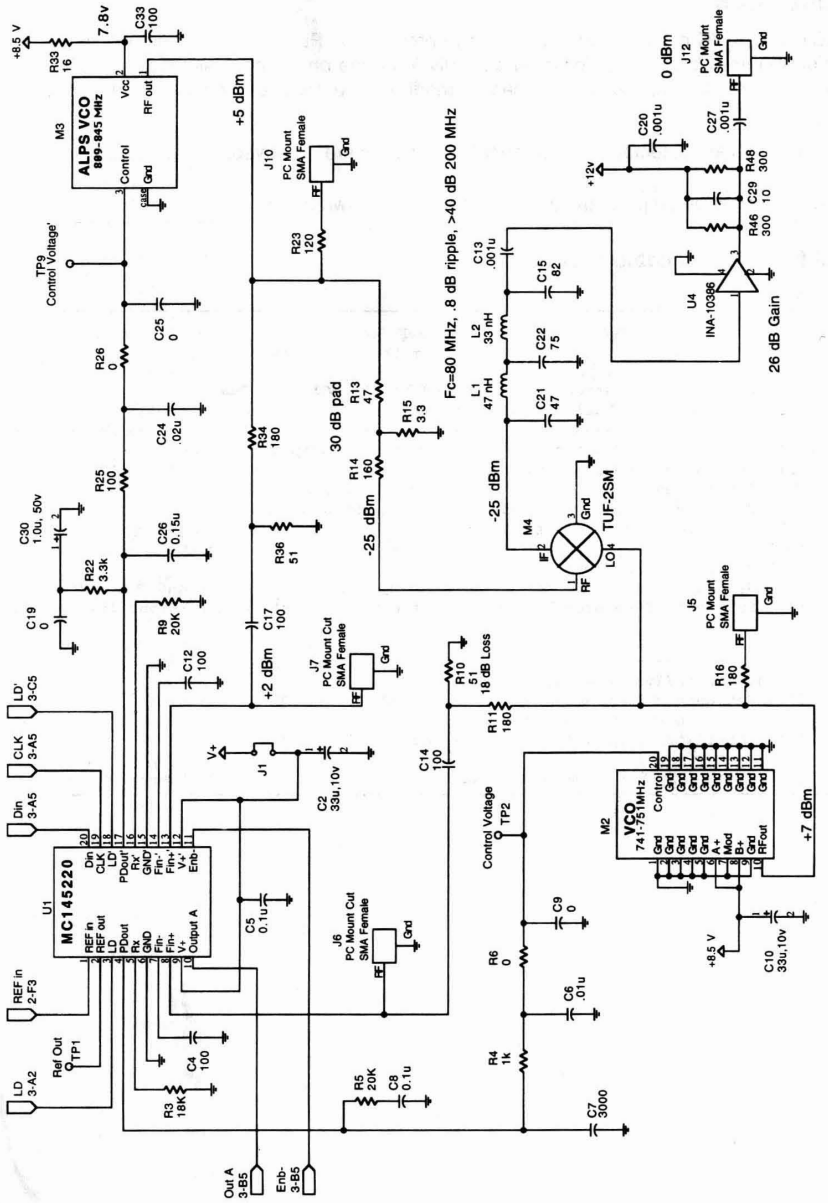
To show the format of the program, a sample screen is shown below:

'Select from the available options'

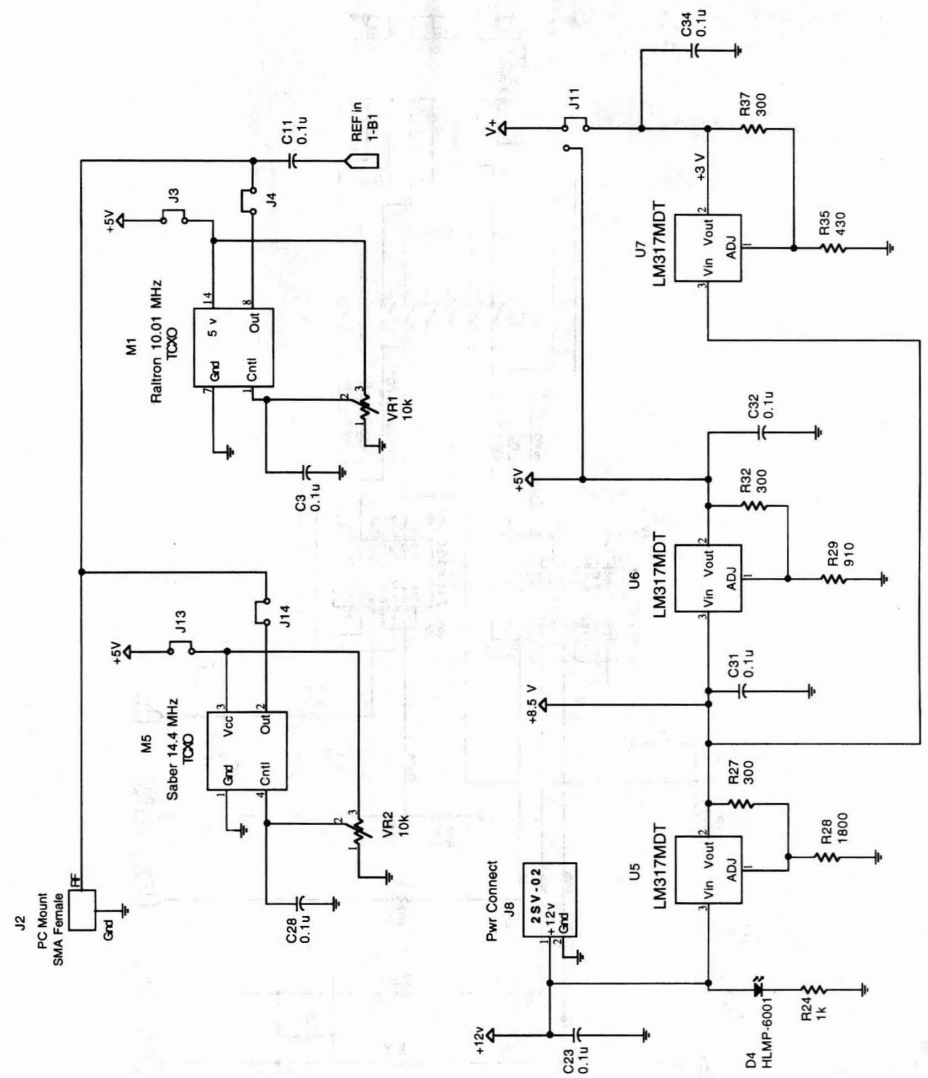
```
                Welcome to MC145xxx EVK Demonstration Program, rev 4.0
                          Select from the available options

Available Boards - Current target board is: A, MC145220 Dual
 Brd [A]!: MC145220 Dual    Brd [-]!: N/A            Brd [-]!: N/A
--------------------------------------------------------------------------------
MC145xxx Frequency Commands - Current Output Frequency is 70 MHz
 [L]! Set to low freq.     60 MHz [W] Change default low freq.
 [M]! Set to med. freq.    70 MHz [Y] Change default med. freq.
 [H]! Set to high freq.    80 MHz [Z] Change default high freq.
 [U]! Step frequency up by step size    [O] Set PLL output frequency
 [D]! Step frequency down by step size  [F] REFin freq. & channel spacing
MC145xxx Additional Commands
 [E]  Set function of output A          [N] Change C register and Prescale
 [R]  Set crystal/reference mode - Current mode is Ref. mode, REFout low


--------------------------------------------------------------------------------
Initialization/System Setup Commands:
 [P]  Set output port address - Current address is $278
 [G]  Change board definitions
 [I]  Initialize board(s), Write all registers

              [X]! Terminate demonstration program. [?]! View help screen.
```

APPENDIX

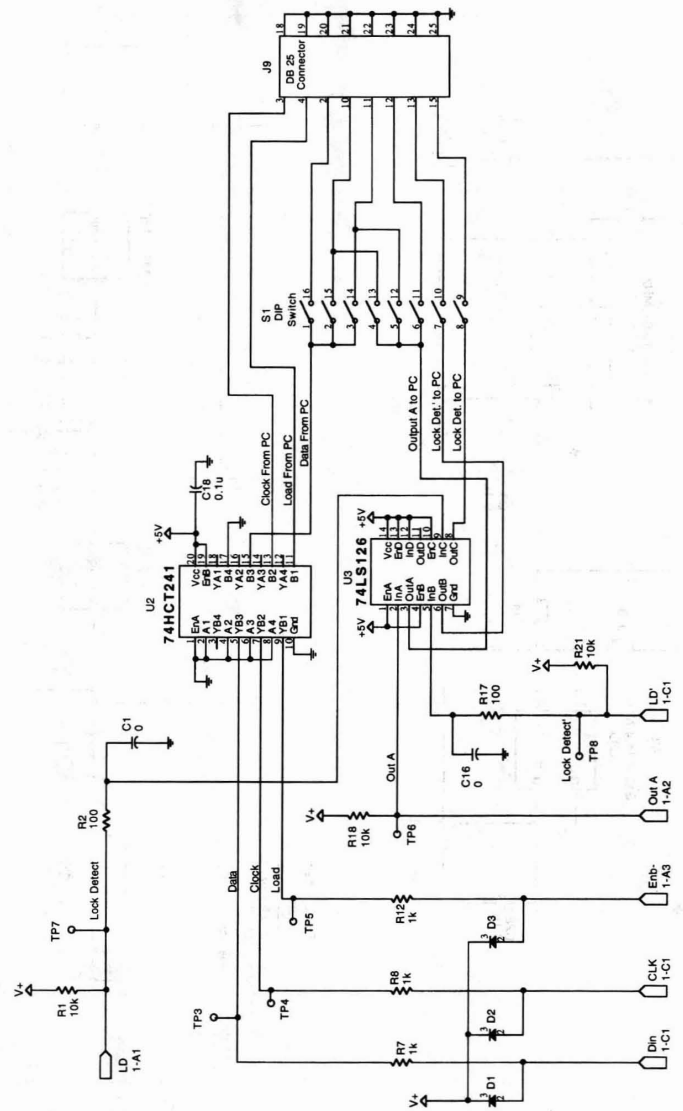
MC145220 PLL Evaluation Board



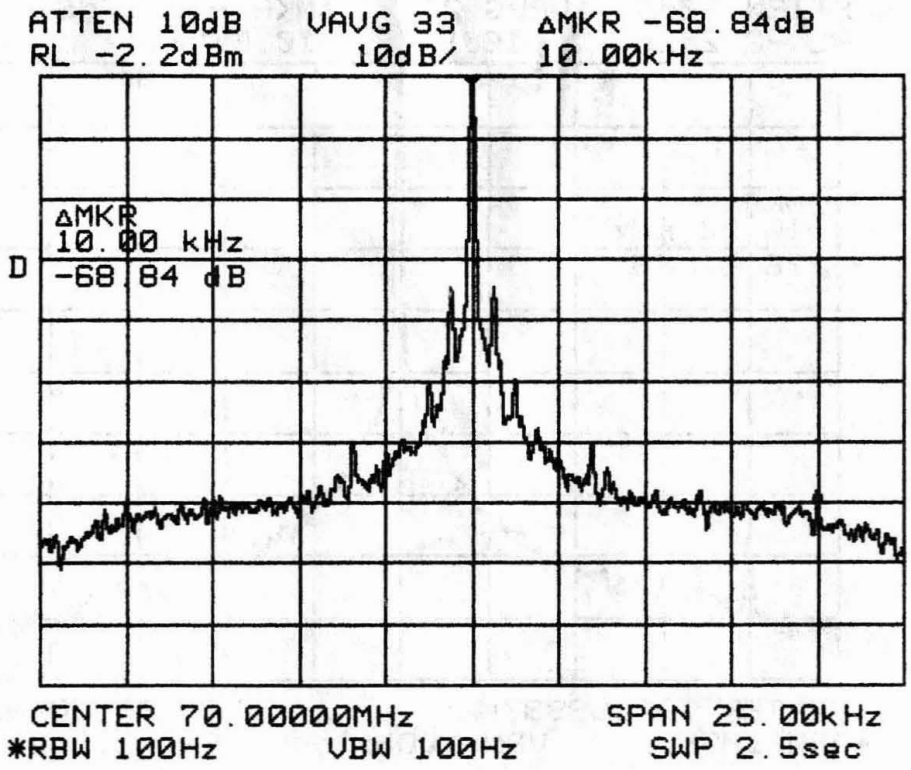
MC145220 Power Supply and Reference



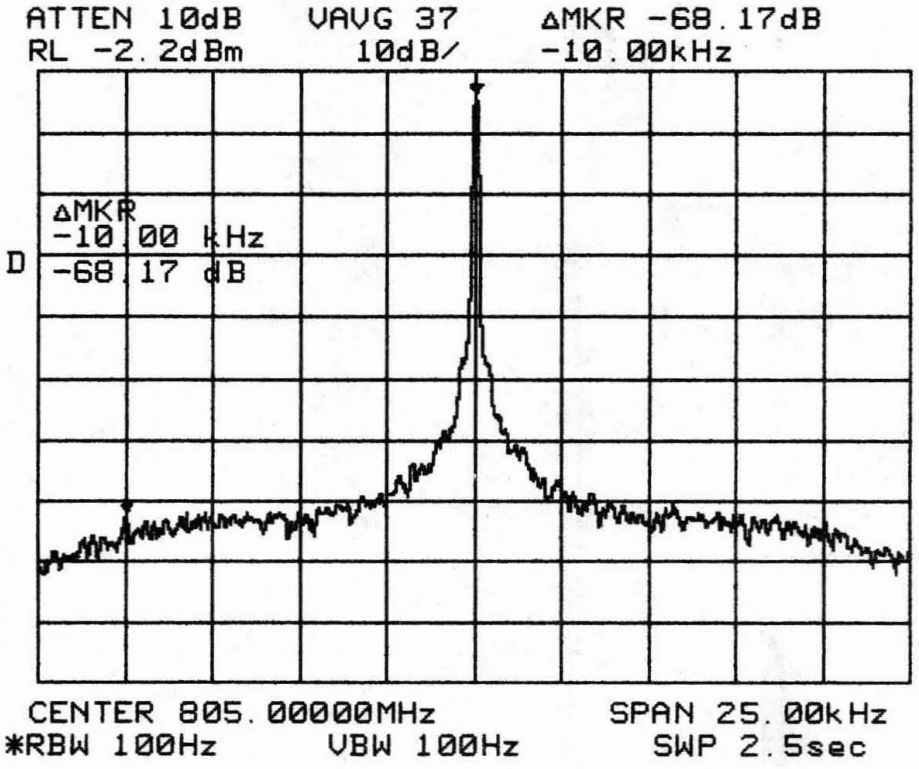
MC145220EVK Bus Interface



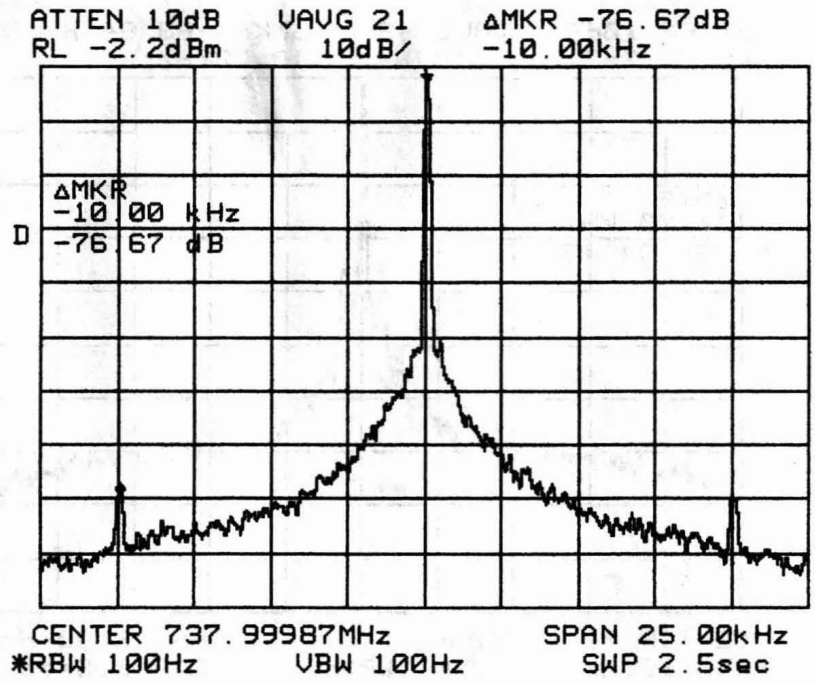
MC145220EVK Signal Plot — Dual Loop Mode Output at 70 MHz



MC145220EVK Signal Plot — Single Loop Mode PLL on 805 MHz



MC145220EVK Signal Plot — Single Loop Mode PLL on 738 MHz



MOTOROLA

MCH12140
MCK12140

Phase-Frequency Detector

The MCH/K12140 is a phase frequency-detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. When used in conjunction with the MC12147, MC12148 or MC12149 VCO, a high bandwidth PLL can be realized. The device is functionally compatible with the MC12040 phase-frequency detector, however the MOSAIC™ III process is used to push the maximum frequency to 800 MHz and significantly reduce the dead zone of the detector. When the Reference (R) and VCO (V) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

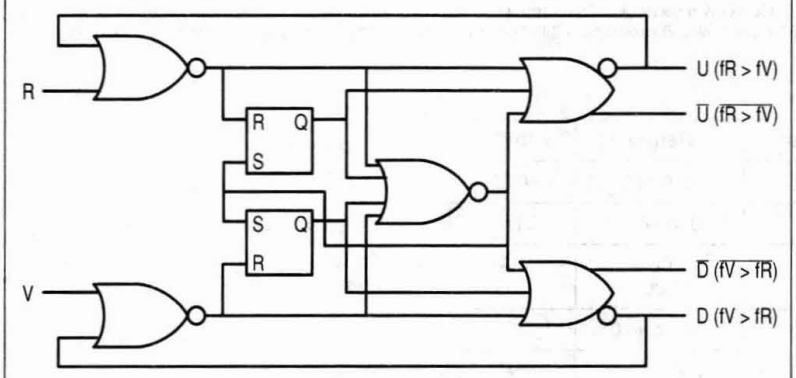
The device is packaged in a small outline, surface mount 8-lead SOIC package. There are two versions of the device to provide I/O compatibility to the two existing ECL standards. The MCH12140 is compatible with MECL10H™ logic levels while the MCK12140 is compatible to 100K ECL logic levels. This device can also be used in +5.0 V systems. Please refer to Motorola Application Note AN1406/D, "Designing with PECL (ECL at +5.0 V)" for more information.

- 800 MHz Typical Bandwidth
- Small Outline 8-Lead SOIC Package
- 75 kΩ Internal Input Pulldown Resistors
- >1000 V ESD Protection

For proper operation, the input edge rate of the R and V inputs should be less than 5ns.

MOSAIC III and MECL 10H are trademarks of Motorola

LOGIC DIAGRAM

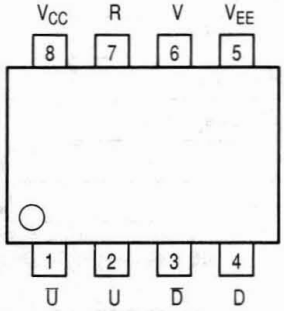


PHASE–FREQUENCY DETECTOR

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCH1214OD	T_A = –40° to +70°C	SO–8
MCK12140D		

ABLE*

put		Output				Input		Output			
	V	U	D	$\overline{U}$	$\overline{D}$	R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X	1	1	0	0	1	1
0	1	X	X	X	X	1	0	0	0	1	1
1	1	X	X	X	X	1	1	0	1	1	0
0	1	X	X	X	X	1	0	0	1	1	0
1	1	1	0	0	1						
0	1	1	0	0	1	1	1	0	1	1	0
1	1	1	0	0	1	0	1	0	1	1	0
1	0	1	0	0	1	1	1	0	0	1	1

NOTE: * This is not strictly a functional table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly.

H–SERIES DC CHARACTERISTICS ($V_{EE} = V_{EE}(min) - V_{EE}(max)$; $V_{CC} = GND$[1], unless otherwise noted.)

Characteristic	Symbol	–40°C		0°C		25°C		70°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Output HIGH Voltage	V_{OH}	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
Output LOW Voltage	V_{OL}	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
Input HIGH Voltage	V_{IH}	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
Input LOW Voltge	V_{IL}	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
Input LOW Current	I_{IL}	0.5	—	0.5	—	0.5	—	0.3	—	µA

NOTE: 1. 10H circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

K–SERIES DC CHARACTERISTICS ($V_{EE} = V_{EE}(min) - V_{EE}(max)$; $V_{CC} = GND$[1], unless otherwise noted.)

Characteristic	Symbol	–40°C			0°C to 70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
Output HIGH Voltage	V_{OH}	–1085	–1005	–880	–1025	–955	–880	mV	$V_{IN} = V_{IH}(max)$
Output LOW Voltage	V_{OL}	–1830	–1695	–1555	–1810	–1705	–1620	mV	or $V_{IL}(min)$
Output HIGH Voltage	V_{OHA}	–1095	—	—	–1035	—	—	mV	$V_{IN} = V_{IH}(min)$
Output LOW Voltage	V_{OLA}	—	—	–1555	—	—	–1610	mV	or $V_{IL}(max)$
Input HIGH Voltage	V_{IH}	–1165	—	–880	–1165	—	–880	mV	
Input LOW Voltge	V_{IL}	–1810	—	–1475	–1810	—	–1475	mV	
Input LOW Current	I_{IL}	0.5	—	—	0.5	—	—	µA	$V_{IN} = V_{IL}(max)$

NOTE: 1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0V)	V_{EE}	–8.0 to 0	VDC
Input Voltage (V_{CC} = 0V)	V_I	0 to –6.0	VDC
Output Current Continuous Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	–40 to +70	°C
Operating Range[1,2]	V_{EE}	–5.7 to –4.2	V

NOTES: 1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: H–Series: –4.20 V to –5.50 V
K–Series: –4.94 V to –5.50 V
3. ESD data available upon request.

DC CHARACTERISTICS ($V_{EE} = V_{EE}(min) - V_{EE}(max)$; V_{CC} = GND, unless otherwise noted.)

Characteristic		Symbol	−40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Current	H	I_{EE}		45		38	45	52	38	45	52	38	45	52	mA
	K			45		38	45	52	38	45	52	42	50	58	
Power Supply Voltage	H	V_{EE}	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	V
	K		−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	
Input HIGH Current		I_{IH}			150			150			150			150	μA

AC CHARACTERISTICS ($V_{EE} = V_{EE}(min) - V_{EE}(max)$; V_{CC} = GND, unless otherwise noted.)

Characteristic		Symbol	−40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Maximum Toggle Frequency		F_{MAX}		800		650	800		650	800		650	800		
Propagation Delay to Output	R to D	t_{PLH}		440		320	440	580	320	440	580	360	480	620	ps
	R to U	t_{PHL}		330		210	330	470	210	330	470	240	360	500	
	V to D			330		210	330	470	210	330	470	240	360	500	
	V to U			440		320	440	580	320	440	580	360	480	620	
Output Rise/Fall Times Q (20 to 80%)		t_r													ps
		t_f		225		100	225	350	100	225	350	100	225	350	

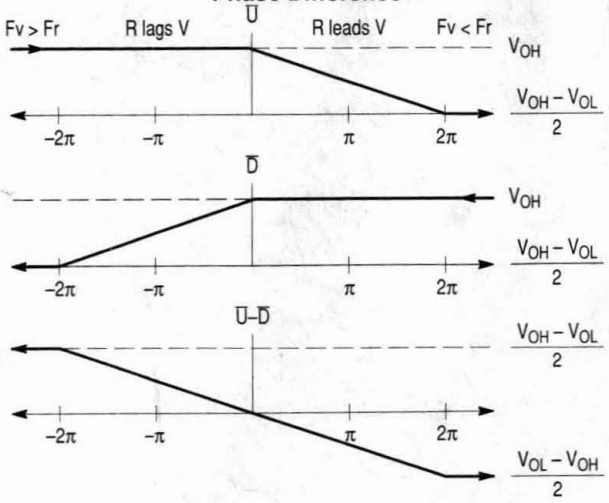
APPLICATIONS INFORMATION

The 12140 is a high speed digital circuit used as a phase comparator in an analog phase-locked loop. The device determines the "lead" or "lag" phase relationship and time difference between the leading edges of a VCO (V) signal and a Reference (R) input. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

The operation of the 12140 can best be described using the plots of Figure 1. Figure 1 plots the average value of $\overline{U}$, $\overline{D}$ and the difference between $\overline{U}$ and $\overline{D}$ versus the phase difference between the V and R inputs.

There are four potential relationships between V and R: R lags or leads V and the frequency of R is less than or greater than the frequency of V. Under these four conditions the 12140 will function as follows:

Figure 1. Average Output Voltage versus Phase Difference



R lags V in phase

When the R and V inputs are equal in frequency and the phase of R lags that of V the $\overline{U}$ output will stay HIGH while the $\overline{D}$ output will pulse from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{D}$ indicates to the VCO to decrease in frequency to bring the loop into lock.

V frequency > R frequency

When the frequency of V is greater t[illegible]hat of R the 12140 behaves in a simlar fashion as above. [illegible]ain the signal on $\overline{D}$ indicates that the VCO frequency must be decreased to bring the loop into lock.

R leads V in phase

When the R and V inputs are equal in frequency and the phase of R leads that of V the $\overline{D}$ output will stay HIGH while the $\overline{U}$ output pulses from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{U}$ indicates to the VCO to increase in frequency to bring the loop into lock.

V frequency < R frequency

When the frequency of V is less than that of R the 12140 behaves in a simlar fashion as above. Again the signal on $\overline{U}$ indicates that the VCO frequency must be decreased to brin[illegible] the loop into lock.

From Figure 1 when V and R are at the same freque[illegible] and in phase the value of $\overline{U} - \overline{D}$ is zero thus providing [illegible] error voltage to the VCO. This situation indicates the [illegible] in lock and the 12140 action will maintain the lo[illegible] locked state.